



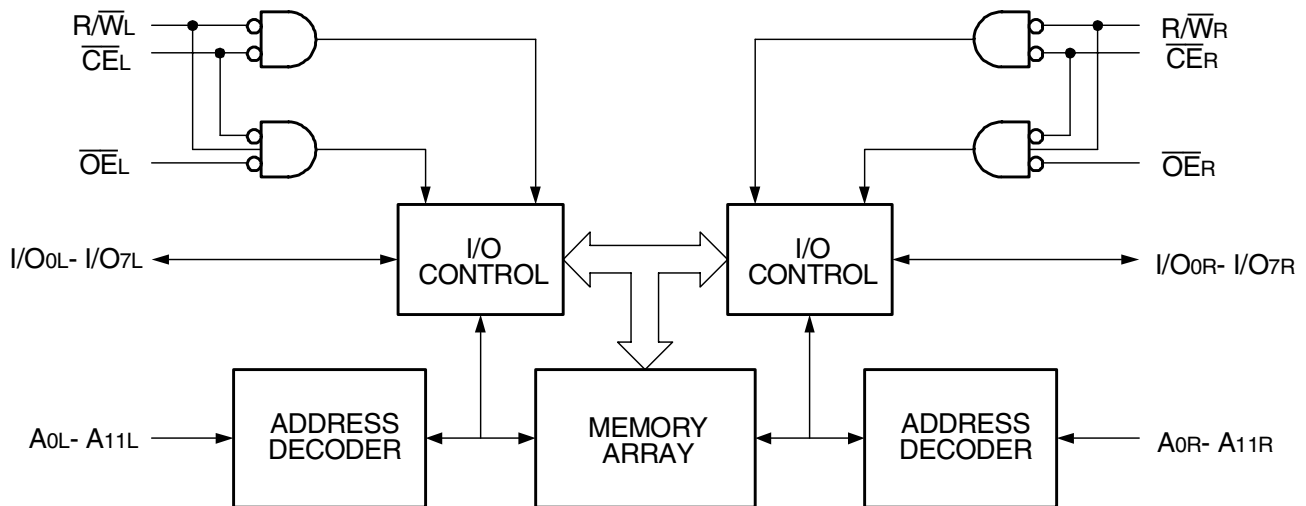
# HIGH-SPEED 4K x 8 DUAL-PORT STATIC SRAM

IDT7134SA/LA

## Features

- ◆ High-speed access
  - Military: 35/45/55/70ns (max.)
  - Industrial: 25/55ns (max.)
  - Commercial: 20/25/35/45/55/70ns (max.)
- ◆ Low-power operation
  - IDT7134SA
    - Active: 700mW (typ.)
    - Standby: 5mW (typ.)
  - IDT7134LA
    - Active: 700mW (typ.)
    - Standby: 1mW (typ.)
- ◆ Fully asynchronous operation from either port
- ◆ Battery backup operation—2V data retention (LA only)
- ◆ TTL-compatible; single 5V ( $\pm 10\%$ ) power supply
- ◆ Available in 48-pin DIP, LCC, Flatpack and 52-pin PLCC
- ◆ Military product compliant to MIL-PRF-38535 QML
- ◆ Industrial temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) is available for selected speeds
- ◆ Green parts available, see ordering information

## Functional Block Diagram



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FEBRUARY 2013

## Description

The IDT7134 is a high-speed 4K x 8 Dual-Port Static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same Dual-Port RAM location.

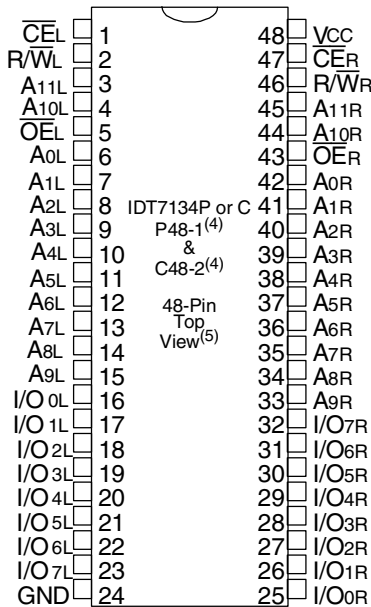
The IDT7134 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power down feature,

controlled by  $\overline{CE}$ , permits the on-chip circuitry of each port to enter a very low standby power mode.

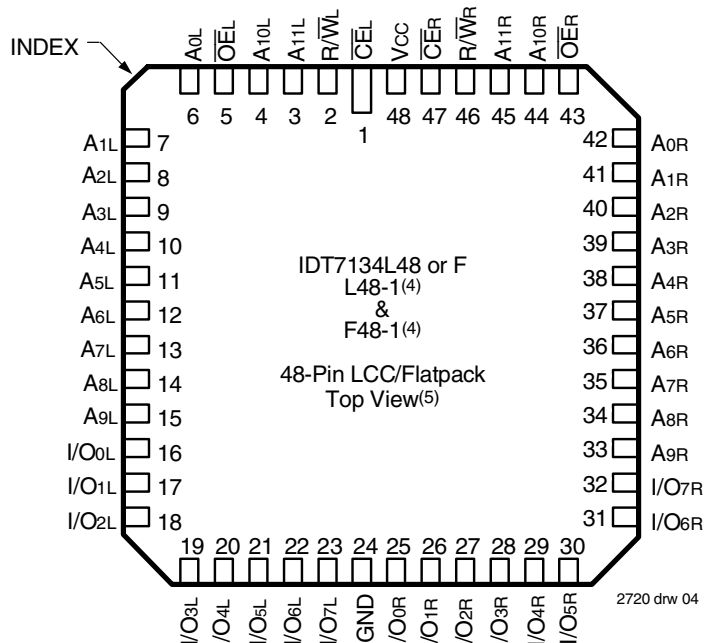
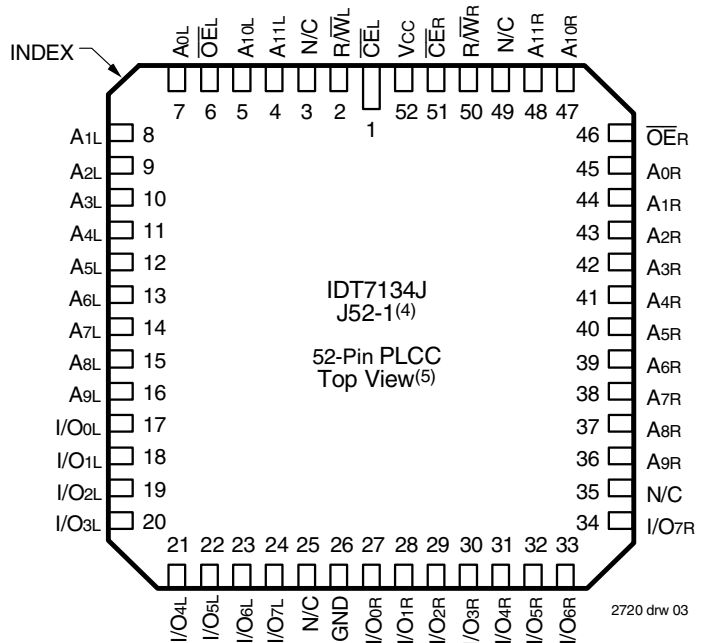
Fabricated using CMOS high-performance technology, these Dual-Ports typically operate on only 700mW of power. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming 200 $\mu$ W from a 2V battery.

The IDT7134 is packaged on either a sidebrazed or plastic 48-pin DIP, 48-pin LCC, 52-pin PLCC and 48-pin Flatpack. Military grade product is manufactured in compliance with MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## Pin Configurations<sup>(1,2,3)</sup>



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### NOTES:

1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. P48-1 package body is approximately .55 in x 2.43 in x .18 in.  
C48-2 package body is approximately .62 in x 2.43 in x .15 in.  
J52-1 package body is approximately .75 in x .75 in x .17 in.  
L48-1 package body is approximately .57 in x .57 in x .68 in.  
F48-1 package body is approximately .75 in x .75 in x .11 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of actual part-marking.

### Absolute Maximum Ratings<sup>(1)</sup>

| Symbol                           | Rating                               | Commercial & Industrial | Military     | Unit |
|----------------------------------|--------------------------------------|-------------------------|--------------|------|
| V <sub>TERM</sub> <sup>(2)</sup> | Terminal Voltage with Respect to GND | -0.5 to +7.0            | -0.5 to +7.0 | V    |
| T <sub>BIAS</sub>                | Temperature Under Bias               | -55 to +125             | -65 to +135  | °C   |
| T <sub>STG</sub>                 | Storage Temperature                  | -65 to +150             | -65 to +150  | °C   |
| P <sub>T</sub> <sup>(3)</sup>    | Power Dissipation                    | 1.5                     | 1.5          | W    |
| I <sub>OUT</sub>                 | DC Output Current                    | 50                      | 50           | mA   |

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**NOTES:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>TERM</sub> must not exceed V<sub>CC</sub> + 10% for more than 25% of the cycle time or 10 ns maximum, and is limited to ≤ 20mA for the period of V<sub>TERM</sub> ≥ V<sub>CC</sub> + 10%.
- V<sub>TERM</sub> = 5.5V.

### Capacitance<sup>(1)</sup> (T<sub>A</sub> = +25°C, f = 1.0MHz)

| Symbol           | Parameter          | Conditions <sup>(2)</sup> | Max. | Unit |
|------------------|--------------------|---------------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance  | V <sub>IN</sub> = 3dV     | 11   | pF   |
| C <sub>OUT</sub> | Output Capacitance | V <sub>OUT</sub> = 3dV    | 11   | pF   |

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**NOTES:**

- This parameter is determined by device characterization but is not production tested.
- 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V and from 3V to 0V.

### Recommended Operating Temperature and Supply Voltage<sup>(1,2)</sup>

| Grade      | Ambient Temperature | GND | V <sub>CC</sub> |
|------------|---------------------|-----|-----------------|
| Military   | -55°C to +125°C     | 0V  | 5.0V ± 10%      |
| Commercial | 0°C to +70°C        | 0V  | 5.0V ± 10%      |
| Industrial | -40°C to +85°C      | 0V  | 5.0V ± 10%      |

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**NOTES:**

- This is the parameter T<sub>A</sub>. This is the "instant on" case temperature.

### Recommended DC Operating Conditions

| Symbol          | Parameter          | Min.                | Typ. | Max.               | Unit |
|-----------------|--------------------|---------------------|------|--------------------|------|
| V <sub>CC</sub> | Supply Voltage     | 4.5                 | 5.0  | 5.5                | V    |
| GND             | Ground             | 0                   | 0    | 0                  | V    |
| V <sub>IH</sub> | Input High Voltage | 2.2                 | —    | 6.0 <sup>(2)</sup> | V    |
| V <sub>IL</sub> | Input Low Voltage  | -0.5 <sup>(1)</sup> | —    | 0.8                | V    |

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**NOTES:**

- V<sub>IL</sub> (min.) ≥ -1.5V for pulse width less than 10ns.
- V<sub>TERM</sub> must not exceed V<sub>CC</sub> + 10%.

### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V<sub>CC</sub> = 5V ± 10%)

| Symbol          | Parameter                            | Test Conditions  | 7134SA |      | 7134LA |      | Unit |
|-----------------|--------------------------------------|--|--------|------|--------|------|------|
|                 |                                      |  | Min.   | Max. | Min.   | Max. |      |
| I <sub>I</sub>  | Input Leakage Current <sup>(1)</sup> | V <sub>CC</sub> = 5.5V, V <sub>IN</sub> = 0V to V <sub>CC</sub>              | —      | 10   | —      | 5    | μA   |
| I <sub>O</sub>  | Output Leakage Current               | $\overline{CE}$ - V <sub>IH</sub> , V <sub>OUT</sub> = 0V to V <sub>CC</sub> | —      | 10   | —      | 5    | μA   |
| V <sub>OL</sub> | Output Low Voltage                   | I <sub>OL</sub> = 6mA  | —      | 0.4  | —      | 0.4  | V    |
|                 |                                      | I <sub>OL</sub> = 8mA  | —      | 0.5  | —      | 0.5  | V    |
| V <sub>OH</sub> | Output High Voltage                  | I <sub>OH</sub> = -4mA   | 2.4    | —    | 2.4    | —    | V    |

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**NOTES:**

- At V<sub>CC</sub> ≤ 2.0V input leakages are undefined.

### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(1,2)</sup> ( $V_{CC} = 5.0V \pm 10\%$ )

| Symbol           | Parameter   | Test Condition   | Version   |    | 7134X20<br>Com'l Only |      | 7134X25<br>Com'l & Ind |      | 7134X35<br>Com'l<br>& Military |      | Unit |
|------------------|---|--|-----------|----|-----------------------|------|------------------------|------|--------------------------------|------|------|
|                  |   |  |           |    | Typ.                  | Max. | Typ.                   | Max. | Typ.                           | Max. |      |
| I <sub>CC</sub>  | Dynamic Operating Current<br>(Both Ports Active)            | $\overline{CE} = V_{IL}$<br>Outputs Disabled<br>$f = f_{MAX}^{(3)}$  | COM'L     | SA | 170                   | 280  | 160                    | 280  | 150                            | 260  | mA   |
|                  |   |  |           | LA | 170                   | 240  | 160                    | 220  | 150                            | 210  |      |
| I <sub>SB1</sub> | Standby Current<br>(Both Ports - TTL<br>Level Inputs)       | $\overline{CE}_L$ and $\overline{CE}_R = V_{IH}$<br>$f = f_{MAX}^{(3)}$  | COM'L     | SA | 25                    | 100  | 25                     | 80   | 25                             | 75   | mA   |
|                  |   |  |           | LA | 25                    | 80   | 25                     | 50   | 25                             | 45   |      |
| I <sub>SB2</sub> | Standby Current<br>(One Port - TTL<br>Level Inputs)         | $\overline{CE}^A = V_{IL}$ and $\overline{CE}^B = V_{IH}$<br>Active Port Outputs Disabled,<br>$f = f_{MAX}^{(3)}$  | COM'L     | SA | 105                   | 180  | 95                     | 180  | 85                             | 170  | mA   |
|                  |   |  |           | LA | 105                   | 150  | 95                     | 140  | 85                             | 130  |      |
| I <sub>SB3</sub> | Full Standby Current<br>(Both Ports -<br>CMOS Level Inputs) | Both Ports $\overline{CE}_L$ and<br>$\overline{CE}_R \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$ or<br>$V_{IN} \leq 0.2V, f = 0^{(3)}$                                      | COM'L     | SA | 1.0                   | 15   | 1.0                    | 15   | 1.0                            | 15   | mA   |
|                  |   |  |           | LA | 0.2                   | 4.5  | 0.2                    | 4.0  | 0.2                            | 4.0  |      |
| I <sub>SB4</sub> | Full Standby Current<br>(One Port -<br>CMOS Level Inputs)   | One Port $\overline{CE}^A$ or<br>$\overline{CE}^B \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$<br>Active Port Outputs Disabled,<br>$f = f_{MAX}^{(3)}$ | COM'L     | SA | 105                   | 170  | 95                     | 170  | 85                             | 160  | mA   |
|                  |   |  |           | LA | 105                   | 130  | 95                     | 120  | 85                             | 110  |      |
|                  |   |  | MIL & IND | SA | —                     | —    | 160                    | 310  | 150                            | 300  |      |
|                  |   |  |           | LA | —                     | —    | 160                    | 260  | 150                            | 250  |      |
|                  |   |  | MIL & IND | SA | —                     | —    | 25                     | 100  | 25                             | 75   |      |
|                  |   |  |           | LA | —                     | —    | 25                     | 80   | 25                             | 55   |      |
|                  |   |  | MIL & IND | SA | —                     | —    | 95                     | 210  | 85                             | 200  |      |
|                  |   |  |           | LA | —                     | —    | 95                     | 170  | 85                             | 160  |      |
|                  |   |  | MIL & IND | SA | —                     | —    | 1.0                    | 30   | 1.0                            | 30   |      |
|                  |   |  |           | LA | —                     | —    | 0.2                    | 10   | 0.2                            | 10   |      |
|                  |   |  | MIL & IND | SA | —                     | —    | 75                     | 180  | 85                             | 170  |      |
|                  |   |  |           | LA | —                     | —    | 75                     | 150  | 85                             | 130  |      |

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| Symbol           | Parameter   | Test Condition   | Version   |    | 7134X45<br>Com'l & Military |      | 7134X55<br>Com'l, Ind<br>& Military |      | 7134X70<br>Com'l & Military |      | Unit |
|------------------|---|--|-----------|----|-----------------------------|------|-------------------------------------|------|-----------------------------|------|------|
|                  |   |  |           |    | Typ.                        | Max. | Typ.                                | Max. | Typ.                        | Max. |      |
| I <sub>CC</sub>  | Dynamic Operating Current<br>(Both Ports Active)            | $\overline{CE} = V_{IL}$<br>Outputs Disabled<br>$f = f_{MAX}^{(3)}$  | COM'L     | SA | 140                         | 240  | 140                                 | 240  | 140                         | 240  | mA   |
|                  |   |  |           | LA | 140                         | 200  | 140                                 | 200  | 140                         | 200  |      |
| I <sub>SB1</sub> | Standby Current<br>(Both Ports - TTL<br>Level Inputs)       | $\overline{CE}_L$ and $\overline{CE}_R = V_{IH}$<br>$f = f_{MAX}^{(3)}$  | COM'L     | SA | 25                          | 70   | 25                                  | 70   | 25                          | 70   | mA   |
|                  |   |  |           | LA | 25                          | 40   | 25                                  | 40   | 25                          | 40   |      |
| I <sub>SB2</sub> | Standby Current<br>(One Port - TTL<br>Level Inputs)         | $\overline{CE}^A = V_{IL}$ and $\overline{CE}^B = V_{IH}$<br>Active Port Outputs Disabled,<br>$f = f_{MAX}^{(3)}$  | COM'L     | SA | 75                          | 160  | 75                                  | 160  | 75                          | 160  | mA   |
|                  |   |  |           | LA | 75                          | 130  | 75                                  | 130  | 75                          | 130  |      |
| I <sub>SB3</sub> | Full Standby Current<br>(Both Ports -<br>CMOS Level Inputs) | Both Ports $\overline{CE}_L$ and<br>$\overline{CE}_R \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$ or<br>$V_{IN} \leq 0.2V, f = 0^{(3)}$                                      | COM'L     | SA | 1.0                         | 15   | 1.0                                 | 15   | 1.0                         | 15   | mA   |
|                  |   |  |           | LA | 0.2                         | 4.0  | 0.2                                 | 4.0  | 0.2                         | 4.0  |      |
| I <sub>SB4</sub> | Full Standby Current<br>(One Port -<br>CMOS Level Inputs)   | One Port $\overline{CE}^A$ or<br>$\overline{CE}^B \geq V_{CC} - 0.2V$<br>$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$<br>Active Port Outputs Disabled,<br>$f = f_{MAX}^{(3)}$ | COM'L     | SA | 75                          | 150  | 75                                  | 150  | 75                          | 150  | mA   |
|                  |   |  |           | LA | 75                          | 100  | 75                                  | 100  | 75                          | 100  |      |
|                  |   |  | MIL & IND | SA | 140                         | 280  | 140                                 | 270  | 140                         | 270  |      |
|                  |   |  |           | LA | 140                         | 240  | 140                                 | 220  | 140                         | 220  |      |
|                  |   |  | MIL & IND | SA | 25                          | 70   | 25                                  | 70   | 25                          | 70   |      |
|                  |   |  |           | LA | 25                          | 50   | 25                                  | 50   | 25                          | 50   |      |
|                  |   |  | MIL & IND | SA | 75                          | 160  | 75                                  | 160  | 75                          | 160  |      |
|                  |   |  |           | LA | 75                          | 130  | 75                                  | 130  | 75                          | 130  |      |
|                  |   |  | MIL & IND | SA | 1.0                         | 30   | 1.0                                 | 30   | 1.0                         | 30   |      |
|                  |   |  |           | LA | 0.2                         | 10   | 0.2                                 | 10   | 0.2                         | 10   |      |
|                  |   |  | MIL & IND | SA | 75                          | 180  | 75                                  | 170  | 75                          | 170  |      |
|                  |   |  |           | LA | 75                          | 120  | 75                                  | 120  | 75                          | 120  |      |

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**NOTES:**

- 'X' in part number indicates power rating (SA or LA).
- $V_{CC} = 5V$ ,  $T_A = +25^\circ C$  for typical, and parameters are not production tested.
- $f_{MAX} = 1/RC =$  All inputs cycling at  $f = 1/RC$  (except Output Enable).  $f = 0$  means no address or control lines change. Applies only to inputs at CMOS level standby I<sub>SB3</sub>.

## Data Retention Characteristics Over All Temperature Ranges

(LA Version Only)  $V_{LC} = 0.2V$ ,  $V_{HC} = V_{CC} - 0.2V$

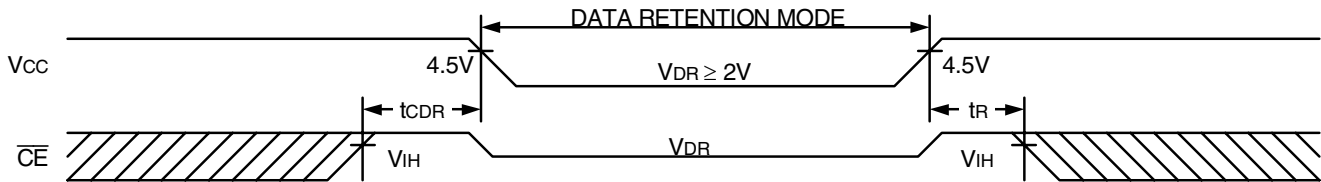
| Symbol                          | Parameter                            | Test Condition   | Min.                           | Typ. <sup>(1)</sup> | Max. | Unit |
|---------------------------------|--------------------------------------|--|--------------------------------|---------------------|------|------|
| V <sub>DR</sub>                 | V <sub>CC</sub> for Data Retention   | V <sub>CC</sub> = 2V   | 2.0                            | —                   | —    | V    |
| I <sub>CCDR</sub>               | Data Retention Current               | $\overline{CE} \geq V_{HC}$<br>$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$ | MIL. & IND.<br>—               | 100                 | 4000 | μA   |
|                                 |                                      |  | COM'L.<br>—                    | 100                 | 1500 |      |
| t <sub>CDR</sub> <sup>(3)</sup> | Chip Deselect to Data Retention Time |  | 0                              | —                   | —    | ns   |
| t <sub>R</sub> <sup>(3)</sup>   | Operation Recovery Time              |  | t <sub>RC</sub> <sup>(2)</sup> | —                   | —    | ns   |

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### NOTES:

- V<sub>CC</sub> = 2V, T<sub>A</sub> = +25°C, and are not production tested.
- t<sub>RC</sub> = Read Cycle Time.
- This parameter is guaranteed by device characterization, but not production tested.

## Data Retention Waveform

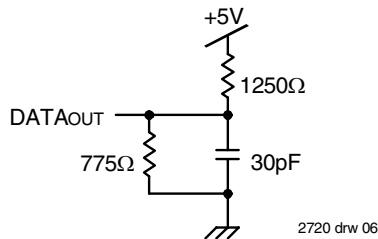


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## AC Test Conditions

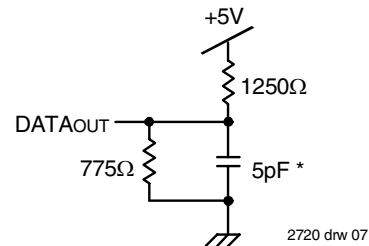
|                               |                 |
|-------------------------------|-----------------|
| Input Pulse Levels            | GND to 3.0V     |
| Input Rise/Fall Times         | 5ns             |
| Input Timing Reference Levels | 1.5V            |
| Output Reference Levels       | 1.5V            |
| Output Load                   | Figures 1 and 2 |

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Figure 1. AC Output Test Load



2720 drw 07

Figure 2. Output Test Load  
(for t<sub>LZ</sub>, t<sub>HZ</sub>, t<sub>WZ</sub>, t<sub>OW</sub>)  
\*Including scope and jig

### AC Electrical Characteristics Over the Operating Temperature and Supply Voltage<sup>(3)</sup>

| Symbol            | Parameter                                      | 7134X20<br>Com'l Only |      | 7134X25<br>Com'l & Ind |      | 7134X35<br>Com'l<br>& Military |      | Unit |
|-------------------|--|-----------------------|------|------------------------|------|--------------------------------|------|------|
|                   |  | Min.                  | Max. | Min.                   | Max. | Min.                           | Max. |      |
| <b>READ CYCLE</b> |  |                       |      |                        |      |                                |      |      |
| t <sub>RC</sub>   | Read Cycle Time                                | 20                    | —    | 25                     | —    | 35                             | —    | ns   |
| t <sub>AA</sub>   | Address Access Time                            | —                     | 20   | —                      | 25   | —                              | 35   | ns   |
| t <sub>ACE</sub>  | Chip Enable Access Time                        | —                     | 20   | —                      | 25   | —                              | 35   | ns   |
| t <sub>AOE</sub>  | Output Enable Access Time                      | —                     | 15   | —                      | 15   | —                              | 20   | ns   |
| t <sub>OH</sub>   | Output Hold from Address Change                | 0                     | —    | 0                      | —    | 0                              | —    | ns   |
| t <sub>LZ</sub>   | Output Low-Z Time <sup>(1,2)</sup>             | 0                     | —    | 0                      | —    | 0                              | —    | ns   |
| t <sub>HZ</sub>   | Output High-Z Time <sup>(1,2)</sup>            | —                     | 15   | —                      | 15   | —                              | 20   | ns   |
| t <sub>PU</sub>   | Chip Enable to Power Up Time <sup>(2)</sup>    | 0                     | —    | 0                      | —    | 0                              | —    | ns   |
| t <sub>PD</sub>   | Chip Disable to Power Down Time <sup>(2)</sup> | —                     | 20   | —                      | 25   | —                              | 35   | ns   |

2720 tbl 09a

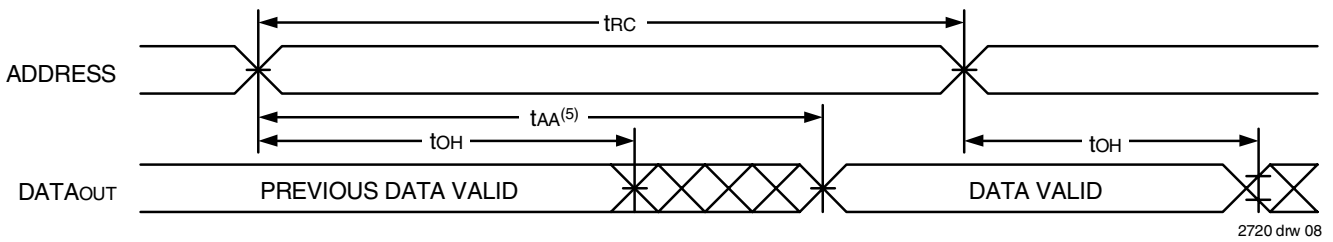
| Symbol            | Parameter                                      | 7134X45<br>Com'l &<br>Military |      | 7134X55<br>Com'l, Ind<br>& Military |      | 7134X70<br>Com'l &<br>Military |      | Unit |
|-------------------|--|--------------------------------|------|-------------------------------------|------|--------------------------------|------|------|
|                   |  | Min.                           | Max. | Min.                                | Max. | Min.                           | Max. |      |
| <b>READ CYCLE</b> |  |                                |      |                                     |      |                                |      |      |
| t <sub>RC</sub>   | Read Cycle Time                                | 45                             | —    | 55                                  | —    | 70                             | —    | ns   |
| t <sub>AA</sub>   | Address Access Time                            | —                              | 45   | —                                   | 55   | —                              | 70   | ns   |
| t <sub>ACE</sub>  | Chip Enable Access Time                        | —                              | 45   | —                                   | 55   | —                              | 70   | ns   |
| t <sub>AOE</sub>  | Output Enable Access Time                      | —                              | 25   | —                                   | 30   | —                              | 40   | ns   |
| t <sub>OH</sub>   | Output Hold from Address Change                | 0                              | —    | 0                                   | —    | 0                              | —    | ns   |
| t <sub>LZ</sub>   | Output Low-Z Time <sup>(1,2)</sup>             | 5                              | —    | 5                                   | —    | 5                              | —    | ns   |
| t <sub>HZ</sub>   | Output High-Z Time <sup>(1,2)</sup>            | —                              | 20   | —                                   | 25   | —                              | 30   | ns   |
| t <sub>PU</sub>   | Chip Enable to Power Up Time <sup>(2)</sup>    | 0                              | —    | 0                                   | —    | 0                              | —    | ns   |
| t <sub>PD</sub>   | Chip Disable to Power Down Time <sup>(2)</sup> | —                              | 45   | —                                   | 50   | —                              | 50   | ns   |

2720 tbl 09b

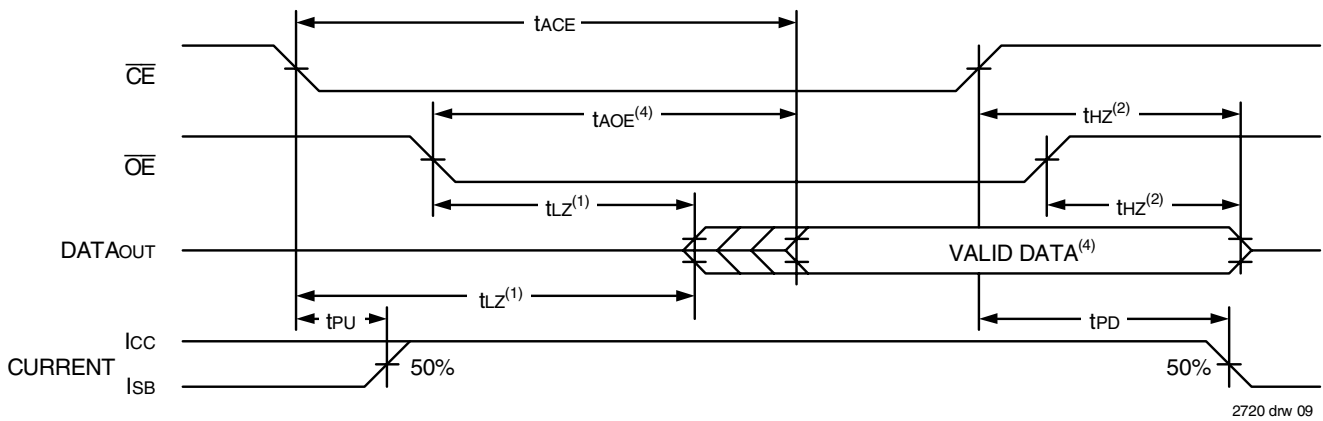
**NOTES:**

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. 'X' in part number indicates power rating (SA or LA).

### Timing Waveform of Read Cycle No. 1, Either Side<sup>(1,2,4)</sup>



### Timing Waveform of Read Cycle No. 2, Either Side<sup>(1,3)</sup>



**NOTES:**

1. Timing depends on which signal is asserted last,  $\overline{OE}$  or  $\overline{CE}$ .
2. Timing depends on which signal is de-asserted first,  $\overline{OE}$  or  $\overline{CE}$ .
3.  $R/\overline{W} = V_{IH}$ .
4. Start of valid data depends on which timing becomes effective,  $t_{AOE}$ ,  $t_{ACE}$  or  $t_{AA}$ .
5.  $t_{AA}$  for RAM Address Access and  $t_{SAA}$  for Semaphore Address Access.

## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage<sup>(5)</sup>

| Symbol             | Parameter  | 7134X20<br>Com'l Only |      | 7134X25<br>Com'l & Ind |      | 7134X35<br>Com'l<br>& Military |      | Unit |
|--------------------|--|-----------------------|------|------------------------|------|--------------------------------|------|------|
|                    |  | Min.                  | Max. | Min.                   | Max. | Min.                           | Max. |      |
| <b>WRITE CYCLE</b> |  |                       |      |                        |      |                                |      |      |
| t <sub>WC</sub>    | Write Cycle Time                                   | 20                    | —    | 25                     | —    | 35                             | —    | ns   |
| t <sub>EW</sub>    | Chip Enable to End-of-Write                        | 15                    | —    | 20                     | —    | 30                             | —    | ns   |
| t <sub>AW</sub>    | Address Valid to End-of-Write                      | 15                    | —    | 20                     | —    | 30                             | —    | ns   |
| t <sub>AS</sub>    | Address Set-up Time                                | 0                     | —    | 0                      | —    | 0                              | —    | ns   |
| t <sub>WP</sub>    | Write Pulse Width                                  | 15                    | —    | 20                     | —    | 25                             | —    | ns   |
| t <sub>WR</sub>    | Write Recovery Time                                | 0                     | —    | 0                      | —    | 0                              | —    | ns   |
| t <sub>DW</sub>    | Data Valid to End-of-Write                         | 15                    | —    | 15                     | —    | 20                             | —    | ns   |
| t <sub>HZ</sub>    | Output High-Z Time <sup>(1,2)</sup>                | —                     | 15   | —                      | 15   | —                              | 20   | ns   |
| t <sub>DH</sub>    | Data Hold Time <sup>(3)</sup>                      | 0                     | —    | 0                      | —    | 3                              | —    | ns   |
| t <sub>WZ</sub>    | Write Enable to Output in High-Z <sup>(1,2)</sup>  | —                     | 15   | —                      | 15   | —                              | 20   | ns   |
| t <sub>OW</sub>    | Output Active from End-of-Write <sup>(1,2,3)</sup> | 3                     | —    | 3                      | —    | 3                              | —    | ns   |
| t <sub>WDD</sub>   | Write Pulse to Data Delay <sup>(4)</sup>           | —                     | 40   | —                      | 50   | —                              | 60   | ns   |
| t <sub>DDD</sub>   | Write Data Valid to Read Data Delay <sup>(4)</sup> | —                     | 30   | —                      | 30   | —                              | 35   | ns   |

2720 tbl 10a

| Symbol             | Parameter  | 7134X45<br>Com'l &<br>Military |      | 7134X55<br>Com'l, Ind<br>& Military |      | 7134X70<br>Com'l &<br>Military |      | Unit |
|--------------------|--|--------------------------------|------|-------------------------------------|------|--------------------------------|------|------|
|                    |  | Min.                           | Max. | Min.                                | Max. | Min.                           | Max. |      |
| <b>WRITE CYCLE</b> |  |                                |      |                                     |      |                                |      |      |
| t <sub>WC</sub>    | Write Cycle Time                                   | 45                             | —    | 55                                  | —    | 70                             | —    | ns   |
| t <sub>EW</sub>    | Chip Enable to End-of-Write                        | 40                             | —    | 50                                  | —    | 60                             | —    | ns   |
| t <sub>AW</sub>    | Address Valid to End-of-Write                      | 40                             | —    | 50                                  | —    | 60                             | —    | ns   |
| t <sub>AS</sub>    | Address Set-up Time                                | 0                              | —    | 0                                   | —    | 0                              | —    | ns   |
| t <sub>WP</sub>    | Write Pulse Width                                  | 40                             | —    | 50                                  | —    | 60                             | —    | ns   |
| t <sub>WR</sub>    | Write Recovery Time                                | 0                              | —    | 0                                   | —    | 0                              | —    | ns   |
| t <sub>DW</sub>    | Data Valid to End-of-Write                         | 20                             | —    | 25                                  | —    | 30                             | —    | ns   |
| t <sub>HZ</sub>    | Output High-Z Time <sup>(1,2)</sup>                | —                              | 20   | —                                   | 25   | —                              | 30   | ns   |
| t <sub>DH</sub>    | Data Hold Time <sup>(3)</sup>                      | 3                              | —    | 3                                   | —    | 3                              | —    | ns   |
| t <sub>WZ</sub>    | Write Enable to Output in High-Z <sup>(1,2)</sup>  | —                              | 20   | —                                   | 25   | —                              | 30   | ns   |
| t <sub>OW</sub>    | Output Active from End-of-Write <sup>(1,2,3)</sup> | 3                              | —    | 3                                   | —    | 3                              | —    | ns   |
| t <sub>WDD</sub>   | Write Pulse to Data Delay <sup>(4)</sup>           | —                              | 70   | —                                   | 80   | —                              | 90   | ns   |
| t <sub>DDD</sub>   | Write Data Valid to Read Data Delay <sup>(4)</sup> | —                              | 45   | —                                   | 55   | —                              | 70   | ns   |

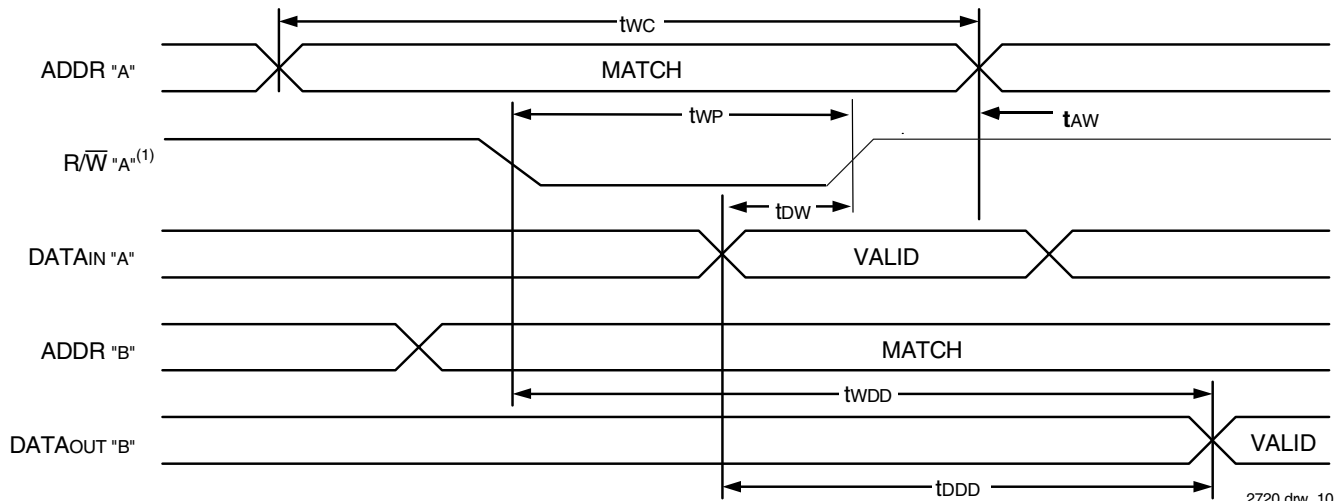
2720 tbl 10b

### NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The specification for t<sub>DH</sub> must be met by the device supplying write data to the RAM under all operating conditions. Although t<sub>DH</sub> and t<sub>OW</sub> values will vary over voltage and temperature, the actual t<sub>DH</sub> will always be smaller than the actual t<sub>OW</sub>.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read".
5. 'X' in part number indicates power rating (SA or LA).



### Timing Waveform of Write with Port-to-Port Read<sup>(1,2,3)</sup>

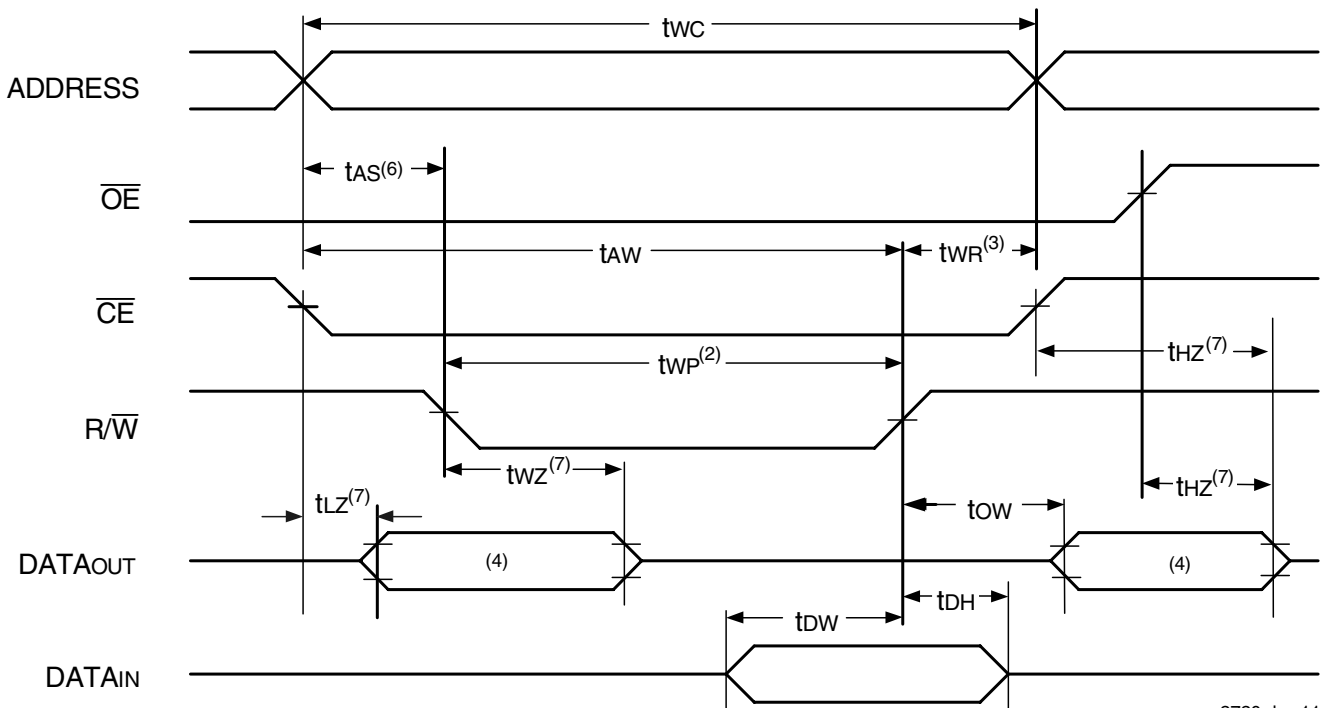


NOTES:

1. Write cycle parameters should be adhered to, in order to ensure proper writing.
2.  $\overline{CE}_L = \overline{CE}_R = V_{IL}$ ,  $\overline{OE}'_B = V_{IL}$ .
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

2720 drw 10

### Timing Waveform of Write Cycle No. 1, R/W Controlled Timing<sup>(1,5,8)</sup>

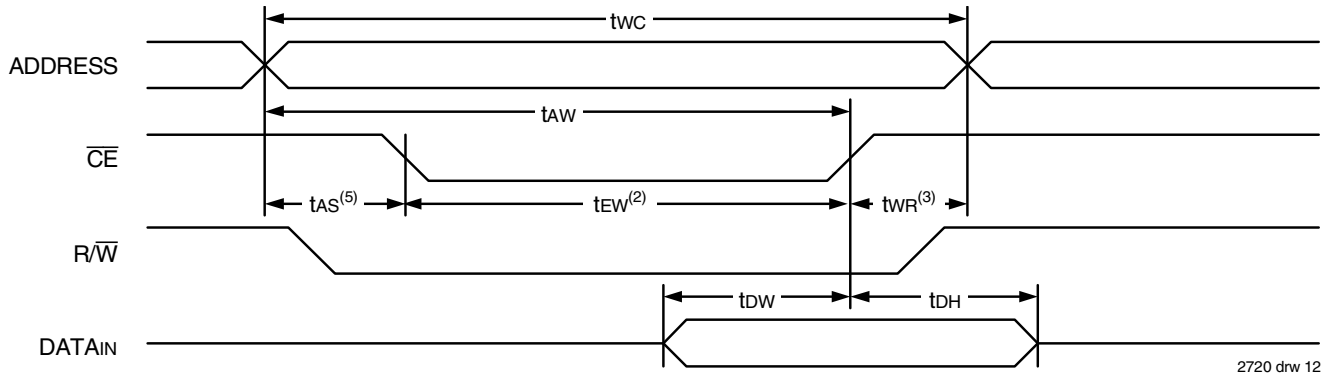


NOTES:

1.  $\overline{R/W}$  or  $\overline{CE}$  must be HIGH during all address transitions.
2. A write occurs during the overlap ( $t_{EW}$  or  $t_{WP}$ ) of a  $\overline{CE} = V_{IL}$  and  $\overline{R/W} = V_{IL}$ .
3.  $t_{WR}$  is measured from the earlier of  $\overline{CE}$  or  $\overline{R/W}$  going to  $V_{IH}$  to the end-of-write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CE} = V_{IL}$  transition occurs simultaneously with or after the  $\overline{R/W} = V_{IL}$  transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ( $\overline{CE}$  or  $\overline{R/W}$ ) is asserted last.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If  $\overline{OE} = V_{IL}$  during a  $\overline{R/W}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or  $(t_{WZ} + t_{OW})$  to allow the I/O drivers to turn off data to be placed on the bus for the required  $t_{OW}$ . If  $\overline{OE} = V_{IH}$  during an  $\overline{R/W}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .

2720 drw 11

### Timing Waveform of Write Cycle No. 2, $\overline{\text{CE}}$ Controlled Timing<sup>(1,4)</sup>



2720 drw 12

**NOTES:**

1.  $\overline{\text{R/W}}$  or  $\overline{\text{CE}}$  must be HIGH during all address transitions.
2. A write occurs during the overlap ( $t_{\text{EW}}$  or  $t_{\text{WP}}$ ) of a  $\overline{\text{CE}} = \text{V}_{\text{IL}}$  and  $\overline{\text{R/W}} = \text{V}_{\text{IL}}$ .
3.  $t_{\text{WR}}$  is measured from the earlier of  $\overline{\text{CE}}$  or  $\overline{\text{R/W}}$  going HIGH to the end-of-write cycle.
4. If the  $\overline{\text{CE}}$  LOW transition occurs simultaneously with or after the  $\overline{\text{R/W}}$  LOW transition, the outputs remain in the High-impedance state.
5. Timing depends on which enable signal ( $\overline{\text{CE}}$  or  $\overline{\text{R/W}}$ ) is asserted last.

### Functional Description

The IDT7134 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by  $\overline{\text{CE}}$ . The  $\overline{\text{CE}}$  controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ( $\overline{\text{CE}}$  HIGH). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ( $\overline{\text{OE}}$ ). In the read mode, the port's  $\overline{\text{OE}}$  turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Truth Table I.

### Truth Table I – Read/Write Control

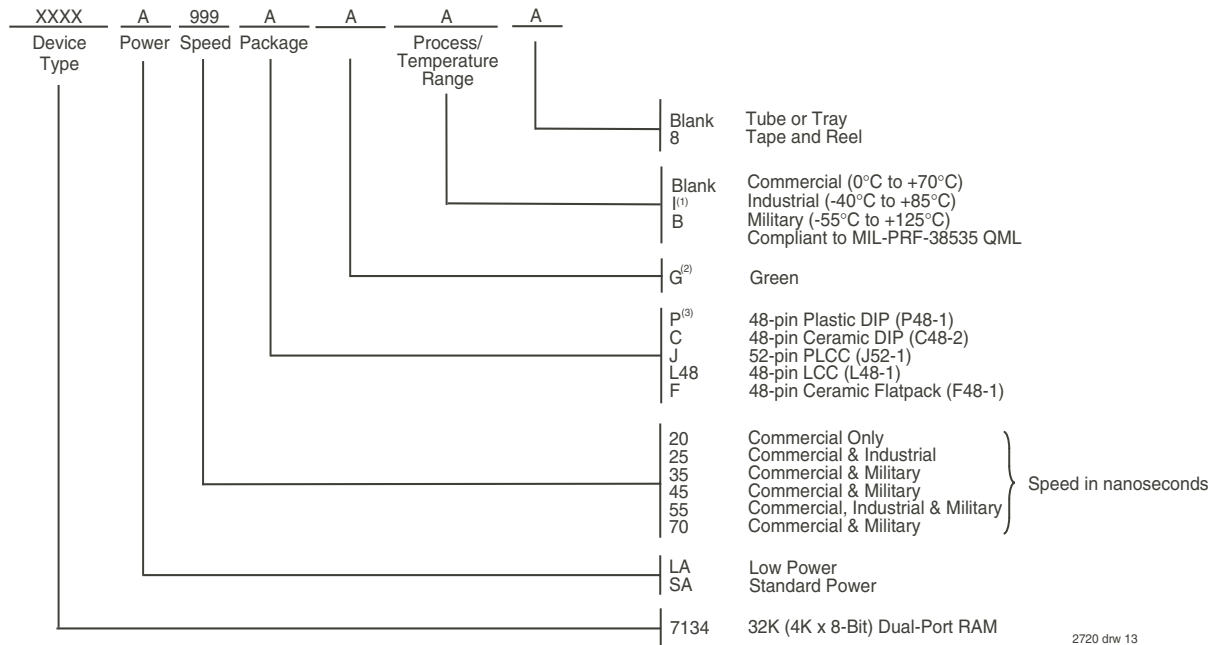
| Left or Right Port <sup>(1)</sup> |                        |                        |                     |   |
|-----------------------------------|------------------------|------------------------|---------------------|---|
| $\overline{\text{R/W}}$           | $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | D0-7                | Function  |
| X                                 | H                      | X                      | Z                   | Port Deselected and in Power-Down Mode, ISB2 or ISB4  |
| X                                 | H                      | X                      | Z                   | $\overline{\text{CE}}_{\text{R}} = \overline{\text{CE}}_{\text{L}} = \text{H}$ , Power Down Mode ISB1 or ISB3 |
| L                                 | L                      | X                      | DATA <sub>IN</sub>  | Data on port written into memory  |
| H                                 | L                      | L                      | DATA <sub>OUT</sub> | Data in memory output on port   |
| X                                 | X                      | H                      | Z                   | High impedance outputs  |

2720 tbl 11

**NOTE:**

1. A0L - A11L  $\neq$  A0R - A11R  
"H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>, "X" = Don't Care, and "Z" = High Impedance

## Ordering Information



### NOTES:

1. Contact your local sales office for industrial temp. range for other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.
3. For "P", plastic DIP, when ordering green package the suffix is "PDG".

## Datasheet Document History

|           |             |   |
|-----------|-------------|---|
| 03/25/99: |             | Initiated datasheet document history<br>Converted to new format<br>Cosmetic and typographical corrections |
| 06/09/99: | Pages 2     | Added additional notes to pin configurations<br>Changed drawing format                                    |
| 10/01/99: |             | Added Industrial Temperature Ranges and removed corresponding notes                                       |
| 11/10/99: |             | Replaced IDT logo   |
| 12/22/99: | Page 1      | Made corrections to drawing   |
| 03/03/00: |             | Corrected block diagram and pin configurations<br>Changed ±500mV to 0mV                                   |
| 01/12/00: | Pages 1 2   | Moved "Description to page 2 and adjusted page layout   |
|           | Page 1      | Added "LA only)" to paragraph   |
|           | Page 2      | Fixed P48-1 package description   |
|           | Page 3      | Increased storage temperature parameters<br>Clarified TA parameter  |
|           | Page 4      | DC Electrical parameters—changed wording from "open" to "disabled"  |
|           | Page 10     | Fixed Truth Table specification in "Functional Description" paragraph                                     |
| 01/17/06: | Page 1      | Added green availability to features  |
|           | Page 11     | Added green indicator to ordering information   |
|           | Page 1 & 11 | Replaced old IDT™ with new IDT™ logo  |
| 08/12/08: | Page 11     | Corrected typo in the ordering information  |

## Datasheet Document History (con't.)

|           |                  |  |
|-----------|------------------|--|
| 08/12/08: | Page 11          | Corrected typo in the ordering information   |
| 10/21/08: | Page 11          | Removed "IDT" from orderable part number   |
| 02/04/13: | Page 1, 4, 6 & 8 | Removed Military 25ns & Industrial 35ns speed grades from Features and corrected the headers of the DC Chars and AC Chars tables to indicate this change |
|           | Page 11          | Added T & R indicator to and removed Military 25ns & Industrial 35ns speed grades from the ordering information  |
|           | Page 2           | Typo/correction  |



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