

ISL22346

Quad Digitally Controlled Potentiometers (XDCP™) Low Noise, Low Power I<sup>2</sup>C™ Bus, 128 Taps

FN6177  
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The ISL22346 integrates four digitally controlled potentiometers (DCP) and non-volatile memory on a monolithic CMOS integrated circuit.

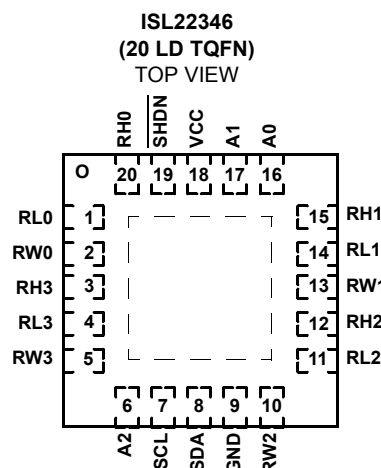
The digitally controlled potentiometers are implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I<sup>2</sup>C bus interface. Each potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper. At power-up the device recalls the contents of the two DCP's IVR to the corresponding WRs.

The DCPs can be used as a three-terminal potentiometers or as a two-terminal variable resistors in a wide variety of applications including control, parameter adjustments, and signal processing.

**Features**

- Four potentiometers in one package
- 128 resistor taps
- I<sup>2</sup>C serial interface
  - Three address pins, up to eight devices/bus
- Non-volatile storage of wiper position
- Wiper resistance: 70Ω typical @ V<sub>CC</sub> = 3.3V
- Shutdown mode
- Shutdown current 5μA max
- Power supply: 2.7V to 5.5V
- 50kΩ or 10kΩ total resistance
- High reliability
  - Endurance: 1,000,000 data changes per bit per register
  - Register data retention: 50 years @ T ≤ +55°C
- 20 Ld TSSOP or 20 Ld TQFN package
- Pb-free (RoHS compliant)

**Pinouts**



## Ordering Information

| PART NUMBER<br>(Note) | PART<br>MARKING | RESISTANCE OPTION<br>(k $\Omega$ ) | TEMP. RANGE<br>(°C) | PACKAGE<br>(Pb-free) | PKG.<br>DWG. # |
|-----------------------|-----------------|------------------------------------|---------------------|----------------------|----------------|
| ISL22346UFV20Z*       | 22346 UFVZ      | 50                                 | -40 to +125         | 20 Ld TSSOP          | M20.173        |
| ISL22346UFRT20Z*      | 223 46UFZ       | 50                                 | -40 to +125         | 20 Ld 4x4 TQFN       | L20.4x4A       |
| ISL22346WFV20Z*       | 22346 WFVZ      | 10                                 | -40 to +125         | 20 Ld TSSOP          | M20.173        |
| ISL22346WFRT20Z*      | 223 46WFZ       | 10                                 | -40 to +125         | 20 Ld 4x4 TQFN       | L20.4x4A       |

\*Add "-TK" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Block Diagram



## Pin Descriptions

| TSSOP PIN NUMBER | TQFN PIN NUMBER | PIN NAME | DESCRIPTION   |
|------------------|-----------------|----------|---|
| 1                | 3               | RH3      | "High" terminal of DCP3                                       |
| 2                | 4               | RL3      | "Low" terminal of DCP3  |
| 3                | 5               | RW3      | "Wiper" terminal of DCP3                                      |
| 4                | 6               | A2       | Device address input for the I <sup>2</sup> C interface       |
| 5                | 7               | SCL      | Open drain I <sup>2</sup> C interface clock input             |
| 6                | 8               | SDA      | Open drain Serial data I/O for the I <sup>2</sup> C interface |
| 7                | 9               | GND      | Device ground pin   |
| 8                | 10              | RW2      | "Wiper" terminal of DCP2                                      |
| 9                | 11              | RL2      | "Low" terminal of DCP2  |
| 10               | 12              | RH2      | "High" terminal of DCP2                                       |
| 11               | 13              | RW1      | "Wiper" terminal of DCP1                                      |
| 12               | 14              | RL1      | "Low" terminal of DCP1  |
| 13               | 15              | RH1      | "High" terminal of DCP1                                       |
| 14               | 16              | A0       | Device address input for the I <sup>2</sup> C interface       |

**Pin Descriptions** (Continued)

| TSSOP PIN NUMBER | TQFN PIN NUMBER | PIN NAME                 | DESCRIPTION   |
|------------------|-----------------|--------------------------|---|
| 15               | 17              | A1                       | Device address input for the I <sup>2</sup> C interface |
| 16               | 18              | VCC                      | Power supply pin  |
| 17               | 19              | $\overline{\text{SHDN}}$ | Shutdown active low input                               |
| 18               | 20              | RH0                      | "High" terminal of DCP0                                 |
| 19               | 1               | RL0                      | "Low" terminal of DCP0                                  |
| 20               | 2               | RW0                      | "Wiper" terminal of DCP0                                |
|                  | EPAD*           |                          | Exposed Die Pad internally connected to GND             |

\*Note: PCB thermal land for QFN EPAD should be connected to GND plane or left floating. For more information refer to <http://www.intersil.com/data/tb/TB389.pdf>

**Absolute Maximum Ratings**

|   |                            |
|---|----------------------------|
| Storage Temperature   | -65°C to +150°C            |
| Voltage at any Digital Interface Pin<br>with Respect to GND | -0.3V to $V_{CC} + 0.3$    |
| $V_{CC}$  | -0.3V to +6V               |
| Voltage at any DCP Pin with Respect to GND                  | -0.3V to $V_{CC}$          |
| $I_W$ (10s)   | ±6mA                       |
| Latchup (Note 4)  | Class II, Level B @ +125°C |
| <b>ESD Ratings</b>  |                            |
| Human Body Model  | 2.5kV                      |
| Machine Model   | 350V                       |

**Thermal Information**

|  |   |                      |
|--|---|----------------------|
| Thermal Resistance (Typical)                   | $\theta_{JA}$ (°C/W)  | $\theta_{JC}$ (°C/W) |
| 20 Lead TSSOP (Note 1)                         | 95  | N/A                  |
| 20 Lead TQFN (Notes 2, 3)                      | 40  | 3.0                  |
| Maximum Junction Temperature (Plastic Package) | +150°C  |                      |
| Pb-free Reflow Profile                         | see link below<br><a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a> |                      |

**Recommended Operating Conditions**

|   |                 |
|---|-----------------|
| Temperature Range (Extended Industrial) | -40°C to +125°C |
| $V_{CC}$                                | 2.7V to 5.5V    |
| Power Rating                            | 15mW            |
| Wiper Current                           | ±3.0mA          |

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

**NOTES:**

- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.
- Jedec Class II pulse conditions and failure criterion used. Level B exceptions are: using a max positive pulse of 6.5V on the SHDN pin, and using a max negative pulse of -0.8V for all pins.

**Analog Specifications** Over recommended operating conditions, unless otherwise stated.

| SYMBOL   | PARAMETER                               | TEST CONDITIONS   | MIN<br>(Note 21) | TYP<br>(Note 5) | MAX<br>(Note 21) | UNIT                |
|--|---|---|------------------|-----------------|------------------|---------------------|
| $R_{TOTAL}$  | $R_H$ to $R_L$ Resistance               | W option  |                  | 10              |                  | k $\Omega$          |
|  |   | U option  |                  | 50              |                  | k $\Omega$          |
|  | $R_H$ to $R_L$ Resistance Tolerance     | W and U option  | -20              |                 | +20              | %                   |
|  | End-to-End Temperature Coefficient      | W option  |                  |                 | ±50              |                     |
| U option   |   |   |                  | ±80             |                  | ppm/°C<br>(Note 18) |
| $V_{RH}$ , $V_{RL}$  | $V_{RH}$ and $V_{RL}$ Terminal Voltages | $V_{RH}$ and $V_{RL}$ to GND  | 0                |                 | $V_{CC}$         | V                   |
| $R_W$  | Wiper Resistance                        | $V_{CC} = 3.3V$ , wiper current = $V_{CC}/R_{TOTAL}$  |                  | 70              | 200              | $\Omega$            |
| $C_H/C_L/C_W$<br>(Note 20)   | Potentiometer Capacitance               |   |                  | 10/10/25        |                  | pF                  |
| $I_{LkgDCP}$   | Leakage on DCP Pins                     | Voltage at pin from GND to $V_{CC}$   |                  | 0.1             | 1                | $\mu A$             |
| <b>VOLTAGE DIVIDER MODE</b> (0V @ $R_L$ ; $V_{CC}$ @ $R_H$ ; measured at $R_{Wi}$ , unloaded; $i = 0, 1, 2, \text{ or } 3$ ) |   |   |                  |                 |                  |                     |
| INL<br>(Note 10)   | Integral Non-linearity                  | Monotonic over all tap positions  | -1               |                 | 1                | LSB<br>(Note 6)     |
| DNL<br>(Note 9)  | Differential Non-linearity              | Monotonic over all tap positions  | -0.5             |                 | 0.5              | LSB<br>(Note 6)     |
| ZSerror<br>(Note 7)  | Zero-scale Error                        | W option  | 0                | 1               | 5                | LSB<br>(Note 6)     |
|  |   | U option  | 0                | 0.5             | 2                |                     |
| FSerror<br>(Note 8)  | Full-scale error                        | W option  | -5               | -1              | 0                | LSB<br>(Note 6)     |
|  |   | U option  | -2               | -1              | 0                |                     |
| $V_{MATCH}$<br>(Note 11)   | DCP to DCP Matching                     | Any two DCPs at same tap position, same voltage at all $R_H$ terminals, and same voltage at all $R_L$ terminals | -2               |                 | 2                | LSB<br>(Note 6)     |

**Analog Specifications** Over recommended operating conditions, unless otherwise stated. (Continued)

| SYMBOL   | PARAMETER                           | TEST CONDITIONS   | MIN<br>(Note 21) | TYP<br>(Note 5) | MAX<br>(Note 21) | UNIT            |
|--|-------------------------------------|---|------------------|-----------------|------------------|-----------------|
| $TC_V$<br>(Note 12)  | Ratiometric Temperature Coefficient | DCP register set to 40 hex  |                  | ±4              |                  | ppm/°C          |
| <b>RESISTOR MODE</b> (Measurements between $R_{W_i}$ and $R_{L_i}$ with $R_{H_i}$ not connected, or between $R_{W_i}$ and $R_{H_i}$ with $R_{L_i}$ not connected. $i = 0, 1, 2$ or $3$ ) |                                     |   |                  |                 |                  |                 |
| $R_{INL}$<br>(Note 16)   | Integral Non-linearity              | DCP register set between 10h and 7Fh;<br>monotonic over all tap positions           | -1               |                 | 1                | MI<br>(Note 13) |
| $RDNL$<br>(Note 15)  | Differential Non-linearity          | DCP register set between 10h and 7Fh;<br>monotonic over all tap positions, W option | -1               |                 | 1                | MI<br>(Note 13) |
|  |                                     | DCP register set between 10h and 7Fh;<br>monotonic over all tap positions, U option | -0.5             |                 | 0.5              | MI<br>(Note 13) |
| Roffset<br>(Note 14)   | Offset                              | W option  | 0                | 1               | 5                | MI<br>(Note 13) |
|  |                                     | U option  | 0                | 0.5             | 2                | MI<br>(Note 13) |
| $R_{MATCH}$<br>(Note 17)   | DCP to DCP Matching                 | Any two DCPs at the same tap position with<br>the same terminal voltages            | -2               |                 | 2                | MI<br>(Note 13) |

**Operating Specifications** Over the recommended operating conditions, unless otherwise specified.

| SYMBOL                     | PARAMETER  | TEST CONDITIONS  | MIN<br>(Note 21) | TYP<br>(Note 5) | MAX<br>(Note 21) | UNIT |
|----------------------------|--|--|------------------|-----------------|------------------|------|
| $I_{CC1}$                  | $V_{CC}$ Supply Current (Volatile Write/Read)          | $f_{SCL} = 400\text{kHz}$ ; SDA = Open; (for I <sup>2</sup> C, active, read and write states)  |                  |                 | 0.5              | mA   |
| $I_{CC2}$                  | $V_{CC}$ Supply Current (Non-volatile Write/Read)      | $f_{SCL} = 400\text{kHz}$ ; SDA = Open; (for I <sup>2</sup> C, active, read and write states)  |                  |                 | 3                | mA   |
| $I_{SB}$                   | $V_{CC}$ Current (Standby)                             | $V_{CC} = +5.5\text{V @ } +85^\circ\text{C}$ , I <sup>2</sup> C interface in standby state     |                  |                 | 5                | μA   |
|                            |  | $V_{CC} = +5.5\text{V @ } +125^\circ\text{C}$ , I <sup>2</sup> C interface in standby state    |                  |                 | 7                | μA   |
|                            |  | $V_{CC} = +3.6\text{V @ } +85^\circ\text{C}$ , I <sup>2</sup> C interface in standby state     |                  |                 | 3                | μA   |
|                            |  | $V_{CC} = +3.6\text{V @ } +125^\circ\text{C}$ , I <sup>2</sup> C interface in standby state    |                  |                 | 5                | μA   |
| $I_{SD}$                   | $V_{CC}$ Current (Shutdown)                            | $V_{CC} = +5.5\text{V @ } +85^\circ\text{C}$ , I <sup>2</sup> C interface in standby state     |                  |                 | 3                | μA   |
|                            |  | $V_{CC} = +5.5\text{V @ } +125^\circ\text{C}$ , I <sup>2</sup> C interface in standby state    |                  |                 | 5                | μA   |
|                            |  | $V_{CC} = +3.6\text{V @ } +85^\circ\text{C}$ , I <sup>2</sup> C interface in standby state     |                  |                 | 2                | μA   |
|                            |  | $V_{CC} = +3.6\text{V @ } +125^\circ\text{C}$ , I <sup>2</sup> C interface in standby state    |                  |                 | 4                | μA   |
| $I_{LkDig}$                | Leakage Current, at Pins A0, A1, A2, SHDN, SDA and SCL | Voltage at pin from GND to $V_{CC}$  | -1               |                 | 1                | μA   |
| $t_{WRT}$<br>(Note 20)     | DCP Wiper Response Time                                | SCL falling edge of last bit of DCP data byte to wiper new position                            |                  | 1.5             |                  | μs   |
| $t_{ShdnRec}$<br>(Note 20) | DCP Recall Time from Shutdown Mode                     | From rising edge of $\overline{\text{SHDN}}$ signal to wiper stored position and RH connection |                  | 1.5             |                  | μs   |
|                            |  | SCL falling edge of last bit of ACR data byte to wiper stored position and RH connection       |                  | 1.5             |                  | μs   |
| $V_{por}$                  | Power-on Recall Voltage                                | Minimum $V_{CC}$ at which memory recall occurs   | 2.0              |                 | 2.6              | V    |

**Operating Specifications** Over the recommended operating conditions, unless otherwise specified. (Continued)

| SYMBOL                                 | PARAMETER   | TEST CONDITIONS  | MIN<br>(Note 21)     | TYP<br>(Note 5) | MAX<br>(Note 21)      | UNIT   |
|--|---|--|----------------------|-----------------|-----------------------|--------|
| V <sub>CC</sub> Ramp                   | V <sub>CC</sub> Ramp Rate   |  | 0.2                  |                 |                       | V/ms   |
| t <sub>D</sub>                         | Power-up Delay  | V <sub>CC</sub> above V <sub>por</sub> , to DCP Initial Value Register recall completed, and I <sup>2</sup> C Interface in standby state |                      |                 | 3                     | ms     |
| <b>EEPROM SPECIFICATION</b>            |   |  |                      |                 |                       |        |
|  | EEPROM Endurance  |  | 1,000,000            |                 |                       | Cycles |
|  | EEPROM Retention  | Temperature T ≤ +55°C  | 50                   |                 |                       | Years  |
| t <sub>WC</sub><br>(Note 19)           | Non-volatile Write Cycle Time   |  |                      | 12              | 20                    | ms     |
| <b>SERIAL INTERFACE SPECIFICATIONS</b> |   |  |                      |                 |                       |        |
| V <sub>IL</sub>                        | A2, A1, A0, $\overline{\text{SHDN}}$ , SDA, and SCL Input Buffer LOW Voltage  |  | -0.3                 |                 | 0.3*V <sub>CC</sub>   | V      |
| V <sub>IH</sub>                        | A2, A1, A0, $\overline{\text{SHDN}}$ , SDA, and SCL Input Buffer HIGH Voltage |  | 0.7*V <sub>CC</sub>  |                 | V <sub>CC</sub> + 0.3 | V      |
| Hysteresis                             | SDA and SCL Input Buffer Hysteresis   |  | 0.05*V <sub>CC</sub> |                 |                       | V      |
| V <sub>OL</sub>                        | SDA Output Buffer LOW Voltage, Sinking 4mA                                    |  | 0                    |                 | 0.4                   | V      |
| C <sub>pin</sub><br>(Note 20)          | A2, A1, A0, $\overline{\text{SHDN}}$ , SDA, and SCL Pin Capacitance           |  |                      | 10              |                       | pF     |
| f <sub>SCL</sub>                       | SCL Frequency   |  |                      |                 | 400                   | KHz    |
| t <sub>sp</sub>                        | Pulse Width Suppression Time at SDA and SCL Inputs                            | Any pulse narrower than the max spec is suppressed   |                      |                 | 50                    | ns     |
| t <sub>AA</sub>                        | SCL Falling Edge to SDA Output Data Valid                                     | SCL falling edge crossing 30% of V <sub>CC</sub> , until SDA exits the 30% to 70% of V <sub>CC</sub> window                              |                      |                 | 900                   | ns     |
| t <sub>BUF</sub>                       | Time the Bus Must be Free Before the Start of a New Transmission              | SDA crossing 70% of V <sub>CC</sub> during a STOP condition, to SDA crossing 70% of V <sub>CC</sub> during the following START condition | 1300                 |                 |                       | ns     |
| t <sub>LOW</sub>                       | Clock LOW Time  | Measured at the 30% of V <sub>CC</sub> crossing  | 1300                 |                 |                       | ns     |
| t <sub>HIGH</sub>                      | Clock HIGH Time   | Measured at the 70% of V <sub>CC</sub> crossing  | 600                  |                 |                       | ns     |
| t <sub>SU:STA</sub>                    | START Condition Setup Time  | SCL rising edge to SDA falling edge; both crossing 70% of V <sub>CC</sub>  | 600                  |                 |                       | ns     |
| t <sub>HD:STA</sub>                    | START Condition Hold Time   | From SDA falling edge crossing 30% of V <sub>CC</sub> to SCL falling edge crossing 70% of V <sub>CC</sub>                                | 600                  |                 |                       | ns     |
| t <sub>SU:DAT</sub>                    | Input Data Setup Time   | From SDA exiting the 30% to 70% of V <sub>CC</sub> window, to SCL rising edge crossing 30% of V <sub>CC</sub>                            | 100                  |                 |                       | ns     |
| t <sub>HD:DAT</sub>                    | Input Data Hold Time  | From SCL rising edge crossing 70% of V <sub>CC</sub> to SDA entering the 30% to 70% of V <sub>CC</sub> window                            | 0                    |                 |                       | ns     |
| t <sub>SU:STO</sub>                    | STOP Condition Setup Time   | From SCL rising edge crossing 70% of V <sub>CC</sub> , to SDA rising edge crossing 30% of V <sub>CC</sub>                                | 600                  |                 |                       | ns     |
| t <sub>HD:STO</sub>                    | STOP Condition Hold Time for Read, or Volatile Only Write                     | From SDA rising edge to SCL falling edge; both crossing 70% of V <sub>CC</sub>   | 1300                 |                 |                       | ns     |
| t <sub>DH</sub>                        | Output Data Hold Time   | From SCL falling edge crossing 30% of V <sub>CC</sub> , until SDA enters the 30% to 70% of V <sub>CC</sub> window                        | 0                    |                 |                       | ns     |
| t <sub>R</sub>                         | SDA and SCL Rise Time   | From 30% to 70% of V <sub>CC</sub>   | 20 +<br>0.1*Cb       |                 | 250                   | ns     |

**Operating Specifications** Over the recommended operating conditions, unless otherwise specified. (Continued)

| SYMBOL            | PARAMETER                                    | TEST CONDITIONS   | MIN<br>(Note 21) | TYP<br>(Note 5) | MAX<br>(Note 21) | UNIT |
|-------------------|--|---|------------------|-----------------|------------------|------|
| t <sub>F</sub>    | SDA and SCL Fall Time                        | From 70% to 30% of V <sub>CC</sub>  | 20 +<br>0.1*Cb   |                 | 250              | ns   |
| C <sub>b</sub>    | Capacitive Loading of SDA or SCL             | Total on-chip and off-chip  | 10               |                 | 400              | pF   |
| R <sub>pu</sub>   | SDA and SCL Bus Pull-up Resistor<br>Off-chip | Maximum is determined by t <sub>R</sub> and t <sub>F</sub><br>For C <sub>b</sub> = 400pF, max is about 2kΩ~2.5kΩ<br>For C <sub>b</sub> = 40pF, max is about 15kΩ~20kΩ | 1                |                 |                  | kΩ   |
| t <sub>SU:A</sub> | A2, A1 and A0 Setup Time                     | Before START condition  | 600              |                 |                  | ns   |
| t <sub>HD:A</sub> | A2, A1 and A0 Hold Time                      | After STOP condition  | 600              |                 |                  | ns   |

## NOTES:

- Typical values are for T<sub>A</sub> = +25°C and 3.3V supply voltage.
- LSB:  $[V(RW)_{127} - V(RW)_0]/127$ . V(RW)<sub>127</sub> and V(RW)<sub>0</sub> are V(RW) for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
- ZS error = V(RW)<sub>0</sub>/LSB.
- FS error =  $[V(RW)_{127} - V_{CC}]/LSB$ .
- DNL =  $[V(RW)_i - V(RW)_{i-1}]/LSB - 1$ , for i = 1 to 127. i is the DCP register setting.
- INL =  $[V(RW)_i - i \cdot LSB - V(RW)_0]/LSB$  for i = 1 to 127.
- V<sub>MATCH</sub> =  $[V(RW)_x - V(RW)_y]/LSB$ , for i = 1 to 127, x = 0 to 3 and y = 0 to 3.
- $TC_V = \frac{\text{Max}(V(RW)_i) - \text{Min}(V(RW)_i)}{[\text{Max}(V(RW)_i) + \text{Min}(V(RW)_i)]/2} \times \frac{10^6}{+165^\circ\text{C}}$  for i = 16 to 112 decimal, T = -40°C to +125°C. Max( ) is the maximum value of the wiper voltage and Min( ) is the minimum value of the wiper voltage over the temperature range.
- MI =  $|RW_{127} - RW_0|/127$ . RW<sub>127</sub> and RW<sub>0</sub> are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.
- R<sub>offset</sub> = RW<sub>0</sub>/MI, when measuring between RW and RL.  
R<sub>offset</sub> = RW<sub>127</sub>/MI, when measuring between RW and RH.
- RDNL =  $(RW_i - RW_{i-1})/MI - 1$ , for i = 16 to 127.
- RINL =  $[RW_i - (MI \cdot i) - RW_0]/MI$ , for i = 16 to 127.
- R<sub>MATCH</sub> =  $(RW_{i,x} - RW_{i,y})/MI$ , for i = 1 to 127, x = 0 to 3 and y = 0 to 3.
- $TC_R = \frac{[\text{Max}(Ri) - \text{Min}(Ri)]}{[\text{Max}(Ri) + \text{Min}(Ri)]/2} \times \frac{10^6}{+165^\circ\text{C}}$  for i = 16 to 112, T = -40°C to +125°C. Max( ) is the maximum value of the resistance and Min( ) is the minimum value of the resistance over the temperature range.
- t<sub>WC</sub> is the time from a valid STOP condition at the end of a Write sequence of I<sup>2</sup>C serial interface, to the end of the self-timed internal non-volatile write cycle.
- Limits should be considered typical and are not production tested.
- Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

**SDA vs SCL Timing**



**A0, A1, and A2 Pin Timing**



**Typical Performance Curves**



FIGURE 1. WIPER RESISTANCE vs TAP POSITION [  $I(RW) = V_{CC}/R_{TOTAL}$  ] FOR 10k $\Omega$  (W)



FIGURE 2. STANDBY  $I_{CC}$  vs  $V_{CC}$



**Typical Performance Curves** (Continued)



**FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)**



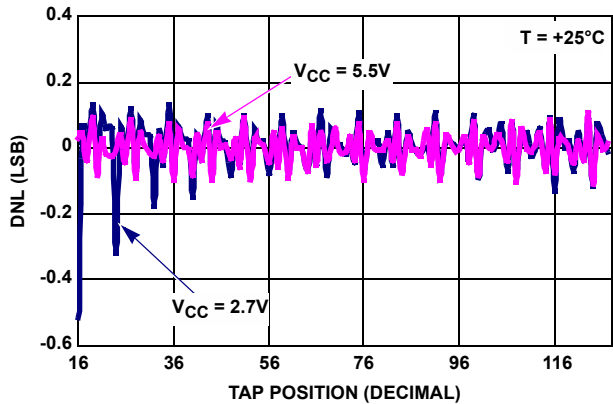
**FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)**



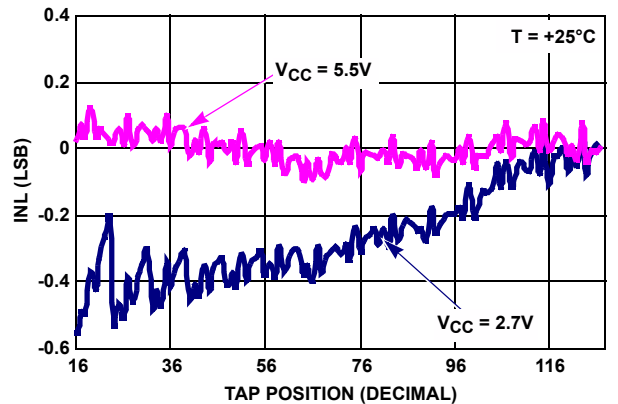
**FIGURE 5. ZSEERROR vs TEMPERATURE**



**FIGURE 6. FSEERROR vs TEMPERATURE**



**FIGURE 7. DNL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)**



**FIGURE 8. INL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)**

**Typical Performance Curves** (Continued)



FIGURE 9. END TO END R<sub>TOTAL</sub> % CHANGE vs TEMPERATURE



FIGURE 10. TC FOR VOLTAGE DIVIDER MODE IN ppm



FIGURE 11. TC FOR RHEOSTAT MODE IN ppm



FIGURE 12. FREQUENCY RESPONSE (2.6MHz)



FIGURE 13. MIDSCALE GLITCH, CODE 3Fh TO 40h



FIGURE 14. LARGE SIGNAL SETTLING TIME

## Pin Descriptions

### Potentiometers Pins

#### RHI AND RLI (i = 0, 1, 2 OR 3)

The high (RHi) and low (RLi) terminals of the ISL22346 are equivalent to the fixed terminals of a mechanical potentiometer. RHi and RLi are referenced to the relative position of the wiper and not the voltage potential on the terminals. With WRi set to 127 decimal, the wiper will be closest to RHi, and with the WRi set to 0, the wiper is closest to RLi.

#### RWI (i = 0, 1, 2 OR 3)

RWi is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WRi register.

#### SHDN

The SHDN pin forces the resistor to end-to-end open circuit condition on RHi and shorts RWi to RLi. When SHDN is returned to logic high, the previous latch settings put RWi at the same resistance setting prior to shutdown. This pin is logically ANDed with SHDN bit in ACR register. I<sup>2</sup>C interface is still available in shutdown mode and all registers are accessible. This pin must remain HIGH for normal operation.



FIGURE 15. DCP CONNECTION IN SHUTDOWN MODE

### Bus Interface Pins

#### SERIAL DATA INPUT/OUTPUT (SDA)

The SDA is a bidirectional serial data input/output pin for I<sup>2</sup>C interface. It receives device address, operation code, wiper address and data from an I<sup>2</sup>C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock.

SDA requires an external pull-up resistor, since it is an open drain input/output.

#### SERIAL CLOCK (SCL)

This is the serial clock input of the I<sup>2</sup>C serial interface. SCL requires an external pull-up resistor, since it is an open drain input.

#### DEVICE ADDRESS (A2 - A0)

The address inputs are used to set the least significant 3 bits of the 7-bit I<sup>2</sup>C interface slave address. A match in the slave address serial data stream must match with the Address input

pins in order to initiate communication with the ISL22346. A maximum of 8 ISL22346 devices may occupy the I<sup>2</sup>C serial bus.

## Principles of Operation

The ISL22346 is an integrated circuit incorporating four DCPs with their associated registers, non-volatile memory and an I<sup>2</sup>C serial interface providing direct communication between a host and the potentiometers and memory. The resistor arrays are comprised of individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions.

When the device is powered down, the last value stored in IVRi will be maintained in the non-volatile memory. When power is restored, the contents of the IVRi are recalled and loaded into the corresponding WRi to set the wipers to the initial value.

### DCP Description

Each DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (RH and RL pins). The RW pin of each DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by volatile Wiper Register (WR). Each DCP has its own WR. When the WR of a DCP contains all zeroes (WR[6:0]= 00h), its wiper terminal (RW) is closest to its “Low” terminal (RL). When the WR register of a DCP contains all ones (WR[6:0]= 7Fh), its wiper terminal (RW) is closest to its “High” terminal (RH). As the value of the WR increases from all zeroes (0) to all ones (127 decimal), the wiper moves monotonically from the position closest to RL to the closest to RH. At the same time, the resistance between RW and RL increases monotonically, while the resistance between RH and RW decreases monotonically.

While the ISL22346 is being powered up, all four WRs are reset to 40h (64 decimal), which locates RW roughly at the center between RL and RH. After the power supply voltage becomes large enough for reliable non-volatile memory reading, all WRs will be reload with the value stored in corresponding non-volatile Initial Value Registers (IVRs).

The WRs can be read or written to directly using the I<sup>2</sup>C serial interface as described in the following sections. The I<sup>2</sup>C interface Address Byte has to be set to 00h, 01h, 02h or 03h to access the WR of DCP0, DCP1, DCP2 or DCP3 respectively.

### Memory Description

The ISL22346 contains seven non-volatile and five volatile 8-bit registers. The memory map of ISL22346 is on Table 1. The four non-volatile registers (IVRi) at address 0, 1, 2 and 3 contain initial wiper value and volatile registers (WRi) contain

current wiper position. In addition, three non-volatile General Purpose registers from address 4 to address 6 are available.

**TABLE 1. MEMORY MAP**

| ADDRESS | NON-VOLATILE    | VOLATILE      |
|---------|-----------------|---------------|
| 8       | —               | ACR           |
| 7       | Reserved        |               |
| 6       | General Purpose | Not Available |
| 5       | General Purpose | Not Available |
| 4       | General Purpose | Not Available |
| 3       | IVR3            | WR3           |
| 2       | IVR2            | WR2           |
| 1       | IVR1            | WR1           |
| 0       | IVR0            | WR0           |

The non-volatile IVR<sub>i</sub> and volatile WR<sub>i</sub> registers are accessible with the same address.

The Access Control Register (ACR) contains information and control bits described in Table 2. The VOL bit at access control register (ACR[7]) determines whether the access is to wiper registers WR<sub>i</sub> or initial value registers IVR<sub>i</sub>.

**TABLE 2. ACCESS CONTROL REGISTER (ACR)**

| VOL | SHDN | WIP | 0 | 0 | 0 | 0 | 0 |
|-----|------|-----|---|---|---|---|---|
|     |      |     | 0 | 0 | 0 | 0 | 0 |

If VOL bit is 0, the non-volatile IVR<sub>i</sub> registers are accessible. If VOL bit is 1, only the volatile WR<sub>i</sub> are accessible. Note, value is written to IVR<sub>i</sub> register also is written to the corresponding WR<sub>i</sub>. The default value of this bit is 0.

The SHDN bit (ACR[6]) disables or enables Shutdown mode. This bit is logically ANDed with  $\overline{\text{SHDN}}$  pin. When this bit is 0, all DCPs are in Shutdown mode. Default value of SHDN bit is 1.

The WIP bit (ACR[5]) is read only bit. It indicates that non-volatile write operation is in progress. It is impossible to write to the WR<sub>i</sub> or ACR while WIP bit is 1.

### Shutdown Mode

The device can be put in Shutdown mode either by pulling the SHDN pin to GND or setting the SHDN bit in the ACR register to 0. The truth table for Shutdown mode is in Table 3.

**TABLE 3.**

| $\overline{\text{SHDN}}$ pin | SHDN bit | Mode             |
|------------------------------|----------|------------------|
| High                         | 1        | Normal operation |
| Low                          | 1        | Shutdown         |
| High                         | 0        | Shutdown         |
| Low                          | 0        | Shutdown         |

### I<sup>2</sup>C Serial Interface

The ISL22346 supports an I<sup>2</sup>C bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always

initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL22346 operates as a slave device in all applications.

All communication over the I<sup>2</sup>C interface is conducted by sending the MSB of each byte of data first.

### Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 16). On power-up of the ISL22346, the SDA pin is in the input mode.

All I<sup>2</sup>C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL22346 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 16). A START condition is ignored during the power-up of the device.

All I<sup>2</sup>C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 16). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 17).

The ISL22346 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL22346 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 1010 as the four MSBs, and the following three bits matching the logic values present at pins A2, A1, and A0. The LSB is the Read/Write bit. Its value is "1" for a Read operation, and "0" for a Write operation (see Table 4).

**TABLE 4. IDENTIFICATION BYTE FORMAT**

Logic values at pins A2, A1, and A0 respectively

|       |   |   |   |    |    |    |       |
|-------|---|---|---|----|----|----|-------|
| 1     | 0 | 1 | 0 | A2 | A1 | A0 | R/W   |
| (MSB) |   |   |   |    |    |    | (LSB) |



FIGURE 16. VALID DATA CHANGES, START AND STOP CONDITIONS



FIGURE 17. ACKNOWLEDGE RESPONSE FROM RECEIVER



FIGURE 18. BYTE WRITE SEQUENCE

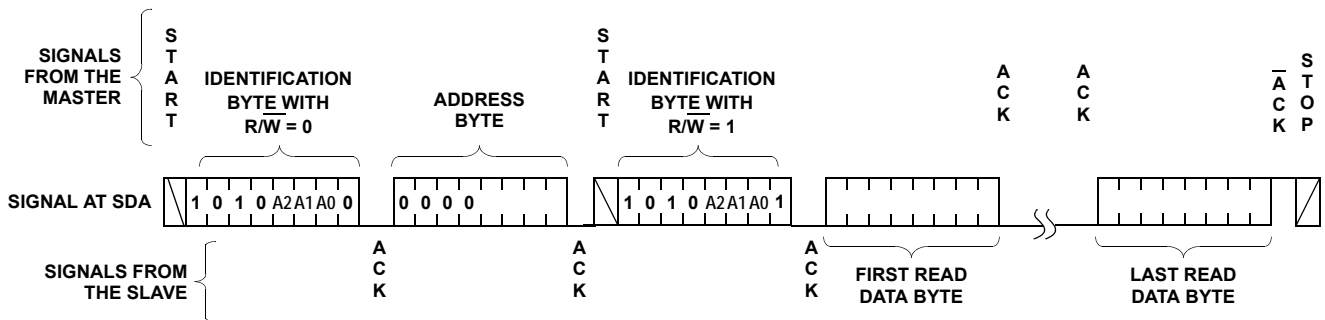


FIGURE 19. READ SEQUENCE

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### **Write Operation**

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL22346 responds with an ACK. At this time, the device enters its standby state (see Figure 18). Device can receive more than one byte of data by auto incrementing the address after each received byte. Note after reaching the address 08h, the internal pointer “rolls over” to address 00h. The non-volatile write cycle starts after STOP condition is determined and it requires up to 20ms delay for the next non-volatile write. Thus, non-volatile registers must be written individually.

### **Read Operation**

A Read operation consist of a three byte instruction followed by one or more Data Bytes (See Figure 19). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/W bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/W bit set to “1”. After each of the three bytes, the ISL22346 responds with an ACK. Then the ISL22346 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a  $\overline{\text{ACK}}$  and a STOP condition) following the last bit of the last Data Byte (see Figure 19).

The Data Bytes are from the registers indicated by an internal pointer. This pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 08h, the pointer “rolls over” to 00h, and the device continues to output data for each ACK received.

In order to read back the non-volatile IVR, it is recommended that the application reads the ACR first to verify the WIP bit is 0. If the WIP bit (ACR[5]) is not 0, the host should repeat its reading sequence again.

**Thin Micro Lead Frame Plastic Package (TMLFP)**



**L20.4x4A**  
**20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE**  
**(COMPLIANT TO JEDEC MO-220WGGD-1 ISSUE I)**

| SYMBOL | MILLIMETERS |         |      | NOTES |
|--------|-------------|---------|------|-------|
|        | MIN         | NOMINAL | MAX  |       |
| A      | 0.70        | 0.75    | 0.80 | -     |
| A1     | -           | 0.02    | 0.05 | -     |
| A2     | -           | 0.55    | 0.80 | 9     |
| A3     | 0.20 REF    |         |      | 9     |
| b      | 0.18        | 0.25    | 0.30 | 5, 8  |
| D      | 4.00 BSC    |         |      | -     |
| D1     | 3.75 BSC    |         |      | 9     |
| D2     | 1.95        | 2.10    | 2.25 | 7, 8  |
| E      | 4.00 BSC    |         |      | -     |
| E1     | 3.75 BSC    |         |      | 9     |
| E2     | 1.95        | 2.10    | 2.25 | 7, 8  |
| e      | 0.50 BSC    |         |      | -     |
| k      | 0.20        | -       | -    | -     |
| L      | 0.35        | 0.60    | 0.75 | 8     |
| N      | 20          |         |      | 2     |
| Nd     | 5           |         |      | 3     |
| Ne     | 5           |         |      | 3     |
| P      | -           | -       | 0.60 | 9     |
| θ      | -           | -       | 12   | 9     |

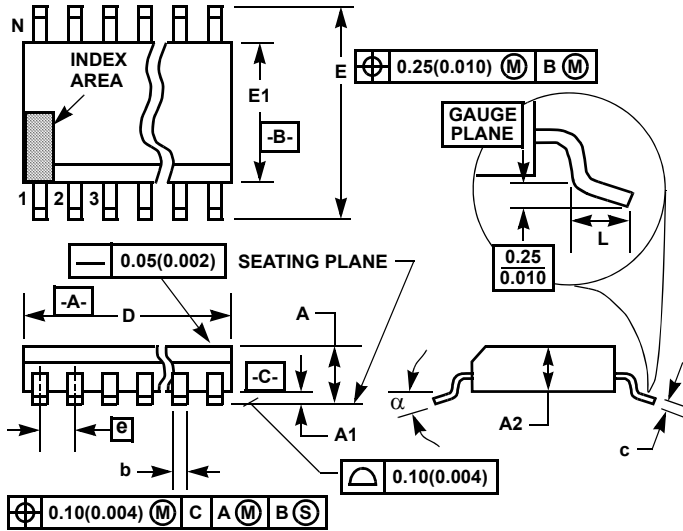
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**NOTES:**

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.



**Thin Shrink Small Outline Plastic Packages (TSSOP)**



**M20.173**  
**20 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL   | INCHES    |        | MILLIMETERS |      | NOTES |
|----------|-----------|--------|-------------|------|-------|
|          | MIN       | MAX    | MIN         | MAX  |       |
| A        | -         | 0.047  | -           | 1.20 | -     |
| A1       | 0.002     | 0.006  | 0.05        | 0.15 | -     |
| A2       | 0.031     | 0.051  | 0.80        | 1.05 | -     |
| b        | 0.0075    | 0.0118 | 0.19        | 0.30 | 9     |
| c        | 0.0035    | 0.0079 | 0.09        | 0.20 | -     |
| D        | 0.252     | 0.260  | 6.40        | 6.60 | 3     |
| E1       | 0.169     | 0.177  | 4.30        | 4.50 | 4     |
| e        | 0.026 BSC |        | 0.65 BSC    |      | -     |
| E        | 0.246     | 0.256  | 6.25        | 6.50 | -     |
| L        | 0.0177    | 0.0295 | 0.45        | 0.75 | 6     |
| N        | 20        |        | 20          |      | 7     |
| $\alpha$ | 0°        | 8°     | 0°          | 8°   | -     |

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**NOTES:**

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

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- Оценку стоимости проекта по компонентам.
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