RoHS

COMPLIANT

HALOGEN





Integrated DrMOS Power Stage

DESCRIPTION

The SiC779 is an integrated solution that contains PWM optimized n-channel MOSFETs (high side and low side) and a full featured MOSFET driver IC. The device complies with the Intel DrMOS standard for desktop and server V_{core} power stages. The SiC779 delivers up to 40 A continuous output current and operates from an input voltage range of 3 V to 16 V. The integrated MOSFETs are optimized for output voltages in the ranges of 0.8 V to 2.0 V with a nominal input voltage of 12 V. The device can also deliver very high power at 5 V output for ASIC applications.

The SiC779 incorporates an advanced MOSFET gate driver IC. This IC accepts a single PWM input from the V_B controller and converts it into the high side and low side MOSFET gate drive signals. The driver IC is designed to implement the skip mode (SMOD) function for light load efficiency improvement. Adaptive dead time control also works to improve efficiency at all load points. The SiC779 has a thermal warning (THDN) that alerts the system of excessive junction temperature. The driver IC includes an enable pin, UVLO and shoot through protection.

The SiC779 is optimized for high frequency buck applications. Operating frequencies in excess of 1 MHz can easily be achieved.

The SiC779 is packaged in Vishay Siliconix high performance PowerPAK MLP 6 x 6 package. Compact co-packaging of components helps to reduce stray inductance, and hence increases efficiency.

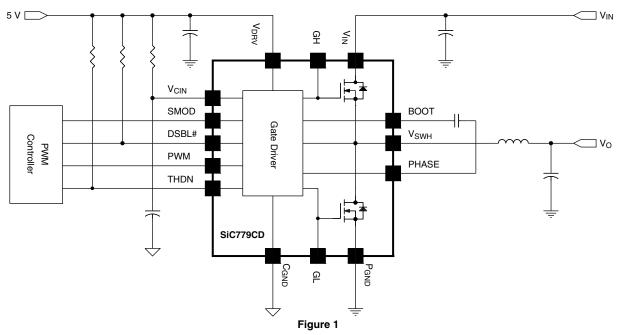
FEATURES

- Industry benchmark Gen III MOSFETs with integrated Schottky diode
- DrMOS compliant gate driver IC
- Enables V_{core} switching at 1 MHz
- Easily achieve > 93 % efficiency in multi-phase, low output voltage solutions
- · Low ringing on the VSWH pin reduces EMI
- Pin compatible with DrMOS 6 x 6 version 4.0
- Tri-state PWM input function prevents negative output voltage swing
- 5 V logic levels on PWM
- MOSFET threshold voltage optimized for 5 V driver bias
- Automatic skip mode operation (SMOD) for light load efficiency
- Under-voltage lockout
- Built-in bootstrap schottky diode
- Adaptive deadtime and shoot through protection
- Thermal shutdown warning flag
- Low profile, thermally enhanced PowerPAK® MLP 6 x 6 40 pin package
- Halogen-free according to IEC 61249-2-21 definition
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- CPU and GPU core voltage regulation
- Server, computer, workstation, game console, graphics boards, PC

SIC779 APPLICATION DIAGRAM



Document Number: 67538 S11-0703-Rev. B, 18-Apr-11



ORDERING INFORMATION				
Part Number	Package			
SiC779CD-T1-GE3	PowerPAK MLP66-40			
SiC779DB	Reference board			

Parameter	Symbol	Min.	Max.	Unit
Input Voltage	V _{IN}	- 0.3	20	
Switch Node Voltage (DC)	V _{SW}	- 0.3	20	
Drive Input Voltage	V _{DRV}	- 0.3	7	
Control Input Voltage	V _{CIN}	- 0.3	7	
Logic Pins	V _{PWM} , V _{DSBL#} , V _{THDN} , V _{SMOD}	- 0.3	V _{CIN} + 0.3	V
Boot Voltage DC (referenced to C _{GND})	V	- 0.3	27	
Boot Voltage < 200 ns Transient (referenced to C _{GND})	V _{BS}	- 0.3	29	
Boot to Phase Voltage DC	V	- 0.3	7	
Boot to Phase Voltage < 200 ns	V _{BS_PH}	- 0.3	9	
Ambient Temperature Range	T _A	- 40	125	
Maximum Junction Temperature	T _J		150	
Storage Junction Temperature	T _{STG}	- 65	150	°C
Soldering Peak Temperature			260	

Note:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS					
Parameter	Symbol	Min.	Тур.	Max.	Unit
Input Voltage	V _{IN}	3	12	16	
Control Input Voltage	V _{CIN}	4.5		5.5	V
Drive Input Voltage	V _{DRV}	4.5		5.5	v
Switch Node	V _{SW_DC}		12	16	

a. Recommended operating conditions are specified over the entire temperature range, and all voltages referenced to P_{GND} = C_{GND} unless otherwise noted.

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Тур.	Max.	Unit
Maximum Power Dissipation at T _{PCB} = 25 °C	P _{D_25C}		25	W
Maximum Power Dissipation at T _{PCB} = 100 °C	P _{D_100C}		10	VV
Thermal Resistance from Junction to Top	R _{th J TOP}		15	0C/M
Thermal Resistance from Junction to PCB	R _{th J PCB}		5	°C/W

a. T_A = 25 °C and all voltages referenced to P_{GND} = C_{GND} unless otherwise noted.





ELECTRICAL SPECIFICATION	NS					
Parameter	Symbol	Test Conditions Unless Specified $V_{DSBL\#} = V_{SMOD} = 5 \text{ V},$ $V_{IN} = 12 \text{ V}, V_{VDRV} = V_{VCIN} 5 \text{ V},$ $T_A = 25 \text{ °C}$	Min.	Typ. ^a	Max.	Unit
Power Supplies	- 1				I	
• •		V _{DSBL#} = 0 V, no switching		60		
V _{CIN} Control Input Current	I _{VCIN}	V _{DSBL#} = 5 V, no switching		400		μΑ
		V _{DSBL#} = 5 V, f _s = 300 kHz, D = 0.1		600		
Drive Issued Comment (Domestic)		f _s = 300 kHz, D = 0.1		15	22	4
Drive Input Current (Dynamic)	I_{VDRV}	f _s = 1000 kHz, D = 0.1		48	70	mA
Bootstrap Supply			•	•		
Bootstrap Switch Forward Voltage	V _{BS Diode}	V _{VCIN} = 5 V, forward bias current 2 mA		0.60	0.75	V
Control Inputs (PWM, DSBL#, SMOD)	_					
PWM Rising Threshold	$V_{th_pwm_r}$		3.5	3.8	4.2	
PWM Falling Threshold	V _{th_pwm_f}		0.8	1.0	1.2	v
PWM Tristate Rising Threshold	V _{th_tri_r}		0.9	1.3	1.8	V
PWM Tristate Falling Threshold	$V_{th_tri_f}$		3.4	3.7	4.0	
PWM Tristate Rising Threshold Hysteresis	V _{hys_tri_r}			300		mV
PWM Tristate Falling Threshold Hysteresis	V _{hys_tri_f}			170		1117
Tristate Hold-Off Time ^b	t _{TSHO}			150		ns
PWM Input Current	I=	$V_{PWM} = 5 V$		250		μΑ
1 WW Input Ourient	I _{PWM}	$V_{PWM} = 0 V$		- 250		μΛ
SMOD, DSBL# Logic Input Voltage	V _{LOGIC_LH}	Rising (low to high)	2			V
SWOD, DODE# Logic Input Voltage	V _{LOGIC_LH}	Falling (high to low)			0.8	V
Pull Down Impedance	R _{THDN}	5 k Ω resistor pull-up to V _{CIN}		40		Ω
THDN Output Low	V_{THDNL}	3 K22 Tesistor pair up to VCIN		0.07		V
Protection						
Thermal Warning Flag Set				150		
Thermal Warning Flag Clear				135		°C
Thermal Warning Flag Hysteresis				15		
Under Voltage Lockout	V _{UVLO}	Rising, on threshold		3.3	3.9	V
Under Voltage Lockout	VUVLO	Falling, off threshold	2.5	2.9		٧
Under Voltage Lockout Hysteresis	V _{UVLO_HYST}			400		mV
High Side Gate Discharge Resistor ^b	R _{HS_DSCRG}	$V_{VDRV} = V_{VCIN} = 0 V; V_{IN} = 12 V$		20.2		kΩ

Notes:

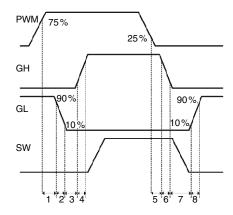
b. Guaranteed by design.

TIMING SPECIFICATIONS						
Parameter	Symbol	Test Conditions Unless Specified $V_{VDRV} = V_{VCIN} = V_{DSBL\#} = 5 \text{ V},$ $V_{VIN} = 12 \text{ V}, T_A = 25 \text{ °C}$	Min.	Тур.	Max.	Unit
Turn Off Propagation Delay High Side ^a	t _{d_on_HS}	25 % of PWM to 90 % of GH	10	20	30	
Rise Time High Side	t _{r_HS}	10 % to 90 % of GH		8		
Fall Time High Side	t _{f_HS}	90 % to 10 % of GH		8		
Turn Off Propagation Delay Low Side ^a	t _{d_off_LS}	75 % of PWM to 90 % of GL	10	20	30	ns
Rise Time Low Side	t _{r_LS}	10 % to 90 % of GL		15		
Fall Time Low Side	t _{f_LS}	90 % to 10 % of GL		8		
Dead Time Rising	t _{dead_on}	10 % of GL to 10 % of GH		15		
Dead Time Falling	t _{dead_off}	10 % of GH to 10 % of GL		15		

a. Min. and Max. are not 100 % production tested.

a. Typical limits are established by characterization and are not production tested.

TIMING DEFINITIONS



Region	Definition	Symbol
1	Turn off propagation delay LS	t _{d_off_LS}
2	Fall time LS	t _{f_LS}
3	Dead time rising	t _{dead_on}
4	Rise time HS	t _{r_HS}
5	Turn off propagation delay HS	t _{d_off_HS}
6	Fall time HS	t _{f_HS}
7	Dead time falling	t _{dead_off}
8	Rise time LS	t _{r LS}

Note:

GH is referenced to the high side source. GL is referenced to the low side source

SiC779 BLOCK DIAGRAM

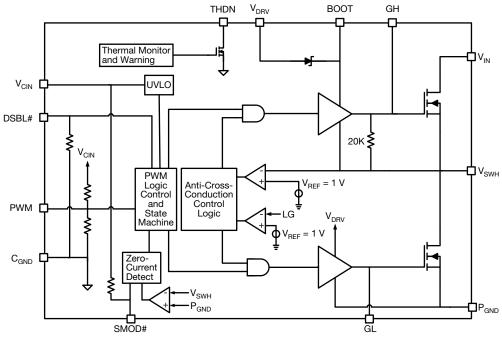
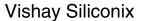


Figure 2





DETAILED OPERATIONAL DESCRIPTION

PWM Input with Tristate Function

The PWM input receives the PWM control signal from the V_R controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate Tristate logic (H, L and Tristate) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above $V_{th\ pwm\ r}$ the low side is turned off and the high side is turned on. When PWM input is driven below $V_{th_pwm_f}$ the high side turns off and the Low side turns on. For Tristate logic, the PWM input operates as above for driving the MOSFETs. However, there is an third state that is entered into as the PWM output of Tristate compatible controller enters its high impedance state during shut-down. The high impedance state of the controller's PWM output allows the SiC779 to pull the PWM input into the Tristate region (see the Tristate Voltage Threshold Diagram below). If the PWM input stays in this region for the Tristate Hold-Off Period, t_{TSHO}, both high side and low side MOSFETs are turned off. This function allows the V_R phase to be disabled without negative output voltage swing caused by inductor ringing and saves a Schottky diode clamp. The PWM and Tristate regions are separated by hysteresis to prevent false triggering. The SiC779 incorporates PWM voltage thresholds that are compatible with 5 V logic.

Disable (DSBL#)

In the low state, the DSBL# pin shuts down the driver IC and disables both high-side and low-side MOSFET. In this state, the standby current is minimized. If DSBL# is left unconnected an internal pull-down resistor will pull the pin down to $C_{\mbox{\footnotesize GND}}$ and shut down the IC.

Diode Emulation Mode (SMOD) Skip Mode

When SMOD pin is low the diode emulation mode is enabled. This is a non-synchronous conversion mode that improves light load efficiency by reducing switching losses. Conducted losses that occur in synchronous buck regulators when inductor current is negative are also reduced. Circuitry in the gate drive IC detects the inductor valley current when inductor current crosses zero and automatically stops switching the low side MOSFET. See SMOD Operation Diagram for additional details. This function can be also be used for a pre-biased output voltage. If SMOD is left unconnected, an internal pull up resistor will pull the pin up to V_{CIN} (Logic High) to disable the SMOD function.

Thermal Shutdown Warning (THDN)

The THDN pin is an open drain signal that flags the presence of excessive junction temperature. Connect a maximum of 20 $k\Omega$ to pull this pin up to $V_{\text{CIN}}.$ An internal temperature sensor detects the junction temperature. The temperature threshold is 150 °C. When this junction temperature is exceeded the THDN flag is set. When the junction temperature drops below 135 °C the device will clear the THDN signal. The SiC779 does not stop operation when the flag is set. The decision to shutdown must be made by an external thermal control function.

Voltage Input (V_{IN})

This is the power input to the drain of the high-side Power MOSFET. This pin is connected to the high power intermediate BUS rail.

Switch Node (V_{SWH} and PHASE)

The Switch node V_{SWH} is the circuit PWM regulated output. This is the output applied to the filter circuit to deliver the regulated high output for the buck converter. The PHASE pin is internally connected to the switch node V_{SWH}. This pin is to be used exclusively as the return pin for the BOOT capacitor. A 20.2 k Ω resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET in the event that V_{CIN} goes to zero while V_{IN} is still applied.

Ground connections (C_{GND} and P_{GND})

P_{GND} (power ground) should be externally connected to C_{GND} (control signal ground). The layout of the Printed Circuit Board should be such that the inductance separating the C_{GND} and P_{GND} should be a minimum. Transient differences due to inductance effects between these two pins should not exceed 0.5 V.

Control and Drive Supply Voltage Input (V_{DRV}, V_{CIN})

 V_{CIN} is the bias supply for the gate drive control IC. V_{DRV} is the bias supply for the gate drivers. It is recommended to separate these pins through a resistor. This creates a low pass filtering effect to avoid coupling of high frequency gate drive noise into the IC.

Bootstrap Circuit (BOOT)

The internal bootstrap switch and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a boot strap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin.

Shoot-Through Protection and Adaptive Dead Time (AST)

The SiC779 has an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high-side and low-side MOSFET are not turned on the same time. The adaptive dead time control operates as follows. When PWM input goes high the LS gate starts to go low after a few ns. When this signal crosses through 1.7 V the logic to switch the HS gate on is activated. When PWM goes low the HS gate goes low. When the HS gate-to-source drive signal crosses through 1.7 V the logic to turn on the LS gate is activated. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

Under Voltage Lockout (UVLO)

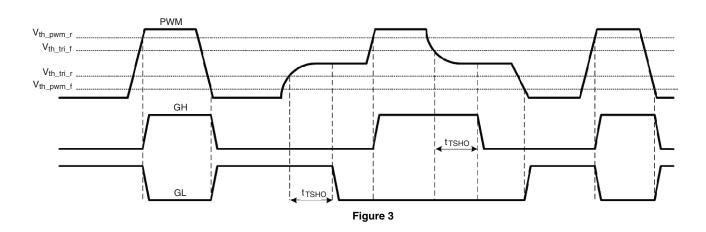
During the start up cycle, the UVLO disables the gate drive holding high-side and low-side MOSFET gate low until the input voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC779 also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device. As an added precaution, a 20.2 k Ω resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET.

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DEVICE TRUTH	ΓABLE			
DSBL#	SMOD	PWM	GH	GL
Open	Х	X	L	L
L	Х	X	L	L
Н	L	L	L	$H (I_L > 0), L (I_L \le 0)$
Н	L	Н	Н	L
Н	Н	Н	Н	L
Н	Н	L	L	Н

TRISTATE PWM VOLTAGE THRESHOLD DIAGRAM



SMOD OPERATION DIAGRAM

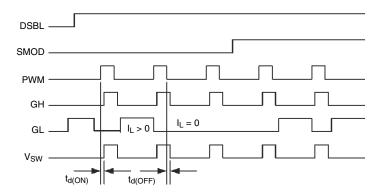


Figure 4



PIN CONFIGURATION

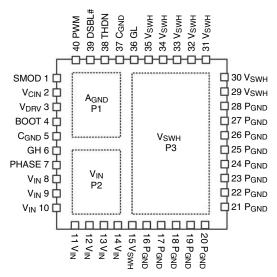
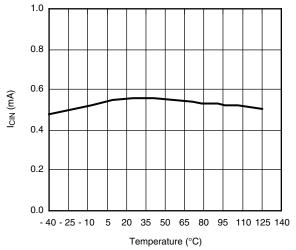
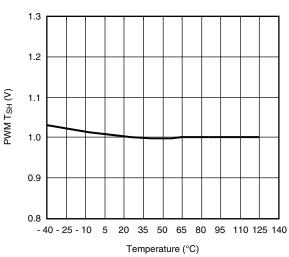


Figure 5 - PowerPAK MLP 6 x 6 40P Pin Out - Top View

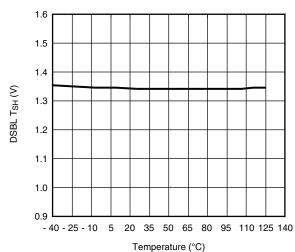
PIN DESCR	RIPTION	
Pin Number	Symbol	Description
1	SMOD	Disable low side gate operation. Active low.
2	V _{CIN}	This will be the bias supply input for control IC (5 V).
3	V_{DRV}	IC bias supply and gate drive supply voltage (5 V).
4	BOOT	High side driver bootstrap voltage pin for external bootstrap capacitor.
5, 37, PAD1	C _{GND}	Control signal ground. It should be connected to P _{GND} externally. All pins internally connected.
6	GH	Gate signal output pin for high side MOSFET. Pin for monitoring.
7	PHASE	Return pin for the HS bootstrap capacitor. Connect a 0.1 µF ceramic capacitor from this pin to the boot pin (4).
8 to 14, PAD2	V_{IN}	Input voltage for power stage. It is the drain of the high-side MOSFET.
15, 29 to 35, PAD3	V _{SWH}	It is the phase node between high side MOSFET source and low side MOSFET drain. It should be connected to an output inductor. All pins internally connected.
16 to 28	P_{GND}	Power ground.
36	GL	Gate signal output pin for low side MOSFET. Pin for monitoring.
38	THDN	Thermal shutdown open drain output. Use a 10K pull up resistor to V _{CIN} .
39	DSBL#	Disable pin. Active low.
40	PWM	PWM input logic signal. Compatible with Tristate controller function.



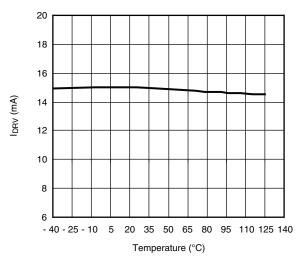
 I_{CIN} (mA) vs. Temperature at Frequency = 300 kHz $D = 10 \%, V_{CIN} = V_{DRV} = 5 V$



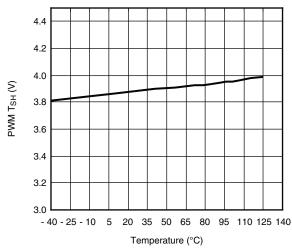
PWM Falling Threshold (V) vs. Temperature (°C) $V_{CIN} = V_{DRV} = 5 V$



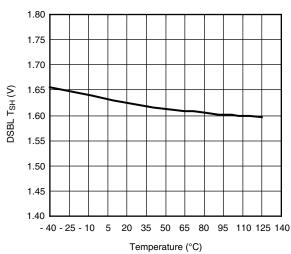
DSBL Falling Threshold (V) vs. Temperature (°C) $V_{CIN} = V_{DRV} = 5 V$



 I_{DRV} (mA) vs. Temperature at Frequency = 300 kHz $D = 10 \%, V_{CIN} = V_{DRV} = 5 V$



PWM Rising Threshold (V) vs. Temperature (°C) $V_{CIN} = V_{DRV} = 5 V$

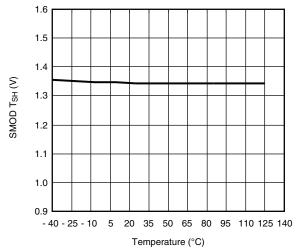


DSBL Rising Threshold (V) vs. Temperature (°C) $V_{CIN} = V_{DRV} = 5 V$

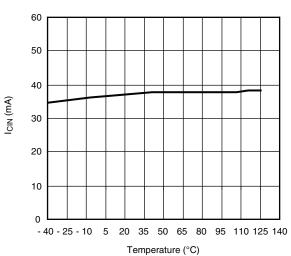




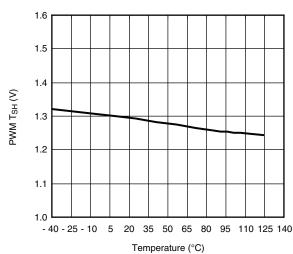




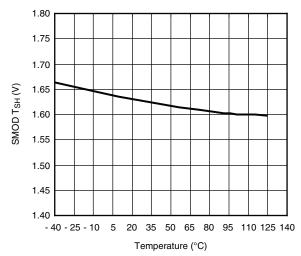
SMOD Falling Threshold (V) vs. Temperature (°C) $V_{CIN} = V_{DRV} = 5 \text{ V}$



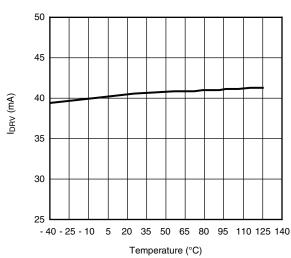
 $I_{CIN} + I_{DRV}$ (mA) vs. Temperature at Frequency = 1 MHz D = 10 %, $V_{CIN} = V_{DRV} = 5$ V



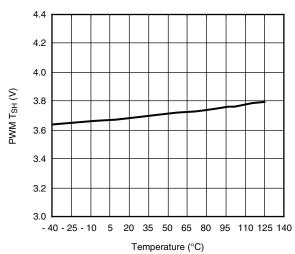
PWM Falling Tristate (V) vs. Temperature (°C) $V_{CIN} = V_{DRV} = 5 V$



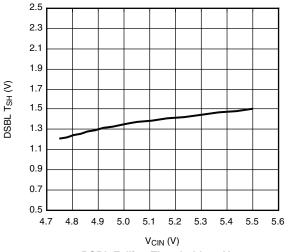
SMOD Rising Threshold (V) vs. Temperature (°C) V_{CIN} = V_{DRV} = 5 V



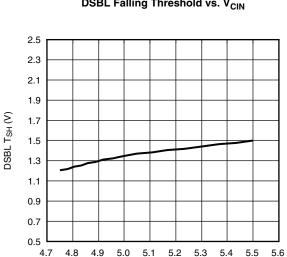
 I_{DRV} (mA) vs. Temperature at Frequency = 1 MHz D = 10 %, V_{CIN} = V_{DRV} = 5 V



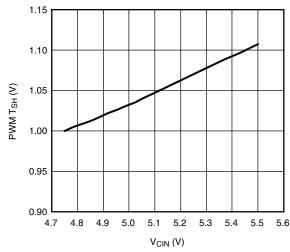
PWM Rising Tristate Threshold (V) vs. Temperature (°C) $V_{CIN} = V_{DRV} = 5 \text{ V}$



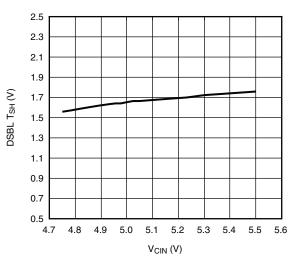
DSBL Falling Threshold vs. $V_{\rm CIN}$



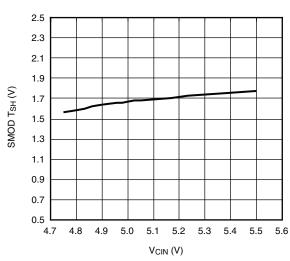
 $V_{CIN}(V)$ SMOD Falling Threshold vs. $V_{\rm CIN}$



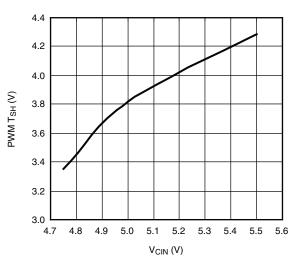
PWM Falling Threshold vs. $V_{\rm CIN}$



DSBL Rising Threshold vs. $V_{\rm CIN}$



SMOD Rising Threshold vs. $V_{\rm CIN}$



PWM Rising Threshold vs. $V_{\rm CIN}$



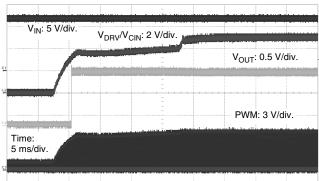
ELECTRICAL CHARACTERISTICS

GH: 10 V/div.

V_{SWH}: 10 V/div.

GL: 5 V/div.

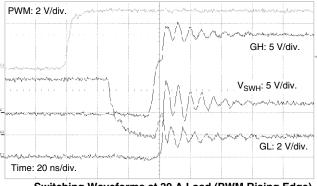
I_L: 5 A/div.



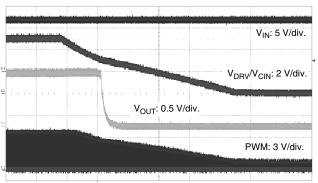
Startup at V_{DRV}/V_{CIN} Ramping up V_{IN} = 12 V, V_{OUT} = 1.2 V, F_{SW} = 500 kHz



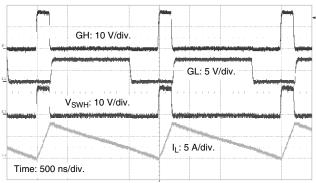
Switching Waveforms with SMOD enabled $V_{IN} = 12 \text{ V}, V_{OUT} = 1.2 \text{ V}, F_{SW} = 500 \text{ kHz}$



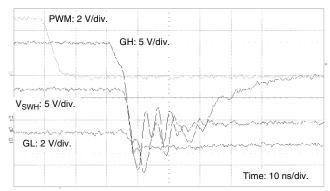
Switching Waveforms at 30 A Load (PWM Rising Edge) $V_{IN} = 12 \text{ V}, V_{OUT} = 1.2 \text{ V}, F_{SW} = 500 \text{ kHz}$



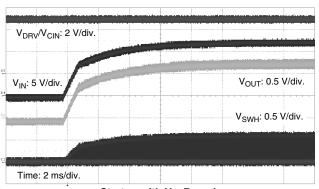
Startup at V_{DRV}/V_{CIN} Ramping down V_{IN} = 12 V, V_{OUT} = 1.2 V, F_{SW} = 500 kHz



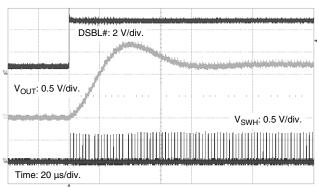
Switching Waveforms with SMOD disabled $V_{IN} = 12 \text{ V}, V_{OUT} = 1.2 \text{ V}, F_{SW} = 500 \text{ kHz}$



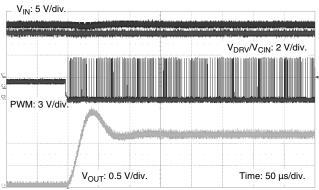
Switching Waveforms at 30 A Load (PWM Falling Edge) V_{IN} = 12 V, V_{OUT} = 1.2 V, F_{SW} = 500 kHz



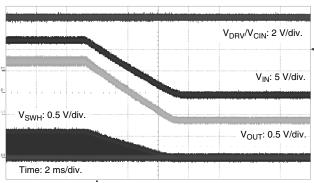
Startup with $V_{\mbox{\scriptsize IN}}$ Ramping up V_{IN} = 12 V, V_{OUT} = 1.2 V, F_{SW} = 500 kHz



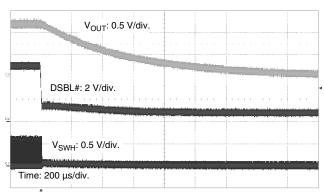
Startup with DSBL# Toggle High $V_{IN} = 12 \text{ V}, V_{OUT} = 1.2 \text{ V}, F_{SW} = 500 \text{ kHz}$



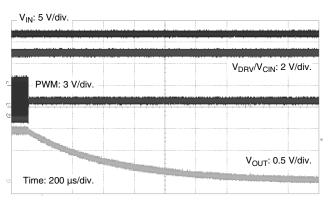
Startup with PWM existing Tri-state V_{IN} = 12 V, V_{OUT} = 1.2 V, F_{SW} = 500 kHz



Power Off with V_{IN} Ramping down $V_{IN} = 12 \text{ V}, V_{OUT} = 1.2 \text{ V}, F_{SW} = 500 \text{ kHz}$



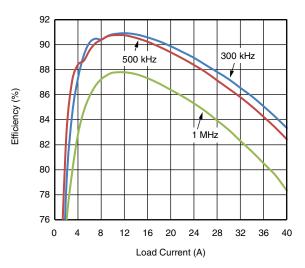
Shutdown with DSBL# Toggle Low $V_{IN} = 12 \text{ V}, V_{OUT} = 1.2 \text{ V}, F_{SW} = 500 \text{ kHz}$



Shutdown with PWM entering Tri-state $V_{IN} = 12 \text{ V}, V_{OUT} = 1.2 \text{ V}, F_{SW} = 500 \text{ kHz}$



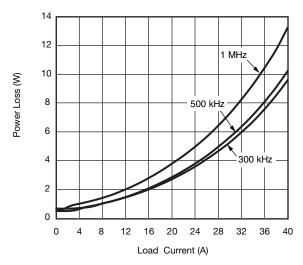
TYPICAL EFFICIENCY CURVES



 $V_{IN} = 12 \text{ V, } V_{OUT} = 1.2 \text{ V, } V_{DRV} = V_{CIN} = 5 \text{ V; No Air Flow:} \\ Inductance = 0.22 \ \mu\text{H, DCR} = 0.29 \ m\Omega; \\ \text{(Efficiency includes SiC779 and inductor loss.)}$

Figure 6a

TYPICAL POWER LOSS

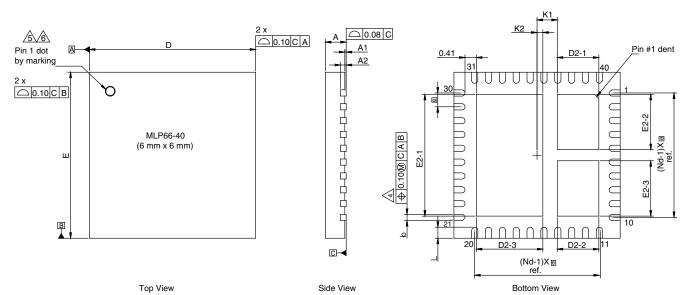


$$\begin{split} V_{\text{IN}} = 12 \text{ V, } V_{\text{OUT}} = 1.2 \text{ V, } V_{\text{DRV}} = V_{\text{CIN}} = 5 \text{ V; No Air Flow:} \\ & \text{Inductance} = 0.22 \text{ } \mu\text{H, DCR} = 0.29 \text{ } m\Omega; \\ & \text{(Power loss includes SiC779 and inductor loss.)} \end{split}$$

Figure 6b

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PACKAGE DIMENSIONS



		MILLIMETERS			INCHES	
DIM	Min.	Nom.	Max.	Min.	Nom.	Max.
A ⁽⁸⁾	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b ⁽⁴⁾	0.20	0.25	0.30	0.078	0.098	0.011
D		6.00 BSC			0.236 BSC	
e	0.50 BSC				0.019 BSC	
E	6.00 BSC			0.236 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017
N ⁽³⁾		40		40		
Nd ⁽³⁾		10			10	
Ne ⁽³⁾		10			10	
D2-1	1.45	1.50	1.55	0.057	0.059	0.061
D2-2	1.45	1.50	1.55	0.057	0.059	0.061
D2-3	2.35	2.40	2.45	0.095	0.094	0.096
E2-1	4.35	4.40	4.45	0.171	0.173	0.175
E2-2	1.95	2.00	2.05	0.076	0.078	0.080
E2-3	1.95	2.00	2.05	0.076	0.078	0.080
K1		0.73 BSC		0.028 BSC		
K2		0.21 BSC			0.008 BSC	

Notes:

- 1. Use millimeters as the primary measurement.
- 2. Dimensioning and tolerances conform to ASME Y14.5M-1994.
- 3. N is the number of terminals.

Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction .

🔔 Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip.

The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body.

6. Exact shape and size of this feature is optional.

7. Package warpage max. 0.08 mm.

Applied only for terminals.

Figure 7 - PowerPAK MLP 66-40



LAND PATTERN DIMENSIONS

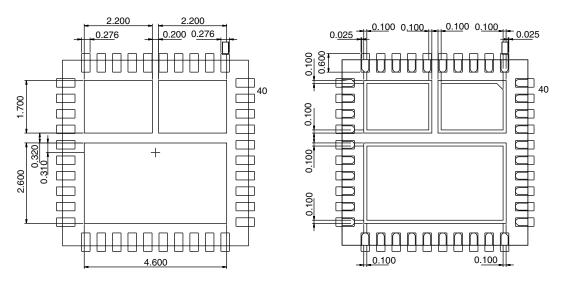
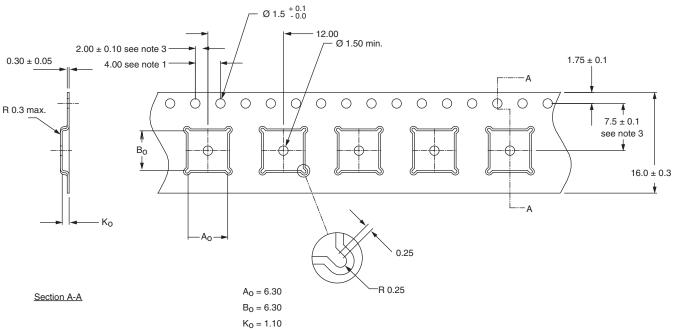


Figure 8 - PowerPAK MLP 66-40

TAPE AND REEL CARRIER TAPE DIMENSIONS



Notes:

- 1. 10 sprocket hole pitch cumulative tolerance \pm 0.2.
- 2. Camber in compliance with EIA 481.
- 3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

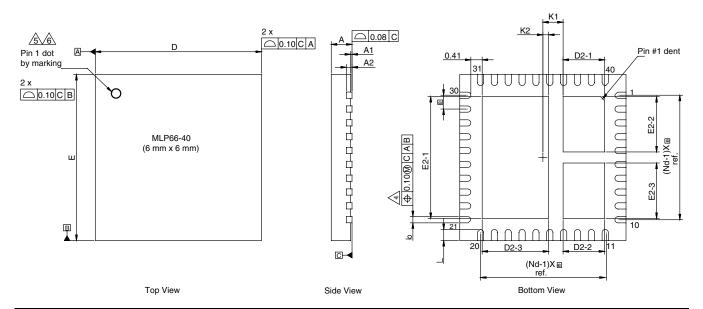
Figure 9 - PowerPAK MLP 66-40

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Document Number: 67538 www.vishay.com S11-0703-Rev. B, 18-Apr-11



PowerPAK® MLP66-40 CASE OUTLINE



DIM.	MILLIMETERS			INCHES		
DIWI.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A (8)	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b ⁽⁴⁾	0.20	0.25	0.30	0.078	0.098	0.011
D		6.00 BSC			0.236 BSC	
е	0.50 BSC				0.019 BSC	
Е	6.00 BSC				0.236 BSC	
L	0.35	0.40	0.45	0.013	0.015	0.017
N (3)	40				40	
Nd ⁽³⁾		10			10	
Ne ⁽³⁾		10		10		
D2-1	1.45	1.50	1.55	0.057	0.059	0.061
D2-2	1.45	1.50	1.55	0.057	0.059	0.061
D2-3	2.35	2.40	2.45	0.095	0.094	0.096
E2-1	4.35	4.40	4.45	0.171	0.173	0.175
E2-2	1.95	2.00	2.05	0.076	0.078	0.080
E2-3	1.95	2.00	2.05	0.076	0.078	0.080
K1	0.73 BSC			0.028 BSC		
K2	0.21 BSC				0.008 BSC	

ECN: T09-0195-Rev. A, 04-May-09

DWG: 5986

Notes

- 1. Use millimeters as the primary measurement
- 2. Dimensioning and tolerances conform to ASME Y14.5M. 1994
- 3. N is the number of terminals. Nd is the number of terminals in Y-direction and Ne is the number of terminals in Y-direction
- Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
- The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
- Exact shape and size of this feature is optional
- 7. Package warpage max. 0.08 mm
- Applied only for terminals

Document Number: 64846 www.vishay.com 04-May-09 1



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Revision: 02-Oct-12 Document Number: 91000



OOO «ЛайфЭлектроникс" "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 P/C 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 3010181090000000703 БИК 044030703

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- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
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- Оценку стоимости проекта по компонентам.
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