LTM9003 Digital Predistortion Receiver Subsystem

DESCRIPTION

Demonstration circuit 1437B is an evaluation board featuring Linear Technology Corporation's LTM®9003 12-Bit Predistortion Receiver Subsystem. DC1437 demonstrates good circuit layout techniques and recommended external circuitry for optimal system performance.

DC1437 comes with Linear Technology's 12-bit LTM9003 receiver subsystem installed. The board includes output LVDS buffers. DC1437 plugs into the DC890 Data Acquisition demo board and the output can be easily analyzed with Linear Technology's PScope™ data processing software, which is available for no charge on our website at http://www.linear.com/software.

Design files for this circuit board are available at http://www.linear.com/demo

CONNECTION DIAGRAM

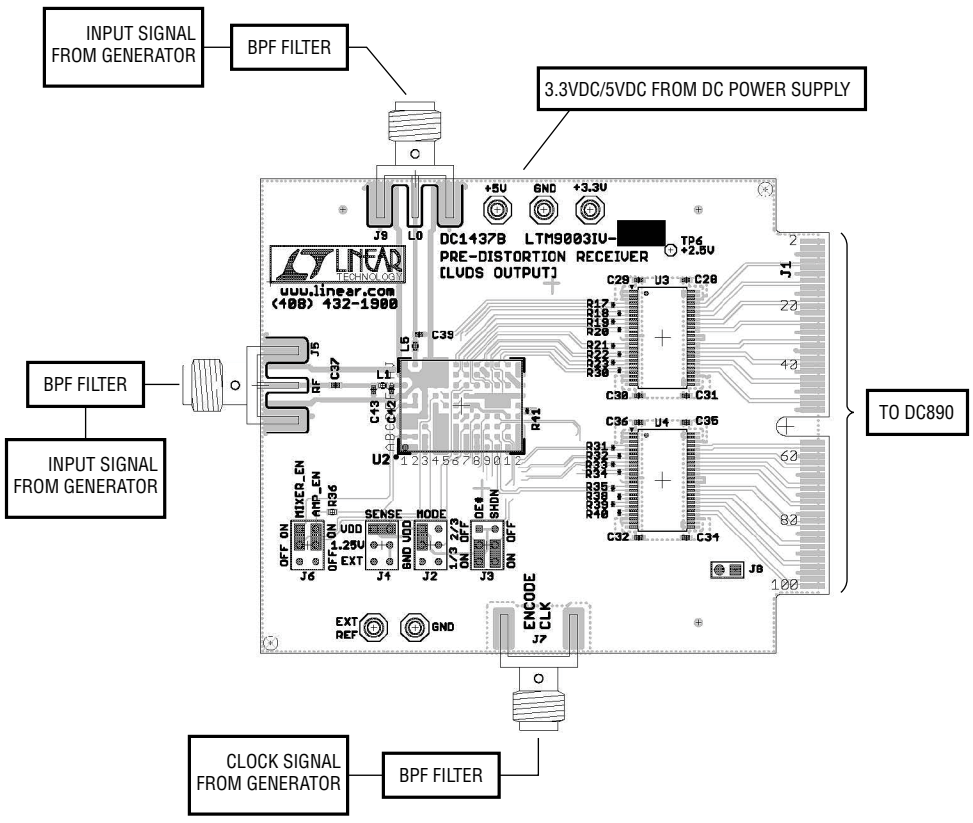

Figure 1. DC1437B Connection Diagram

QUICK START PROCEDURE

Validating the performance of the LTM9003 is simple with DC1437, and requires only two input sources, a clock source, a computer, and a lab power supply. Note the RF and LO inputs are matched for 1.4GHz to 2.2GHz, and 0.9GHz to 3GHz, respectively. Refer to the schematic in Figure 4 for other matching configurations to accommodate other frequency ranges. Refer to Figure 1 for proper board evaluation equipment setup and follow the procedure below:

1. Plug the DC1437B to the DC890 USB High Speed Data Collection Board using edge connector P1.
2. Connect the DC890 to a host PC with a standard USB A/B cable. Note the DC890B will also require an external 6V, 1A power supply when receiving LVDS format signals.
3. Run the PScope software (PScope.exe version K76 or later) which can be downloaded from www.linear.com/designtools/software. Complete software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically as new features may be added.
4. The PScope software should recognize the DC1437B and configure itself automatically. See Figure 3 for the default configuration settings.
5. Connect the power supply as shown in Figure 1. There are onboard low noise voltage regulators that provide the supply voltage for the DC1437. Note that the LTM9003-AA requires a 3.3V supply voltage for the mixer, whereas the LTM9003-AB requires 5V. As such, only the DC1437B-AB board requires 5V as well as 3.3V input; the DC1437B-AA board can be powered from 3.3V only. The entire board and all components share a common ground. The power supply should still be a low noise lab power supply capable of supplying at least 1A.
6. Provide an encode clock to the ADC via SMA connector J7. Use a low-phase-noise clock source such as a filtered RF signal generator or a high quality clock oscillator. Note that, similar to having a noisy input, a high jitter (high phase noise) encode clock will degrade the signal-to-noise ratio (SNR) of the system.
7. Apply an RF input signal to the board. For best results, use a low distortion, low noise signal generator with sufficient filtering to avoid degrading the performance of the receiver.
8. Apply an LO input signal to the board. Note that the difference in frequency between this signal and the RF signal will be the IF frequency resulting at the IF filter and ADC input.
9. Click the Collect button (see Figure 2) to begin acquiring data. The Collect button then should change to Pause. To stop data acquisition, click the Pause button.

Table 1. DC1437B Assembly Options

ASSEMBLY VERSION	U2 PART NUMBER	MAX CONVERSION RATE	NUMBER OF BITS	MIXER SUPPLY VOLTAGE	RF FREQUENCY RANGE
DC1437B-AA	LTM9003-AA	250Msps	12	3.3V	400MHz TO 3800MHz
DC1437B-AB	LTM9003-AB	250Msps	12	5V	400MHz TO 3700MHz

DC1437B CONNECTORS AND JUMPERS

Connector Definitions

J5 – RF Board RF Signal Input. Impedance matched to 50Ω for use with lab signal generators.

J7 – CLK Board Clock Input. Impedance matched to 50Ω. Drive with a low phase-noise clock oscillator or filtered sine wave signal source.

J9 – LO Board LO Signal Input. Impedance matched to 50Ω for use with lab signal generators.

Jumper Definitions

J2 – MODE Sets the output format and clock duty stabilizer. The default setting is V_{DD}. This enables 2's complement format and disables the clock duty cycle stabilizer.

J3 – SHDN/$\overline{OE}$ Enables/disables the ADC. The default setting for both jumpers is ON.

J4 – SENSE Sets the SENSE mode. The default setting is V_{DD}. This selects the internal reference and a ±1V input range at the ADC.

J6 – MIXER/AMP ENABLE Enables the internal mixer and amplifiers. The default setting for both jumpers is ON.

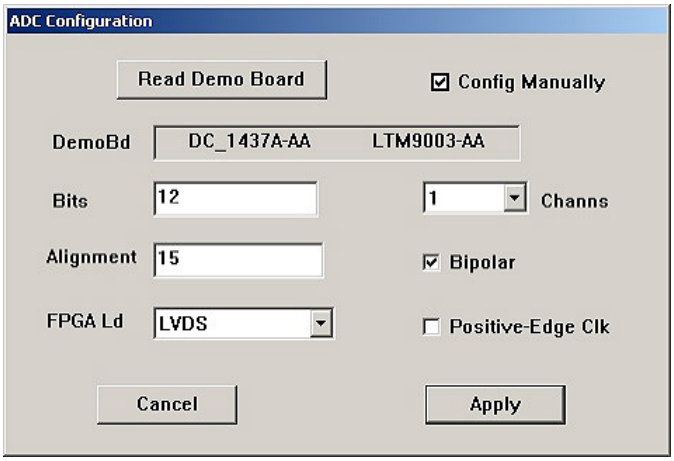

Figure 3. PScope Configuration Menu

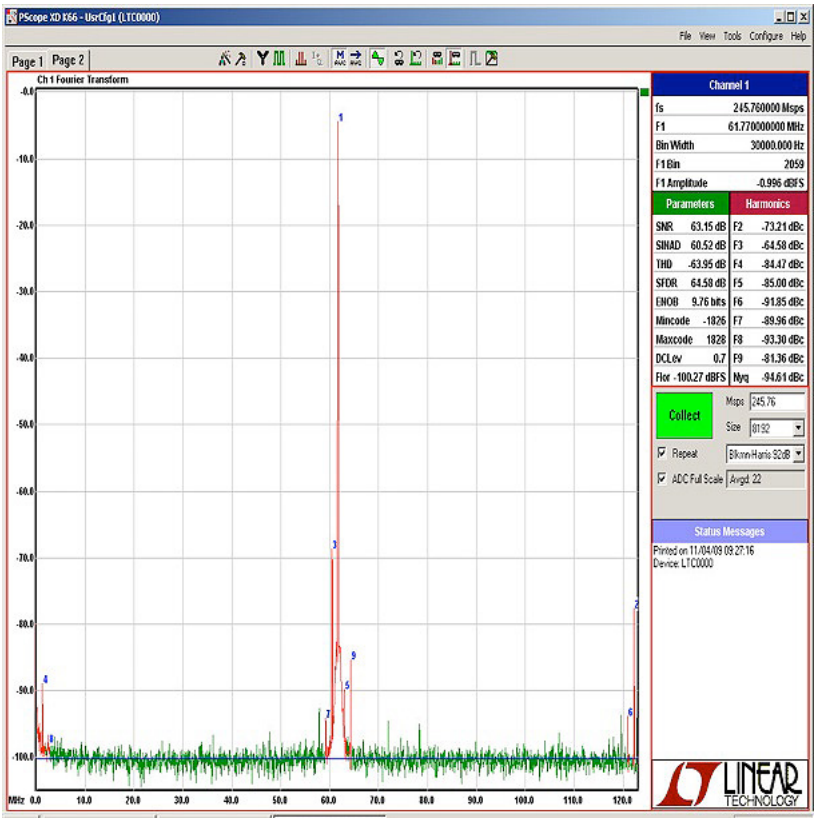

Figure 2. PScope Screen Shot

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	T2	BALUN, 1:1, SMT, SM-22	MACOM/MABA-007159-000000
2	0	C37, C42	DNI	
3	1	C43	CAP, NPO, 1.0pF, 50V, 0.25pF, 0402	AVX/04025A1R0CAT2A
4	1	C39	CAP, NPO, 0.5pF, 50V, 0.25pF, 0402	AVX/04025A0R5CAT2A
5	1	C4	CAP, NPO, 8.2pF, 50V, 0.25pF, 0402	AVX/04025A8R2CAT2A
6	3	C1, C2, C44	CAP, X5R, 0.01µF, 16V, 10%, 0402	AVX/0402YC103KAT
7	10	C19, C27-32, C34-36	CAP, X5R, 0.1µF, 10V, 10%, 0402	AVX/0402ZD104KAT
8	1	C45	CAP, X5R, 10µF, 6.3V, 20%, 0805	AVX/08056D106MAT
9	2	C5, C6	CAP, X5R, 4.7µF, 10V, 20%, 0805	AVX/0805ZD475MAT
10	2	C3, C7	CAP, X7R, 0.1µF, 16V, 10%, 0603	AVX/0603YC104KAT
11	3	J5, J7, J9	CONN, SMA, 50Ω, EDGE-LAUNCH, FEMALE	AMPHENOL_CONNEX/132357
12	0	J8	DNI	
13	4	J2, J3, J4, J6	HEADER, 3 × 2, 2mm	SAMTEC TMM103-02-L-D
14	1	L1	IND, 3.9nH, 5%, 0402	COILCRAFT/0402CS-3N9XJLW
15	1	L5	IND, 2.7nH, 5%, 0402	COILCRAFT/0402CS-2N7XJLW
16	1	U1	IC, Serial_EEPROM, TSSOP8	MICROCHIP/24LC025-I_ST
17	1	U10	IC, VREG, ADJ, 500MA, SO8	LINEAR_TECH/LT1763CDE
18	2	U3, U4	IC, RPTR, LVDS, OCTAL, SMT, TSSOP	FAIRCHILD/FIN1108
19	3	R3, R13, R14	RES, 0 _OHM_JUMPER, 0805	VISHAY CRCW08050000Z0EA
20	14	R17-23, R28, R30-35	RES, 100, 1%, 1/20, 0201	VISHAY CRCW0201100RF
21	0	R9, R38-R41	DNI	
22	3	R9, R10, R24	RES, 100k, 1%, 1/16, 0402	VISHAY CRCW0402100KFKED
23	1	R12	RES, 10k, 1%, 1/16, 0402	VISHAY CRCW040210K0FKED
24	2	R4, R5	RES, 4.99, 1%, 1/16, 0402	VISHAY CRCW04024R99FKED
25	2	R1, R2	RES, 49.9, 1%, 1/16, 0402	VISHAY CRCW040249R9FKED
26	5	R25, R26, R27, R29, R36	RES, 4990, 1%, 1/16, 0402	VISHAY CRCW04024K99FKED
27	2	R7, R11	RES, 499, 1%, 1/10W, 0603	VISHAY CRCW0603499RFKEA
28	2	R6, R8	RES, 1000, 1%, 1/10W, 0603	VISHAY CRCW06031K00FKEA
29	5	TP1-5	TURRET	MILL_MAX/2308-2
30	4		STAND-OFF, NYLON 0.25" TALL	KEYSTONE, 8831 (SNAP ON)
DC1437B-AA Required Circuit Components				
1	1	DC1437B	General BOM	
2	0	R15	Res., DNI	
3	1	R16	RES, 0Ω JUMPER, 0805	VISHAY CRCW08050000Z0EA
4	1	U2	I.C., µModule	Linear Tech. Corp. LTM9003CV-AA
DC1437B-AB Required Circuit Components				
1	1	DC1437B	General BOM	
2	0	R16	Res., DNI	
3	1	R15	RES, 0Ω JUMPER, 0805	VISHAY CRCW08050000Z0EA
4	1	U2	I.C., µModule	Linear Tech. Corp. LTM9003CV-AB

SCHEMATIC DIAGRAM

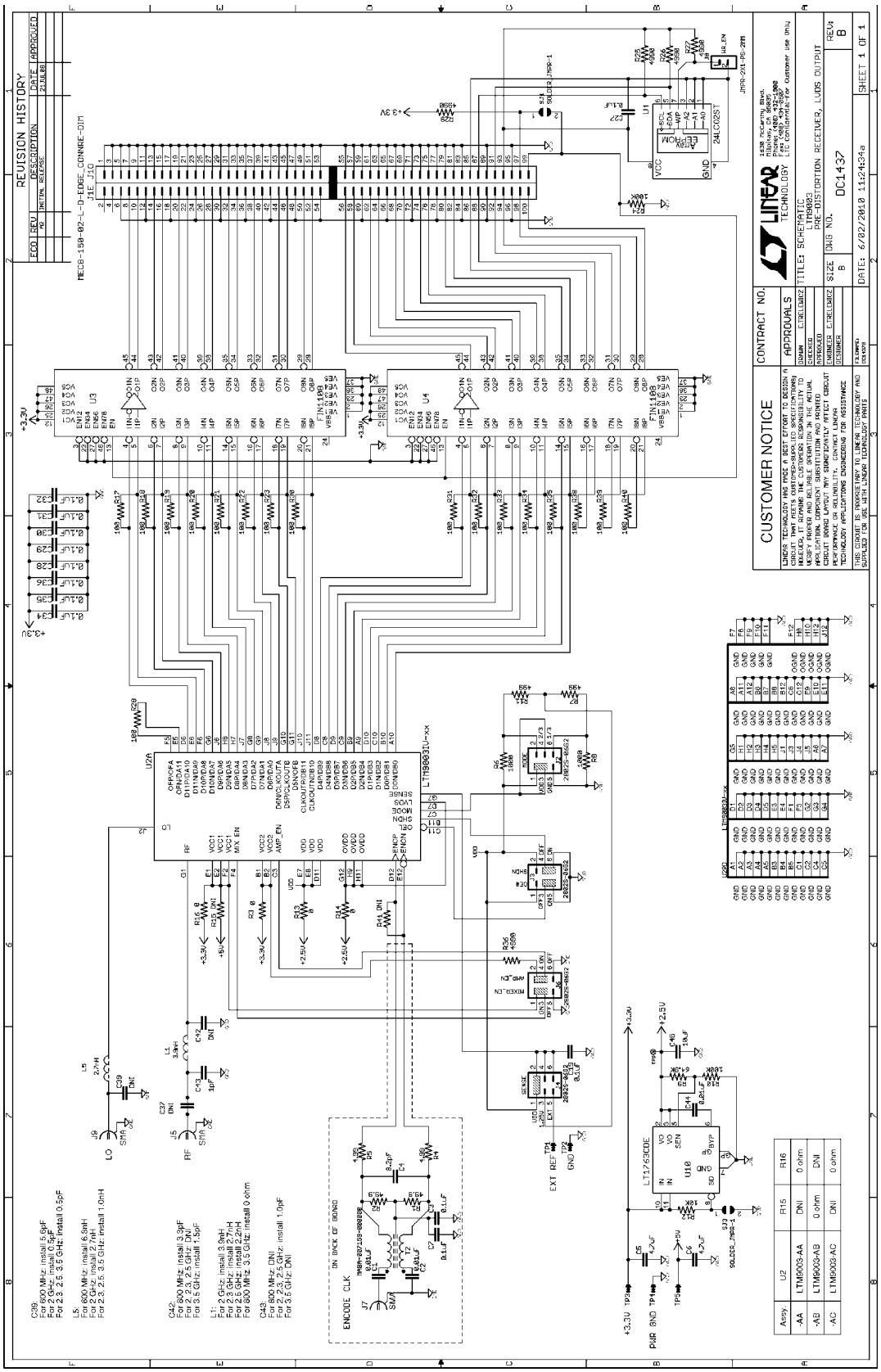

Figure 4. DC1437B Schematic Diagram

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