

# 2.5/3.3 V, 200 MHz High-Speed Multi-Phase PLL Clock Buffer

## Features

- 2.5 V or 3.3 V operation
- Split output bank power supplies
- Output frequency range: 6 MHz to 200 MHz
- 50 ps typical matched-pair output-output skew
- 50 ps typical cycle-cycle jitter
- 49.5 / 50.5% typical output duty cycle
- Selectable output drive strength
- Selectable positive or negative edge synchronization
- Eight LVTTTL outputs driving 50Ω terminated lines
- LVCMOS / LVTTTL overvoltage tolerant reference input
- Phase adjustments in 625 / 1250 ps steps up to ±7.5 ns
- 2×, 4× multiply and (1/2)×, (1/4)× divide ratios
- Spread spectrum compatible
- Industrial temperature range: -40 °C to +85 °C
- 32-pin TQFP package

## Functional Description

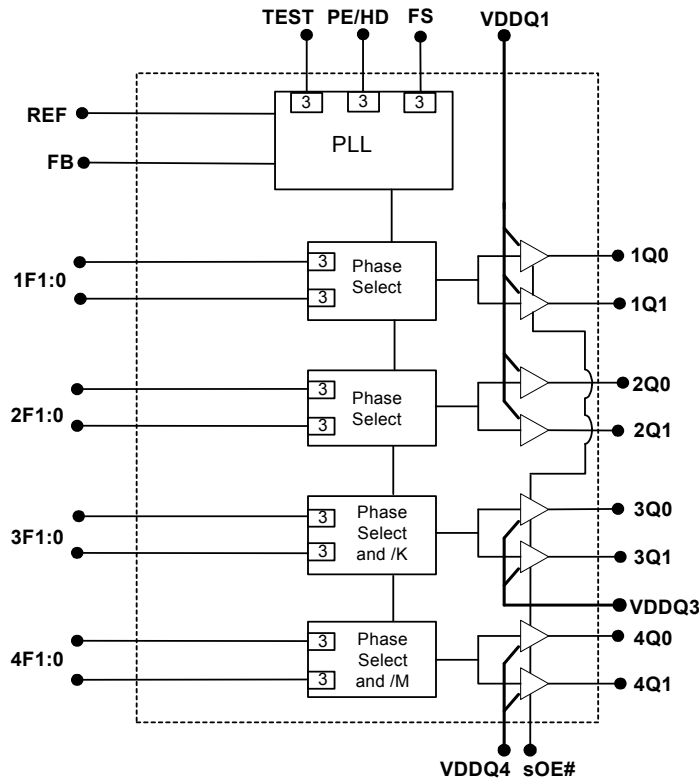
The CY7B9950 RoboClock® is a low voltage, low power, eight-output, 200 MHz clock driver. It features output phase programmability which is necessary to optimize the clock tree design of high performance computer and communication systems.

The user can program the phase of the output banks through nF[0:1] pins. The adjustable phase feature enables the user to skew the outputs to lead or lag the reference clock. Any one of the outputs can be connected to the feedback input to achieve different reference frequency multiplications, divide ratios, and zero input-output delay.

The device also features split output bank power supplies, which enable the user to run two banks (1Qn and 2Qn) at a power supply level different from that of the other two banks (3Qn and 4Qn). Additionally, the three-level PE/HD pin controls the synchronization of the output signals to either the rising or falling edge of the reference clock and selects the drive strength of the output buffers. The high drive option (PE/HD = MID) increases the output current from ± 12 mA to ± 24 mA(3.3 V).

For a complete list of related documentation, [click here](#).

## Logic Block Diagram

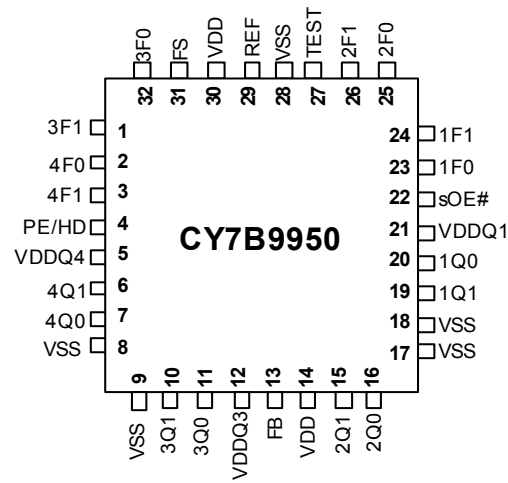


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**Pinouts**

**Figure 1. 32-pin TQFP pinout (Top View)**



## Pin Definitions

Pin	Name	I/O <sup>[1]</sup>	Type	Description
29	REF	I	LVTTL / LVCMOS	Reference clock input.
13	FB	I	LVTTL	Feedback input.
27	TEST	I	Three-level	When MID or HIGH, disables PLL <sup>[2]</sup> . REF goes to outputs of Bank 1 and Bank 2. REF also goes to outputs of Bank 3 and Bank 4 through output dividers K and M. Set LOW for normal operation.
22	sOE#	I, PD	Two-level	Synchronous output enable. When HIGH, it stops clock outputs (except 2Q0 and 2Q1) in a Low state (for PE = H or M) – 2Q0, and 2Q1 may be used as the feedback signal to maintain phase lock. When test is held at MID level and sOE# is HIGH, the nF[1:0] pins act as output disable controls for individual banks when nF[1:0] = LL. Set sOE# Low for normal operation.
4	PE/HD	I, PU	Three-level	Selects Positive or negative edge control and High or low output drive strength. When Low/High the outputs are synchronized with the negative/positive edge of the reference clock, respectively. When at MID level, the output drive strength is increased and the outputs synchronize with the positive edge of the reference clock (see <a href="#">Table 6 on page 5</a> ).
24, 23, 26, 25, 1, 32, 3, 2	nF[1:0]	I	Three-level	Select frequency and phase of the outputs (see <a href="#">Table 1</a> , <a href="#">Table 2</a> , <a href="#">Table 3 on page 5</a> , <a href="#">Table 4 on page 5</a> , and <a href="#">Table 5 on page 5</a> ).
31	FS	I	Three-level	Selects VCO operating frequency range (see <a href="#">Table 4 on page 5</a> )
19, 20, 15, 16, 10, 11, 6, 7	nQ[1:0]	O	LVTTL	Four banks of two outputs (see <a href="#">Table 1</a> , <a href="#">Table 2</a> , and <a href="#">Table 3 on page 5</a> )
21	V <sub>DDQ1</sub> <sup>[3]</sup>	PWR	Power	Power supply for Bank 1 and Bank 2 output buffers (see <a href="#">Table 7 on page 5</a> for supply level constraints).
12	V <sub>DDQ3</sub> <sup>[3]</sup>	PWR	Power	Power supply for Bank 3 output buffers (see <a href="#">Table 7 on page 5</a> for supply level constraints).
5	V <sub>DDQ4</sub> <sup>[3]</sup>	PWR	Power	Power supply for Bank 4 output buffers (see <a href="#">Table 7 on page 5</a> for supply level constraints).
14, 30	V <sub>DD</sub> <sup>[3]</sup>	PWR	Power	Power supply for internal circuitry (see <a href="#">Table 7 on page 5</a> for supply level constraints).
8, 9, 17, 18, 28	V <sub>SS</sub>	PWR	Power	Ground

### Notes

1. PD indicates an internal pull-down and PU indicates an internal pull-up. 3 indicates a three-level input buffer.
2. When TEST = MID and sOE# = HIGH, PLL remains active with nF[1:0] = LL functioning as an output disable control for individual output banks. Skew selections remain in effect unless nF[1:0] = LL.
3. A bypass capacitor (0.1µF) must be placed as close as possible to each positive power pin (< 0.2"). If these bypass capacitors are not close to the pins their high-frequency filtering characteristic are cancelled by the lead inductance of the traces.

## Device Configuration

The outputs of the CY7B9950 can be configured to run at frequencies ranging from 6 to 200 MHz. Banks 3 and 4 output dividers are controlled by 3F[1:0] and 4F[1:0] as indicated in Table 1 and Table 2, respectively.

**Table 1. Output Divider Settings — Bank 3**

3F[1:0]	K — Bank3 output divider
LL	2
HH	4
Other <sup>[4]</sup>	1

**Table 2. Output Divider Settings — Bank 4**

4F[1:0]	M — Bank4 output divider
LL	2
Other <sup>[4]</sup>	1

The three-level FS control pin setting determines the nominal operating frequency range of the divide-by-one outputs of the device. The CY7B9950 PLL operating frequency range that corresponds to each FS level is given in Table 3 on page 5.

**Table 3. Frequency Range Select**

FS	PLL frequency range
L	24 to 50 MHz
M	48 to 100 MHz
H	96 to 200 MHz

The selectable output skew is in discrete increments of time units ( $t_U$ ). The value of  $t_U$  is determined by the FS setting and the maximum nominal frequency. The equation used to determine the  $t_U$  value is:  $t_U = 1 / (f_{NOM} \times MF)$ , where MF is a multiplication factor, which is determined by the FS setting as indicated in Table 4.

**Table 4. MF Calculation**

FS	MF	$f_{NOM}$ at which $t_U$ is 1.0 ns (MHz)
L	32	31.25
M	16	62.5
H	8	125

**Table 5. Output Skew Settings**

nF[1:0]	Skew (1Q[0:1],2Q[0:1])	Skew (3Q[0:1])	Skew (4Q[0:1])
LL <sup>[5]</sup>	$-4t_U$	Divide by 2	Divide by 2
LM	$-3t_U$	$-6t_U$	$-6t_U$

**Notes**

- These states are used to program the phase of the respective banks (see Table 5 on page 5).
- LL disables outputs if TEST = MID and sOE# = HIGH.
- When 4Q[0:1] are set to run inverted (HH mode), sOE# disables these outputs HIGH when PE/HD = HIGH or MID and sOE# disables them LOW when PE/HD = LOW.
- Please refer to "DC Parameters" section for  $I_{QH}/I_{OL}$  specifications.
- $V_{DDQ1/3/4}$  must not be set at a level higher than that of  $V_{DD}$ . They can be set at different levels from each other, e.g.,  $V_{DD} = 3.3$  V,  $V_{DDQ1} = 3.3$  V,  $V_{DDQ3} = 2.5$  V and  $V_{DDQ4} = 2.5$  V.

**Table 5. Output Skew Settings(continued)**

nF[1:0]	Skew (1Q[0:1],2Q[0:1])	Skew (3Q[0:1])	Skew (4Q[0:1])
LH	$-2t_U$	$-4t_U$	$-4t_U$
ML	$-1t_U$	$-2t_U$	$-2t_U$
MM	Zero skew	Zero skew	Zero skew
MH	$+1t_U$	$+2t_U$	$+2t_U$
HL	$+2t_U$	$+4t_U$	$+4t_U$
HM	$+3t_U$	$+6t_U$	$+6t_U$
HH	$+4t_U$	Divide by 4	Inverted <sup>[6]</sup>

In addition to determining whether the outputs synchronize to the rising or the falling edge of the reference signal, the 3-level PE/HD pin controls the output buffer drive strength as indicated in Table 6.

The CY7B9950 RoboClock® features split power supply buses for Banks 1 and 2, Bank 3 and Bank 4, which enables the user to obtain both 3.3 V and 2.5 V output signals from one device. The core power supply ( $V_{DD}$ ) must be set at a level that is equal to or higher than any one of the output power supplies.

**Table 6. PE/HD Settings**

PE/HD	Synchronization	Output drive strength <sup>[7]</sup>
L	Negative	Low drive
M	Positive	High drive
H	Positive	Low drive

**Table 7. Power Supply Constraints**

$V_{DD}$	$V_{DDQ1}$ <sup>[8]</sup>	$V_{DDQ3}$ <sup>[8]</sup>	$V_{DDQ4}$ <sup>[8]</sup>
3.3 V	3.3 V or 2.5 V	3.3 V or 2.5 V	3.3 V or 2.5 V
2.5 V	2.5 V	2.5 V	2.5 V

## Governing Agencies

The following agencies provide specifications that apply to the CY7B9950 RoboClock®. The agency name and relevant specification is listed below.

**Table 8. Governing Agencies and Specifications**

Agency name	Specification
JEDEC	JESD 51 (theta JA), JESD 65 (skew, jitter)
IEEE	1596.3 (jitter specs)
UL-194_V0	94 (moisture grading)
MIL	883E method 1012.1 (therma theta JC)

## Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V <sub>DD</sub>	Supply voltage		–	4.6	V
V <sub>IN(MIN)</sub>	Input voltage	Relative to V <sub>SS</sub>	V <sub>SS</sub> – 0.3	–	V
V <sub>IN(MAX)</sub>	Input voltage	Relative to V <sub>DD</sub>	–	V <sub>DD</sub> + 0.3	V
T <sub>S</sub>	Temperature, storage	Non-functional	–65	150	°C
T <sub>J</sub>	Temperature, junction	Functional	–	155	°C
∅ <sub>JC</sub>	Dissipation, junction to case	Mil-Spec 883E Method 1012.1	–	42	°C/W
∅ <sub>JA</sub>	Dissipation, junction to ambient	JEDEC (JESD 51)	–	105	°C/W
ESD <sub>HBM</sub>	ESD protection (human body model)	MIL-STD-883, Method 3015	2000	–	V
UL-94	Flammability rating	At 1/8 in.	V–0		
MSL	Moisture sensitivity level		3		
FIT	Failure in time	Manufacturing testing	10		ppm

## Operating Conditions

Parameter	Description	Condition	Min	Max	Unit
V <sub>DD</sub>	Operating voltage	2.5 V ± 5%	2.375	2.625	V
		3.3 V ± 10%	2.97	3.63	V
T <sub>A</sub>	Temperature, operating ambient		–40	85	°C

**DC Electrical Specifications at 2.5 V**

Parameter	Description	Condition	Min	Max	Unit	
$V_{IL}$	Input low voltage	REF, FB and sOE# Inputs	–	0.7	V	
$V_{IH}$	Input high voltage		1.7	–	V	
$V_{IHH}^{[9]}$	Input high voltage	3-level inputs (TEST, FS, nF[1:0], PE/HD) (These pins are normally wired to $V_{DD}$ , GND, or unconnected.)	$V_{DD} - 0.4$	–	V	
$V_{IMM}^{[9]}$	Input MID voltage		$V_{DD}/2 - 0.2$	$V_{DD}/2 + 0.2$	V	
$V_{ILL}^{[9]}$	Input low voltage		–	0.4	V	
$I_{IL}$	Input leakage current	$V_{IN} = V_{DD}/GND$ , $V_{DD} = \text{max.}$ (REF and FB inputs)	–5	5	$\mu\text{A}$	
$I_3$	3-level input DC current	HIGH, $V_{IN} = V_{DD}$	3-level inputs (TEST, FS, nF[1:0], PE/HD)	–	200	$\mu\text{A}$
		MID, $V_{IN} = V_{DD}/2$		–50	50	$\mu\text{A}$
		LOW, $V_{IN} = V_{SS}$		–200	–	$\mu\text{A}$
$I_{PU}$	Input pull-up current	$V_{IN} = V_{SS}$ , $V_{DD} = \text{max.}$	–25	–	$\mu\text{A}$	
$I_{PD}$	Input pull-down current	$V_{IN} = V_{DD}$ , $V_{DD} = \text{max.}$ , (sOE#)	–	100	$\mu\text{A}$	
$V_{OL}$	Output low voltage	$I_{OL} = 12 \text{ mA}$ (PE/HD = L/H), (nQ[0:1])	–	0.4	V	
		$I_{OL} = 20 \text{ mA}$ (PE/HD = MID), (nQ[0:1])	–	0.4	V	
$V_{OH}$	Output high voltage	$I_{OH} = -12 \text{ mA}$ (PE/HD = L/H), (nQ[0:1])	2.0	–	V	
		$I_{OH} = -20 \text{ mA}$ (PE/HD = MID), (nQ[0:1])	2.0	–	V	
$I_{DDQ}$	Quiescent supply current	$V_{DD} = \text{max.}$ , TEST = MID, REF = LOW, sOE# = LOW, outputs not loaded	–	2	mA	
$I_{DD}$	Dynamic supply current	At 100 MHz	150		mA	
$C_{IN}$	Input pin capacitance		4		pF	

**Note**

9. These inputs are normally wired to  $V_{DD}$ , GND or unconnected. Internal termination resistors bias unconnected inputs to  $V_{DD}/2$ .

**DC Electrical Specifications at 3.3 V**

Parameter	Description	Condition	Min	Max	Unit	
$V_{IL}$	Input LOW voltage	REF, FB and sOE# Inputs	–	0.8	V	
$V_{IH}$	Input HIGH voltage		2.0	–	V	
$V_{IHH}^{[10]}$	Input HIGH voltage	3-level inputs (TEST, FS, nF[1:0], PE/HD) (These pins are normally wired to $V_{DD}$ , GND or unconnected.)	$V_{DD} - 0.6$	–	V	
$V_{IMM}^{[10]}$	Input MID voltage		$V_{DD}/2 - 0.3$	$V_{DD}/2 + 0.3$	V	
$V_{ILL}^{[10]}$	Input LOW voltage		–	0.6	V	
$I_{IL}$	Input leakage current	$V_{IN} = V_{DD}/G_{ND}$ , $V_{DD} = \text{max.}$ (REF and FB inputs)	–5	5	$\mu\text{A}$	
$I_3$	3-level input DC current	HIGH, $V_{IN} = V_{DD}$	3-level inputs (TEST, FS, nF[1:0], DS[1:0], PD#/DIV, PE/HD)	–	200	$\mu\text{A}$
		MID, $V_{IN} = V_{DD}/2$		–50	50	$\mu\text{A}$
		LOW, $V_{IN} = V_{SS}$		–200	–	$\mu\text{A}$
$I_{PU}$	Input pull-up current	$V_{IN} = V_{SS}$ , $V_{DD} = \text{max.}$	–100	–	$\mu\text{A}$	
$I_{PD}$	Input pull-down current	$V_{IN} = V_{DD}$ , $V_{DD} = \text{max.}$ , (sOE#)	–	100	$\mu\text{A}$	
$V_{OL}$	Output LOW voltage	$I_{OL} = 12 \text{ mA}$ (PE/HD = L/H), (nQ[0:1])	–	0.4	V	
		$I_{OL} = 24 \text{ mA}$ (PE/HD = MID), (nQ[0:1])	–	0.4	V	
$V_{OH}$	Output HIGH voltage	$I_{OH} = -12 \text{ mA}$ (PE/HD = L/H), (nQ[0:1])	2.4	–	V	
		$I_{OH} = -24 \text{ mA}$ (PE/HD = MID), (nQ[0:1])	2.4	–	V	
$I_{DDQ}$	Quiescent supply current	$V_{DD} = \text{max.}$ , TEST = MID, REF = LOW, sOE# = LOW, outputs not loaded	–	2	mA	
$I_{DD}$	Dynamic supply current	At 100 MHz	230		mA	
$C_{IN}$	Input pin capacitance		4		pF	

**Note**

10. These inputs are normally wired to  $V_{DD}$ , GND or unconnected. Internal termination resistors bias unconnected inputs to  $V_{DD}/2$ .



### Thermal Resistance

Parameter <sup>[11]</sup>	Description	Test Conditions	32-pin TQFP	Unit
$\theta_{JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	65	°C/W
$\theta_{JC}$	Thermal resistance (junction to case)		12	°C/W

### AC Test Loads and Waveforms

Figure 2. AC Test Loads

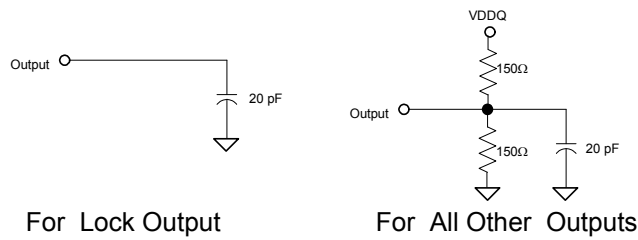


Figure 3. Output Waveforms

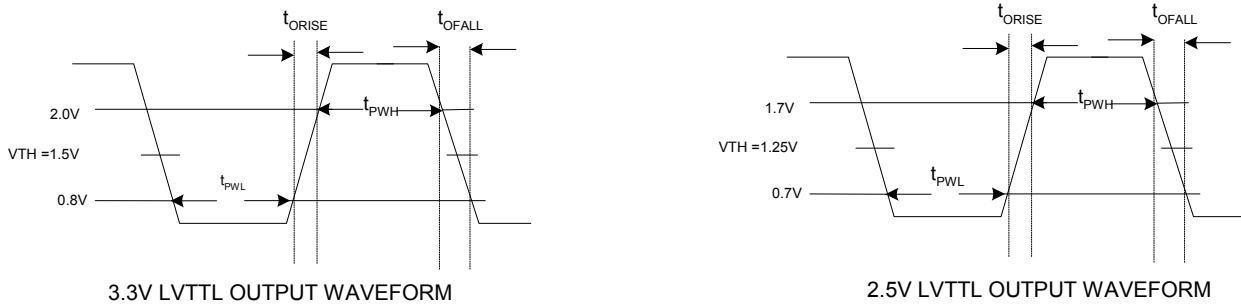
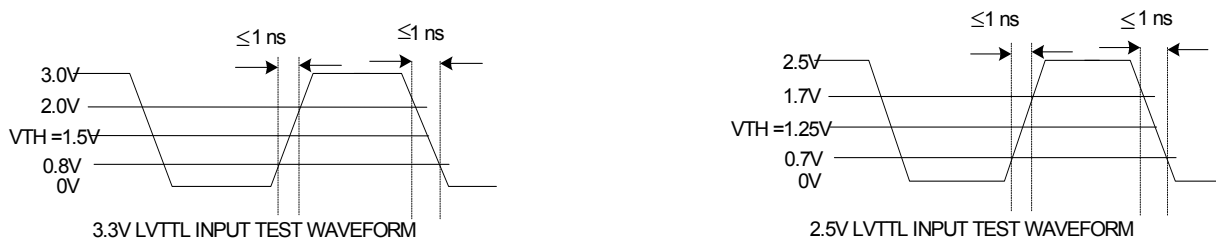


Figure 4. Test Waveforms



**Note**

11. These parameters are guaranteed by design and are not tested.

## AC Input Specifications

Parameter	Description	Condition	Min	Max	Unit
$T_{R,T_F}$	Input rise/fall time	0.8 V–2.0 V	–	10	ns/V
$T_{PWC}$	Input clock pulse	HIGH or LOW	2	–	ns
$T_{DCIN}$	Input duty cycle		10	90	%
$F_{REF}$	Reference input frequency	FS = LOW	6	50	MHz
		FS = MID	12	100	
		FS = HIGH	24	200	

## Switching Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
F <sub>OR</sub>	Output frequency range		6	–	200	MHz
VCO <sub>LR</sub>	VCO lock range		200	–	400	MHz
VCO <sub>LBW</sub>	VCO loop bandwidth		0.25	–	3.5	MHz
t <sub>SKEWPR</sub>	Matched-pair skew <sup>[10]</sup>	Skew between the earliest and the latest output transitions within the same bank.	–	50	100	ps
t <sub>SKEW0</sub>	Output-output skew <sup>[10]</sup>	Skew between the earliest and the latest output transitions among all outputs at 0t <sub>U</sub> .	–	100	200	ps
t <sub>SKEW1</sub>		Skew between the earliest and the latest output transitions among all outputs for which the same phase delay has been selected.	–	100	200	ps
t <sub>SKEW2</sub>		Skew between the nominal output rising edge to the inverted output falling edge.	–	–	500	ps
t <sub>SKEW3</sub>	Output-output skew <sup>[10]</sup>	Skew between non-inverted outputs running at different frequencies.	–	–	500	ps
t <sub>SKEW4</sub>		Skew between nominal to inverted outputs running at different frequencies.	–	–	500	ps
t <sub>SKEW5</sub>		Skew between nominal outputs at different power supply levels.	–	–	650	ps
t <sub>PART</sub>	Part-part skew	Skew between the outputs of any two devices under identical settings and conditions (V <sub>DDQ</sub> , V <sub>DD</sub> , temp, air flow, frequency, etc.).	–	–	750	ps
t <sub>PD0</sub>	Ref-FB propagation delay <sup>[11]</sup>		–250	–	+250	ps
t <sub>ODCV</sub>	Output duty cycle	F <sub>out</sub> < 100 MHz, measured at V <sub>DD</sub> /2	48	49.5/50.5	52	%
		F <sub>out</sub> > 100 MHz, measured at V <sub>DD</sub> /2	45	48/52	55	
t <sub>PWH</sub>	Output high time deviation from 50%	Measured at 2.0V for V <sub>DD</sub> = 3.3 V and at 1.7 V for V <sub>DD</sub> = 2.5V.	–	–	1.5	ns
t <sub>PWL</sub>	Output low time deviation from 50%	Measured at 0.8 V for V <sub>DD</sub> = 3.3 V and at 0.7 V for V <sub>DD</sub> = 2.5 V.	–	–	2.0	ns
t <sub>R</sub> /t <sub>F</sub>	Output rise/fall time	Measured at 0.8 V–2.0 V for V <sub>DD</sub> = 3.3 V and 0.7 V–1.7 V for V <sub>DD</sub> = 2.5 V.	0.15	–	1.5	ns
t <sub>LOCK</sub>	PLL lock time <sup>[12,13]</sup>		–	–	0.5	ms
t <sub>CCJ</sub>	Cycle-cycle jitter	Divide by one output frequency, FS = L, FB = divide by 1, 2, 4.	–	50	100	ps
		Divide by one output frequency, FS = M/H, FB = divide by 1, 2, 4.	–	70	150	ps

### Notes

10. Test load = 20 pF, terminated to V<sub>CC</sub>/2. All outputs are equally loaded.

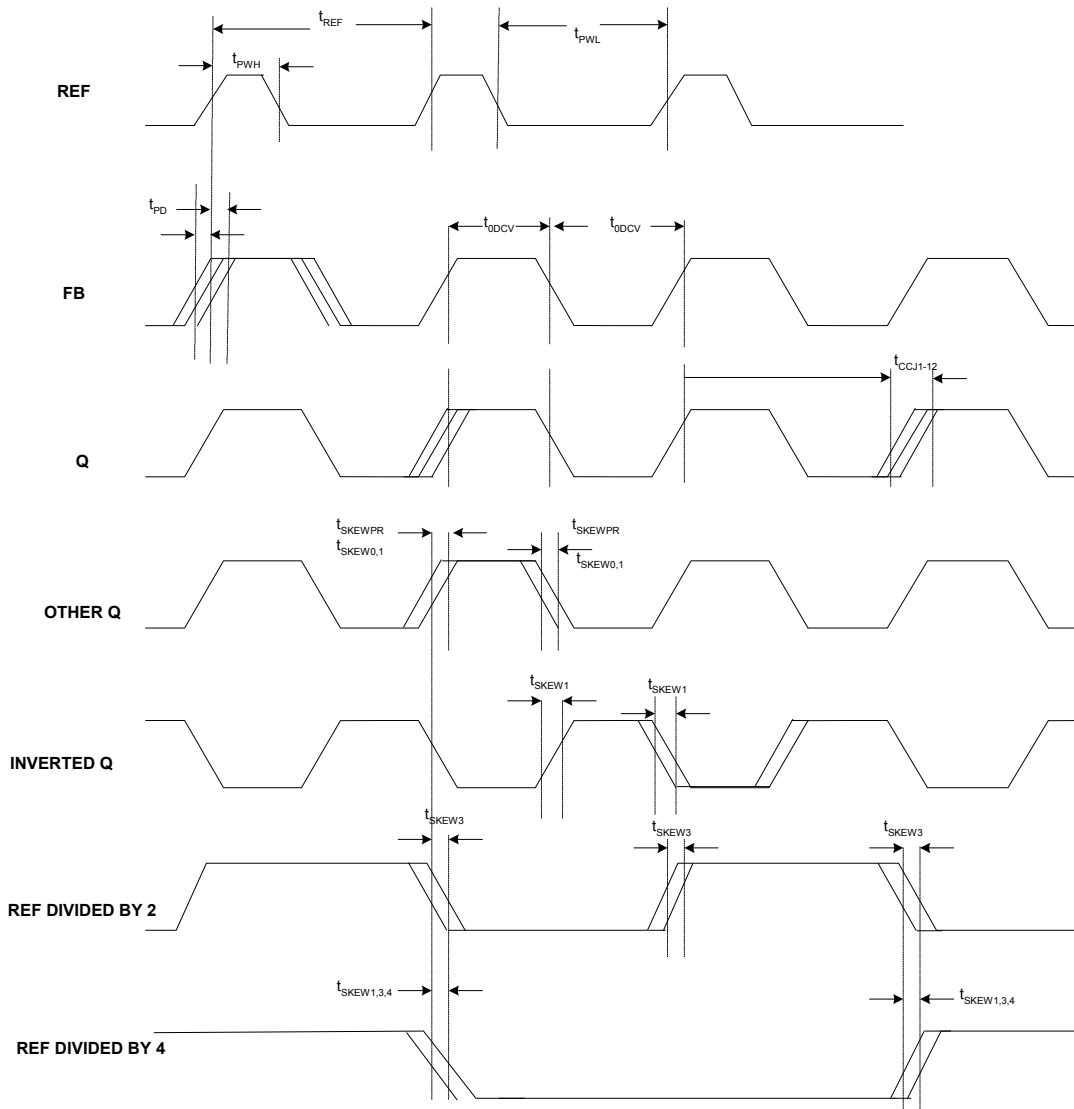
11. t<sub>PD</sub> is measured at 1.5 V for V<sub>DD</sub> = 3.3 V and at 1.25 V for V<sub>DD</sub> = 2.5 V with REF rise/fall times of 0.5 ns between 0.8 V–2.0 V.

12. t<sub>LOCK</sub> is the time that is required before outputs synchronize to REF. This specification is valid with stable power supplies which are within normal operating limits.

13. Lock detector circuit may be unreliable for input frequencies lower than 4 MHz, or for input signals which contain significant jitter.

**AC Timing Definitions**

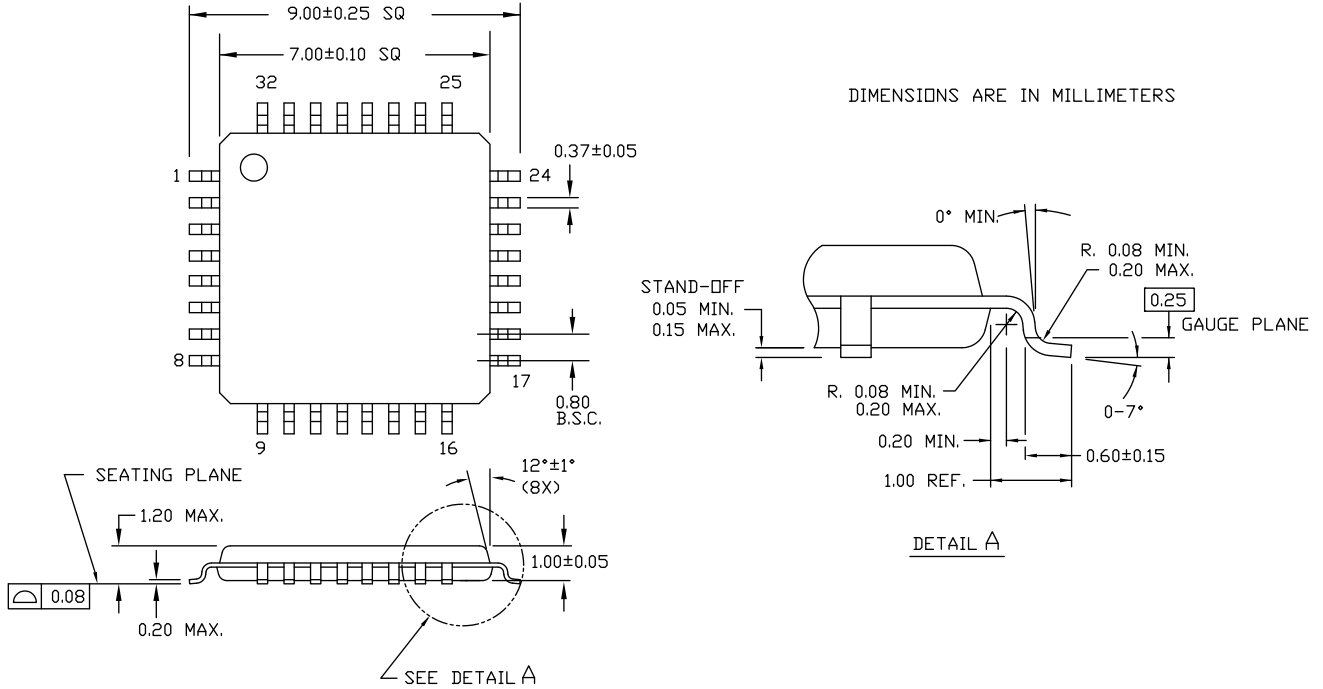
**Figure 5. Timing Definitions**





**Package Diagram**

**Figure 6. 32-pin TQFP (7 × 7 × 1.0 mm) A3210 Package Outline, 51-85063**



51-85063 \*E

## Acronyms

**Table 9. Acronyms Used in this Document**

Acronym	Description
CLKOUT	Clock Output
CMOS	Complementary Metal Oxide Semiconductor
DPM	Die Pick Map
EPROM	Erasable Programmable Read Only Memory
NTSC	National Television System Committee
OE	Output Enable
PAL	Phase Alternate Line
PD	Power Down
PLL	Phase Locked Loop
PPM	Parts Per Million
TTL	Transistor-Transistor Logic

## Document Conventions

### Units of Measure

**Table 10. Units of Measure**

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	μW	microwatt
dB	decibel	mA	milliampere
fC	femtoCoulomb	mm	millimeter
fF	femtofarad	ms	millisecond
Hz	hertz	mV	millivolt
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolt
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
μA	microampere	pp	peak-to-peak
μF	microfarad	ppm	parts per million
μH	microhenry	ps	picosecond
μs	microsecond	sps	samples per second
μV	microvolt	σ	sigma: one standard deviation
μVrms	microvolts root-mean-square		

**Document History Page**

Document Title: CY7B9950 RoboClock®, 2.5/3.3 V, 200 MHz High-Speed Multi-Phase PLL Clock Buffer Document Number: 38-07338				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	121663	11/25/02	RGL	New data sheet.
*A	122548	12/12/02	RGL	Updated <a href="#">DC Electrical Specifications at 2.5 V</a> : Updated details in “Condition” column corresponding to $V_{IH}$ , $V_{IM}$ and $V_{IL}$ parameters (Removed PD#/DIV and DS[1:0]). Updated <a href="#">DC Electrical Specifications at 3.3 V</a> : Updated details in “Condition” column corresponding to $V_{IH}$ , $V_{IM}$ and $V_{IL}$ parameters (Removed PD#/DIV and DS[1:0]).
*B	124646	03/05/03	RGL	Updated <a href="#">Pin Definitions</a> : Updated details in “Description” column corresponding to pin 27 and pin 12. Updated <a href="#">Absolute Maximum Conditions</a> : Changed minimum value of $V_{DD}$ parameter corresponding to Test Condition “Functional @ 2.5V ± 5%” from 2.25 V to 2.375 V. Changed maximum value of $V_{DD}$ parameter corresponding to Test Condition “Functional @ 2.5V ± 5%” from 2.75 V to 2.625 V.
*C	433662	See ECN	RGL	Updated <a href="#">Features</a> : Updated details corresponding to “Output-output skew” and “Cycle-cycle jitter”. Updated <a href="#">Switching Characteristics</a> : Added a column “Typ”. Updated <a href="#">Ordering Information</a> : Updated part numbers.
*D	1562063	See ECN	PYG / AESA	Updated <a href="#">Ordering Information</a> : Updated part numbers. Added a column “Status”.
*E	2894960	03/17/10	KVM	Updated <a href="#">Device Configuration</a> : Updated <a href="#">Table 5</a> : Fixed typo in output skew settings. Updated <a href="#">Absolute Maximum Conditions</a> : Updated $V_{DD}$ value. Added <a href="#">Operating Conditions</a> . Updated <a href="#">Ordering Information</a> : Updated part numbers. Removed the column “Status”. Updated <a href="#">Package Diagram</a> . Updated <a href="#">Sales, Solutions, and Legal Information</a> : Updated links.
*F	3058099	10/14/10	BASH	Added <a href="#">Ordering Code Definitions</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated to new template.
*G	4176123	10/28/2013	CINM	Updated <a href="#">Package Diagram</a> : spec 51-85063 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*H	4571728	11/17/2014	CINM	Updated <a href="#">Functional Description</a> : Added “For a complete list of related documentation, <a href="#">click here.</a> ” at the end.
*I	4764256	05/13/2015	XHT	Updated <a href="#">Absolute Maximum Conditions</a> : Changed value of MSL parameter from 1 to 3. Updated <a href="#">Package Diagram</a> : spec 51-85063 – Changed revision from *D to *E.
*J	5257087	05/03/2016	PSR	Added <a href="#">Thermal Resistance</a> . Updated to new template.



**Document History Page(continued)**

<b>Document Title: CY7B9950 RoboClock<sup>®</sup>, 2.5/3.3 V, 200 MHz High-Speed Multi-Phase PLL Clock Buffer</b>				
<b>Document Number: 38-07338</b>				
<b>Rev.</b>	<b>ECN No.</b>	<b>Submission Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
*K	5493833	10/25/2016	XHT	Updated to new template. Completing Sunset Review.
*L	5992901	12/13/2017	AESATMP8	Updated logo and Copyright.

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