# NCP3337

# Ultra High Accuracy, Low Iq, 500 mA with Power Good Low Dropout Regulator

The NCP3337 is a high performance, low dropout regulator. With accuracy of ±0.9% over line and load and ultra−low quiescent current and noise it encompasses all of the necessary features required by today's consumer electronics. This unique device is guaranteed to be stable without a minimum load current requirement and stable with any type of capacitor as small as 1.0 μF. The NCP3337 also comes equipped with sense and noise reduction pins to increase the overall utility of the device. The NCP3337 offers reverse bias protection.

### Features

- High Accuracy Over Line and Load (±0.9% at 25°C)
- Ultra−Low Dropout Voltage at Full Load (260 mV typ)
- No Minimum Output Current Required for Stability
- Low Noise (33 μVrms w/10 nF $C_{nr}$ and 52 μVrms w/out $C_{nr}$)
- Low Shutdown Current (< 1 mA)
- Reverse Bias Protected
- 2.9 V to 12 V Supply Range
- Thermal Shutdown Protection
- Current Limitation
- Requires Only 1.0 μF Output Capacitance for Stability
- Stable with Any Type of Capacitor (including MLCC)
- Available in 1.8 V, 2.5 V, 3.3 V, 5.0 V and Adjustable Output Voltages
- Power Good Output
- These are Pb−Free Devices

### Applications

- PCMCIA Card
- Cellular Phones
- Camcorders and Cameras
- Networking Systems, DSL/Cable Modems
- Cable Set−Top Box
- MP3/CD Players
- DSP Supply
- Displays and Monitors

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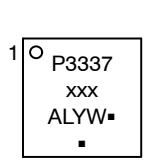
**DFN10**
**MN SUFFIX**
**CASE 485C**

### MARKING DIAGRAM




Pin 1, 2. $V_{out}$
3. Sense / ADJ
4. GND
5. PWRG
6. NC
7. NR
8. $\overline{SD}$
9, 10. $V_{in}$
EP, GND

xxx = Specific Device Marking
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 15 of this data sheet.

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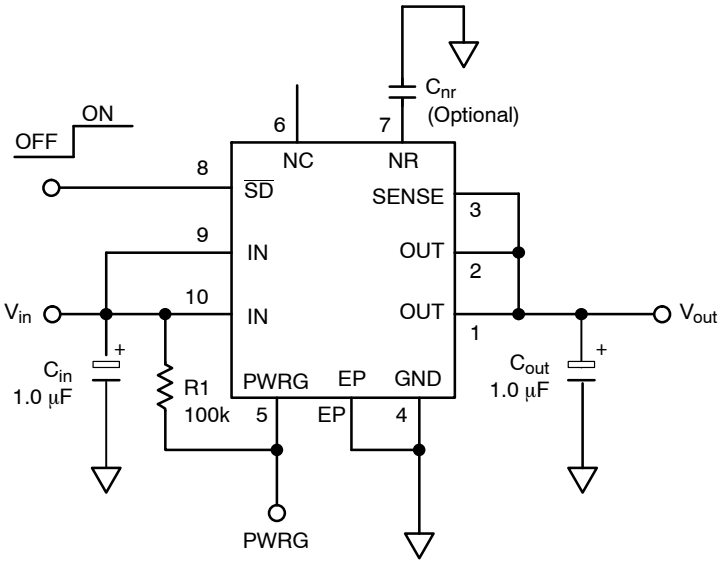



**Figure 1. Typical Fixed Version Application Schematic**

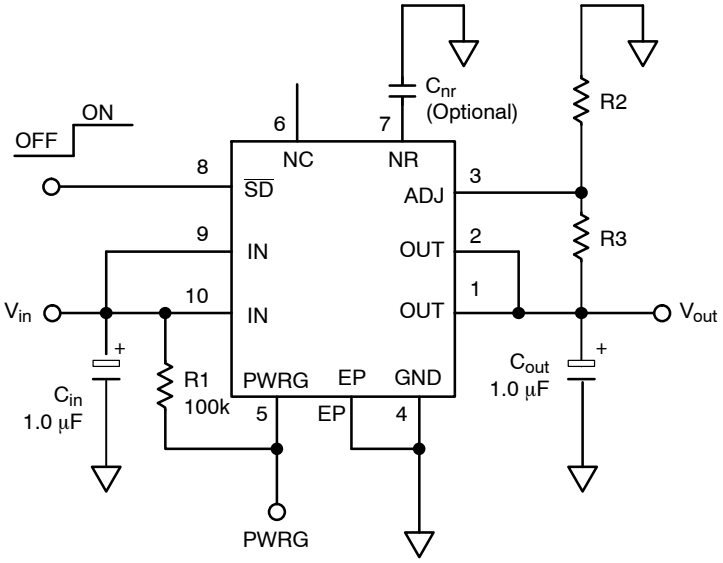



**Figure 2. Typical Adjustable  Version Application Schematic**

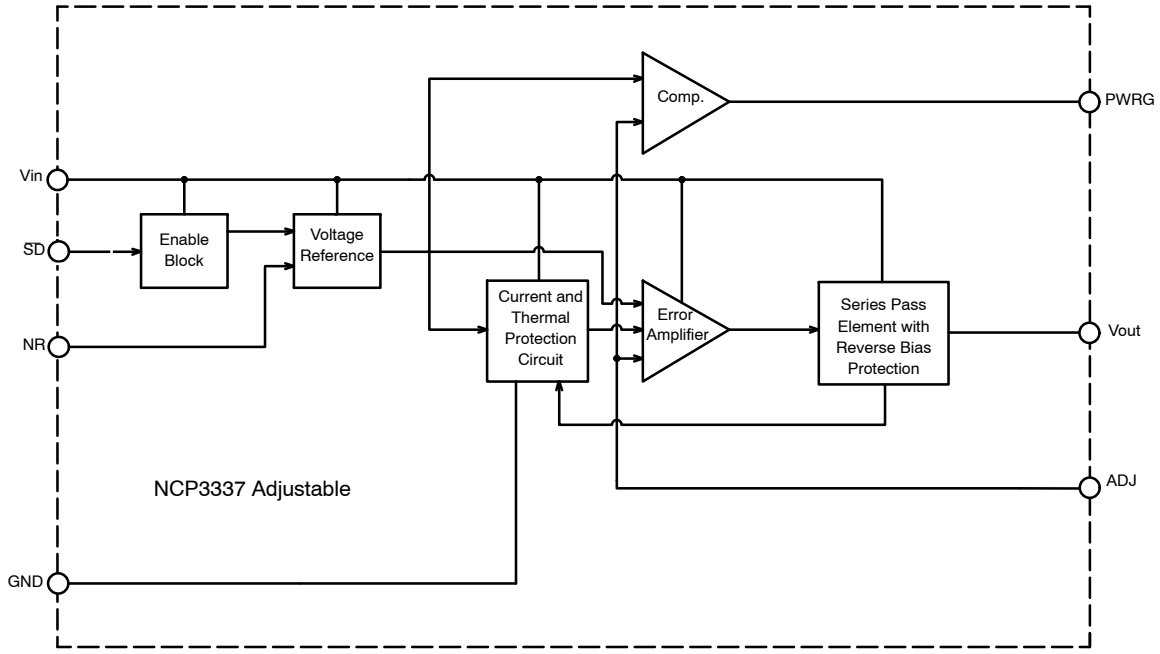



**Figure 3. Block Diagram, Adjustable Output Version**

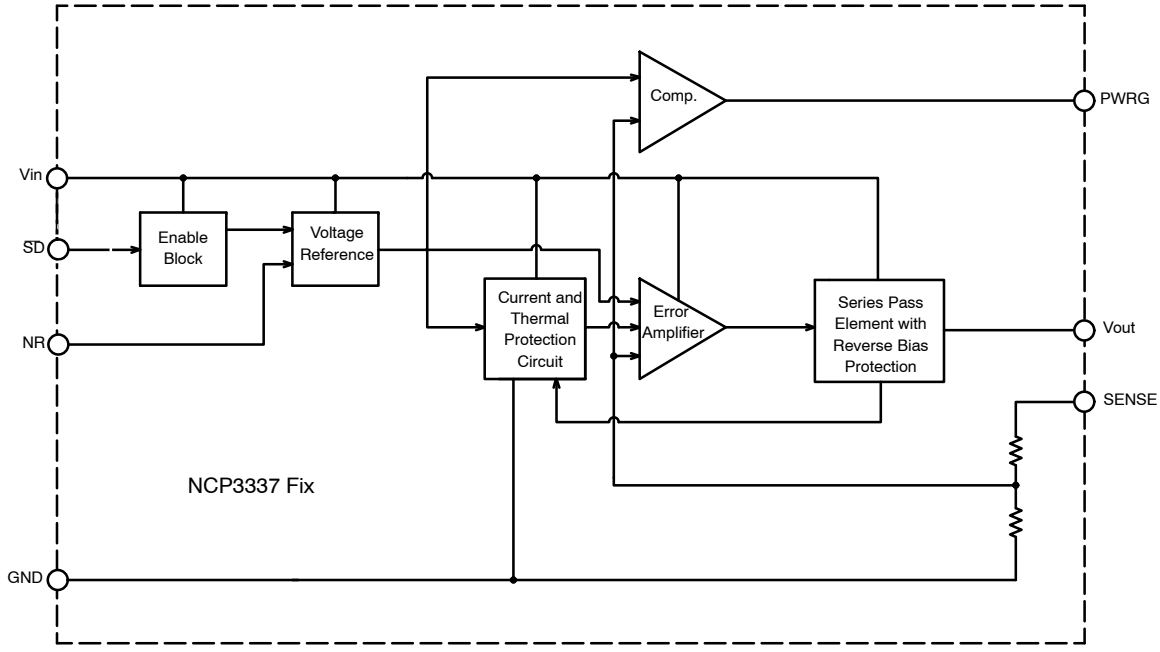



**Figure 4. Block Diagram, Fixed Output Version**

## PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Description |
|---|---|---|
| 1, 2 | $V_{out}$ | Regulated output voltage. Bypass to ground with $C_{out} \geq 1.0\ \mu F$ |
| 3 | SENSE/ADJ | For output voltage sensing, connect to Pins 1 and 2.at Fixed output Voltage version<br>Adjustable pin at Adjustable output version |
| 4 | GND | Power Supply Ground |
| 5 | PWRG | Power Good |
| 6 | NC | Not Connected |
| 7 | NR | Noise Reduction Pin. This is an optional pin used to further reduce noise. |
| 8 | $\overline{SD}$ | Shutdown pin. When not in use, this pin should be connected to the input pin. |
| 9, 10 | $V_{in}$ | Power Supply Input Voltage |
| EPAD | EPAD | Exposed thermal pad should be connected to ground. |

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage | $V_{in}$ | −0.3 to +16 | V |
| Output Voltage | $V_{out}$ | −0.3 to $V_{in}$ +0.3 or 10 V* | V |
| PWRG Pin Voltage | $V_{PWRG}$ | −0.3 to +16 | V |
| Shutdown Pin Voltage | $V_{sh}$ | −0.3 to +16 | V |
| Junction Temperature Range | $T_J$ | −40 to +150 | °C |
| Storage Temperature Range | $T_{stg}$ | −50 to +150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device series contains ESD protection and exceeds the following tests:
Human Body Model (HBM) JESD 22−A114−B
Machine Model (MM) JESD 22−A115−A

*Which ever is less. Reverse bias protection feature valid only if ($V_{out} - V_{in}$) ≤ 7 V.

## THERMAL CHARACTERISTICS

| Characteristic | Test Conditions (Typical Value) | | Unit |
|---|---|---|---|
| | **Min Pad Board** (Note 1) | **1″ Pad Board** (Note 1) | |
| Junction−to−Air, θJA | 215 | 66 | °C/W |
| Junction−to−Pin, J−L4 | 58 | 18 | °C/W |

1. As mounted on a 35 x 35 x 1.5 mm FR4 Substrate, with a single layer of a specified copper area of 2 oz (0.07 mm thick) copper traces and heat spreading area. JEDEC 51 specifications for a low and high conductivity test board recommend a 2 oz copper thickness. Test conditions are under natural convection or zero air flow.

**ELECTRICAL CHARACTERISTICS – 5 V** ($V_{out}$ = 5.0 V typical, $V_{in}$ = 5.4 V, $T_A$ = −40°C to +85°C, unless otherwise noted, Note 2)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage (Accuracy)<br>$V_{in}$ = 5.4 V to 7.3 V, $I_{load}$ = 0.1 mA to 500 mA, $T_A$ = 25°C | $V_{out}$ | −0.90%<br>4.955 | 5 | 0.90%<br>5.045 | V |
| Output Voltage (Accuracy)<br>$V_{in}$ = 5.4 V to 7.3 V, $I_{load}$ = 0.1 mA to 500 mA, $T_A$ = 0°C to +85°C | $V_{out}$ | −1.40%<br>4.930 | 5 | 1.40%<br>5.070 | V |
| Output Voltage (Accuracy)<br>$V_{in}$ = 5.4 V to 7.3 V, $I_{load}$ = 0.1 mA to 500 mA, $T_A$ = −40°C to +125°C | $V_{out}$ | −1.50%<br>4.925 | 5 | 1.50%<br>5.075 | V |
| Line Regulation<br>$V_{in}$ = 5.4 V to 12 V, $I_{load}$ = 0.1 mA | $Line_{Reg}$ | | 0.04 | | mV/V |
| Load Regulation<br>$V_{in}$ = 5.4 V, $I_{load}$ = 0.1 mA to 500 mA | $Load_{Reg}$ | | 0.04 | | mV/mA |
| Dropout Voltage (See Application Note)<br>$I_{load}$ = 500 mA<br>$I_{load}$ = 300 mA<br>$I_{load}$ = 50 mA<br>$I_{load}$ = 0.1 mA | $V_{DO}$ | | | <br>340<br>230<br>110<br>10 | mV |
| Peak Output Current (See Figure 14) | $I_{pk}$ | 500 | 700 | 830 | mA |
| Short Output Current (See Figure 14) $V_{in}$ < 7 V, $T_A$ = 25°C | $I_{sc}$ | | | 930 | mA |
| Thermal Shutdown / Hysteresis | $T_J$ | | 160/10 | | °C |
| Ground Current<br>In Regulation<br>$I_{load}$ = 500 mA (Note 4)<br>$I_{load}$ = 300 mA (Note 4)<br>$I_{load}$ = 50 mA<br>$I_{load}$ = 0.1 mA<br>In Dropout<br>$V_{in}$ = 3.2 V, $I_{load}$ = 0.1 mA<br>In Shutdown<br>$V_{SD}$ = 0 V | $I_{GND}$<br><br><br><br><br><br><br><br>$I_{GNDsh}$ | | <br><br>9<br>4.6<br>0.8<br>–<br><br><br><br> | <br><br>14<br>7.5<br>2.5<br>220<br><br>500<br><br>1 | <br><br>mA<br><br><br>μA<br><br>μA<br><br>μA |
| Output Noise<br>$C_{nr}$ = 0 nF, $I_{load}$ = 500 mA, f = 10 Hz to 100 kHz, $C_{out}$ = 10 μF<br>$C_{nr}$ = 10 nF, $I_{load}$ = 500 mA, f = 10 Hz to 100 kHz, $C_{out}$ = 10 μF | $V_{noise}$ | | <br>93<br>58 | | μVrms |
| Power Good Voltage<br>Low Threshold<br>Hysteresis<br>High Threshold | $V_{elft}$ | <br>93 | <br>95<br>2<br>97 | <br><br><br>99 | % of $V_{out}$ |
| Power Good Pin Voltage Saturation ($I_{ef}$ = 1.0 mA) | $V_{efdo}$ | | 200 | | mV |
| Power Good Pin Leakage | $I_{efleak}$ | | 1 | | μA |
| Power Good Blanking Time (Note 3) | $t_{ef}$ | | 50 | | μs |
| Shutdown<br>Threshold Voltage ON<br>Threshold Voltage OFF | $V_{SD}$ | <br>2 | | <br><br>0.4 | V |
| SD Input Current, $V_{SD}$ = 0 V to 0.4 V or $V_{SD}$ = 2.0 V to $V_{in}$ | $I_{SD}$ | | 0.07 | 1 | μA |
| Output Current In Shutdown Mode, $V_{out}$ = 0 V | $I_{OSD}$ | | 0.07 | 1 | μA |
| Reverse Bias Protection, Current Flowing from the Output Pin to GND<br>($V_{in}$ = 0 V, $V_{out_forced}$ = 5 V) | $I_{OUTR}$ | | 10 | | μA |

2. Performance guaranteed over the operating temperature range by design and/or characterization, production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
3. Can be disabled per customer request.
4. $T_A$ must be greater than 0°C.

**ELECTRICAL CHARACTERISTICS – 3.3 V** ($V_{out}$ = 3.3 V typical, $V_{in}$ = 3.7 V, $T_A$ = −40°C to +85°C, unless otherwise noted, Note 5)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage (Accuracy)<br>$V_{in}$ = 3.7 V to 7.3 V, $I_{load}$ = 0.1 mA to 500 mA, $T_A$ = 25°C | $V_{out}$ | −0.90%<br>3.270 | 3.3 | 0.90%<br>3.330 | V |
| Output Voltage (Accuracy)<br>$V_{in}$ = 3.7 V to 7.3 V, $I_{load}$ = 0.1 mA to 500 mA, $T_A$ = 0°C to +85°C | $V_{out}$ | −1.40%<br>3.254 | 3.3 | 1.40%<br>3.346 | V |
| Output Voltage (Accuracy)<br>$V_{in}$ = 3.7 V to 7.3 V, $I_{load}$ = 0.1 mA to 500 mA, $T_A$ = −40°C to +125°C | $V_{out}$ | −1.50%<br>3.250 | 3.3 | 1.50%<br>3.350 | V |
| Line Regulation<br>$V_{in}$ = 3.7 V to 12 V, $I_{load}$ = 0.1 mA | $Line_{Reg}$ | | 0.04 | | mV/V |
| Load Regulation<br>$V_{in}$ = 3.7 V, $I_{load}$ = 0.1 mA to 500 mA | $Load_{Reg}$ | | 0.04 | | mV/mA |
| Dropout Voltage (See Application Note)<br>$I_{load}$ = 500 mA<br>$I_{load}$ = 300 mA<br>$I_{load}$ = 50 mA<br>$I_{load}$ = 0.1 mA | $V_{DO}$ | | <br>340<br>230<br>110<br>10 | | mV |
| Peak Output Current (See Figure 14) | $I_{pk}$ | 500 | 700 | 800 | mA |
| Short Output Current (See Figure 14) $V_{in}$ < 7 V, $T_A$ = 25°C | $I_{sc}$ | | | 900 | mA |
| Thermal Shutdown / Hysteresis | $T_J$ | | 160/10 | | °C |
| Ground Current<br>In Regulation<br>$I_{load}$ = 500 mA (Note 7)<br>$I_{load}$ = 300 mA<br>$I_{load}$ = 50 mA<br>$I_{load}$ = 0.1 mA<br>In Dropout<br>$V_{in}$ = 3.7 V, $I_{load}$ = 0.1 mA<br>In Shutdown<br>$V_{SD}$ = 0 V | $I_{GND}$<br><br><br><br><br><br><br><br>$I_{GNDsh}$ | | <br><br>9<br>4.6<br>0.8<br>–<br><br><br><br> | <br><br>14<br>7.5<br>2.5<br>220<br><br>500<br><br>1 | <br><br>mA<br><br><br>μA<br><br>μA<br><br>μA |
| Output Noise<br>$C_{nr}$ = 0 nF, $I_{load}$ = 500 mA, f = 10 Hz to 100 kHz, $C_{out}$ = 10 μF<br>$C_{nr}$ = 10 nF, $I_{load}$ = 500 mA, f = 10 Hz to 100 kHz, $C_{out}$ = 10 μF | $V_{noise}$ | | <br>69<br>46 | | μVrms |
| Power Good Voltage<br>Low Threshold<br>Hysteresis<br>High Threshold | $V_{elft}$ | <br>93 | <br>95<br>2<br>97 | <br><br><br>99 | % of $V_{out}$ |
| Power Good Pin Voltage Saturation ($I_{ef}$ = 1.0 mA) | $V_{efdo}$ | | 200 | | mV |
| Power Good Pin Leakage | $I_{efleak}$ | | 1 | | μA |
| Power Good Blanking Time (Note 6) | $t_{ef}$ | | 50 | | μs |
| Shutdown<br>Threshold Voltage ON<br>Threshold Voltage OFF | $V_{SD}$ | <br>2 | | <br><br>0.4 | V |
| SD Input Current, $V_{SD}$ = 0 V to 0.4 V or $V_{SD}$ = 2.0 V to $V_{in}$ | $I_{SD}$ | | 0.07 | 1 | μA |
| Output Current In Shutdown Mode, $V_{out}$ = 0 V | $I_{OSD}$ | | 0.07 | 1 | μA |
| Reverse Bias Protection, Current Flowing from the Output Pin to GND<br>($V_{in}$ = 0 V, $V_{out_forced}$ = 3.3 V) | $I_{OUTR}$ | | 10 | | μA |

5. Performance guaranteed over the operating temperature range by design and/or characterization, production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
6. Can be disabled per customer request.
7. $T_A$ must be greater than 0°C.

**ELECTRICAL CHARACTERISTICS – 2.5 V** ($V_{out}$ = 2.5 V typical, $V_{in}$ = 2.9 V, $T_A$ = −40°C to +85°C, unless otherwise noted, Note 8)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage (Accuracy)<br>$V_{in}$ = 2.9 V to 6.5 V, $I_{load}$ = 0.1 mA to 500 mA, $T_A$ = 25°C | $V_{out}$ | −0.9%<br>2.477 | 2.5 | +0.9%<br>2.523 | V |
| Output Voltage (Accuracy)<br>$V_{in}$ = 2.9 V to 6.5 V, $I_{load}$ = 0.1 mA to 500 mA, $T_A$ = 0°C to +85°C | $V_{out}$ | −1.4%<br>2.465 | 2.5 | +1.4%<br>2.535 | V |
| Output Voltage (Accuracy)<br>$V_{in}$ = 2.9 V to 6.5 V, $I_{load}$ = 0.1 mA to 500 mA, $T_A$ = −40°C to +125°C | $V_{out}$ | −1.5%<br>2.462 | 2.5 | +1.5%<br>2.538 | V |
| Minimum Input Voltage | $V_{inmin}$ | | 2.9 | | V |
| Line Regulation<br>$V_{in}$ = 2.9 V to 12 V, $I_{load}$ = 0.1 mA | $Line_{Reg}$ | | 0.04 | | mV/V |
| Load Regulation<br>$V_{in}$ = 2.9 V, $I_{load}$ = 0.1 mA to 500 mA | $Load_{Reg}$ | | 0.04 | | mV/mA |
| Dropout Voltage (See Figure 10)<br>$I_{load}$ = 500 mA (Note 9)<br>$I_{load}$ = 300 mA (Note 9)<br>$I_{load}$ = 50 mA<br>$I_{load}$ = 0.1mA | $V_{DO}$ | | <br>340<br>230<br>110<br>10 | | mV |
| Peak Output Current (See Figures 14 and 18) | $I_{pk}$ | 500 | 700 | 800 | mA |
| Short Output Current (See Figure 14) $V_{in}$ < 7 V, $T_A$ = 25°C | $I_{sc}$ | | | 900 | mA |
| Thermal Shutdown / Hysteresis | $T_J$ | | 160/10 | | °C |
| Ground Current<br>In Regulation<br>$I_{load}$ = 500 mA (Note 9)<br>$I_{load}$ = 300 mA (Note 9)<br>$I_{load}$ = 50 mA<br>$I_{load}$ = 0.1 mA<br><br>In Dropout<br>$V_{in}$ = 2.4 V, $I_{load}$ = 0.1 mA<br><br>In Shutdown<br>$V_{SD}$ = 0 V | $I_{GND}$<br><br><br><br><br><br><br><br><br>$I_{GNDsh}$ | | <br><br>9.0<br>4.6<br>0.8<br>–<br><br><br><br>500<br><br><br> | <br><br>14<br>7.5<br>2.5<br>220<br><br><br><br><br><br>1.0 | <br><br>mA<br><br><br>μA<br><br><br><br>μA<br><br><br>μA |
| Output Noise<br>$C_{nr}$ = 0 nF, $I_{load}$ = 500 mA, f = 10 Hz to 100 kHz, $C_{out}$ = 10 μF<br>$C_{nr}$ = 10 nF, $I_{load}$ = 500 mA, f = 10 Hz to 100 kHz, $C_{out}$ = 10 μF | $V_{noise}$ | | <br>56<br>35 | | <br>μVrms<br>μVrms |
| Power Good Voltage<br>Low Threshold<br>Hysteresis<br>High Threshold | $V_{elft}$ | <br>93 | <br>95<br>2<br>97 | <br><br><br>99 | % of $V_{out}$ |
| Power Good Pin Voltage Saturation ($I_{ef}$ – 1.0 mA) | $V_{efdo}$ | | 200 | | mV |
| Power Good Pin Leakage | $I_{efleak}$ | | 1.0 | | μA |
| Power Good Blanking Time (Note 10) | $t_{ef}$ | | 50 | | μs |
| Shutdown<br>Threshold Voltage ON<br>Threshold Voltage OFF | $V_{SD}$ | <br>2.0 | | <br><br>0.4 | <br>V<br>V |
| $S_D$ Input Current, $V_{SD}$ = 0 V to 0.4 V or $V_{SD}$ = 2.0 V to $V_{in}$ | $I_{SD}$ | | 0.07 | 1.0 | μA |
| Output Current In Shutdown Mode, $V_{out}$ = 0 V | $I_{OSD}$ | | 0.07 | 1.0 | μA |
| Reverse Bias Protection, Current Flowing from the Output Pin to GND<br>($V_{in}$ = 0 V, $V_{out_forced}$ = 2.5 V) | $I_{OUTR}$ | | 10 | | μA |

8. Performance guaranteed over the operating temperature range by design and/or characterization, production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
9. $T_A$ must be greater than 0°C.
10. Can be disabled per customer request.

**ELECTRICAL CHARACTERISTICS – 1.8 V** ($V_{out}$ = 1.8 V typical, $V_{in}$ = 2.9 V, $T_A$ = −40°C to +85°C, unless otherwise noted, Note 11)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Output Voltage (Accuracy)<br>$V_{in}$ = 2.9 V to 5.8 V, $I_{load}$ = 0.1 mA to 500 mA, $T_A$ = 25°C | $V_{out}$ | −0.9%<br>1.783 | 1.8 | +0.9%<br>1.817 | V |
| Output Voltage (Accuracy)<br>$V_{in}$ = 2.9 V to 5.8 V, $I_{load}$ = 0.1 mA to 500 mA, $T_A$ = 0°C to +85°C | $V_{out}$ | −1.4%<br>1.774 | 1.8 | +1.4%<br>1.826 | V |
| Output Voltage (Accuracy)<br>$V_{in}$ = 2.9 V to 5.8 V, $I_{load}$ = 0.1 mA to 500 mA, $T_A$ = −40°C to +125°C | $V_{out}$ | −1.5%<br>1.773 | 1.8 | +1.5%<br>1.827 | V |
| Minimum Input Voltage | $V_{inmin}$ | | 2.9 | | V |
| Line Regulation<br>$V_{in}$ = 2.9 V to 12 V, $I_{load}$ = 0.1 mA | $Line_{Reg}$ | | 0.04 | | mV/V |
| Load Regulation<br>$V_{in}$ = 2.9 V, $I_{load}$ = 0.1 mA to 500 mA | $Load_{Reg}$ | | 0.04 | | mV/mA |
| Dropout Voltage (See Figure 9)<br>$I_{load}$ = 500 mA (Notes 12, 13)<br>$I_{load}$ = 300 mA (Notes 12, 13)<br>$I_{load}$ = 50 mA (Notes 12, 13) | $V_{DO}$ | | <br>620<br>230<br>95 | | mV |
| Peak Output Current (See Figures 14 and 17) | $I_{pk}$ | 500 | 700 | 830 | mA |
| Short Output Current (See Figure 14) $V_{in}$ < 7 V, $T_A$ = 25°C | $I_{sc}$ | | | 900 | mA |
| Thermal Shutdown / Hysteresis | $T_J$ | | 160/10 | | °C |
| Ground Current<br>In Regulation<br>$I_{load}$ = 500 mA (Note 12)<br>$I_{load}$ = 300 mA (Note 12)<br>$I_{load}$ = 50 mA<br>$I_{load}$ = 0.1 mA<br><br>In Dropout<br>$V_{in}$ = 2.2 V, $I_{load}$ = 0.1 mA<br><br>In Shutdown<br>$V_{SD}$ = 0 V | $I_{GND}$<br><br><br><br><br><br><br><br><br>$I_{GNDsh}$ | | <br><br>9.0<br>4.6<br>0.8<br>–<br><br><br><br><br> | <br><br>14<br>7.5<br>2.5<br>220<br><br>500<br><br>1.0 | <br><br>mA<br><br><br>μA<br><br>μA<br><br>μA |
| Output Noise<br>$C_{nr}$ = 0 nF, $I_{load}$ = 500 mA, f = 10 Hz to 100 kHz, $C_{out}$ = 10 μF<br>$C_{nr}$ = 10 nF, $I_{load}$ = 500 mA, f = 10 Hz to 100 kHz, $C_{out}$ = 10 μF | $V_{noise}$ | | <br>52<br>33 | | <br>μVrms<br>μVrms |
| Power Good Voltage<br>Low Threshold<br>Hysteresis<br>High Threshold | $V_{elft}$ | <br>93 | <br>95<br>2<br>97 | <br><br><br>99 | % of $V_{out}$ |
| Power Good Pin Voltage Saturation ($I_{ef}$ – 1.0 mA) | $V_{efdo}$ | | 200 | | mV |
| Power Good Pin Leakage | $I_{efleak}$ | | 1.0 | | μA |
| Power Good Blanking Time (Note 10) | $t_{ef}$ | | 50 | | μs |
| Shutdown<br>Threshold Voltage ON<br>Threshold Voltage OFF | $V_{SD}$ | <br>2.0 | | <br><br>0.4 | <br>V<br>V |
| SD Input Current, $V_{SD}$ = 0 V to 0.4 V or $V_{SD}$ = 2.0 V to $V_{in}$ | $I_{SD}$ | | 0.07 | 1.0 | μA |
| Output Current In Shutdown Mode, $V_{out}$ = 0 V | $I_{OSD}$ | | 0.07 | 1.0 | μA |
| Reverse Bias Protection, Current Flowing from the Output Pin to GND<br>($V_{in}$ = 0 V, $V_{out_forced}$ = 1.8 V) | $I_{OUTR}$ | | 10 | | μA |

11. Performance guaranteed over the operating temperature range by design and/or characterization, production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
12. $T_A$ must be greater than 0°C.
13. Maximum dropout voltage is limited by minimum input voltage $V_{in}$ = 2.9 V recommended for guaranteed operation.

**ELECTRICAL CHARACTERISTICS – ADJUSTABLE** ($V_{out}$ = 1.25 V typical, $V_{in}$ = 2.9 V, $T_A$ = −40°C to +85°C, unless otherwise noted, Note 14)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Reference Voltage (Accuracy)<br>$V_{in}$ = 2.9 V to $V_{out}$ +4.0 V, $I_{load}$ = 0.1 mA to 500 mA, $T_A$ = 25°C | $V_{ref}$ | −0.90%<br>1.239 | 1.25 | 0.90%<br>1.261 | V |
| Reference Voltage (Accuracy)<br>$V_{in}$ = 2.9 V to $V_{out}$ + 4.0 V, $I_{load}$ = 0.1 mA to 500 mA, $T_A$ = 0°C to +85°C | $V_{ref}$ | −1.40%<br>1.233 | 1.25 | 1.40%<br>1.268 | V |
| Reference Voltage (Accuracy) (Note 18)<br>$V_{in}$ = 2.9 V to $V_{out}$ + 4.0 V, $I_{load}$ = 0.1 mA to 500 mA, $T_A$ = −40°C to +125°C | $V_{ref}$ | −1.50%<br>1.231 | 1.25 | 1.50%<br>1.269 | V |
| Line Regulation<br>$V_{in}$ = 2.9 V to 12 V, $I_{load}$ = 0.1 mA | $Line_{Reg}$ | | 0.04 | | mV/V |
| Load Regulation<br>$V_{in}$ = 2.9 V to 12 V, $I_{load}$ = 0.1 mA to 500 mA | $Load_{Reg}$ | | 0.04 | | mV/mA |
| Dropout Voltage (See Application Note) ($V_{out}$ = 2.5 V − 10 V)<br>$I_{load}$ = 500 mA (Note 16)<br>$I_{load}$ = 300 mA<br>$I_{load}$ = 50 mA<br>$I_{load}$ = 0.1 mA | $V_{DO}$ | | <br>340<br>230<br>110<br>10 | | mV |
| Peak Output Current (See Figure 14) | $I_{pk}$ | 500 | 700 | 830 | mA |
| Short Output Current (See Figure 14) $V_{in}$ < 7 V, $T_A$ = 25°C<br>$V_{out} \leq$ 3.3 V<br>$V_{out}$ > 3.3 V | $I_{sc}$ | | | <br>900<br>930 | mA |
| Thermal Shutdown / Hysteresis | $T_J$ | | 160/<br>10 | | °C |
| Ground Current<br>In Regulation<br>$I_{load}$ = 500 mA (Note 16)<br>$I_{load}$ = 300 mA (Note 16)<br>$I_{load}$ = 50 mA<br>$I_{load}$ = 0.1 mA<br>In Dropout<br>Vin = $V_{out}$ + 0.1 V or 2.9 V (whichever is higher), $I_{load}$ = 0.1 mA<br>In Shutdown<br>$V_{SD}$ = 0 V | $I_{GND}$<br><br><br><br><br><br><br><br>$I_{GNDsh}$ | | <br><br>9<br>4.6<br>0.8<br><br><br><br> | <br><br>14<br>7.5<br>2.5<br>220<br><br>500<br><br>1 | <br><br>mA<br><br><br>μA<br><br>μA<br><br>μA |
| Output Noise<br>$C_{nr}$ = 0 nF, $I_{load}$ = 500 mA, f = 10 Hz to 100 kHz, $C_{out}$ = 10 μF<br>$C_{nr}$ = 10 nF, $I_{load}$ = 500 mA, f = 10 Hz to 100 kHz, $C_{out}$ = 10 μF | $V_{noise}$ | | <br>69<br>46 | | $\mu V_{rms}$ |
| Power Good Voltage<br>Low Threshold<br>Hysteresis<br>High Threshold | $V_{elft}$ | <br>93 | <br>95<br>2<br>97 | <br><br><br>99 | % of $V_{out}$ |
| Power Good Pin Voltage Saturation ($I_{ef}$ = 1.0 mA) | $V_{efdo}$ | | 200 | | mV |
| Power Good Pin Leakage | $I_{efleak}$ | | 1 | | μA |
| Power Good Pin Blanking Time (Note 15) | $t_{ef}$ | | 50 | | μs |
| Shutdown<br>Threshold Voltage ON<br>Threshold Voltage OFF | $V_{SD}$ | <br>2 | | <br><br>0.4 | V |
| SD Input Current, $V_{SD}$ = 0 V to 0.4 V or $V_{SD}$ = 2.0 V to $V_{in}$<br>$V_{in} \leq$ 5.4 V<br>$V_{in}$ > 5.4 V | $I_{SD}$ | | <br>0.07 | <br>1<br>5 | μA |
| Output Current In Shutdown Mode, $V_{out}$ = 0 V | $I_{OSD}$ | | 0.07 | 1 | μA |
| Reverse Bias Protection, Current Flowing from the Output Pin to GND<br>($V_{in}$ = 0 V, $V_{out_forced}$ = $V_{out\ (nom)}$ ≤ 7 V) (Note 17) | $I_{OUTR}$ | | 1 | | μA |

14. Performance guaranteed over the operating temperature range by design and/or characterization, production tested at $T_J$ = $T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
15. Can be disabled per customer request.
16. $T_A$ must be greater than 0°C.
17. Reverse bias protection feature valid only if $V_{out} - V_{in} \leq 7$ V.
18. For output current capability for $T_A$ < 0°C, please refer to Figures 17 and 18.

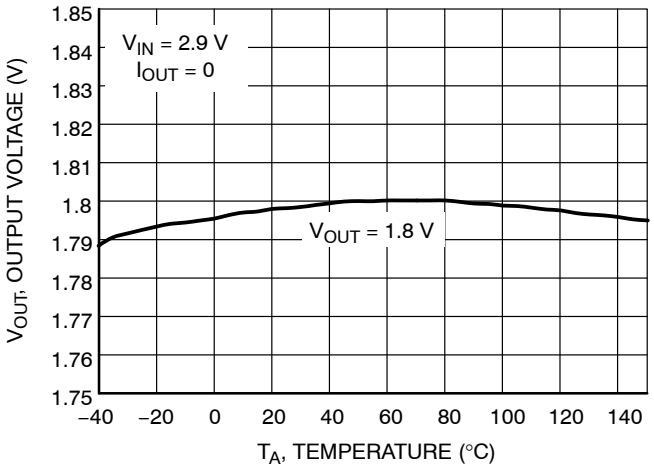



**Figure 5. Output Voltage vs. Temperature 1.8 V Version**

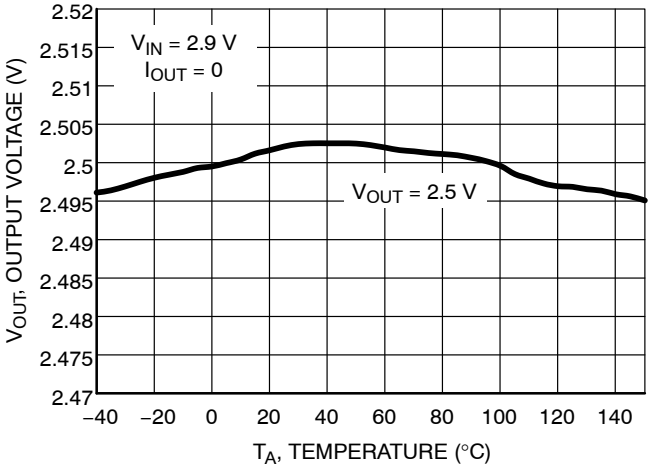



**Figure 6. Output Voltage vs. Temperature 2.5 V Version**

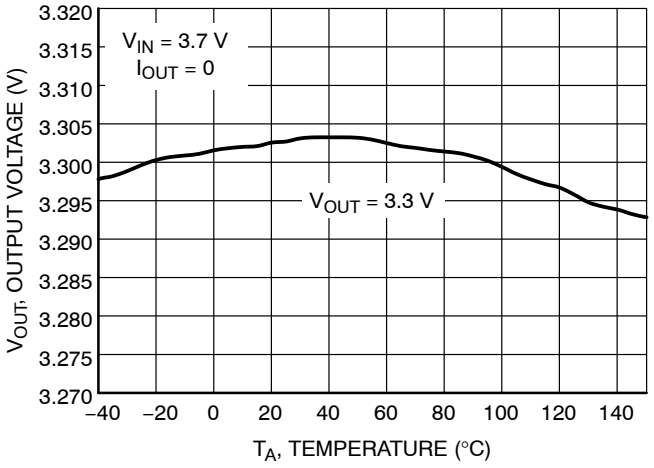



**Figure 7. Output Voltage vs. Temperature 3.3 V Version**

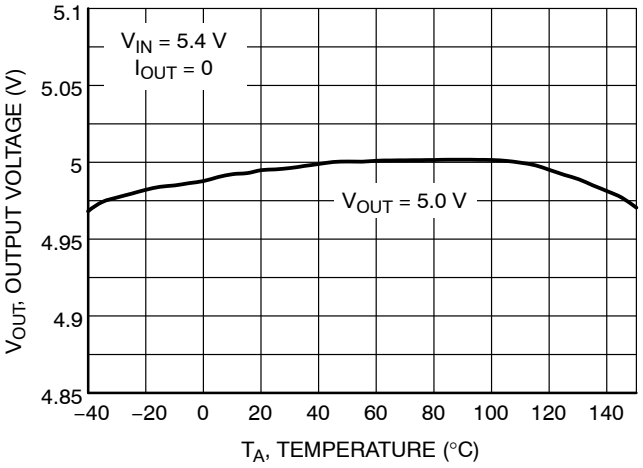



**Figure 8. Output Voltage vs. Temperature 5.0 V Version**

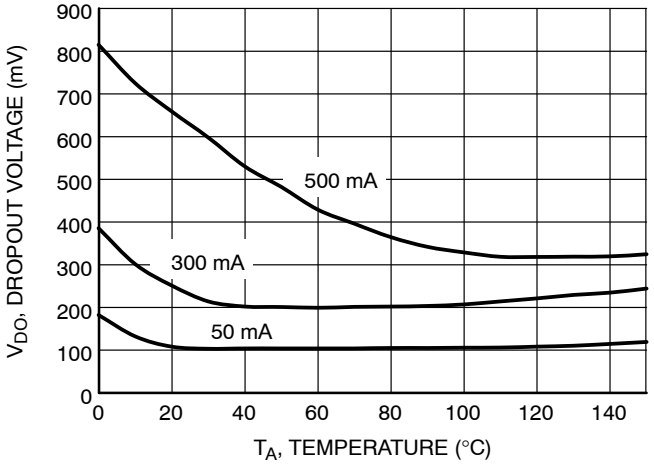



**Figure 9. Dropout Voltage vs. Temperature 1.8 V Version**

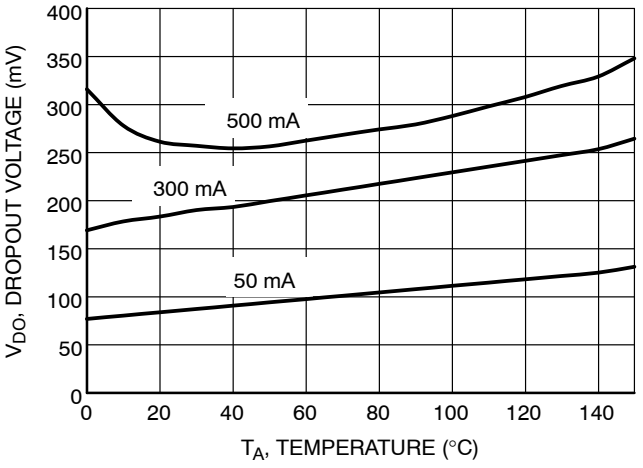



**Figure 10. Dropout Voltage vs. Temperature 2.5 V Version**

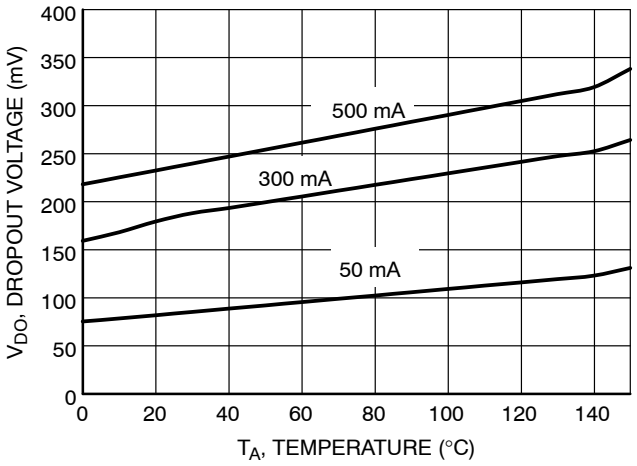



**Figure 11. Dropout Voltage vs. Temperature 3.3 V Version**

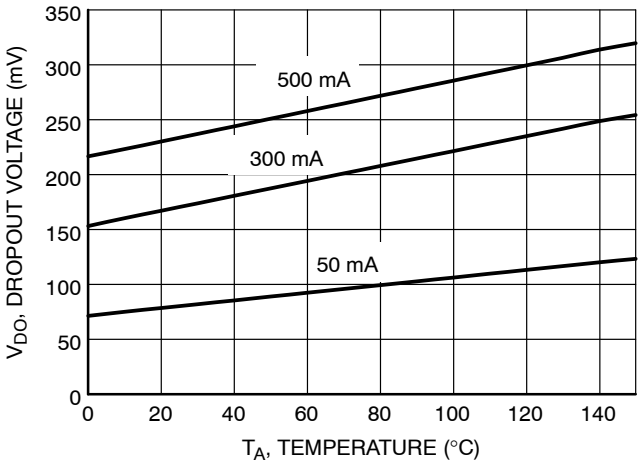



**Figure 12. Dropout Voltage vs. Temperature 5.0 V Version**

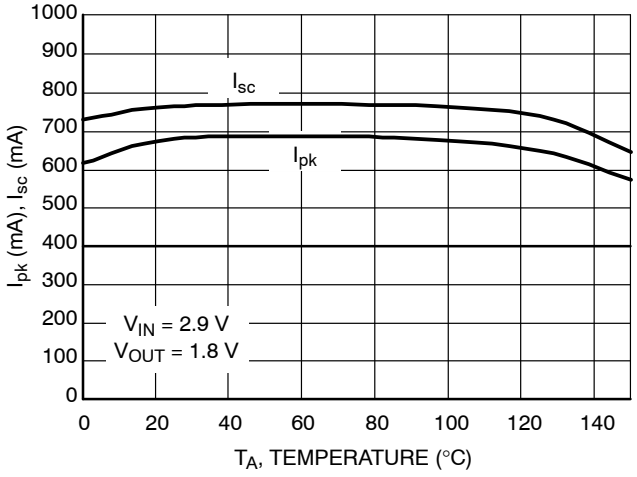
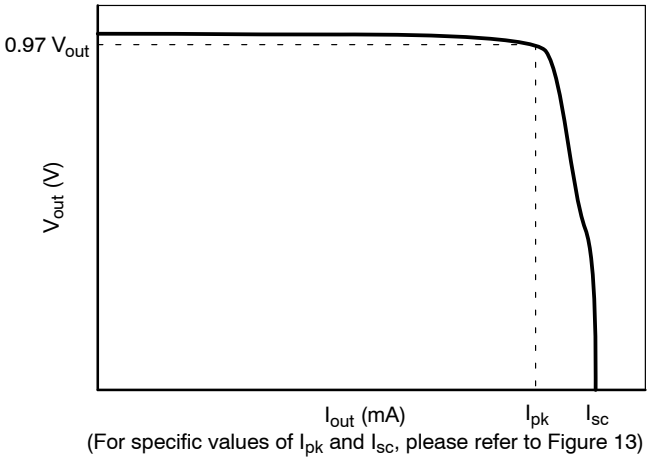



**Figure 13. Peak and Short Current vs. Temperature**




(For specific values of $I_{pk}$ and $I_{sc}$, please refer to Figure 13)

**Figure 14. Output Voltage vs. Output Current**

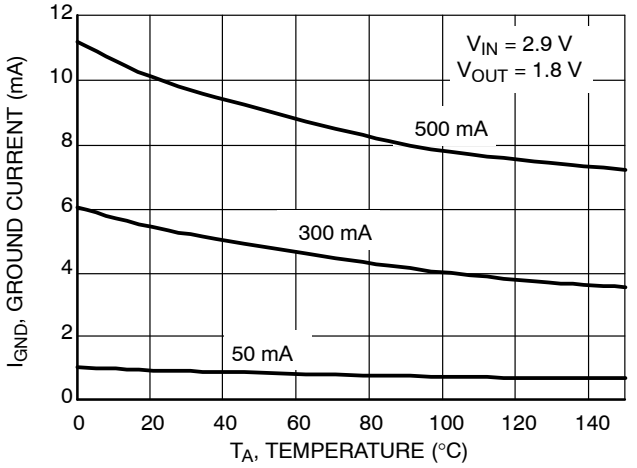



**Figure 15. Ground Current vs. Temperature**

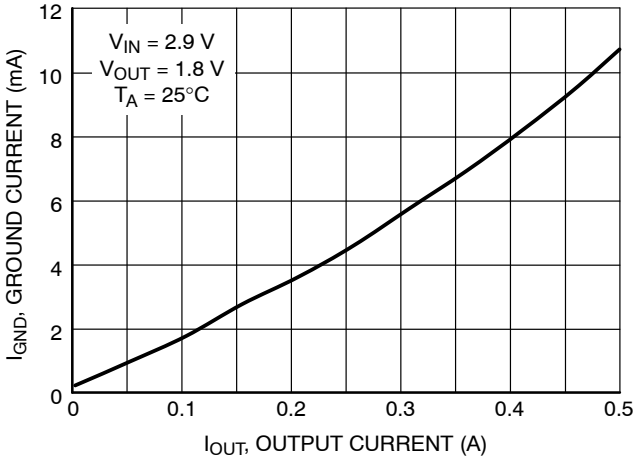



**Figure 16. Ground Current vs. Output Current**

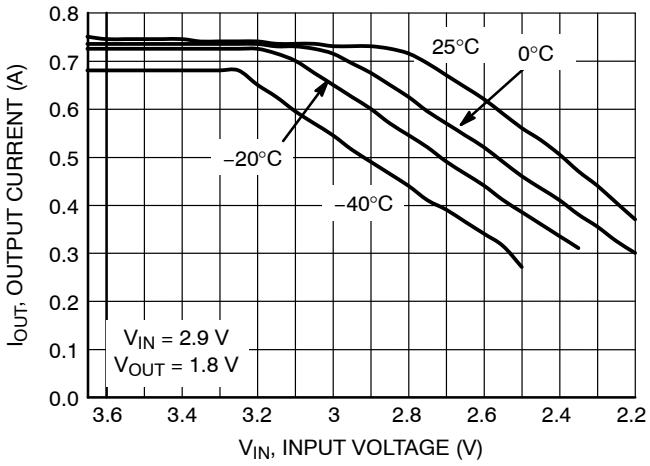



**Figure 17. Output Current Capability for the 1.8 V Version**

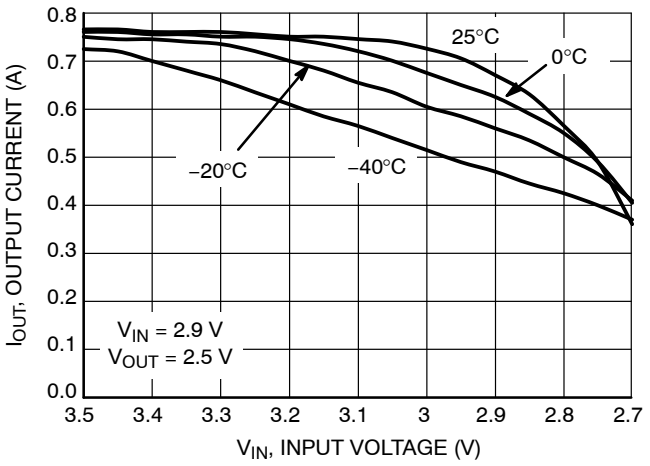



**Figure 18. Output Current Capability for the 2.5 V Version**

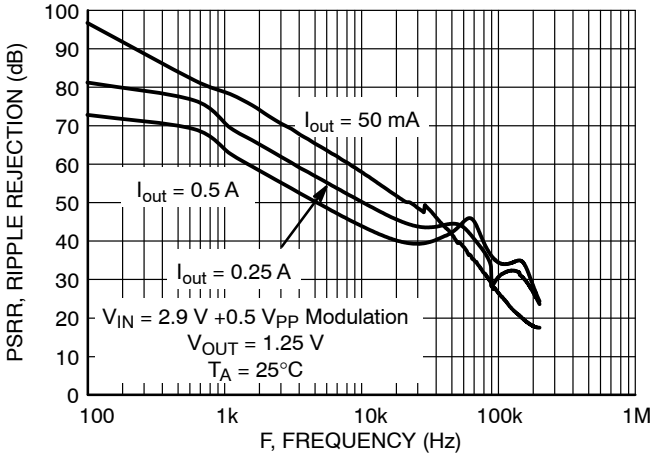



**Figure 20. PSRR vs. Frequency Adjustable Version**

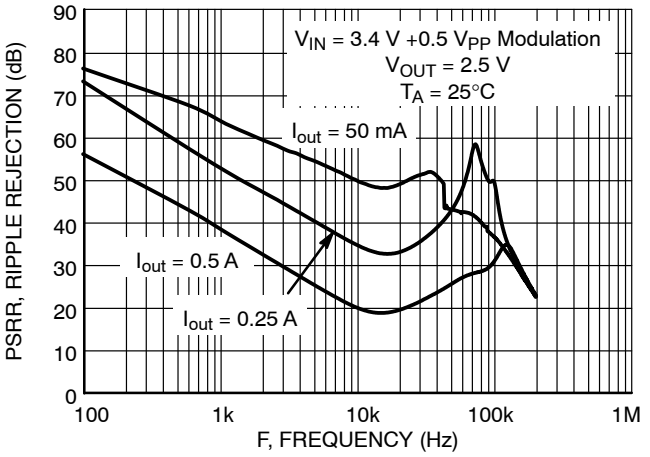



**Figure 21. PSRR vs. Frequency 2.5 V Version**

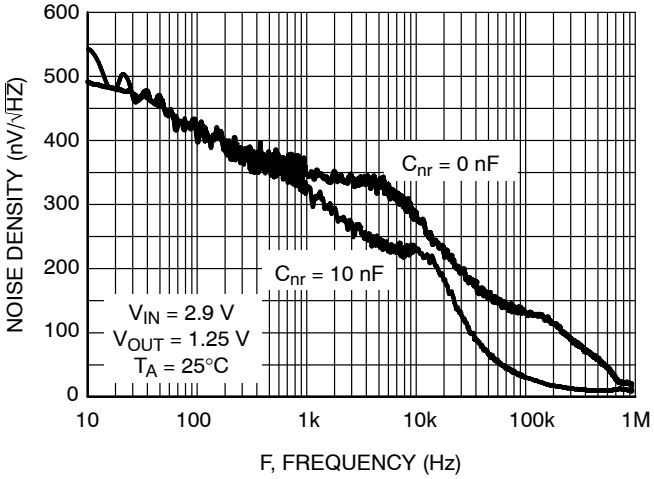



**Figure 22. Output Noise Density Adjustable Version**

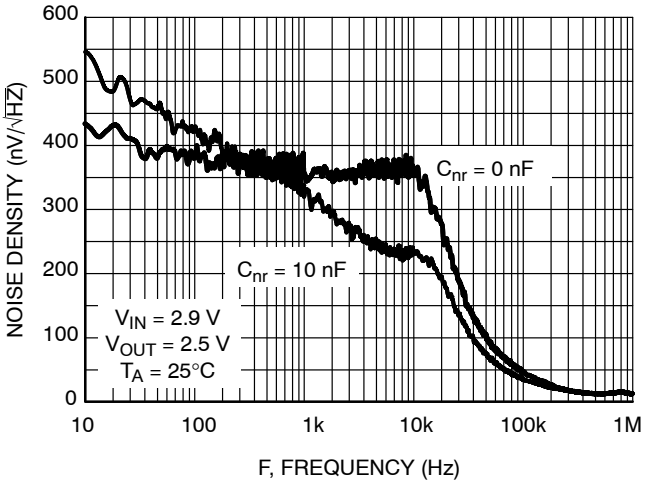



**Figure 23. Output Noise Density 2.5 V Version**

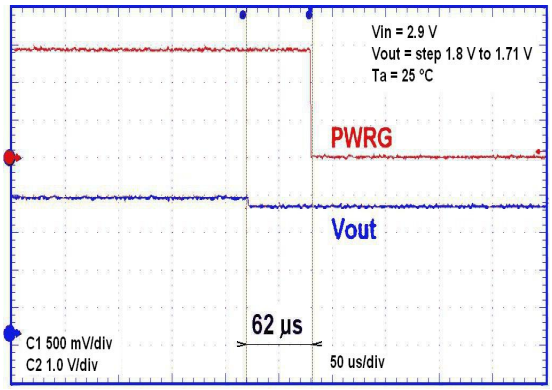



**Figure 24. Power Good Activation**

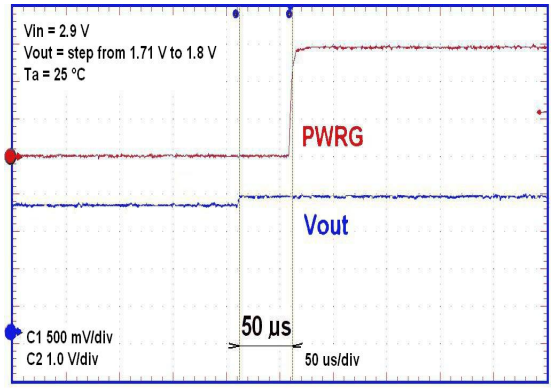



**Figure 25. Power Good Inactivation**

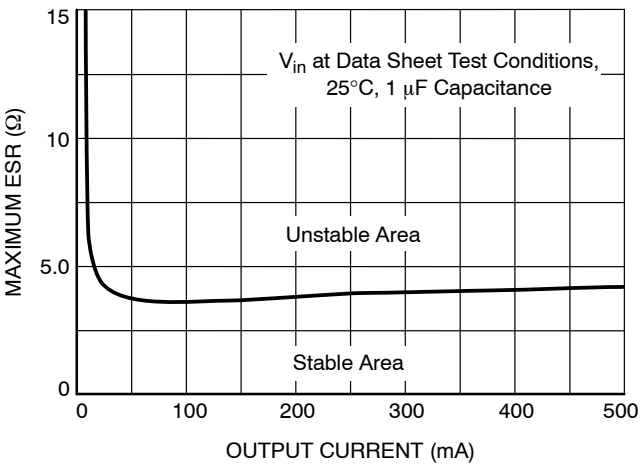



**Figure 26. Stability with ESR vs. Output Current**

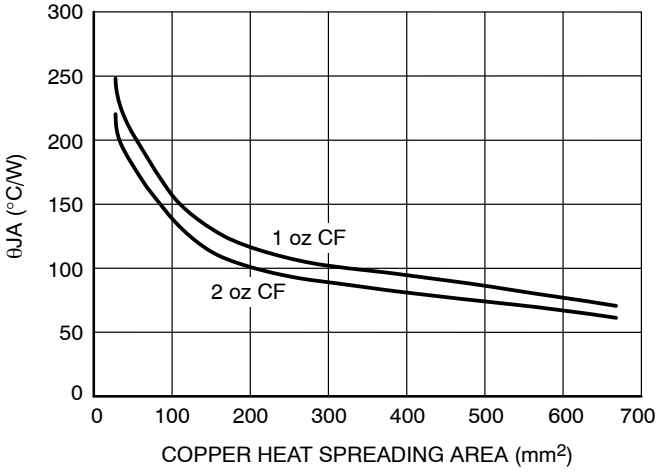



**Figure 27. DFN10 Self−Heating Thermal Characterstics as a Function of Copper Area on the PCB**

NOTE: Typical characteristics were measured with the same conditions as electrical characteristics.

## APPLICATIONS INFORMATION

### Reverse Bias Protection

Reverse bias is a condition caused when the input voltage goes to zero, but the output voltage is kept high either by a large output capacitor or another source in the application which feeds the output pin.

Normally in a bipolar LDO all the current will flow from the output pin to input pin through the PN junction with limited current capability and with the potential to destroy the IC.

Due to an improved architecture, the NCP3337 can withstand up to 7.0 V on the output pin with virtually no current flowing from output pin to input pin, and only negligible amount of current (tens of μA) flowing from the output pin to ground for infinite duration.

### Input Capacitor

An input capacitor of at least 1.0 μF, any type, is recommended to improve the transient response of the regulator and/or if the regulator is located more than a few inches from the power source. It will also reduce the circuit's sensitivity to the input line impedance at high frequencies. The capacitor should be mounted with the shortest possible track length directly across the regular's input terminals.

### Output Capacitor

The NCP3337 remains stable with any type of capacitor as long as it fulfills its 1.0 μF requirement. There are no constraints on the minimum ESR and it will remain stable up to an ESR of 5.0 Ω. Larger capacitor values will improve the noise rejection and load transient response.

### Noise Reduction Pin

Output noise can be greatly reduced by connecting a 10 nF capacitor ($C_{nr}$) between the noise reduction pin and ground (see Figure 1). In applications where very low noise is not required, the noise reduction pin can be left unconnected.

### Dropout Voltage

The voltage dropout is measured at 97% of the nominal output voltage.

### Thermal Considerations

Internal thermal limiting circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. This feature provides protection from a catastrophic device failure due to accidental overheating. This protection feature is not intended to be used as a substitute to heat sinking. The maximum power that can be dissipated, can be calculated with the equation below:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}} \quad \text{(eq. 1)}$$

For improved thermal performance, contact the factory for the DFN package option. The DFN package includes an exposed metal pad that is specifically designed to reduce the junction to air thermal resistance, $R_{\theta JA}$.

### Adjustable Operation

The output voltage can be set by using a resistor divider as shown in Figure 2 with a range of 1.25 to 10 V. The appropriate resistor divider can be found by solving the equation below. The recommended current through the resistor divider is from 10 μA to 100 μA. This can be accomplished by selecting resistors in the kΩ range. As result, the $I_{adj}$ * R2 becomes negligible in the equation and can be ignored.

$$V_{out} = 1.25 * (1 + R3/R2) + I_{adj} * R2 \quad \text{(eq. 2)}$$

### Power Good Operation

The Power Good pin on the NCP3337 will produce a logic Low when it drops below the nominal output voltage. Refer to the electrical characteristics for the threshold values at which point the Power Good goes Low. When the NCP3337 is above the nominal output voltage, the Power Good will remain at logic High.

The external pullup resistor needs to be connected between $V_{in}$ and the Power Good pin. A resistor of approximately 100 kΩ is recommended to minimize the current consumption. No pullup resistor is required if the Power Good output is not being used. The Power Good does not function during thermal shutdown and when the part is disabled.

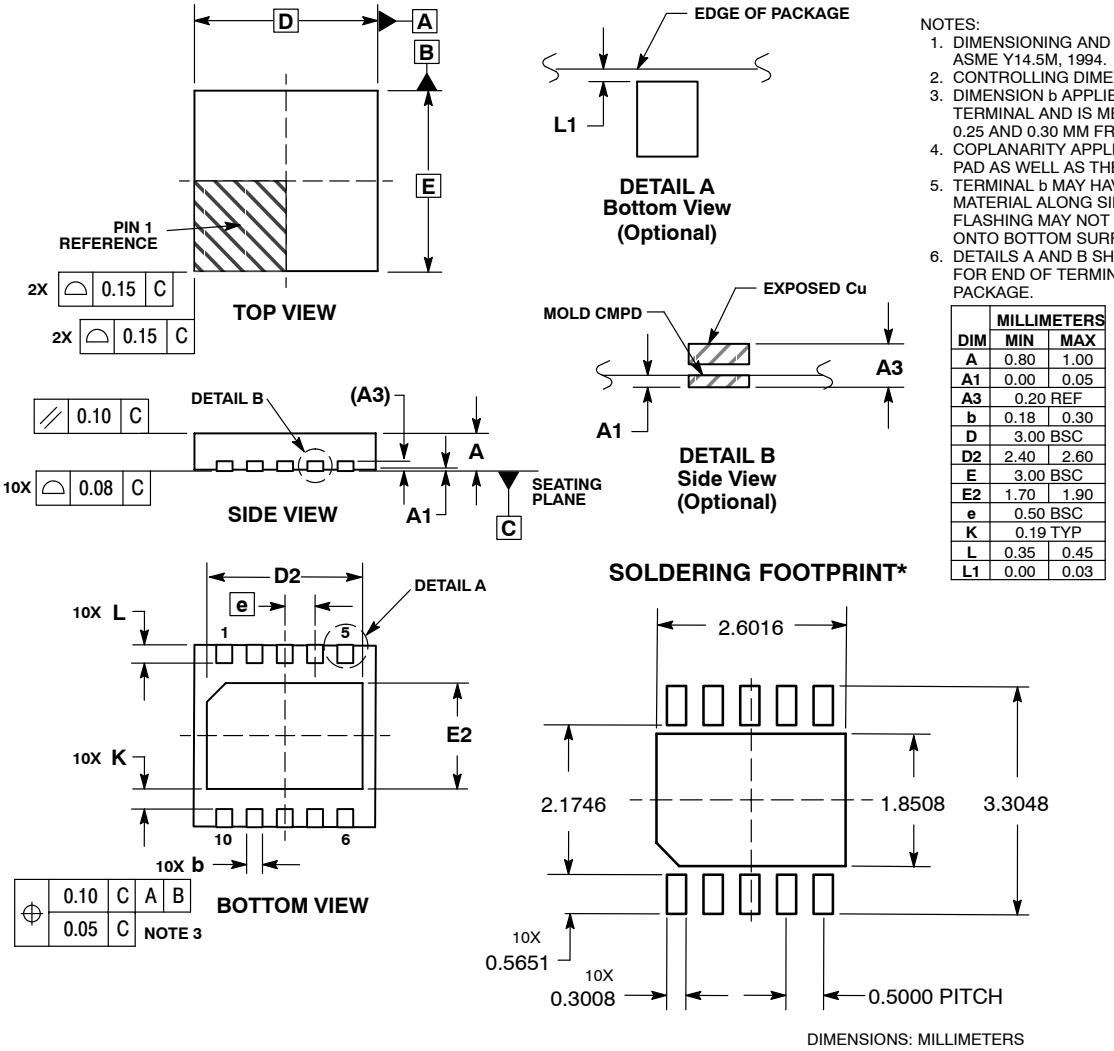
## ORDERING INFORMATION

| Device | Nominal Output Voltage | Marking | Package | Shipping† |
|---|---|---|---|---|
| NCP3337MN180R2G | 1.8 V | P3337 180 | DFN10 (Pb−Free) | 3000 / Tape & Reel |
| NCP3337MN250R2G | 2.5 V | P3337 250 | DFN10 (Pb−Free) | 3000 / Tape & Reel |
| NCP3337MN330R2G | 3.3 V | P3337 330 | DFN10 (Pb−Free) | 3000 / Tape & Reel |
| NCP3337MN500R2G | 5.0 V | P3337 500 | DFN10 (Pb−Free) | 3000 / Tape & Reel |
| NCP3337MNADJR2G | Adj | P3337 ADJ | DFN10 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Please contact factory for other voltage options.

## PACKAGE DIMENSIONS

**DFN10, 3x3, 0.5P**
CASE 485C−01
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASHING MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL b.
6. DETAILS A AND B SHOW OPTIONAL VIEWS FOR END OF TERMINAL LEAD AT EDGE OF PACKAGE.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 3.00 BSC | |
| D2 | 2.40 | 2.60 |
| E | 3.00 BSC | |
| E2 | 1.70 | 1.90 |
| e | 0.50 BSC | |
| K | 0.19 TYP | |
| L | 0.35 | 0.45 |
| L1 | 0.00 | 0.03 |

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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