SMART ARM-Based Microcontrollers

# SAM D20E / SAM D20G / SAM D20J Summary

**DATASHEET SUMMARY**

## Introduction

Atmel® | SMART™ SAM D20 is a series of low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, and ranging from 32- to 64-pins with up to 256KB Flash and 32KB of SRAM. The SAM D20 devices operate at a maximum frequency of 48MHz and reach 2.46 CoreMark®/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

## Features

- Processor
  - ARM Cortex-M0+ CPU running at up to 48MHz
    - Single-cycle hardware multiplier
- Memories
  - 16/32/64/128/256KB in-system self-programmable Flash
  - 2/4/8/16/32KB SRAM Memory
- System
  - Power-on reset (POR) and brown-out detection (BOD)
  - Internal and external clock options with 48MHz Digital Frequency Locked Loop (DFLL48M)
  - External Interrupt Controller (EIC)
  - 16 external interrupts
  - One non-maskable interrupt
  - Two-pin Serial Wire Debug (SWD) programming, test and debugging interface
- Low Power
  - Idle and standby sleep modes
  - SleepWalking peripherals
- Peripherals
  - 8-channel Event System

**This is a summary document. A complete document is available on our Web site at www.atmel.com**

  - Up to five 16-bit Timer/Counters (TC), configurable as either:
    - One 16-bit TC with two compare/capture channels
    - One 8-bit TC with two compare/capture channels
    - One 32-bit TC with two compare/capture channels, by using two TCs
  - 32-bit Real Time Counter (RTC) with clock/calendar function
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - Up to six Serial Communication Interfaces (SERCOM), each configurable to operate as either:
    - USART with full-duplex and single-wire half-duplex configuration
    - Inter-Integrated Circuit ($I^2C$) up to 400kHz
    - Serial Peripheral Interface (SPI)
  - One 12-bit, 350ksps Analog-to-Digital Converter (ADC) with up to 20 channels
    - Differential and single-ended input
    - 1/2x to 16x programmable gain stage
    - Automatic offset and gain error compensation
    - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
  - 10-bit, 350ksps Digital-to-Analog Converter (DAC)
  - Two Analog Comparators (AC) with window compare function
  - Peripheral Touch Controller (PTC)
    - 256-Channel capacitive touch and proximity sensing
- I/O
  - Up to 52 programmable I/O pins
- Packages
  - 64-pin TQFP, QFN
  - 64-ball UFBGA
  - 48-pin TQFP, QFN
  - 45-ball WLCSP
  - 32-pin TQFP, QFN
- Operating Voltage
  - 1.62V – 3.63V
- Power Consumption
  - Down to 70µA/MHz in active mode
  - Down to 8µA running the Peripheral Touch Controller

# Table of Contents


Introduction....1

Features....1

1. Description....4

2. Configuration Summary....5

3. Ordering Information....6
   - 3.1. SAM D20E....6
   - 3.2. SAM D20G....8
   - 3.3. SAM D20J....9
   - 3.4. Device Identification....11

4. Block Diagram....13

5. Pinout....14
   - 5.1. SAM D20J....14
   - 5.2. SAM D20G....16
   - 5.3. SAM D20E....18

6. Product Mapping....19

7. Processor And Architecture....20
   - 7.1. Cortex M0+ Processor....20
   - 7.2. Nested Vector Interrupt Controller....21
   - 7.3. Micro Trace Buffer....23
   - 7.4. High-Speed Bus System....24
   - 7.5. AHB-APB Bridge....24
   - 7.6. PAC - Peripheral Access Controller....25
   - 7.7. Register Description....26

8. Packaging Information....39
   - 8.1. Thermal Considerations....39
   - 8.2. Package Drawings....40
   - 8.3. Soldering Profile....50

# 1. Description

The Atmel® | SMART™ SAM D20 is a series of low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, and ranging from 32- to 64-pins with up to 256KB Flash and 32KB of SRAM. The SAM D20 devices operate at a maximum frequency of 48MHz and reach 2.46 CoreMark/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The SAM D20 devices provide the following features: In-system programmable Flash, eight-channel Event System, programmable interrupt controller, up to 52 programmable I/O pins, 32-bit real-time clock and calendar, up to eight 16-bit Timer/Counters (TC) . The timer/counters can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC. The series provide up to six Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, $I^2C$ up to 400kHz, up to twenty-channel 350ksps 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, one 10-bit 350ksps DAC, two analog comparators with window mode, Peripheral Touch Controller supporting up to 256 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM D20 devices have two software-selectable sleep modes, idle and standby. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped expect those selected to continue running. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

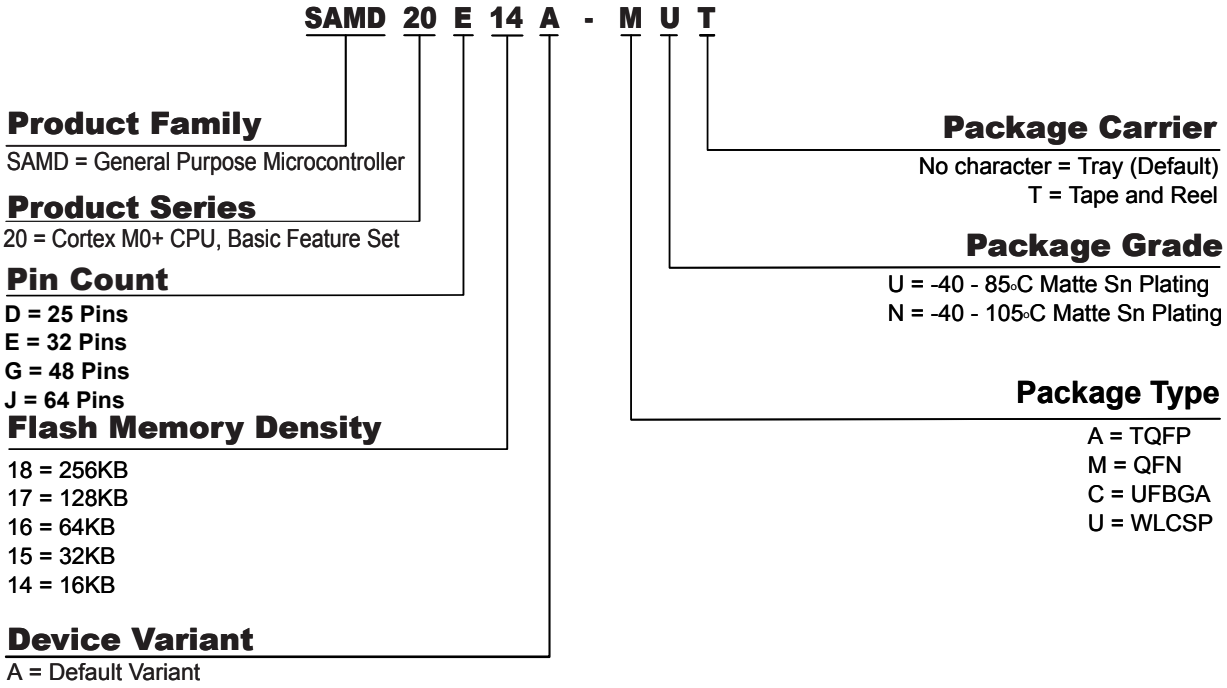
The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip debug of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The SAM D20 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

## 2. Configuration Summary

| | SAM D20J | SAM D20G | SAM D20E |
|---|---|---|---|
| Pins | 64 | 48 | 32 |
| General Purpose I/O-pins (GPIOs) | 52 | 38 | 26 |
| Flash | 256/128/64/32KB | 256/128/64/32KB | 256/128/64/32KB |
| SRAM | 32/16/8/4/2KB | 32/16/8/4/2KB | 32/16/8/4/2KB |
| Timer Counter (TC) instances | 8 | 6 | 6 |
| Waveform output channels per TC instance | 2 | 2 | 2 |
| Serial Communication Interface (SERCOM) instances | 6 | 6 | 4 |
| Analog-to-Digital Converter (ADC) channels | 20 | 14 | 10 |
| Analog Comparators (AC) | 2 | 2 | 2 |
| Digital-to-Analog Converter (DAC) channels | 1 | 1 | 1 |
| Real-Time Counter (RTC) | Yes | Yes | Yes |
| RTC alarms | 1 | 1 | 1 |
| RTC compare values | One 32-bit value or two 16-bit values | One 32-bit value or two 16-bit values | One 32-bit value or two 16-bit values |
| External Interrupt lines | 16 | 16 | 16 |
| Peripheral Touch Controller (PTC) X and Y lines | 16x16 | 12x10 | 10x6 |
| Maximum CPU frequency | 48MHz | | |
| Packages | QFN<br>TQFP<br>UFBGA | QFN<br>TQFP<br>WLCSP | QFN<br>TQFP |
| Oscillators | 32.768kHz crystal oscillator (XOSC32K)<br>0.4-32MHz crystal oscillator (XOSC)<br>32.768kHz internal oscillator (OSC32K)<br>32KHz ultra-low-power internal oscillator (OSCULP32K)<br>8MHz high-accuracy internal oscillator (OSC8M)<br>48MHz Digital Frequency Locked Loop (DFLL48M) | | |
| Event System channels | 8 | 8 | 8 |
| SW Debug Interface | Yes | Yes | Yes |
| Watchdog Timer (WDT) | Yes | Yes | Yes |

# 3. Ordering Information




## 3.1. SAM D20E

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|---|---|---|---|---|
| ATSAMD20E14A-AU | 16K | 2K | TQFP32 | Tray |
| ATSAMD20E14A-AUT | | | | Tape & Reel |
| ATSAMD20E14A-AN | | | | Tray |
| ATSAMD20E14A-ANT | | | | Tape & Reel |
| ATSAMD20E14A-MU | | | QFN32 | Tray |
| ATSAMD20E14A-MUT | | | | Tape & Reel |
| ATSAMD20E14A-MN | | | | Tray |
| ATSAMD20E14A-MNT | | | | Tape & Reel |

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|---|---|---|---|---|
| ATSAMD20E15A-AU | 32K | 4K | TQFP32 | Tray |
| ATSAMD20E15A-AUT | | | | Tape & Reel |
| ATSAMD20E15A-AN | | | | Tray |
| ATSAMD20E15A-ANT | | | | Tape & Reel |
| ATSAMD20E15A-MU | | | QFN32 | Tray |
| ATSAMD20E15A-MUT | | | | Tape & Reel |
| ATSAMD20E15A-MN | | | | Tray |
| ATSAMD20E15A-MNT | | | | Tape & Reel |
| ATSAMD20E16A-AU | 64K | 8K | TQFP32 | Tray |
| ATSAMD20E16A-AUT | | | | Tape & Reel |
| ATSAMD20E16A-AN | | | | Tray |
| ATSAMD20E16A-AFT | | | | Tape & Reel |
| ATSAMD20E16A-MU | | | QFN32 | Tray |
| ATSAMD20E16A-MUT | | | | Tape & Reel |
| ATSAMD20E16A-MN | | | | Tray |
| ATSAMD20E16A-MNT | | | | Tape & Reel |
| ATSAMD20E17A-AU | 128K | 16K | TQFP32 | Tray |
| ATSAMD20E17A-AUT | | | | Tape & Reel |
| ATSAMD20E17A-AN | | | | Tray |
| ATSAMD20E17A-ANT | | | | Tape & Reel |
| ATSAMD20E17A-MU | | | QFN32 | Tray |
| ATSAMD20E17A-MUT | | | | Tape & Reel |
| ATSAMD20E17A-MN | | | | Tray |
| ATSAMD20E17A-MNT | | | | Tape & Reel |
| ATSAMD20E18A-AU | 256K | 32K | TQFP32 | Tray |
| ATSAMD20E18A-AUT | | | | Tape & Reel |
| ATSAMD20E18A-AN | | | | Tray |
| ATSAMD20E18A-AFT | | | | Tape & Reel |
| ATSAMD20E18A-MU | | | QFN32 | Tray |
| ATSAMD20E18A-MUT | | | | Tape & Reel |
| ATSAMD20E18A-MN | | | | Tray |
| ATSAMD20E18A-MNT | | | | Tape & Reel |

## 3.2. SAM D20G

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|---|---|---|---|---|
| ATSAMD20G14A-AU | 16K | 2K | TQFP32 | Tray |
| ATSAMD20G14A-AUT | | | | Tape & Reel |
| ATSAMD20G14A-AN | | | | Tray |
| ATSAMD20G14A-ANT | | | | Tape & Reel |
| ATSAMD20G14A-MU | | | QFN32 | Tray |
| ATSAMD20G14A-MUT | | | | Tape & Reel |
| ATSAMD20G14A-MN | | | | Tray |
| ATSAMD20G14A-MNT | | | | Tape & Reel |
| ATSAMD20G15A-AU | 32K | 4K | TQFP48 | Tray |
| ATSAMD20G15A-AUT | | | | Tape & Reel |
| ATSAMD20G15A-AN | | | | Tray |
| ATSAMD20G15A-ANT | | | | Tape & Reel |
| ATSAMD20G15A-MU | | | QFN48 | Tray |
| ATSAMD20G15A-MUT | | | | Tape & Reel |
| ATSAMD20G15A-MN | | | | Tray |
| ATSAMD20G15A-MNT | | | | Tape & Reel |
| ATSAMD20G16A-AU | 64K | 8K | TQFP48 | Tray |
| ATSAMD20G16A-AUT | | | | Tape & Reel |
| ATSAMD20G16A-AN | | | | Tray |
| ATSAMD20G16A-ANT | | | | Tape & Reel |
| ATSAMD20G16A-MU | | | QFN48 | Tray |
| ATSAMD20G16A-MUT | | | | Tape & Reel |
| ATSAMD20G16A-MN | | | | Tray |
| ATSAMD20G16A-MNT | | | | Tape & Reel |

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|---|---|---|---|---|
| ATSAMD20G17A-AU | 128K | 16K | TQFP48 | Tray |
| ATSAMD20G17A-AUT | | | | Tape & Reel |
| ATSAMD20G17A-AN | | | | Tray |
| ATSAMD20G17A-ANT | | | | Tape & Reel |
| ATSAMD20G17A-MU | | | QFN48 | Tray |
| ATSAMD20G17A-MUT | | | | Tape & Reel |
| ATSAMD20G17A-MN | | | | Tray |
| ATSAMD20G17A-MNT | | | | Tape & Reel |
| ATSAMD20G17A-UUT | | | WLCSP45 | Tape & Reel |
| ATSAMD20G18A-AU | 256K | 32K | TQFP48 | Tray |
| ATSAMD20G18A-AUT | | | | Tape & Reel |
| ATSAMD20G18A-AN | | | | Tray |
| ATSAMD20G18A-ANT | | | | Tape & Reel |
| ATSAMD20G18A-MU | | | QFN48 | Tray |
| ATSAMD20G18A-MUT | | | | Tape & Reel |
| ATSAMD20G18A-MN | | | | Tray |
| ATSAMD20G18A-MNT | | | | Tape & Reel |
| ATSAMD20G18A-UUT | | | WLCSP45 | Tape & Reel |

## 3.3. SAM D20J

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|---|---|---|---|---|
| ATSAMD20J14A-AU | 16K | 2K | TQFP64 | Tray |
| ATSAMD20J14A-AUT | | | | Tape & Reel |
| ATSAMD20J14A-AN | | | | Tray |
| ATSAMD20J14A-ANT | | | | Tape & Reel |
| ATSAMD20J14A-MU | | | QFN64 | Tray |
| ATSAMD20J14A-MUT | | | | Tape & Reel |
| ATSAMD20J14A-MN | | | | Tray |
| ATSAMD20J14A-MNT | | | | Tape & Reel |

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|---|---|---|---|---|
| ATSAMD20J15A-AU | 32K | 4K | TQFP64 | Tray |
| ATSAMD20J15A-AUT | | | | Tape & Reel |
| ATSAMD20J15A-AN | | | | Tray |
| ATSAMD20J15A-ANT | | | | Tape & Reel |
| ATSAMD20J15A-MU | | | QFN64 | Tray |
| ATSAMD20J15A-MUT | | | | Tape & Reel |
| ATSAMD20J15A-MN | | | | Tray |
| ATSAMD20J15A-MNT | | | | Tape & Reel |
| ATSAMD20J16A-AU | 64K | 8K | TQFP64 | Tray |
| ATSAMD20J16A-AUT | | | | Tape & Reel |
| ATSAMD20J16A-AN | | | | Tray |
| ATSAMD20J16A-ANT | | | | Tape & Reel |
| ATSAMD20J16A-MU | | | QFN64 | Tray |
| ATSAMD20J16A-MUT | | | | Tape & Reel |
| ATSAMD20J16A-MN | | | | Tray |
| ATSAMD20J16A-MNT | | | | Tape & Reel |
| ATSAMD20J16A-CU | | | UFBGA64 | Tray |
| ATSAMD20J16A-CUT | | | | Tape & Reel |
| ATSAMD20J17A-AU | 128K | 16K | TQFP64 | Tray |
| ATSAMD20J17A-AUT | | | | Tape & Reel |
| ATSAMD20J17A-AN | | | | Tray |
| ATSAMD20J17A-ANT | | | | Tape & Reel |
| ATSAMD20J17A-MU | | | QFN64 | Tray |
| ATSAMD20J17A-MUT | | | | Tape & Reel |
| ATSAMD20J17A-MN | | | | Tray |
| ATSAMD20J17A-MNT | | | | Tape & Reel |
| ATSAMD20J17A-CU | | | UFBGA64 | Tray |
| ATSAMD20J17A-CUT | | | | Tape & Reel |

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|---|---|---|---|---|
| ATSAMD20J18A-AU | 256K | 32K | TQFP64 | Tray |
| ATSAMD20J18A-AUT | | | | Tape & Reel |
| ATSAMD20J18A-AN | | | | Tray |
| ATSAMD20J18A-ANT | | | | Tape & Reel |
| ATSAMD20J18A-MU | | | QFN64 | Tray |
| ATSAMD20J18A-MUT | | | | Tape & Reel |
| ATSAMD20J18A-MN | | | | Tray |
| ATSAMD20J18A-MNT | | | | Tape & Reel |
| ATSAMD20J18A-CU | | | UFBGA64 | Tray |
| ATSAMD20J18A-CUT | | | | Tape & Reel |

## 3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The device variants have a reset value of DID=0x1001drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

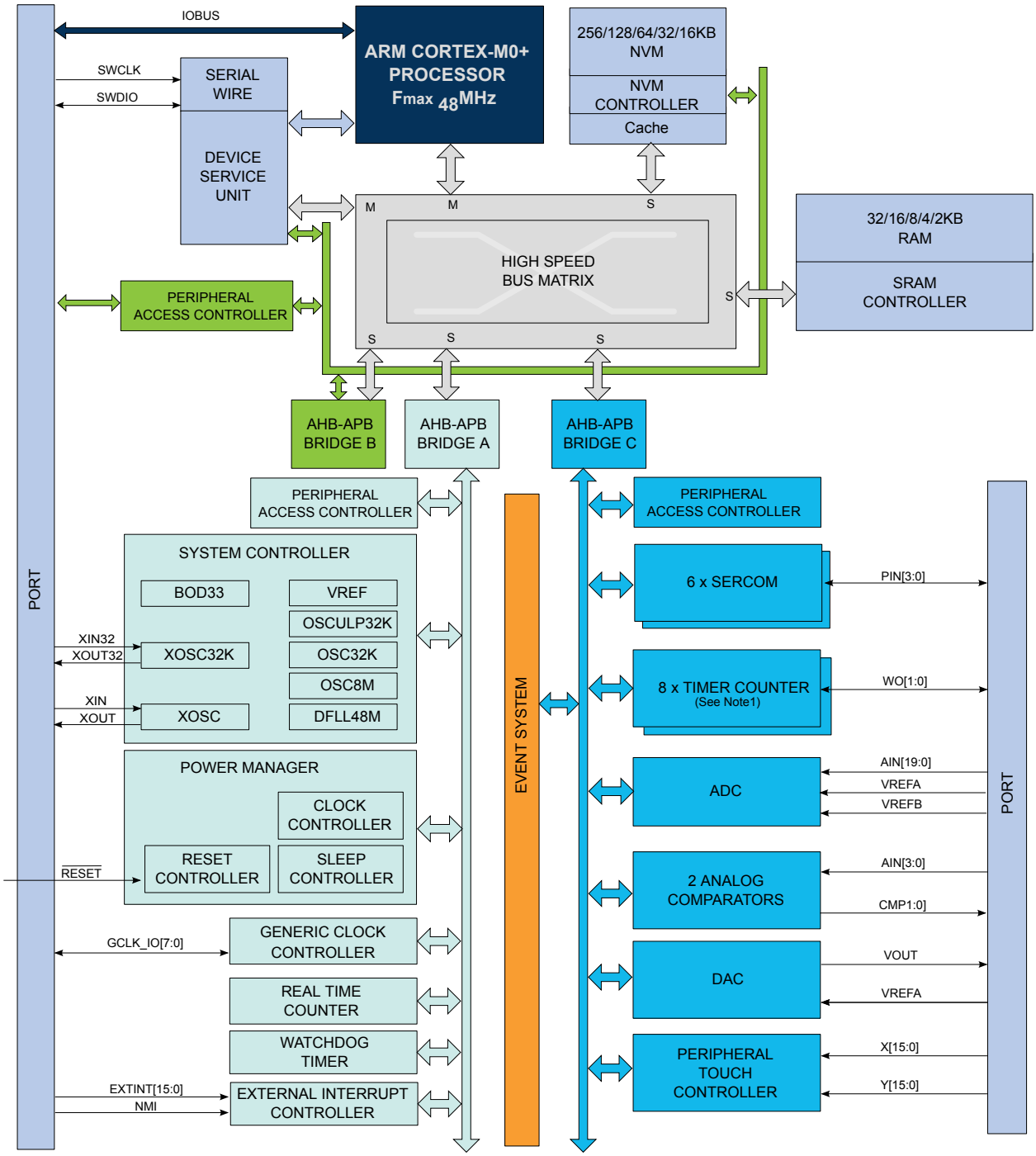
**Table 3-1. Device Identification Values**

| Device Variant | DID.DEVSEL | Device ID (DID) |
|---|---|---|
| SAMD20J18C | 0x00 | 0x10001300 |
| SAMD20J18A | 0x00 | 0x10001300 |
| SAMD20J17A | 0x01 | 0x10001301 |
| SAMD20J16A | 0x02 | 0x10001302 |
| SAMD20J15A | 0x03 | 0x10001303 |
| SAMD20J14A | 0x04 | 0x10001304 |
| SAMD20G18A | 0x05 | 0x10001305 |
| SAMD20G17A | 0x06 | 0x10001306 |
| SAMD20G16A | 0x07 | 0x10001307 |
| SAMD20G15A | 0x08 | 0x10001308 |
| SAMD20G14A | 0x09 | 0x10001309 |
| SAMD20E18A | 0x0A | 0x1000130A |
| SAMD20E17A | 0x0B | 0x1000130B |
| SAMD20E16A | 0x0C | 0x1000130C |
| SAMD20E15A | 0x0D | 0x1000130D |

| Device Variant | DID.DEVSEL | Device ID (DID) |
|---|---|---|
| SAMD20E14A | 0x0E | 0x1000130E |
| Reserved | 0x0F | |
| SAMD20G18U | 0x10 | 0x10001310 |
| SAMD20G17U | 0x11 | 0x10001311 |
| Reserved | 0x12 - 0xFF | |

**Note:** The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die. The device variant denotes functional differences, whereas the die revision marks evolution of the die.

# 4. Block Diagram

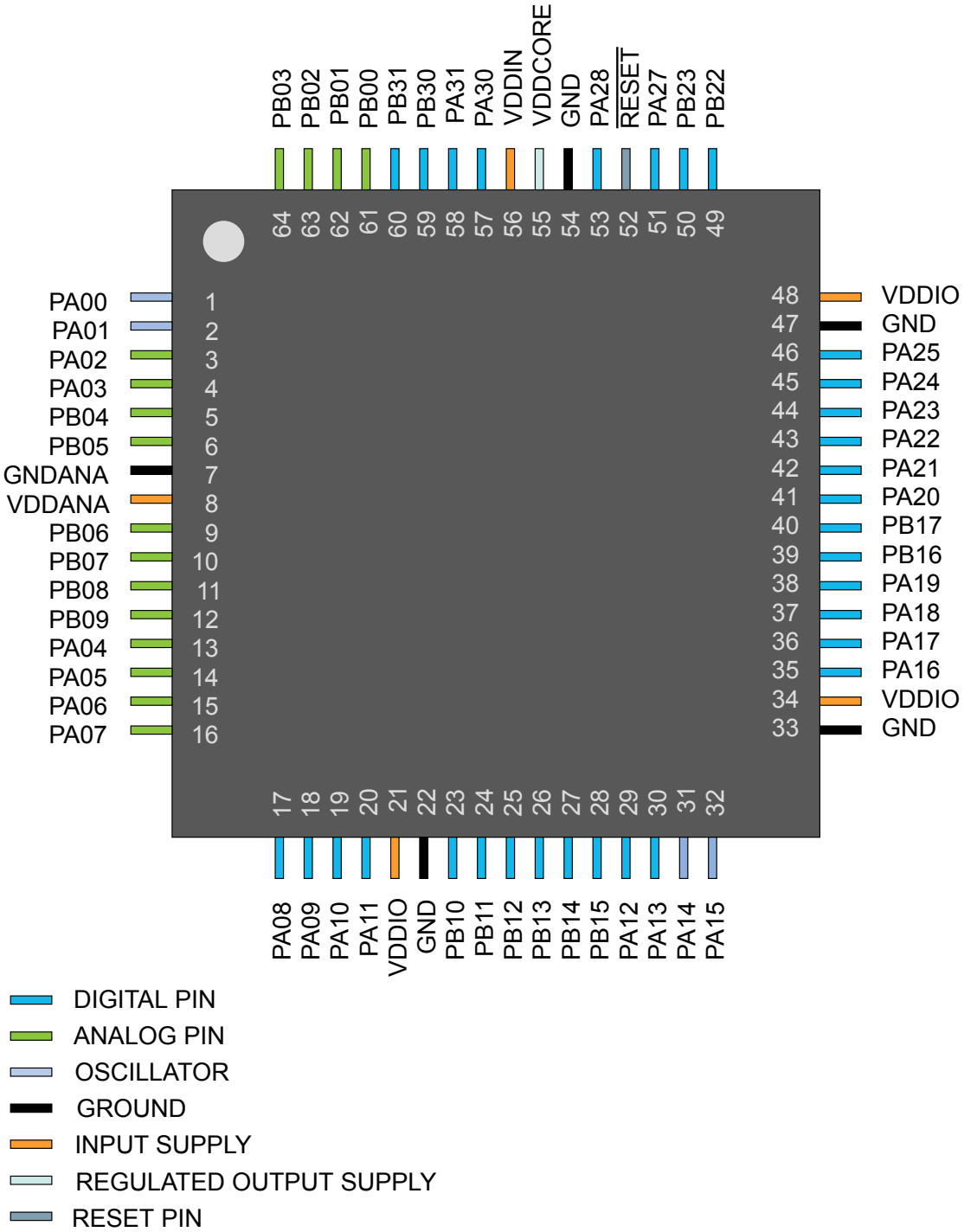



**Note:** 1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals. Refer to *Peripherals Configuration Summary* for details.

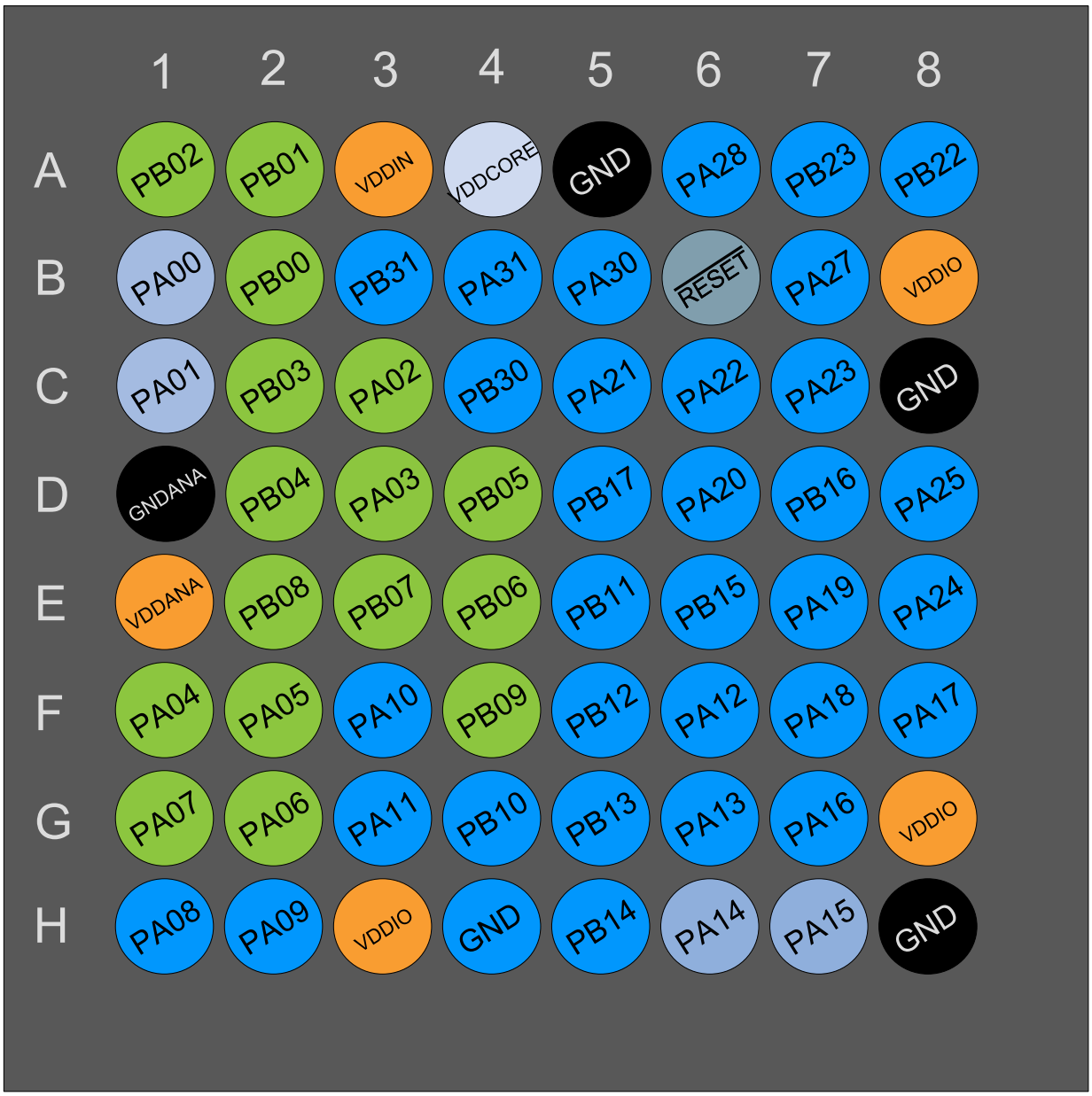
# 5. Pinout

## 5.1. SAM D20J

### 5.1.1. QFN64 / TQFP64



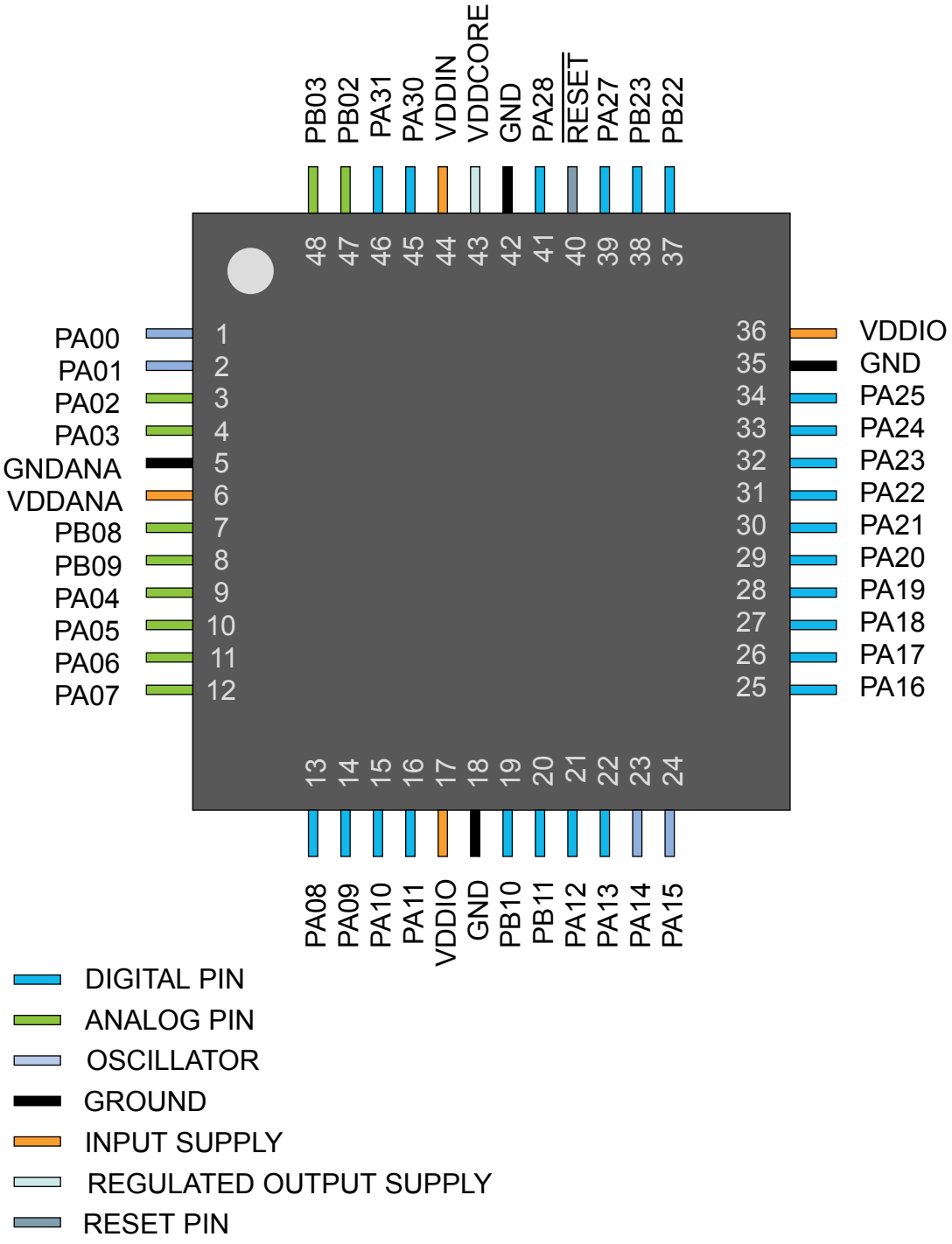
### 5.1.2. UFBGA64



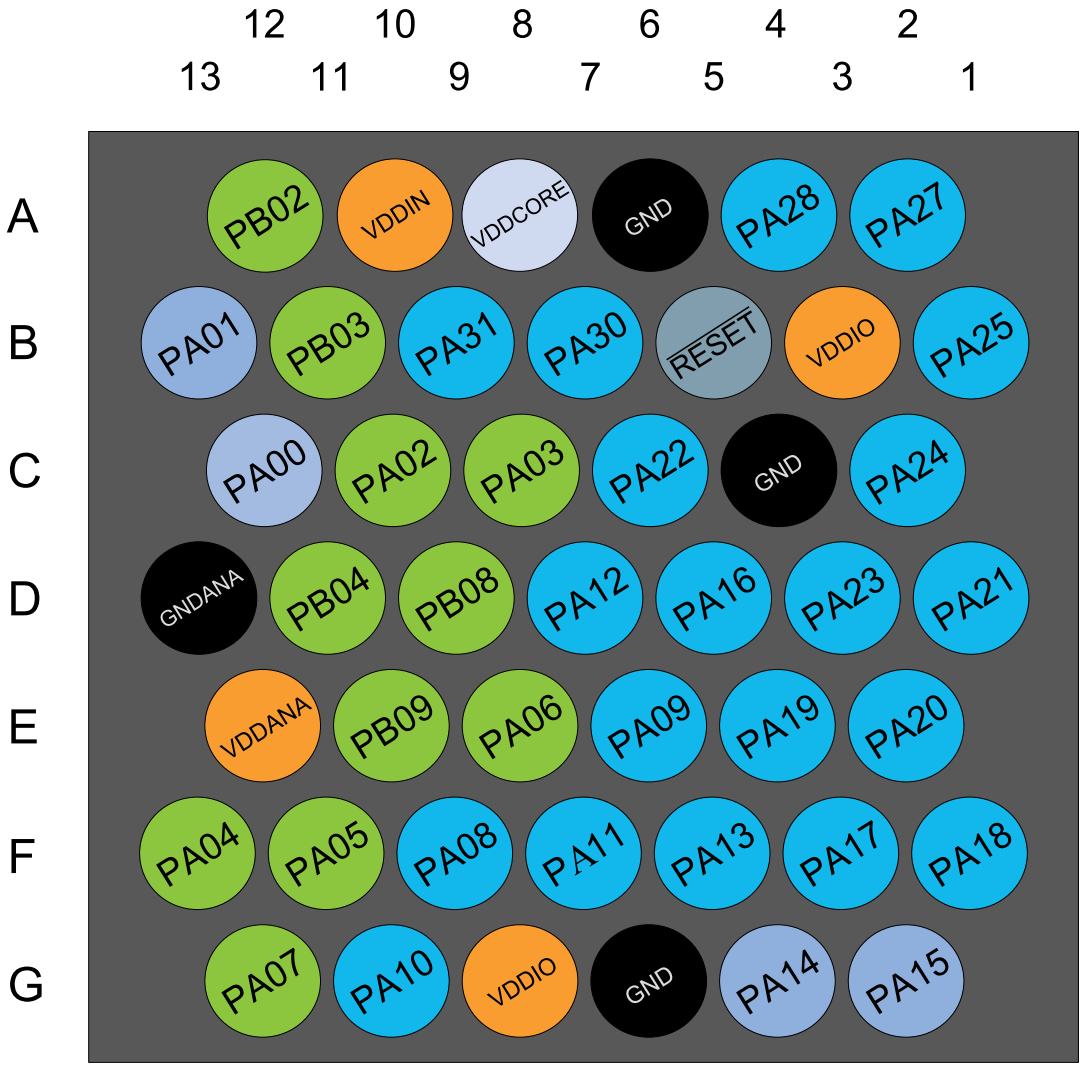

- DIGITAL PIN
- ANALOG PIN
- OSCILLATOR
- GROUND
- INPUT SUPPLY
- REGULATED OUTPUT SUPPLY
- RESET PIN

## 5.2. SAM D20G

### 5.2.1. QFN48 / TQFP48

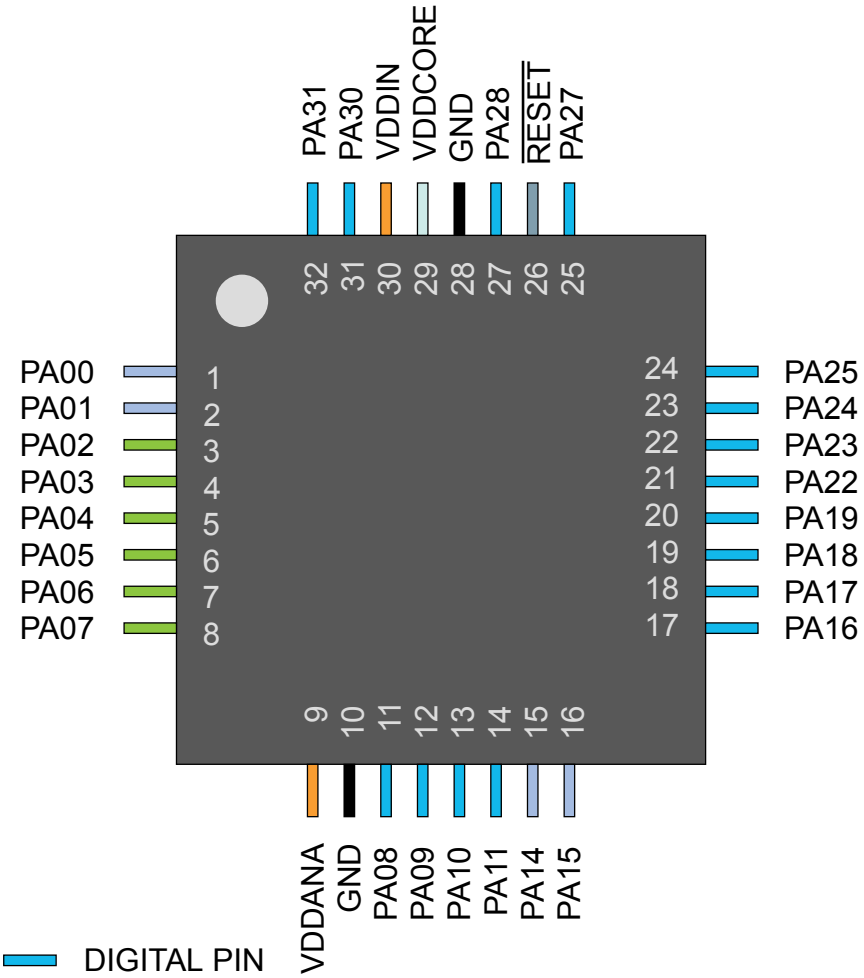


### 5.2.2. WLCSP45


12 10 8 6 4 2
13 11 9 7 5 3 1
A
B
C
D
E
F
G
PB02 VDDIN VDDCORE GND PA28 PA27
PA01 PB03 PA31 PA30 RESET VDDIO PA25
PA00 PA02 PA03 PA22 GND PA24
GNDANA PB04 PB08 PA12 PA16 PA23 PA21
VDDANA PB09 PA06 PA09 PA19 PA20
PA04 PA05 PA08 PA11 PA13 PA17 PA18
PA07 PA10 VDDIO GND PA14 PA15
DIGITAL PIN
ANALOG PIN
OSCILLATOR
GROUND
INPUT SUPPLY
REGULATED OUTPUT SUPPLY
RESET PIN

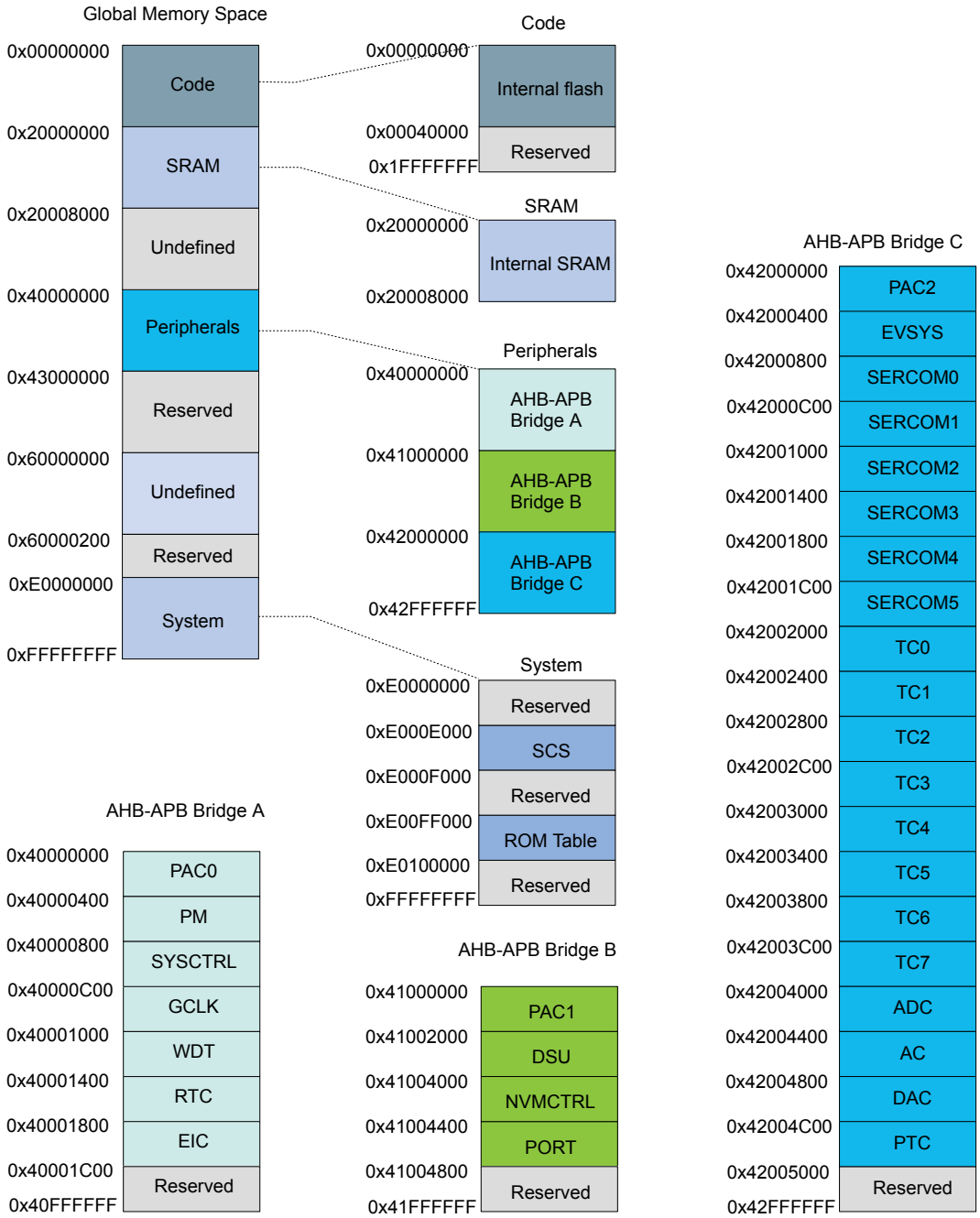
## 5.3. SAM D20E

### 5.3.1. QFN32 / TQFP32



# 6. Product Mapping

**Figure 6-1. Product Mapping**




This figure represents the full configuration of the SAM D20 device with maximum flash and SRAM capabilities and a full set of peripherals. Refer to the Configuration Summary for details.

# 7. Processor And Architecture

## 7.1. Cortex M0+ Processor

The SAM D20 implements the ARM® Cortex®-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The ARM Cortex-M0+ implemented is revision r0p1. For more information refer to http://www.arm.com.

### 7.1.1. Cortex M0+ Configuration

**Table 7-1. Cortex M0+ Configuration**

| Features | Configurable option | Device configuration |
|---|---|---|
| Interrupts | External interrupts 0-32 | 28 |
| Data endianness | Little-endian or big-endian | Little-endian |
| SysTick timer | Present or absent | Present |
| Number of watchpoint comparators | 0, 1, 2 | 2 |
| Number of breakpoint comparators | 0, 1, 2, 3, 4 | 4 |
| Halting debug support | Present or absent | Present |
| Multiplier | Fast or small | Fast (single cycle) |
| Single-cycle I/O port | Present or absent | Present |
| Wake-up interrupt controller | Supported or not supported | Not supported |
| Vector Table Offset Register | Present or absent | Present |
| Unprivileged/Privileged support | Present or absent | Absent(1) |
| Memory Protection Unit | Not present or 8-region | Not present |
| Reset all registers | Present or absent | Absent |
| Instruction fetch width | 16-bit only or mostly 32-bit | 32-bit |

**Note:**

1. All software run in privileged mode only.

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory, which includes flash and RAM.
- Single 32-bit I/O port bus interfacing to the PORT with 1-cycle loads and stores.

### 7.1.2. Cortex-M0+ Peripherals

- System Control Space (SCS)
  - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- System Timer (SysTick)

  - The System Timer is a 24-bit timer that extends the functionality of both the processor and the NVIC. Refer to the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- Nested Vectored Interrupt Controller (NVIC)
  - External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts. Refer to Nested Vector Interrupt Controller and the Cortex-M0+ Technical Reference Manual for details (www.arm.com).
- System Control Block (SCB)
  - The System Control Block provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions. Refer to the Cortex-M0+ Devices Generic User Guide for details (www.arm.com).
- Micro Trace Buffer (MTB)
  - The CoreSight MTB-M0+ (MTB) provides a simple execution trace capability to the Cortex-M0+ processor. Refer to section Micro Trace Buffer and the CoreSight MTB-M0+ Technical Reference Manual for details (www.arm.com).

### 7.1.3. Cortex-M0+ Address Map

**Table 7-2. Cortex-M0+ Address Map**

| Address | Peripheral |
|---|---|
| 0xE000E000 | System Control Space (SCS) |
| 0xE000E010 | System Timer (SysTick) |
| 0xE000E100 | Nested Vectored Interrupt Controller (NVIC) |
| 0xE000ED00 | System Control Block (SCB) |
| 0x41006000 (see also Product Mapping) | Micro Trace Buffer (MTB) |

### 7.1.4. I/O Interface

#### 7.1.4.1. Overview

Because accesses to the AMBA® AHB-Lite™ and the single cycle I/O interface can be made concurrently, the Cortex-M0+ processor can fetch the next instructions while accessing the I/Os. This enables single cycle I/O accesses to be sustained for as long as needed. Refer to *CPU Local Bus* for more information.

#### 7.1.4.2. Description

Direct access to PORT registers.

## 7.2. Nested Vector Interrupt Controller

### 7.2.1. Overview

The Nested Vectored Interrupt Controller (NVIC) in the SAM D20 supports 32 interrupt lines with four different priority levels. For more details, refer to the Cortex-M0+ Technical Reference Manual (www.arm.com).

### 7.2.2. Interrupt Line Mapping

Each of the 28 interrupt lines is connected to one peripheral instance, as shown in the table below. Each peripheral can have one or more interrupt flags, located in the peripheral's Interrupt Flag Status and Clear

(INTFLAG) register. The interrupt flag is set when the interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Set (INTENSET) register, and disabled by writing a one to the corresponding bit in the peripheral's Interrupt Enable Clear (INTENCLR) register. An interrupt request is generated from the peripheral when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt requests for one peripheral are ORed together on system level, generating one interrupt request for each peripheral. An interrupt request will set the corresponding interrupt pending bit in the NVIC interrupt pending registers (SETPEND/CLRPEND bits in ISPR/ICPR). For the NVIC to activate the interrupt, it must be enabled in the NVIC interrupt enable register (SETENA/CLRENA bits in ISER/ICER). The NVIC interrupt priority registers IPR0-IPR7 provide a priority field for each interrupt.

**Table 7-3. Interrupt Line Mapping**

| Peripheral Source | NVIC Line |
|---|---|
| EIC NMI – External Interrupt Controller | NMI |
| PM – Power Manager | 0 |
| SYSCTRL – System Control | 1 |
| WDT – Watchdog Timer | 2 |
| RTC – Real Time Counter | 3 |
| EIC – External Interrupt Controller | 4 |
| NVMCTRL – Non-Volatile Memory Controller | 5 |
| EVSYS – Event System | 6 |
| SERCOM0 – Serial Communication Interface 0 | 7 |
| SERCOM1 – Serial Communication Interface 1 | 8 |
| SERCOM2 – Serial Communication Interface 2 | 9 |
| SERCOM3 – Serial Communication Interface 3 | 10 |
| SERCOM4 – Serial Communication Interface 4 | 11 |
| SERCOM5 – Serial Communication Interface 5 | 12 |
| TC0 – Timer Counter 0 | 13 |
| TC1 – Timer Counter 1 | 14 |
| TC2 – Timer Counter 2 | 15 |
| TC3 – Timer Counter 3 | 16 |
| TC4 – Timer Counter 4 | 17 |
| TC5 – Timer Counter 5 | 18 |
| TC6 – Timer Counter 6 | 19 |
| TC7 – Timer Counter 7 | 20 |
| ADC – Analog-to-Digital Converter | 21 |
| AC – Analog Comparator | 22 |

| Peripheral Source | NVIC Line |
|---|---|
| DAC – Digital-to-Analog Converter | 23 |
| PTC – Peripheral Touch Controller | 24 |

## 7.3. Micro Trace Buffer

### 7.3.1. Features

- Program flow tracing for the Cortex-M0+ processor
- MTB SRAM can be used for both trace and general purpose storage by the processor
- The position and size of the trace buffer in SRAM is configurable by software
- CoreSight compliant

### 7.3.2. Overview

When enabled, the MTB records changes in program flow, reported by the Cortex-M0+ processor over the execution trace interface shared between the Cortex-M0+ processor and the CoreSight MTB-M0+. This information is stored as trace packets in the SRAM by the MTB. An off-chip debugger can extract the trace information using the Debug Access Port to read the trace information from the SRAM. The debugger can then reconstruct the program flow from this information.

The MTB simultaneously stores trace information into the SRAM, and gives the processor access to the SRAM. The MTB ensures that trace write accesses have priority over processor accesses.

The execution trace packet consists of a pair of 32-bit words that the MTB generates when it detects the processor PC value changes non-sequentially. A non-sequential PC change can occur during branch instructions or during exception entry. See the CoreSight MTB-M0+ Technical Reference Manual for more details on the MTB execution trace packet format.

Tracing is enabled when the MASTER.EN bit in the Master Trace Control Register is 1. There are various ways to set the bit to 1 to start tracing, or to 0 to stop tracing. See the CoreSight Cortex-M0+ Technical Reference Manual for more details on the Trace start and stop and for a detailed description of the MTB's MASTER register. The MTB can be programmed to stop tracing automatically when the memory fills to a specified watermark level or to start or stop tracing by writing directly to the MASTER.EN bit. If the watermark mechanism is not being used and the trace buffer overflows, then the buffer wraps around overwriting previous trace packets.

The base address of the MTB registers is 0x41006000; this address is also written in the CoreSight ROM Table. The offset of each register from the base address is fixed and as defined by the CoreSight MTB-M0+ Technical Reference Manual. The MTB has 4 programmable registers to control the behavior of the trace features:

- POSITION: Contains the trace write pointer and the wrap bit,
- MASTER: Contains the main trace enable bit and other trace control fields,
- FLOW: Contains the WATERMARK address and the AUTOSTOP and AUTOHALT control bits,
- BASE: Indicates where the SRAM is located in the processor memory map. This register is provided to enable auto discovery of the MTB SRAM location, by a debug agent.

See the CoreSight MTB-M0+ Technical Reference Manual for a detailed description of these registers.

## 7.4. High-Speed Bus System

### 7.4.1. Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a one-to-one clock frequency with the bus masters

### 7.4.2. Configuration

**Table 7-4. Bus Matrix Masters**

| Bus Matrix Masters | Master ID |
|---|---|
| CM0+ - Cortex M0+ Processor | 0 |
| DSU - Device Service Unit | 1 |

**Table 7-5. Bus Matrix Slaves**

| Bus Matrix Slaves | Slave ID |
|---|---|
| Internal Flash Memory | 0 |
| AHB-APB Bridge A | 1 |
| AHB-APB Bridge B | 2 |
| AHB-APB Bridge C | 3 |

## 7.5. AHB-APB Bridge

The AHB-APB bridge is an AHB slave, providing an interface between the high-speed AHB domain and the low-power APB domain. It is used to provide access to the programmable control registers of peripherals (see *Product Mapping*).

AHB-APB bridge is based on AMBA APB Protocol Specification V2.0 (ref. as APB4) including:

- Wait state support
- Error reporting
- Transaction protection
- Sparse data transfer (byte, half-word and word)

Additional enhancements:

- Address and data cycles merged into a single cycle
- Sparse data transfer also apply to read access

to operate the AHB-APB bridge, the clock (CLK_HPBx_AHB) must be enabled. See *PM – Power Manager* for details.

**Figure 7-1. APB Write Access.**

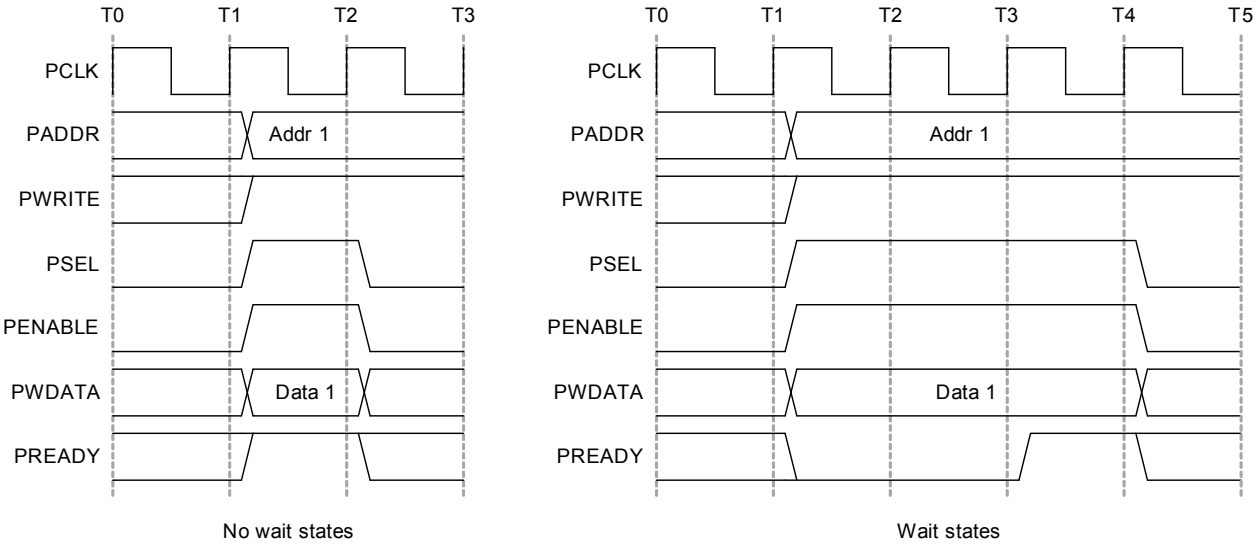
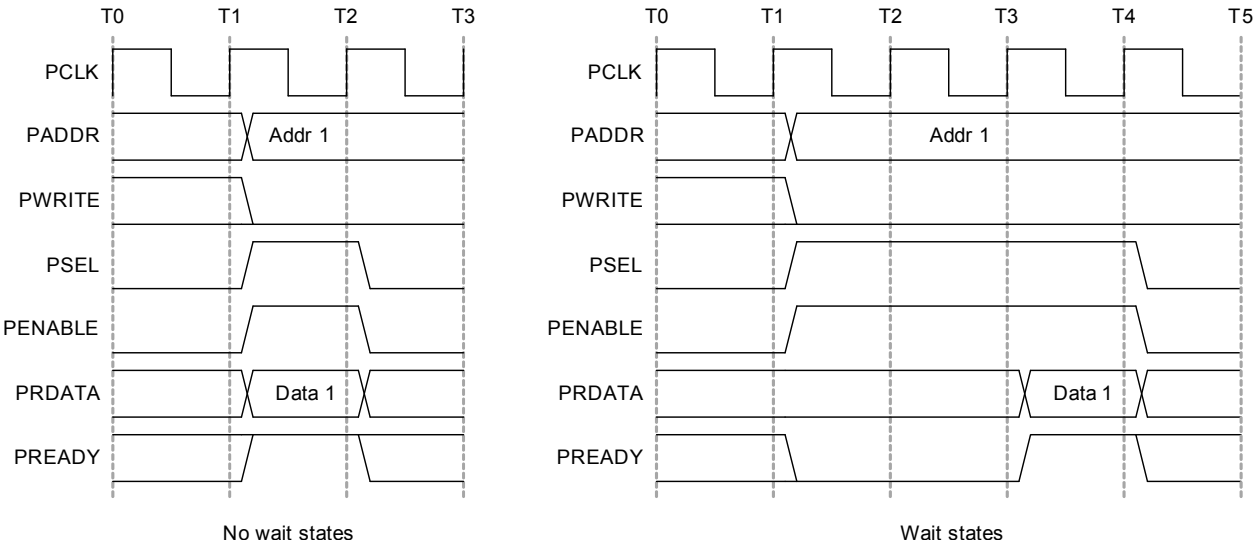



**Figure 7-2. APB Read Access.**




**Related Links**

Product Mapping on page 19

## 7.6. PAC - Peripheral Access Controller

### 7.6.1. Overview

There is one PAC associated with each AHB-APB bridge. The PAC can provide write protection for registers of each peripheral connected on the same bridge.

The PAC peripheral bus clock (CLK_PACx_APB) can be enabled and disabled in the Power Manager. CLK_PAC0_APB and CLK_PAC1_APB are enabled are reset. CLK_PAC2_APB is disabled at reset. Refer to *PM – Power Manager* for details. The PAC will continue to operate in any sleep mode where the selected clock source is running. Write-protection does not apply for debugger access. When the debugger makes an access to a peripheral, write-protection is ignored so that the debugger can update the register.

Write-protect registers allow the user to disable a selected peripheral's write-protection without doing a read-modify-write operation. These registers are mapped into two I/O memory locations, one for clearing and one for setting the register bits. Writing a one to a bit in the Write Protect Clear register (WPCLR) will clear the corresponding bit in both registers (WPCLR and WPSET) and disable the write-protection for the corresponding peripheral, while writing a one to a bit in the Write Protect Set (WPSET) register will set the corresponding bit in both registers (WPCLR and WPSET) and enable the write-protection for the corresponding peripheral. Both registers (WPCLR and WPSET) will return the same value when read.

If a peripheral is write-protected, and if a write access is performed, data will not be written, and the peripheral will return an access error (CPU exception).

The PAC also offers a safety feature for correct program execution, with a CPU exception generated on double write-protection or double unprotection of a peripheral. If a peripheral n is write-protected and a write to one in WPSET[n] is detected, the PAC returns an error. This can be used to ensure that the application follows the intended program flow by always following a write-protect with an unprotect, and vice versa. However, in applications where a write-protected peripheral is used in several contexts, e.g., interrupts, care should be taken so that either the interrupt can not happen while the main application or other interrupt levels manipulate the write-protection status, or when the interrupt handler needs to unprotect the peripheral, based on the current protection status, by reading WPSET.

## 7.7. Register Description

Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly. Refer to the Product Mapping for PAC locations.

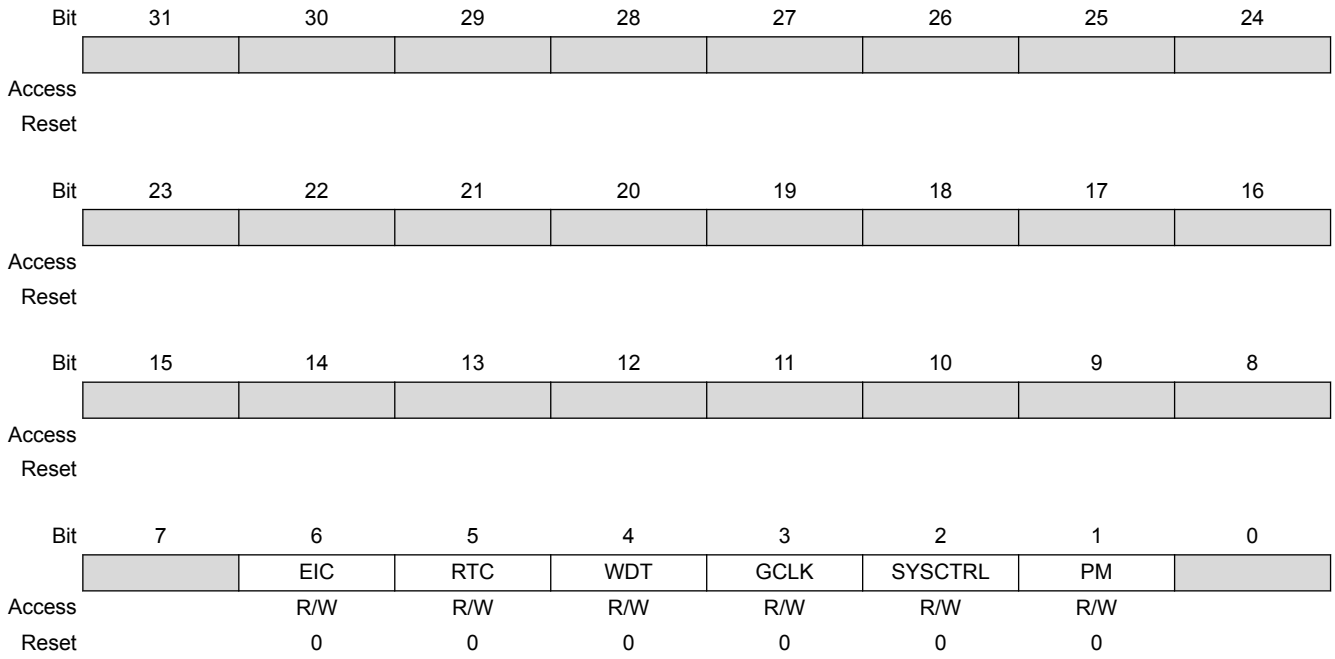
**Related Links**

Product Mapping on page 19

### 7.7.1. PAC0 Register Description

#### 7.7.1.1. Write Protect Clear

**Name:** WPCLR
**Offset:** 0x00
**Reset:** 0x000000
**Property:** –



| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | EIC | RTC | WDT | GCLK | SYSCTRL | PM | |
| Access | | R/W | R/W | R/W | R/W | R/W | R/W | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | |

**Bit 6 – EIC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 5 – RTC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 4 – WDT**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 3 – GCLK**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 2 – SYSCTRL**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

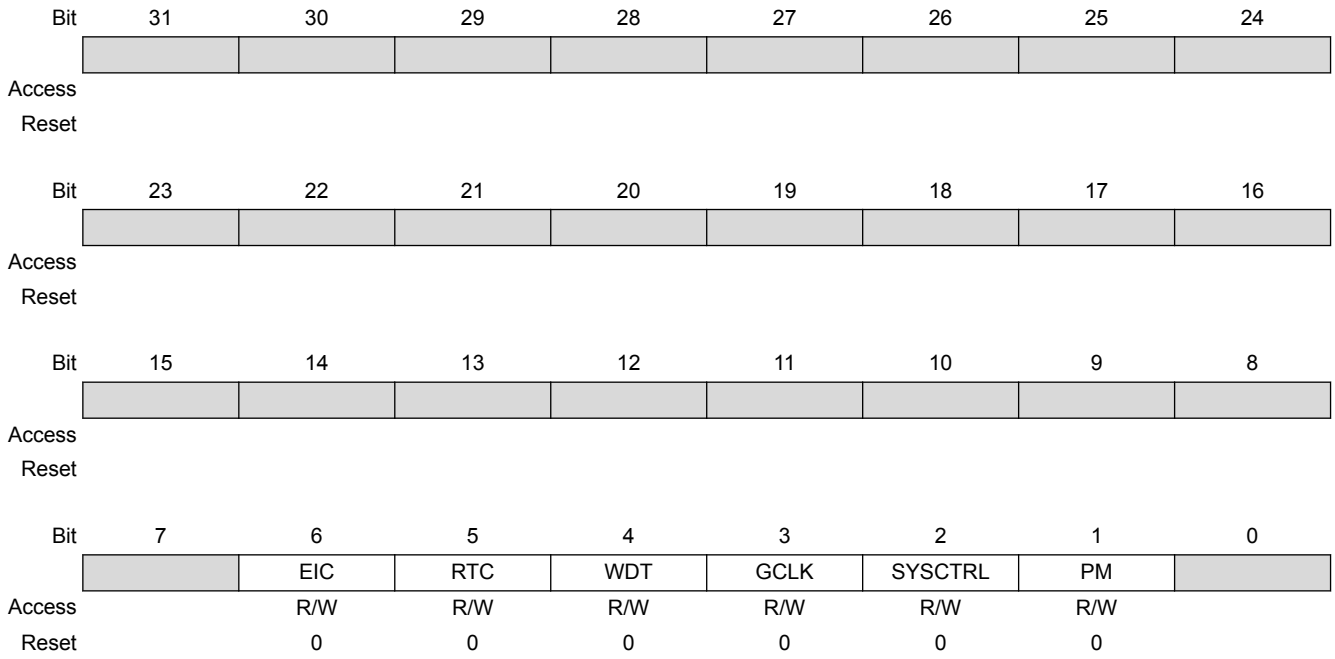
**Bit 1 – PM**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

### 7.7.1.2. Write Protect Set

**Name:** WPSET
**Offset:** 0x04
**Reset:** 0x000000
**Property:** –




**Bit 6 – EIC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 5 – RTC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 4 – WDT**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 3 – GCLK**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 2 – SYSCTRL**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 1 – PM**
Writing a zero to these bits has no effect.

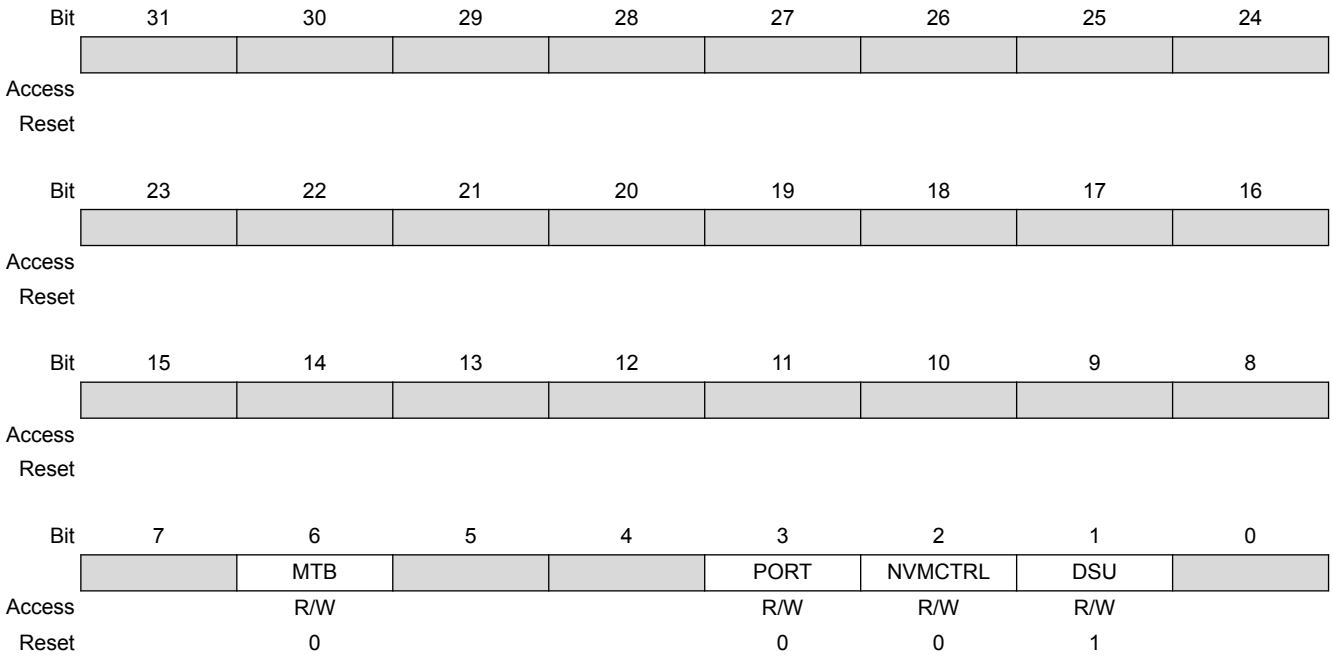
Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

### 7.7.2. PAC1 Register Description

#### 7.7.2.1. Write Protect Clear

**Name:** WPCLR
**Offset:** 0x00
**Reset:** 0x000002
**Property:** –




**Bit 6 – MTB**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 3 – PORT**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 2 – NVMCTRL**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

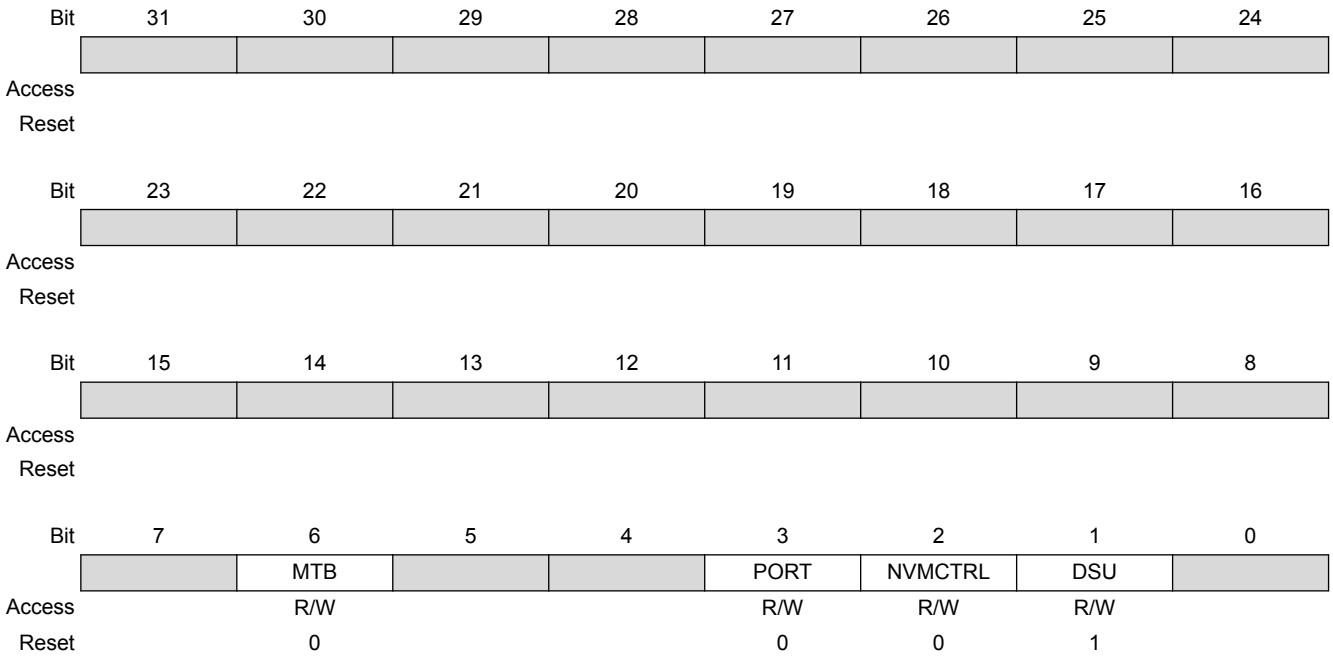
**Bit 1 – DSU**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

### 7.7.2.2. Write Protect Set

**Name:** WPSET
**Offset:** 0x04
**Reset:** 0x000002
**Property:** –



| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | MTB | | | PORT | NVMCTRL | DSU | |
| Access | | R/W | | | R/W | R/W | R/W | |
| Reset | | 0 | | | 0 | 0 | 1 | |

**Bit 6 – MTB**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 3 – PORT**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 2 – NVMCTRL**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 1 – DSU**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

### 7.7.3. PAC2 Register Description

### 7.7.3.1. Write Protect Clear

**Name:** WPCLR
**Offset:** 0x00
**Reset:** 0x00800000
**Property:** –

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | | | | | PTC | DAC | AC | ADC |
| Access | | | | | R/W | R/W | R/W | R/W |
| Reset | | | | | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | TC7 | TC6 | TC5 | TC4 | TC3 | TC2 | TC1 | TC0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SERCOM5 | SERCOM4 | SERCOM3 | SERCOM2 | SERCOM1 | SERCOM0 | EVSYS | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**Bit 19 – PTC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 18 – DAC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 17 – AC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 16 – ADC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bits 15,14,13,12,11,10,9,8 – TCx**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bits 7,6,5,4,3,2 – SERCOMx**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 1 – EVSYS**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

### 7.7.3.2. Write Protect Set

**Name:** WPSET
**Offset:** 0x04
**Reset:** 0x00800000
**Property:** –

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | | | | | PTC | DAC | AC | ADC |
| Access | | | | | R/W | R/W | R/W | R/W |
| Reset | | | | | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | TC7 | TC6 | TC5 | TC4 | TC3 | TC2 | TC1 | TC0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SERCOM5 | SERCOM4 | SERCOM3 | SERCOM2 | SERCOM1 | SERCOM0 | EVSYS | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**Bit 19 – PTC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 18 – DAC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 17 – AC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 16 – ADC**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bits 15,14,13,12,11,10,9,8 – TCx**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bits 7,6,5,4,3,2 – SERCOMx**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

**Bit 1 – EVSYS**
Writing a zero to these bits has no effect.

Writing a one to these bits will clear the Write Protect bit for the corresponding peripherals.

| Value | Description |
|---|---|
| 0 | Write-protection is disabled. |
| 1 | Write-protection is enabled. |

# 8. Packaging Information

## 8.1. Thermal Considerations

### Related Links

Junction Temperature on page 39

### 8.1.1. Thermal Resistance Data

The following *table* summarizes the thermal resistance data depending on the package.

**Table 8-1. Thermal Resistance Data**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ |
|---|---|---|
| 32-pin TQFP | 68.0°C/W | 25.8°C/W |
| 48-pin TQFP | 78.8°C/W | 12.3°C/W |
| 64-pin TQFP | 66.7°C/W | 11.9°C/W |
| 32-pin QFN | 37.2°C/W | 13.1°C/W |
| 48-pin QFN | 33.0°C/W | 11.4°C/W |
| 64-pin QFN | 33.5°C/W | 11.2°C/W |
| 64-ball UFBGA | 67.4°C/W | 12.4°C/W |
| 45-ball WLCSP | 37.0°C/W | 0.36°C/W |

### 8.1.2. Junction Temperature

The average chip-junction temperature, $T_J$, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- $\theta_{JA}$ = Package thermal resistance, Junction-to-ambient (°C/W), see Thermal Resistance Data
- $\theta_{JC}$ = Package thermal resistance, Junction-to-case thermal resistance (°C/W), see Thermal Resistance Data
- $\theta_{HEATSINK}$ = Thermal resistance (°C/W) specification of the external cooling device
- $P_D$ = Device power consumption (W)
- $T_A$ = Ambient temperature (°C)

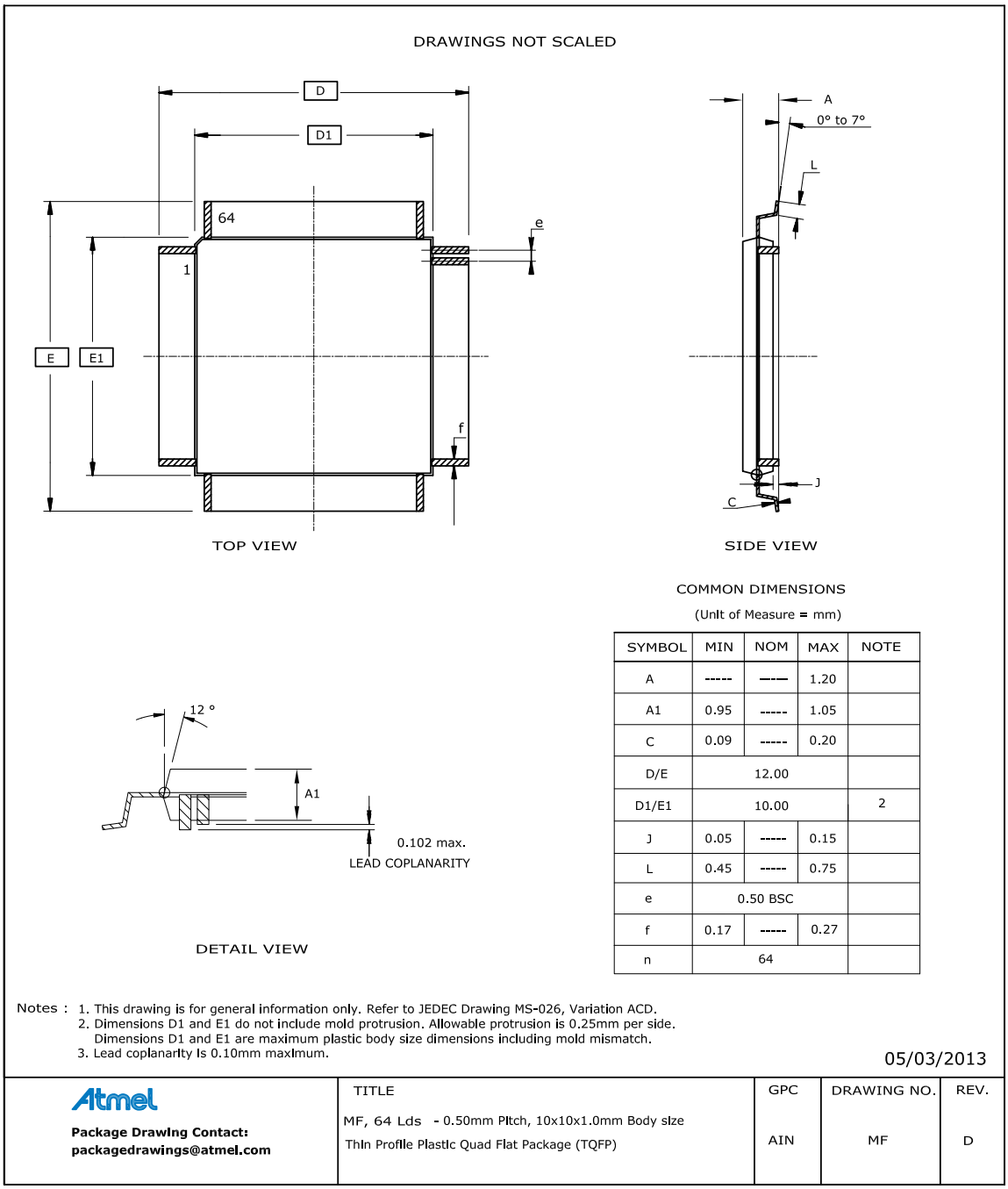
From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature $T_J$ in °C.

### Related Links

Thermal Considerations on page 39

## 8.2. Package Drawings

### 8.2.1. 64 pin TQFP




COMMON DIMENSIONS

(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | ----- | ---- | 1.20 | |
| A1 | 0.95 | ----- | 1.05 | |
| C | 0.09 | ----- | 0.20 | |
| D/E | | 12.00 | | |
| D1/E1 | | 10.00 | | 2 |
| J | 0.05 | ----- | 0.15 | |
| L | 0.45 | ----- | 0.75 | |
| e | | 0.50 BSC | | |
| f | 0.17 | ----- | 0.27 | |
| n | | 64 | | |

Notes :
1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ACD.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

05/03/2013

| Atmel | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| Package Drawing Contact: packagedrawings@atmel.com | MF, 64 Lds - 0.50mm Pitch, 10x10x1.0mm Body size Thin Profile Plastic Quad Flat Package (TQFP) | AIN | MF | D |

**Table 8-2. Device and Package Maximum Weight**

| | |
|---|---|
| 300 | mg |

**Table 8-3. Package Characteristics**

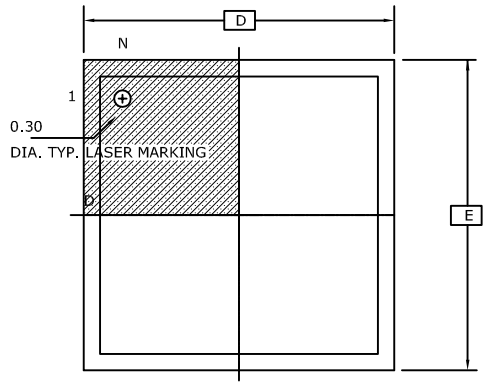
| | |
|---|---|
| Moisture Sensitivity Level | MSL3 |

**Table 8-4. Package Reference**

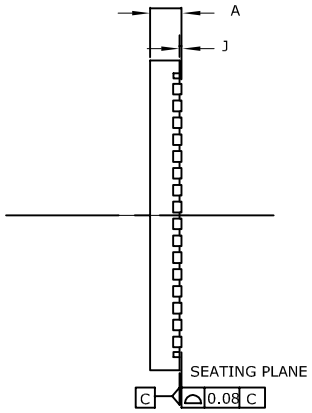
| | |
|---|---|
| JEDEC Drawing Reference | MS-026 |
| JESD97 Classification | E3 |

### 8.2.2. 64 pin QFN

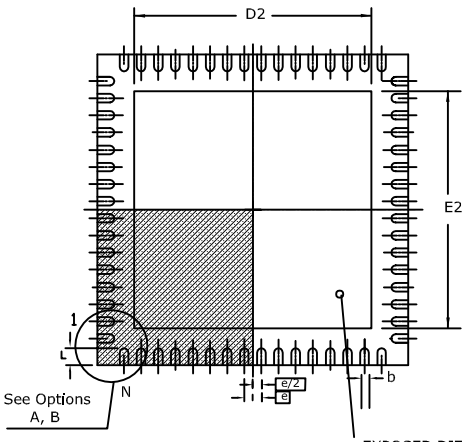
DRAWINGS NOT SCALED




TOP VIEW




SIDE VIEW

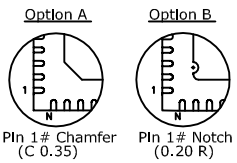



BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 0.80 | ----- | 1.00 | |
| D/E | | 9.00 BSC | | |
| D2/E2 | 4.60 | 4.70 | 4.80 | |
| J | 0.00 | ----- | 0.05 | |
| b | 0.15 | 0.20 | 0.25 | |
| e | | 0.50 BSC | | |
| L | 0.30 | 0.40 | 0.55 | |
| N | | 64 | | |




Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VMMD-4, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

05/27/2011

| | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| Package Drawing Contact: packagedrawings@atmel.com | PA, 64 Leads , 0.50 mm pitch, 9 x 9 x 1 mm Very Thin Quad Flat No Lead Package (VQFN) Sawn | ZST | PA | A |

**Note:** The exposed die attach pad is not connected electrically inside the device.

**Table 8-5. Device and Package Maximum Weight**

| | |
|---|---|
| 200 | mg |

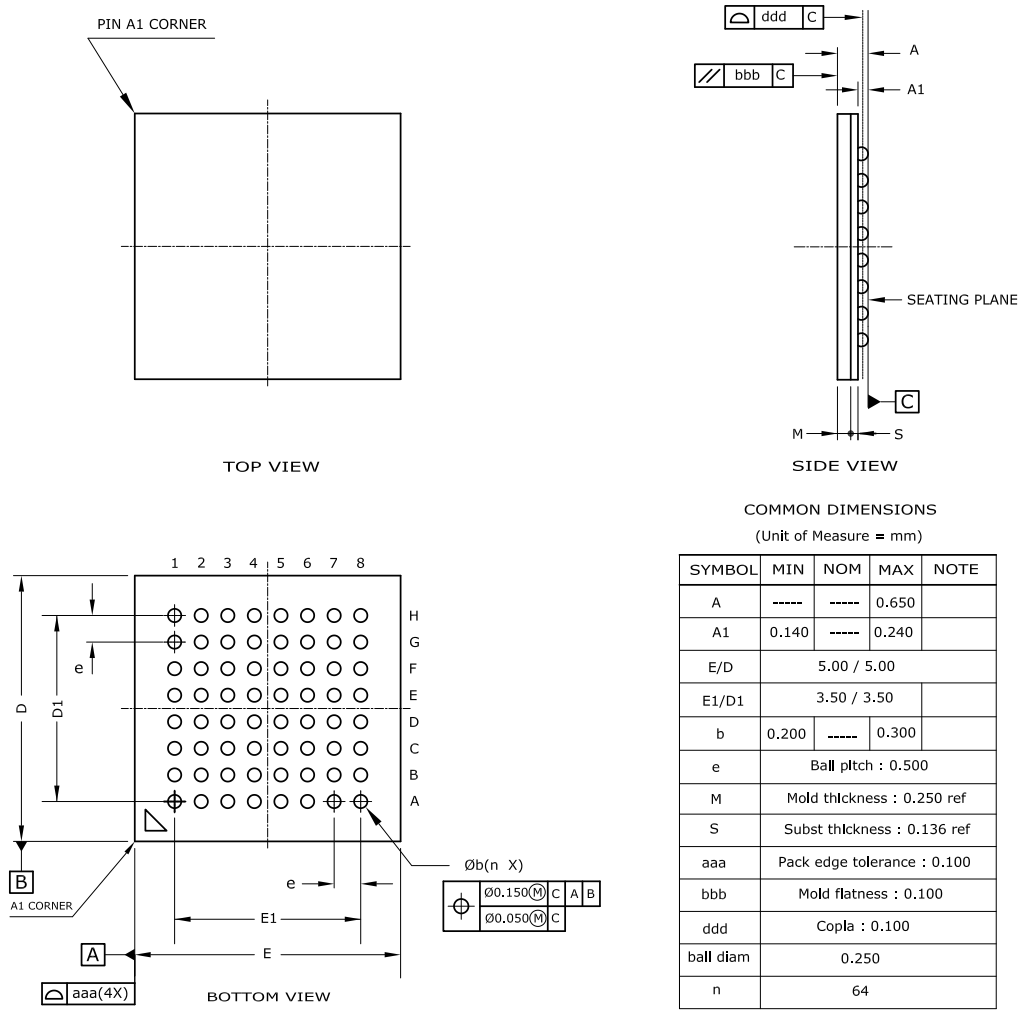
**Table 8-6. Package Charateristics**

| | |
|---|---|
| Moisture Sensitivity Level | MSL3 |

**Table 8-7. Package Reference**

| | |
|---|---|
| JEDEC Drawing Reference | MO-220 |
| JESD97 Classification | E3 |

### 8.2.3. 64-ball UFBGA




COMMON DIMENSIONS

(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | ----- | ----- | 0.650 | |
| A1 | 0.140 | ----- | 0.240 | |
| E/D | 5.00 / 5.00 | | | |
| E1/D1 | 3.50 / 3.50 | | | |
| b | 0.200 | ----- | 0.300 | |
| e | Ball pitch : 0.500 | | | |
| M | Mold thickness : 0.250 ref | | | |
| S | Subst thickness : 0.136 ref | | | |
| aaa | Pack edge tolerance : 0.100 | | | |
| bbb | Mold flatness : 0.100 | | | |
| ddd | Copla : 0.100 | | | |
| ball diam | 0.250 | | | |
| n | 64 | | | |

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-280, Variation UCCBB for proper dimensions, tolerances, datums, etc.
2. Array as seen from the bottom of the package.
3. Dimension A includes stand-off height A1, package body thickness, and lid height, but does not include attached features.
4. Dimension b is measured at the maximum ball diameter, parallel to primary datum C.

**Table 8-8. Device and Package Maximum Weight**

| | |
|---|---|
| 27.4 | mg |

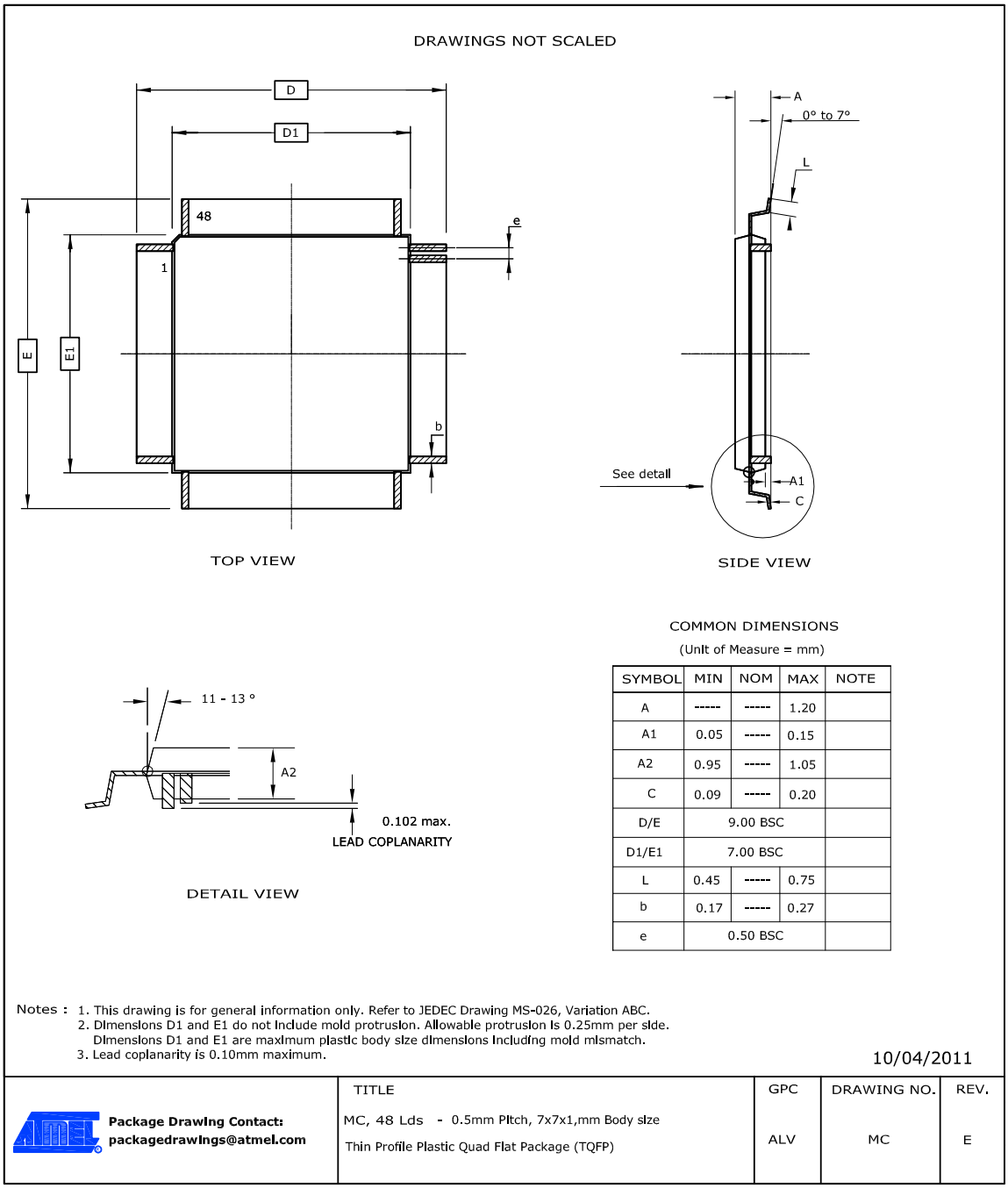
**Table 8-9. Package Characteristics**

| | |
|---|---|
| Moisture Sensitivity Level | MSL3 |

**Table 8-10. Package Reference**

| | |
|---|---|
| JEDEC Drawing Reference | MO-220 |
| JESD97 Classification | E8 |

### 8.2.4. 48 pin TQFP




COMMON DIMENSIONS

(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | ----- | ----- | 1.20 | |
| A1 | 0.05 | ----- | 0.15 | |
| A2 | 0.95 | ----- | 1.05 | |
| C | 0.09 | ----- | 0.20 | |
| D/E | | 9.00 BSC | | |
| D1/E1 | | 7.00 BSC | | |
| L | 0.45 | ----- | 0.75 | |
| b | 0.17 | ----- | 0.27 | |
| e | | 0.50 BSC | | |

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

10/04/2011

| | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| Package Drawing Contact: packagedrawings@atmel.com | MC, 48 Lds - 0.5mm Pitch, 7x7x1,mm Body size<br>Thin Profile Plastic Quad Flat Package (TQFP) | ALV | MC | E |

**Table 8-11. Device and Package Maximum Weight**

| | |
|---|---|
| 140 | mg |

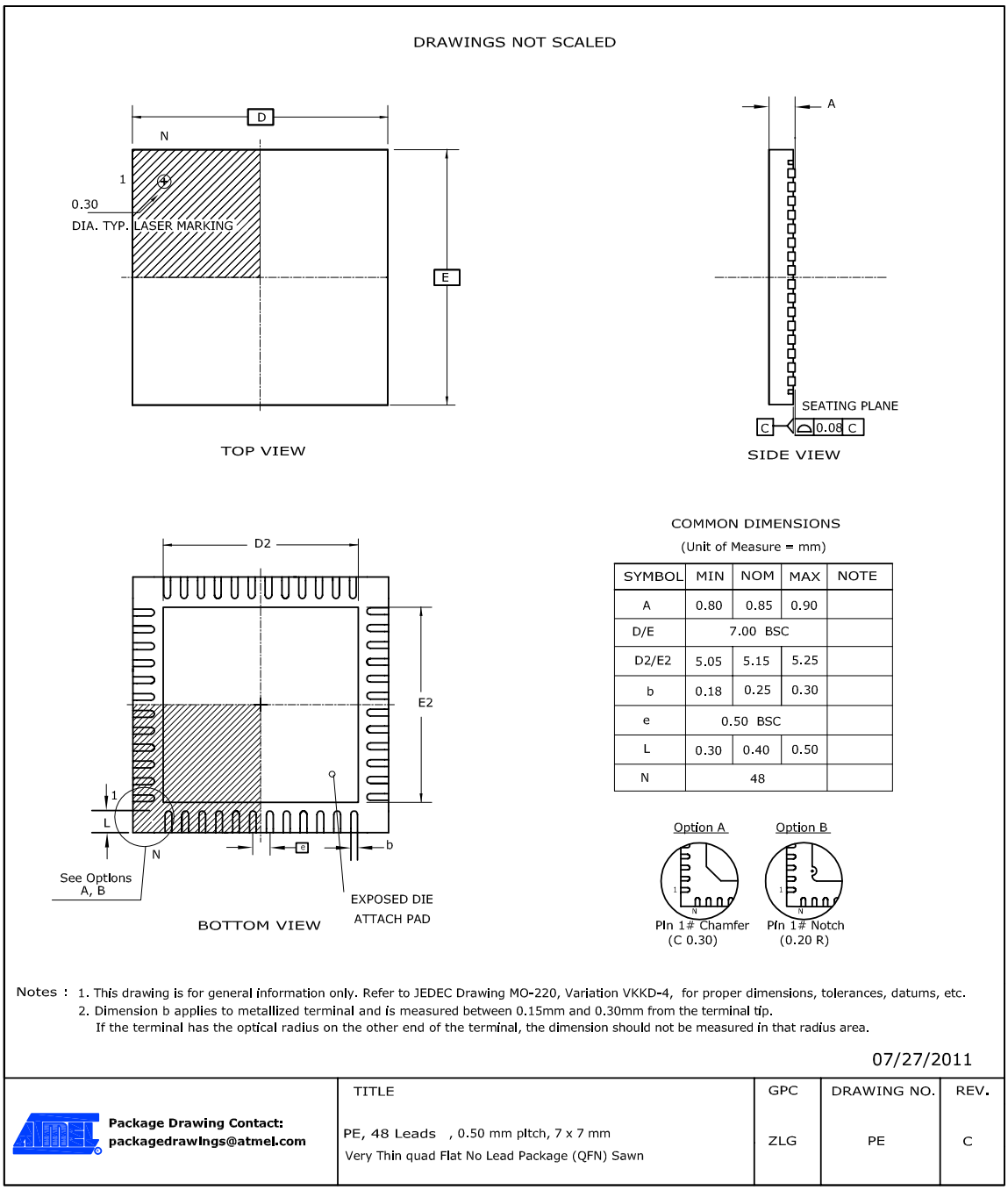
**Table 8-12. Package Characteristics**

| | |
|---|---|
| Moisture Sensitivity Level | MSL3 |

**Table 8-13. Package Reference**

| | |
|---|---|
| JEDEC Drawing Reference | MS-026 |
| JESD97 Classification | E3 |

### 8.2.5. 48 pin QFN




| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 | |
| D/E | | 7.00 BSC | | |
| D2/E2 | 5.05 | 5.15 | 5.25 | |
| b | 0.18 | 0.25 | 0.30 | |
| e | | 0.50 BSC | | |
| L | 0.30 | 0.40 | 0.50 | |
| N | | 48 | | |

**Note:** The exposed die attach pad is not connected electrically inside the device.

**Table 8-14. Device and Package Maximum Weight**

| | |
|---|---|
| 140 | mg |

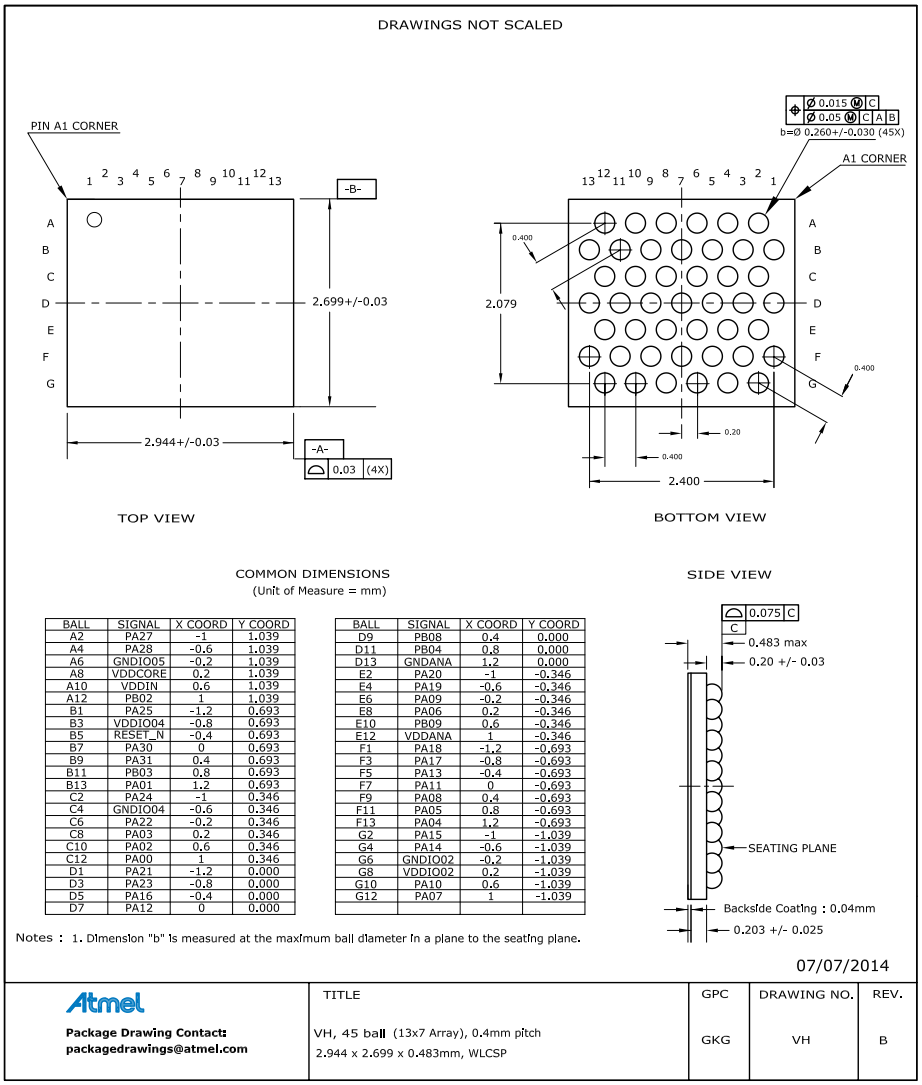
**Table 8-15. Package Characteristics**

| | |
|---|---|
| Moisture Sensitivity Level | MSL3 |

**Table 8-16. Package Reference**

| | |
|---|---|
| JEDEC Drawing Reference | MO-220 |
| JESD97 Classification | E3 |

### 8.2.6. 45-ball WLCSP




| BALL | SIGNAL | X COORD | Y COORD |
|---|---|---|---|
| A2 | PA27 | -1 | 1.039 |
| A4 | PA28 | -0.6 | 1.039 |
| A6 | GNDIO05 | -0.2 | 1.039 |
| A8 | VDDCORE | 0.2 | 1.039 |
| A10 | VDDIN | 0.6 | 1.039 |
| A12 | PB02 | 1 | 1.039 |
| B1 | PA25 | -1.2 | 0.693 |
| B3 | VDDIO04 | -0.8 | 0.693 |
| B5 | RESET_N | -0.4 | 0.693 |
| B7 | PA30 | 0 | 0.693 |
| B9 | PA31 | 0.4 | 0.693 |
| B11 | PB03 | 0.8 | 0.693 |
| B13 | PA01 | 1.2 | 0.693 |
| C2 | PA24 | -1 | 0.346 |
| C4 | GNDIO04 | -0.6 | 0.346 |
| C6 | PA22 | -0.2 | 0.346 |
| C8 | PA03 | 0.2 | 0.346 |
| C10 | PA02 | 0.6 | 0.346 |
| C12 | PA00 | 1 | 0.346 |
| D1 | PA21 | -1.2 | 0.000 |
| D3 | PA23 | -0.8 | 0.000 |
| D5 | PA16 | -0.4 | 0.000 |
| D7 | PA12 | 0 | 0.000 |

| BALL | SIGNAL | X COORD | Y COORD |
|---|---|---|---|
| D9 | PB08 | 0.4 | 0.000 |
| D11 | PB04 | 0.8 | 0.000 |
| D13 | GNDANA | 1.2 | 0.000 |
| E2 | PA20 | -1 | -0.346 |
| E4 | PA19 | -0.6 | -0.346 |
| E6 | PA09 | -0.2 | -0.346 |
| E8 | PA06 | 0.2 | -0.346 |
| E10 | PB09 | 0.6 | -0.346 |
| E12 | VDDANA | 1 | -0.346 |
| F1 | PA18 | -1.2 | -0.693 |
| F3 | PA17 | -0.8 | -0.693 |
| F5 | PA13 | -0.4 | -0.693 |
| F7 | PA11 | 0 | -0.693 |
| F9 | PA08 | 0.4 | -0.693 |
| F11 | PA05 | 0.8 | -0.693 |
| F13 | PA04 | 1.2 | -0.693 |
| G2 | PA15 | -1 | -1.039 |
| G4 | PA14 | -0.6 | -1.039 |
| G6 | GNDIO02 | -0.2 | -1.039 |
| G8 | VDDIO02 | 0.2 | -1.039 |
| G10 | PA10 | 0.6 | -1.039 |
| G12 | PA07 | 1 | -1.039 |

**Table 8-17. Device and Package Maximum Weight**

| | |
|---|---|
| 7.3 | mg |

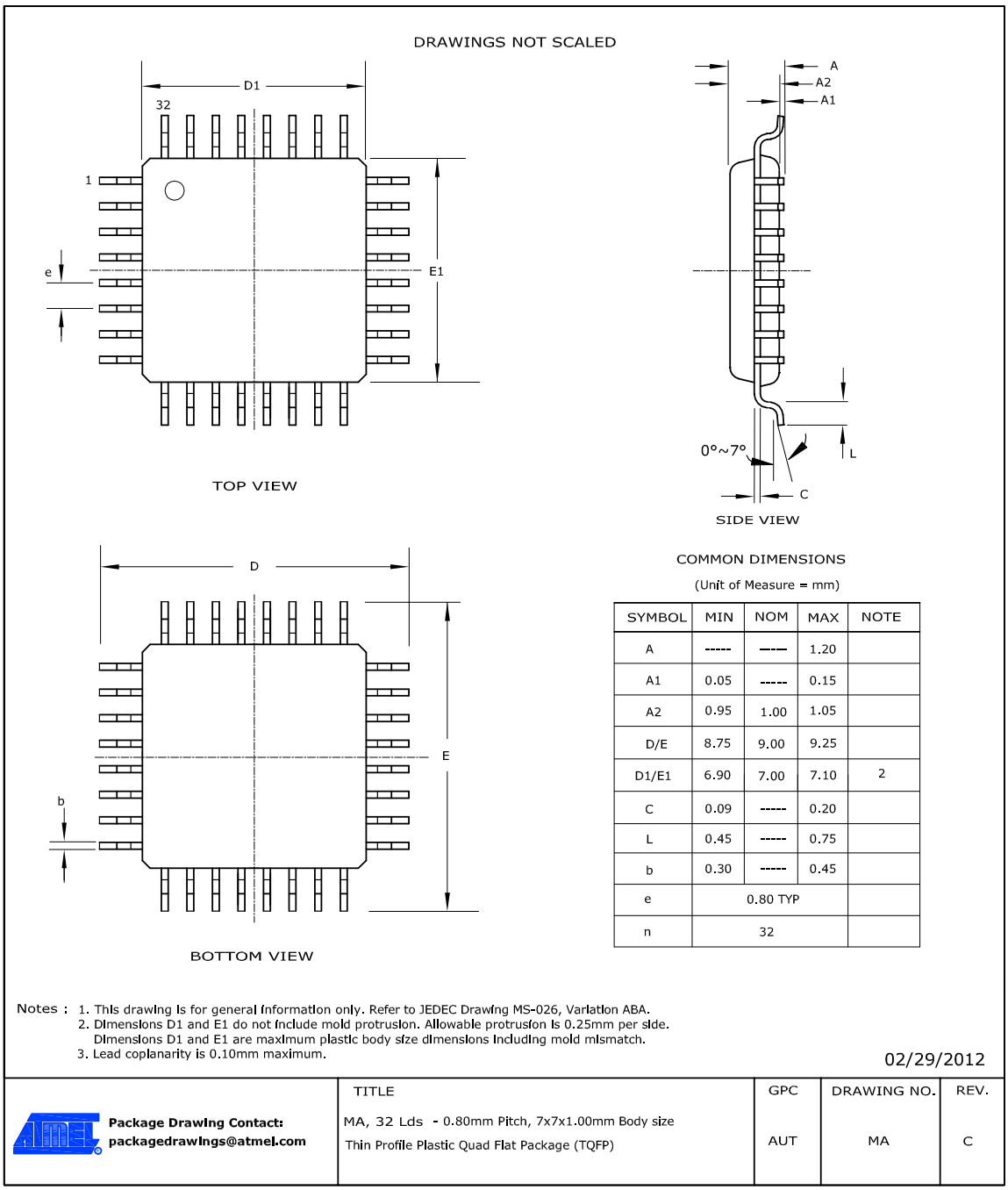
**Table 8-18. Package Characteristics**

| | |
|---|---|
| Moisture Sensitivity Level | MSL1 |

**Table 8-19. Package Reference**

| | |
|---|---|
| JEDEC Drawing Reference | MO-220 |
| JESD97 Classification | E1 |

### 8.2.7. 32 pin TQFP




COMMON DIMENSIONS

(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | ----- | ---- | 1.20 | |
| A1 | 0.05 | ----- | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D/E | 8.75 | 9.00 | 9.25 | |
| D1/E1 | 6.90 | 7.00 | 7.10 | 2 |
| C | 0.09 | ----- | 0.20 | |
| L | 0.45 | ----- | 0.75 | |
| b | 0.30 | ----- | 0.45 | |
| e | 0.80 TYP | | | |
| n | 32 | | | |

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

02/29/2012

| Package Drawing Contact: packagedrawings@atmel.com | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| | MA, 32 Lds - 0.80mm Pitch, 7x7x1.00mm Body size Thin Profile Plastic Quad Flat Package (TQFP) | AUT | MA | C |

**Table 8-20. Device and Package Maximum Weight**

| | |
|---|---|
| 100 | mg |

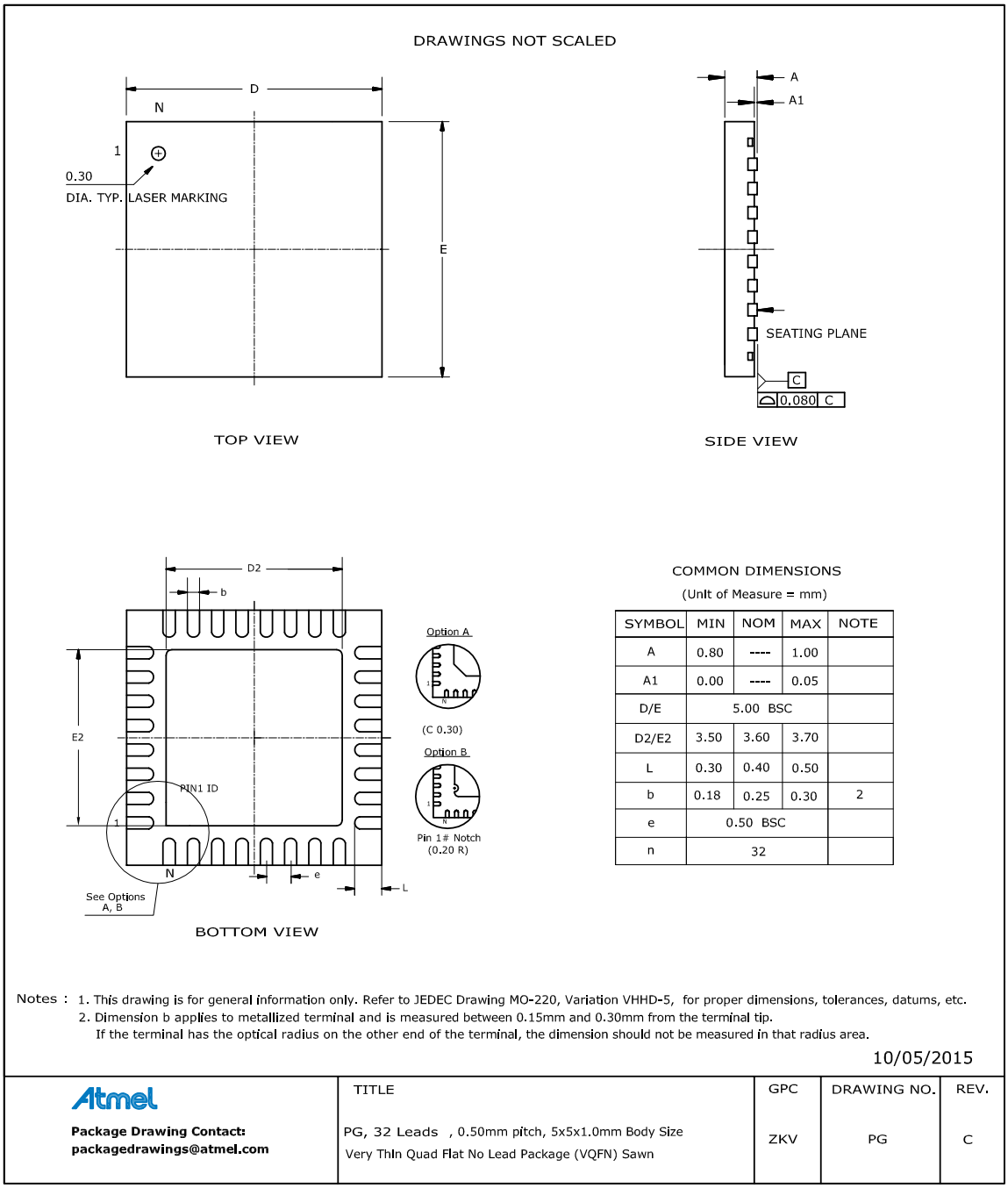
**Table 8-21. Package Charateristics**

| | |
|---|---|
| Moisture Sensitivity Level | MSL3 |

**Table 8-22. Package Reference**

| | |
|---|---|
| JEDEC Drawing Reference | MS-026 |
| JESD97 Classification | E3 |

### 8.2.8. 32 pin QFN




**Note:** The exposed die attach pad is connected inside the device to GND and GNDANA.

**Table 8-23. Device and Package Maximum Weight**

| | |
|---|---|
| 90 | mg |

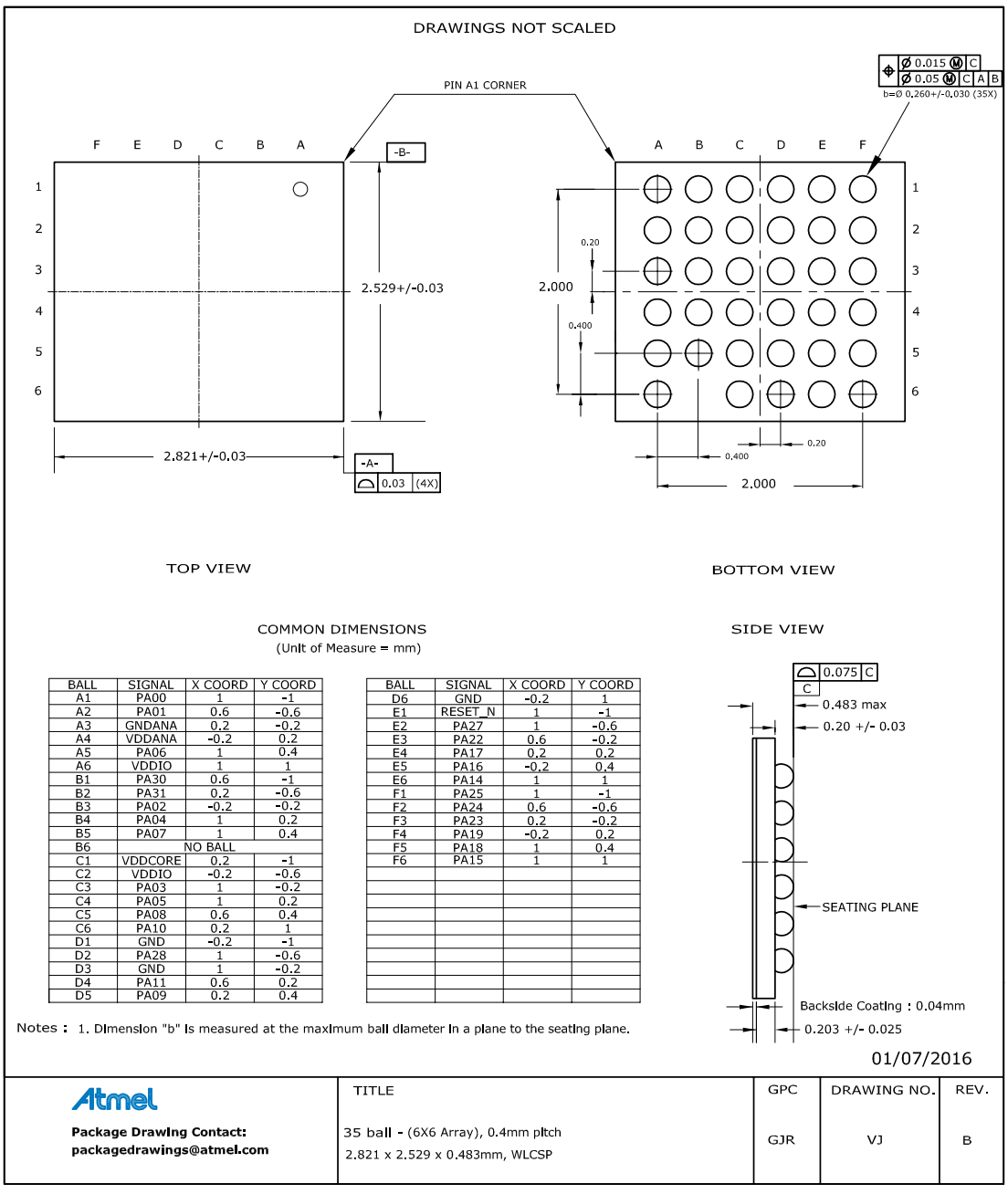
**Table 8-24. Package Characteristics**

| | |
|---|---|
| Moisture Sensitivity Level | MSL3 |

**Table 8-25. Package Reference**

| | |
|---|---|
| JEDEC Drawing Reference | MO-220 |
| JESD97 Classification | E3 |

### 8.2.9. 35 ball WLCSP




| BALL | SIGNAL | X COORD | Y COORD |
|---|---|---|---|
| A1 | PA00 | 1 | -1 |
| A2 | PA01 | 0.6 | -0.6 |
| A3 | GNDANA | 0.2 | -0.2 |
| A4 | VDDANA | -0.2 | 0.2 |
| A5 | PA06 | 1 | 0.4 |
| A6 | VDDIO | 1 | 1 |
| B1 | PA30 | 0.6 | -1 |
| B2 | PA31 | 0.2 | -0.6 |
| B3 | PA02 | -0.2 | -0.2 |
| B4 | PA04 | 1 | 0.2 |
| B5 | PA07 | 1 | 0.4 |
| B6 | NO BALL | | |
| C1 | VDDCORE | 0.2 | -1 |
| C2 | VDDIO | -0.2 | -0.6 |
| C3 | PA03 | 1 | -0.2 |
| C4 | PA05 | 1 | 0.2 |
| C5 | PA08 | 0.6 | 0.4 |
| C6 | PA10 | 0.2 | 1 |
| D1 | GND | -0.2 | -1 |
| D2 | PA28 | 1 | -0.6 |
| D3 | GND | 1 | -0.2 |
| D4 | PA11 | 0.6 | 0.2 |
| D5 | PA09 | 0.2 | 0.4 |

| BALL | SIGNAL | X COORD | Y COORD |
|---|---|---|---|
| D6 | GND | -0.2 | 1 |
| E1 | RESET_N | 1 | -1 |
| E2 | PA27 | 1 | -0.6 |
| E3 | PA22 | 0.6 | -0.2 |
| E4 | PA17 | 0.2 | 0.2 |
| E5 | PA16 | -0.2 | 0.4 |
| E6 | PA14 | 1 | 1 |
| F1 | PA25 | 1 | -1 |
| F2 | PA24 | 0.6 | -0.6 |
| F3 | PA23 | 0.2 | -0.2 |
| F4 | PA19 | -0.2 | 0.2 |
| F5 | PA18 | 1 | 0.4 |
| F6 | PA15 | 1 | 1 |

**Table 8-26. Device and Package Maximum Weight**

| | |
|---|---|
| 6.2 | mg |

**Table 8-27. Package Characteristics**

| | |
|---|---|
| Moisture Sensitivity Level | MSL1 |

**Table 8-28. Package Reference**

| | |
|---|---|
| JEDEC Drawing Reference | MO-220 |
| JESD97 Classification | E1 |

## 8.3. Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

**Table 8-29.**

| Profile Feature | Green Package |
|---|---|
| Average Ramp-up Rate (217°C to peak) | 3°C/s max. |
| Preheat Temperature 175°C ±25°C | 150-200°C |
| Time Maintained Above 217°C | 60-150s |
| Time within 5°C of Actual Peak Temperature | 30s |
| Peak Temperature Range | 260°C |
| Ramp-down Rate | 6°C/s max. |
| Time 25°C to Peak Temperature | 8 minutes max. |

A maximum of three reflow passes is allowed per component.

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ATSAMD20J17A-AU ATSAMD20E18A-AU ATSAMD20E18A-AUT ATSAMD20E18A-MUT ATSAMD20E18A-MU ATSAMD20J16A-CU ATSAMD20J17A-MN ATSAMD20E17A-ANT ATSAMD20E14A-MNT ATSAMD20G14A-MNT ATSAMD20J14A-AN ATSAMD20J15A-CN ATSAMD20J14A-CNT ATSAMD20E16A-MN ATSAMD20G17A-ANT ATSAMD20J18A-CN ATSAMD20J15A-CUT ATSAMD20J16A-CNT ATSAMD20J16A-MN ATSAMD20E17A-MNT ATSAMD20G18A-ANT ATSAMD20J16A-MNT ATSAMD20E15A-MN ATSAMD20J18A-CU ATSAMD20E16A-AN ATSAMD20G14A-ANT ATSAMD20J16A-CUT ATSAMD20E18A-MNT ATSAMD20J16A-CN ATSAMD20J14A-ANT ATSAMD20G18A-AUES ATSAMD20G14A-MN ATSAMD20G17A-MNT ATSAMD20J17A-CU ATSAMD20G17A-UUT ATSAMD20J17A-ANT ATSAMD20G16A-AN ATSAMD20J15A-CNT ATSAMD20J17A-MNT ATSAMD20G15A-MN ATSAMD20G17A-AN ATSAMD20J18A-AN ATSAMD20G15A-ANT ATSAMD20J14A-CN ATSAMD20J18A-ANT ATSAMD20E16A-MNT ATSAMD20E14A-ANT ATSAMD20G16A-ANT ATSAMD20J15A-AN ATSAMD20J15A-ANT ATSAMD20J17A-CUT ATSAMD20J14A-MN ATSAMD20G18A-UUT ATSAMD20E17A-MN ATSAMD20J15A-CU ATSAMD20G18A-MN ATSAMD20G15A-MNT ATSAMD20E15A-MNT ATSAMD20J16A-ANT ATSAMD20G14A-AN ATSAMD20J18A-MN ATSAMD20G16A-MN ATSAMD20E15A-ANT ATSAMD20G18A-MNT ATSAMD20G16A-MNT ATSAMD20J17A-AN ATSAMD20J15A-MN ATSAMD20J14A-CU ATSAMD20E15A-AN ATSAMD20J14A-MNT ATSAMD20G15A-AN ATSAMD20G18A-AN ATSAMD20E14A-AN ATSAMD20J17A-CN ATSAMD20E18A-AN ATSAMD20J16A-AN ATSAMD20J18A-CUT ATSAMD20E16A-ANT ATSAMD20E17A-AN ATSAMD20E14A-MN ATSAMD20J15A-MNT ATSAMD20J14A-CUT ATSAMD20E18A-MN ATSAMD20J18A-MNT ATSAMD20J18A-CNT ATSAMD20G17A-MN ATSAMD20E18A-ANT ATSAMD20J17A-CNT

LifeElectronics
Живое партнерство

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*Тел: +7 (812) 336 43 04 (многоканальный)*
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