

Capacitive Controller ICs Capacitive Switch Controller IC

BU21077MUV

General Description

BU21077MUV is a capacitive switch controller for switch operation.

BU21077MUV has programmable MPU and it control the sensing sequence and how to use value of sensor. It is possible to reduce operational current with devising a sensing sequence.

Features

- Programmable MPU
- 8 Capacitive Sensor Ports
- 2-Wire Serial Bus Interface
- Single Power Supply
- Built-in Power-On-Reset and Oscillator

Applications

- Portable Device such as Smart Phone, PDA.
- Electronic Device with Multi Switches
- Information Appliance such as Projector
- AV Appliance such as Digital TV, HDD Recorder
- PC / PC Peripheral Equipment such as Laptop PC

Key Specifications

- Input Voltage Range 2.7 to 5.5V
- Operating Temperature Range -20 to +85°C

Package

VQFN020V4040

4.00 mm×4.00 mm×1.00 mm



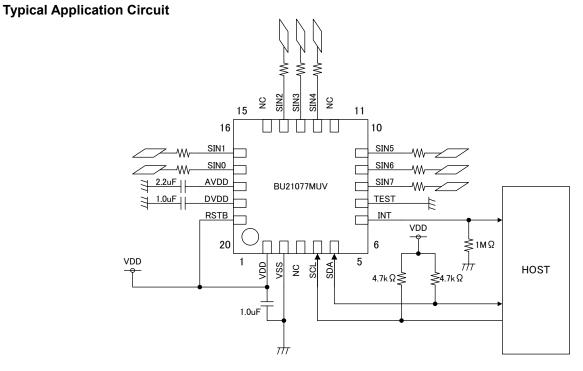


Figure 1. Typical Application Circuit

OProduct structure : Silicon monolithic integrated circuit OThis product has no designed protection against radioactive rays

Pin Configurations

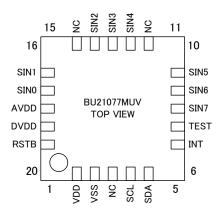


Figure 2. Pin Configurations

Pin Descriptions

Pin No.	Pin Name	I/O	Functions	Note	Power	Initial Condition	I/O Equivalent Circuit	
1	VDD	Power	Power		-	-	-	
2	VSS	Ground	Ground		-	-	-	
3	NC	-	-		-	-	-	
4	SCL	In	Host-I/F SCL pin		VDD	Hi-Z	b	
5	SDA	InOut	Host-I/F SDA pin		VDD	Hi-Z	b	
6	INT	Out	Interrupt output		VDD	Hi-Z	b	
7	TEST	In	Test input	Fix 'L' at the normal operation	VDD	Hi-Z	С	
8	SIN7	InOut	Sensor 7		AVDD	Hi-Z	а	
9	SIN6	InOut	Sensor 6		AVDD	Hi-Z	а	
10	SIN5	InOut	Sensor 5		AVDD	Hi-Z	а	
11	NC	-	-		-	-	-	
12	SIN4	InOut	Sensor 4		AVDD	Hi-Z	а	
13	SIN3	InOut	Sensor 3		AVDD	Hi-Z	а	
14	SIN2	InOut	Sensor 2		AVDD	Hi-Z	а	
15	NC	-	-		-	-	-	
16	SIN1	InOut	Sensor 1		AVDD	Hi-Z	а	
17	SIN0	InOut	Sensor 0		AVDD	Hi-Z	а	
18	AVDD	Power	LDO output for analog blocks		-	-	-	
19	DVDD	Power	LDO output for digital blocks		-	-	-	
20	RSTB	In	Reset bar input	Active 'L'	VDD	Hi-Z	С	

I/O Equivalent Circuits

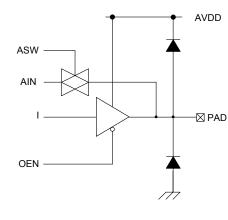
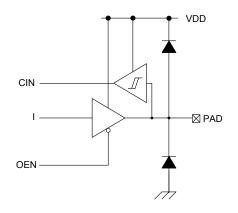


Figure 3. I/O Equivalent Circuit (a)



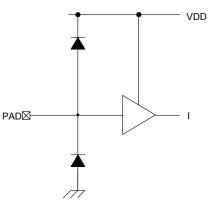
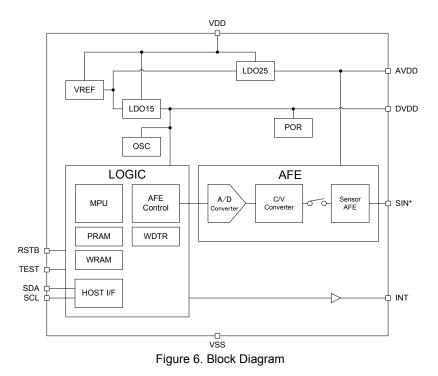


Figure 4. I/O Equivalent Circuit (b)

Figure 5. I/O Equivalent Circuit (c)

Block Diagram



Description of Blocks

- •Sensor AFE, C/V Converter
- Convert from capacitance to voltage for each sensor. •A/D Converter
- Convert from analog value to digital value.
- •LDO25
- 2.5V output LDO for Sensor AFE, C/V Converter, and A/D converter. •LDO15
 - 1.5V output LDO for OSC and Logic blocks.
- •OSC
- Oscillator.
- POR
- Power-On-Reset for system reset.
- MPU
- Control sensor and sequence by program.
- •PRAM
- 8kbyte Program RAM of MPU. It needs to download program from host.
- •WRAM Working RAM for MPU.
- •HOST I/F
- 2-wire serial bus interface compatible with I2C protocol.
- •AFE Control
- Control sequencer for Sensor AFE, C/V Converter, and A/D Converter.
- WDTR

Watchdog timer reset. It issues a reset when the MPU is hang-upped.

Absolute Maximum Ratings

(Ta = 25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VDD	-0.5 to +7.0	V
Input Voltage	V _{IN}	-0.5 to VDD + 0.3	V
Operating Temperature Range	T _{opr}	-20 to +85	°C
Storage Temperature Range	T _{stg}	-55 to +125	°C
Power Dissipation	Pd	0.55 ^(Note 1)	W
Maximum Junction Temperature	T _{jmax}	125	°C

(Note 1) Derate by 5.5mW/°C when operating above Ta=25°C (mounted in 1-layer 74.2×74.2×1.6mm board with 10.22mm² surface capper area)

 P_d of IC is 0.27W and derate by 2.7mW/°C when operating above Ta=25°C. **Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Condition

 $(Ta = -20 \text{ to } +85^{\circ}\text{C})$

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VDD	2.7 to 5.5	V

Electrical Characteristics

(Ta = 25°C, VDD = 3.3V, VSS = 0V)

Parameter	Symbol	Min	Тур	Max	Unit	Conditions
Input High Voltage	VIH	VDD x 0.7	-	VDD + 0.3	V	
Input Low Voltage	VIL	VSS - 0.3	-	VDD x 0.3	V	
Output High Voltage	V _{OH}	VDD - 0.5	-	VDD	V	I _{OH} = -4mA
Output Low Voltage	Vol	VSS	-	VSS + 0.5	V	$I_{OL} = +4mA$
OSC Frequency 1	f _{OSC1}	45	50	55	MHz	
OSC Frequency 2	fosc2	51.2	64	76.8	kHz	
DVDD Voltage	V _{DVDD}	1.35	1.50	1.65	V	
AVDD Voltage	V _{AVDD}	2.40	2.50	2.60	V	

Host Interface

BU21077MUV has 2-wire serial bus interface. It is compatible with I2C protocol and BU21077MUV is a slave device. Slave address of BU21077MUV is 5Ch (Shown 7-bit). And it supports Standard-mode (100 KHz) and Fast-mode (400 kHz). It has sequential read for reduce access time.

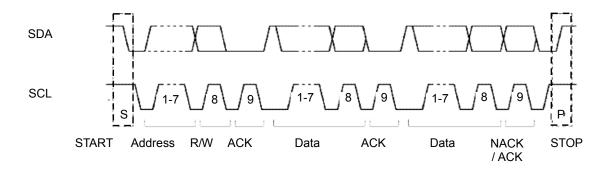


Figure 7. 2-wire Serial Bus Interface Data Format

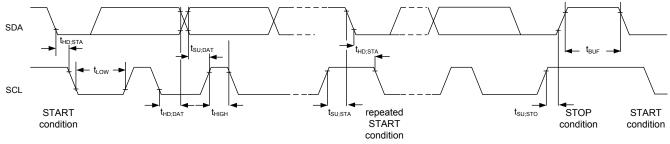


Figure 8. 2-wire Serial Bus Interface Timing Chart

Parameter	Symbol	Standa	rd-mode	Fast-	Unit	
Faiallelei	Symbol	Min	Max	Min	Max	Unit
SCL Clock Frequency	f _{SCL}	0	100	0	400	kHz
Hold Time for (Repeated) START Condition	t _{HD;STA}	4.0	-	0.6	-	μs
Low Period of SCL	t _{LOW}	4.7	-	1.3	-	μs
High Period of SCL	t _{HIGH}	4.0	-	0.6	-	μs
Data Hold Time	t _{HD;DAT}	0.1	3.45	0.1	0.9	μs
Data Setup Time	t _{SU;DAT}	0.25	-	0.1	-	μs
Setup Time for Repeated Start Condition	t _{su;sta}	4.7	-	0.6	-	μs
Setup Time for STOP Condition	t _{su;sto}	4.0	-	0.6	-	μs
Bus Free Time Between STOP and START Condition	t _{BUF}	4.7	-	1.3	-	μs

●Byte Write

S T ⊿			ave x50		ddr	ess	5	R	A C K		Reg n)	;ist	er	Ad	dre	SS		С	to	o R	eg)ata ste	er	dre			A C K	Т
R								Ť	K									K		دە n)	gist.	CI	лu	ure	55		K	P
т								Ė												,								•
	S	S	S	S	S	S	S			R	R	R	R	R	R	R	R		W	W	W	W	W	W	W	W		
	A	А	А	А	А	А	А			А	А	А	А	А	А	А	А		D	D	D	D	D	D	D	D		
	6	5	4	3	2	1	0			7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0		

SA : Slave Address
RA : Register Address
RD : Read Data
RD : Read Data WD : Write Data

Random Read

S T A	Slave Address =0x5C	W A Register Address R C (n) I K	A S Slave Address C T =0x5C K A	R A Read Data E C from Register A K (Register Address	N S A T C O
R		т	R	D =n)	КΡ
,T,		,E	T		
	S S S S S S S	RRRRRRR	R S S S S S S S	6 R R R R R R F	2
	A A A A A A A	A A A A A A A	A A A A A A A A		
	6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	0 6 5 4 3 2 1 0	0 7 6 5 4 3 2 1 0	

Sequential Read

S Slave Address T =0x5C A	W A R C I K		A C K	т	Slave Address =0x5C	Е	С	Read Data from Register (Register Address	A C K		A C K	Read Data from Register (Register Address	N S A T C O
R	Т			R		D		=n)			1	=n+x)	КΡ
T SSSSSSSSS A A A A A A A A 6 5 4 3 2 1 0		R R R R R R R R R A A A A A A A A A 7 6 5 4 3 2 1 0			S S S S S S S S A A A A A A A A 6 5 4 3 2 1 0			R R R R R R R R R D D D D D D D D D 7 6 5 4 3 2 1 0				R R R R R R R R R D D D D D D D D D 7 6 5 4 3 2 1 0	

Figure 9. 2-wire Serial Bus Protocol

Power on Sequence

The power supply pin is only VDD. AVDD and DVDD are generated by built-in LDO, these are not necessary to supply from external.

When the voltage level of RSTB change form low to High after VDD supplying, LDO is wakeup and DVDD voltage is raised. And built-in power on reset (POR) circuit release the system reset and host interface is enable After DVDD voltage reach the normal voltage range.

RSTB pin can not need to be controlled by host and connects to the VDD, because the BU21077MUV has POR circuit. If the RSTB pin is connected to the VDD, the system reset is release automatically after VDD supplying.

Recommended Value of External Capacitors

C 1	1.0uF	Decoupling capacitor for VDD
C2	1.0uF	Decoupling capacitor for DVDD
Сз	2.2uF	Decoupling capacitor for AVDD

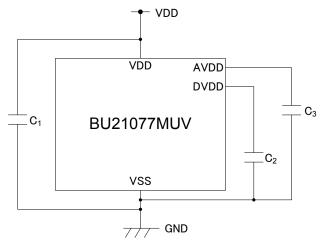


Figure 10. Arrangement of External Capacitors

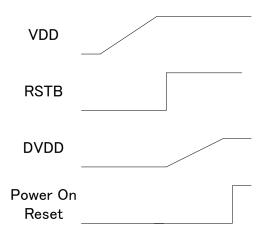


Figure 11. Power on Sequence (Controlled RSTB)

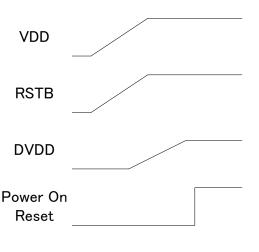


Figure 12. Power on Sequence (VDD Shorted RSTB)

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 74.2mm x 74.2mm x 1.6mm glass epoxy board with 10.22mm² copper areas. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Rush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

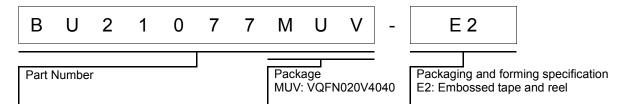
12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input terminals have voltages within the values specified in the electrical characteristics of this IC.

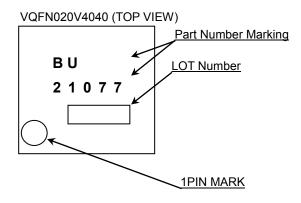
13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

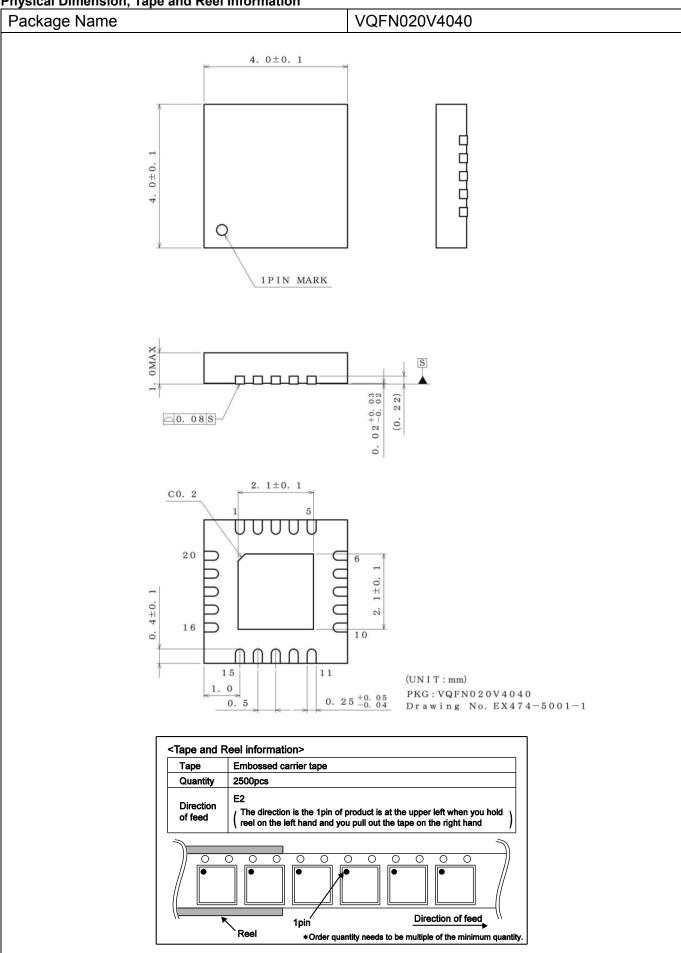
Ordering Information



Marking Diagram







Revision History

Date	Revision	Changes
29.Aug.2013	001	New Release
14.Jul.2016	002	 P3 Correct clerical error (old) MUP (new) MPU P7 Correct recommended value of decoupling capacitor for VDD (old) 0.1uF (new) 1.0uF

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- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



Тел: +7 (812) 336 43 04 (многоканальный) Email: org@lifeelectronics.ru

www.lifeelectronics.ru