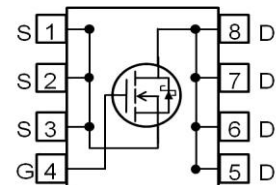


**OptiMOS™ Power-MOSFET**
**Features**

- Optimized SyncFET for high performance buck converter
- Integrated monolithic Schottky-like diode
- Very low on-resistance  $R_{DS(on)}$  @  $V_{GS}=4.5\text{ V}$
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21


**Product Summary**

$V_{DS}$	30	V
$R_{DS(on),max}$	2.8	mΩ
$I_D$	40	A
$Q_{OSS}$	17	nC
$Q_G(0V..10V)$	24	nC

**PG-TSDSON-8 (fused leads)**


Type	Package	Marking
BSZ0902NSI	PG-TSDSON-8 (fused leads)	0902NSI

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$	40	A
		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$	40	
		$V_{GS}=4.5\text{ V}, T_C=25\text{ °C}$	40	
		$V_{GS}=4.5\text{ V}, T_C=100\text{ °C}$	40	
		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=60\text{ K/W}^2)$	21	
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	160	
Avalanche current, single pulse <sup>4)</sup>	$I_{AS}$	$T_C=25\text{ °C}$	20	
Avalanche energy, single pulse	$E_{AS}$	$I_D=20\text{ A}, R_{GS}=25\text{ Ω}$	30	mJ
Gate source voltage	$V_{GS}$		±20	V

<sup>1)</sup> J-STD20 and JESD22

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	$P_{\text{tot}}$	$T_C=25\text{ °C}$	48	W
		$T_A=25\text{ °C}$ , $R_{\text{thJA}}=50\text{ K/W}^2)$	2.5	
Operating and storage temperature	$T_j, T_{\text{stg}}$		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

### Thermal characteristics

Thermal resistance, junction - case	$R_{\text{thJC}}$		-	-	2.6	K/W
		top	-	-	20	
Device on PCB	$R_{\text{thJA}}$	$6\text{ cm}^2\text{ cooling area}^2)$	-	-	50	

Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified

### Static characteristics

Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{ V}, I_{\text{D}}=10\text{ mA}$	30	-	-	V
Breakdown voltage temperature coefficient	$dV_{(\text{BR})\text{DSS}}/dT_j$	$I_{\text{D}}=10\text{ mA}$ , referenced to $25\text{ °C}$	-	15	-	mV/K
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.2	-	2	V
Zero gate voltage drain current	$I_{\text{DSS}}$	$V_{\text{DS}}=24\text{ V}, V_{\text{GS}}=0\text{ V}$	-	-	0.5	mA
		$V_{\text{DS}}=24\text{ V}, V_{\text{GS}}=0\text{ V}$ , $T_j=125\text{ °C}$	-	2	-	
Gate-source leakage current	$I_{\text{GSS}}$	$V_{\text{GS}}=20\text{ V}, V_{\text{DS}}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}}=4.5\text{ V}, I_{\text{D}}=30\text{ A}$	-	3.0	3.7	mΩ
		$V_{\text{GS}}=10\text{ V}, I_{\text{D}}=30\text{ A}$	-	2.3	2.8	
Gate resistance	$R_{\text{G}}$		0.5	0.9	1.8	Ω
Transconductance	$g_{\text{fs}}$	$ V_{\text{DS}} >2 I_{\text{D}} R_{\text{DS(on)max}}$ , $I_{\text{D}}=30\text{ A}$	50	100	-	S

<sup>3)</sup> See figure 3 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V}, f=1\text{ MHz}$	-	1500	1995	pF
Output capacitance	$C_{oss}$		-	630	838	
Reverse transfer capacitance	$C_{rss}$		-	88	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V}, I_D=30\text{ A}, R_{G,ext}=1.6\ \Omega$	-	3.9	-	ns
Rise time	$t_r$		-	5.4	-	
Turn-off delay time	$t_{d(off)}$		-	20	-	
Fall time	$t_f$		-	3.8	-	

**Gate Charge Characteristics<sup>5)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=15\text{ V}, I_D=30\text{ A}, V_{GS}=0\text{ to }4.5\text{ V}$	-	4.0	5.3	nC
Gate charge at threshold	$Q_{g(th)}$		-	2.4	-	
Gate to drain charge	$Q_{gd}$		-	4.0	5.2	
Switching charge	$Q_{sw}$		-	5.6	-	
Gate charge total	$Q_g$		-	12.2	16	
Gate plateau voltage	$V_{plateau}$		-	2.6	-	V
Gate charge total	$Q_g$	$V_{DD}=15\text{ V}, I_D=30\text{ A}, V_{GS}=0\text{ to }10\text{ V}$	-	24	32	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V}, V_{GS}=0\text{ to }4.5\text{ V}$	-	9.8	-	
Output charge	$Q_{oss}$	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	17	23	

**Reverse Diode**

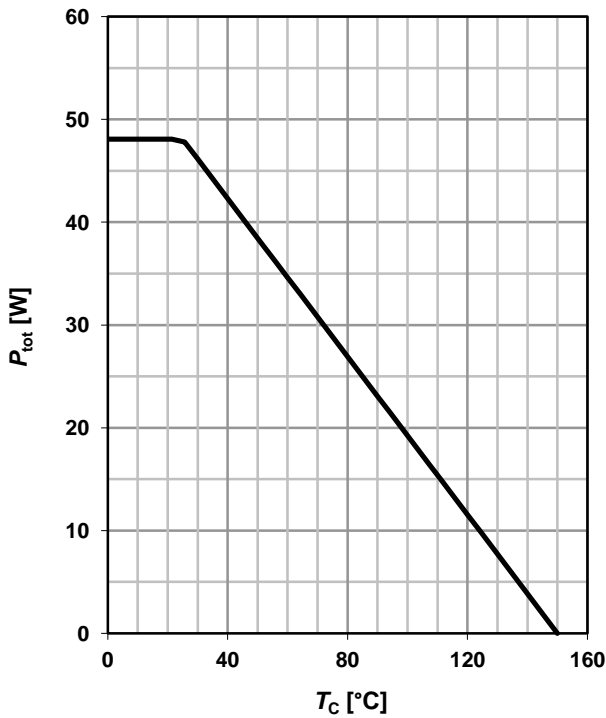
Diode continuous forward current	$I_S$	$T_C=25\text{ °C}$	-	-	40	A
Diode pulse current	$I_{S,pulse}$		-	-	160	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=4\text{ A}, T_j=25\text{ °C}$	-	0.54	0.7	V
Reverse recovery charge	$Q_{rr}$	$V_R=15\text{ V}, I_F=4\text{ A}, di_F/dt=400\text{ A}/\mu\text{s}$	-	5	-	nC

<sup>4)</sup> See figure 13 for more detailed information

<sup>5)</sup> See figure 16 for gate charge parameter definition

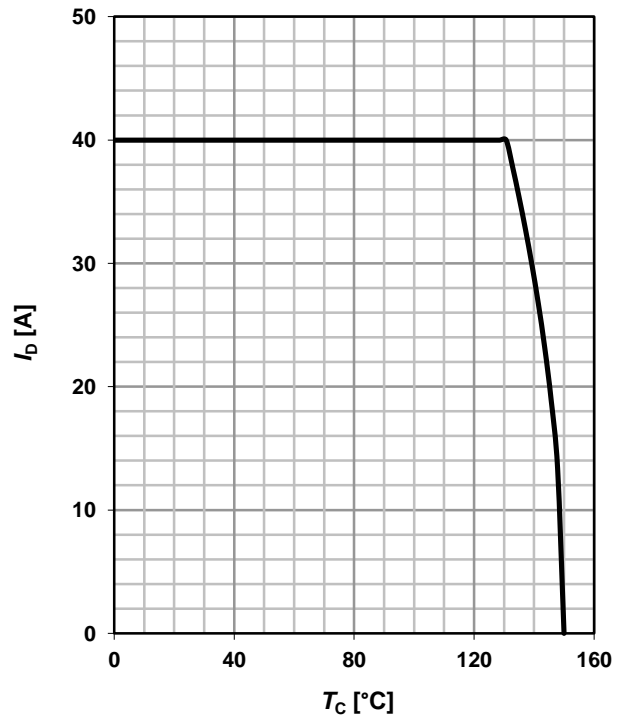
### 1 Power dissipation

$$P_{tot}=f(T_C)$$



### 2 Drain current

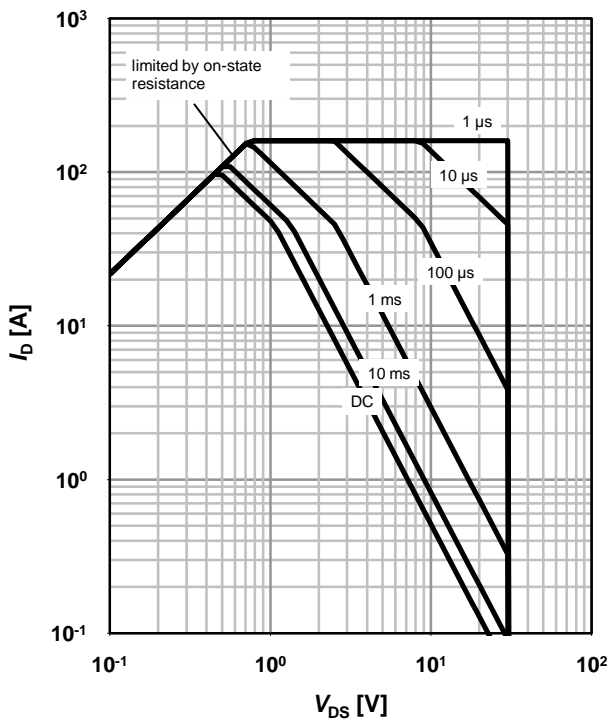
$$I_D=f(T_C); V_{GS} \geq 10 \text{ V}$$



### 3 Safe operating area

$$I_D=f(V_{DS}); T_C=25 \text{ °C}; D=0$$

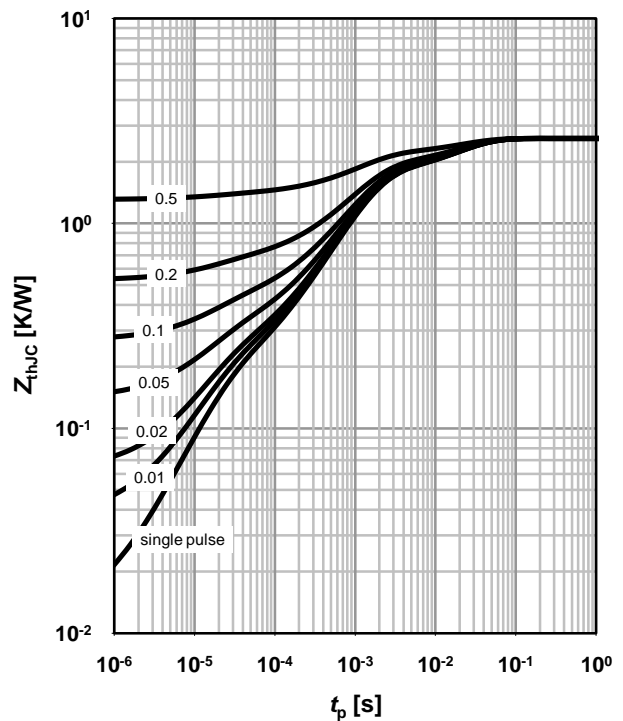
parameter:  $t_p$



### 4 Max. transient thermal impedance

$$Z_{thJC}=f(t_p)$$

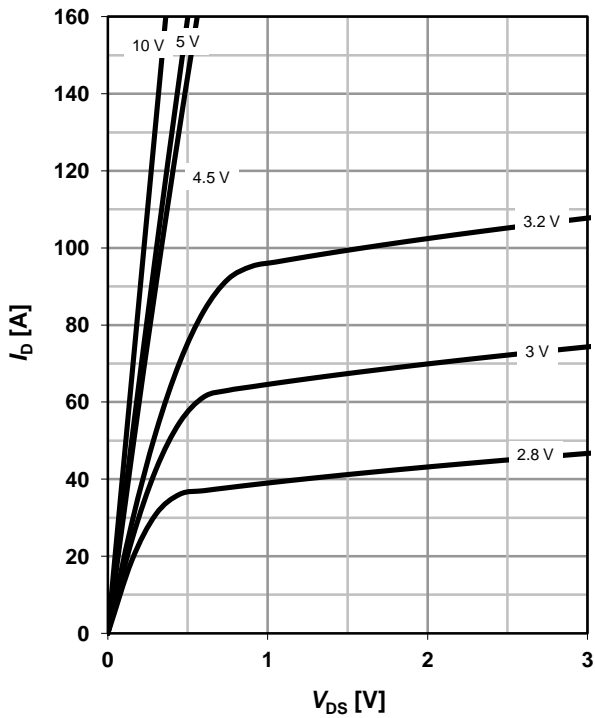
parameter:  $D=t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

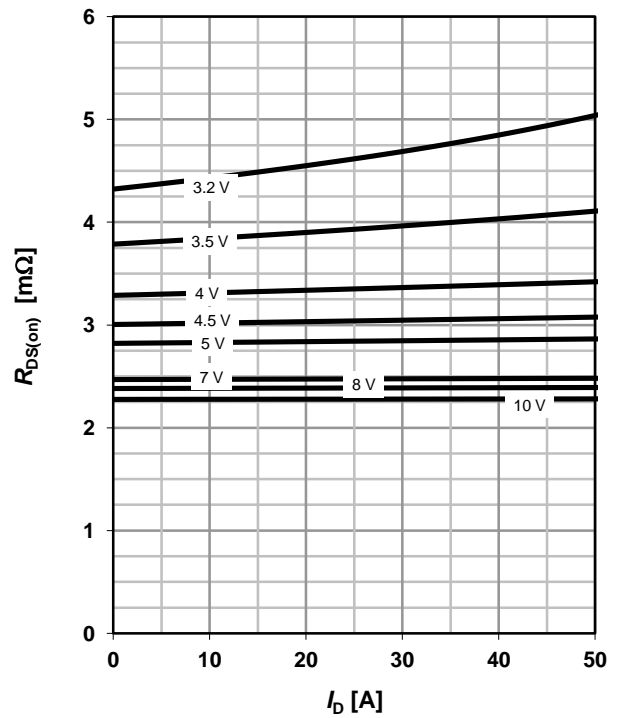
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

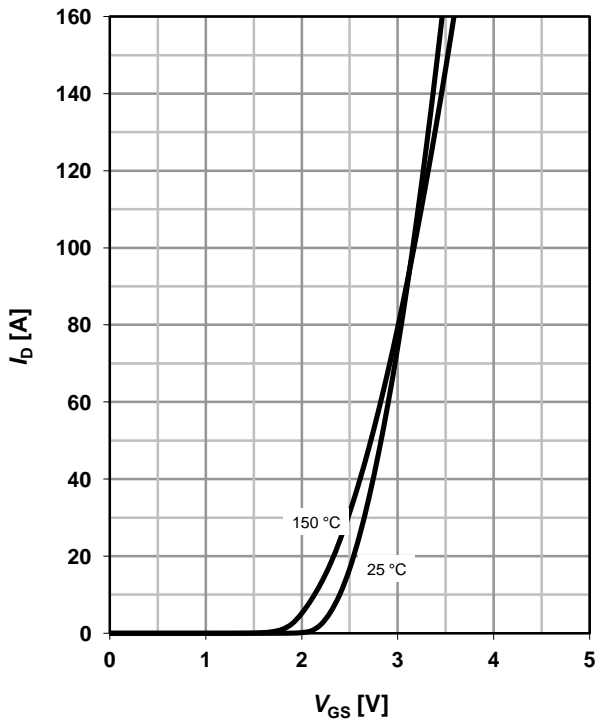
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

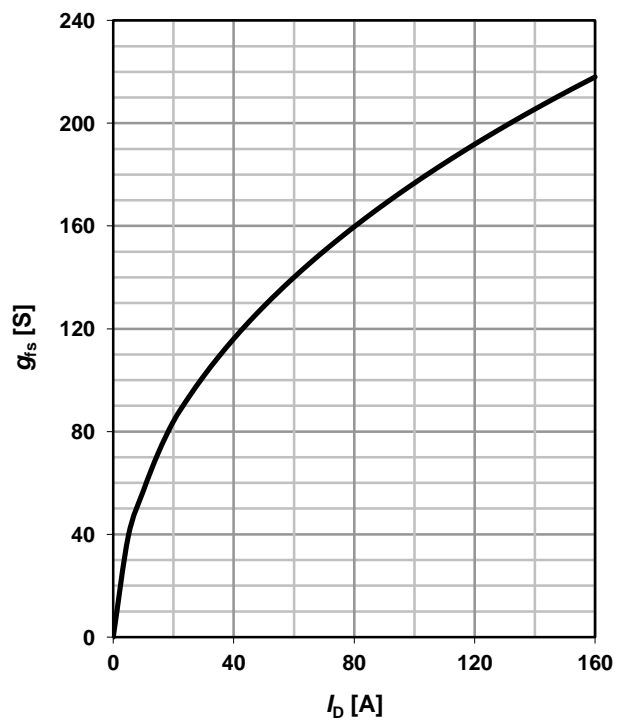
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter:  $T_j$



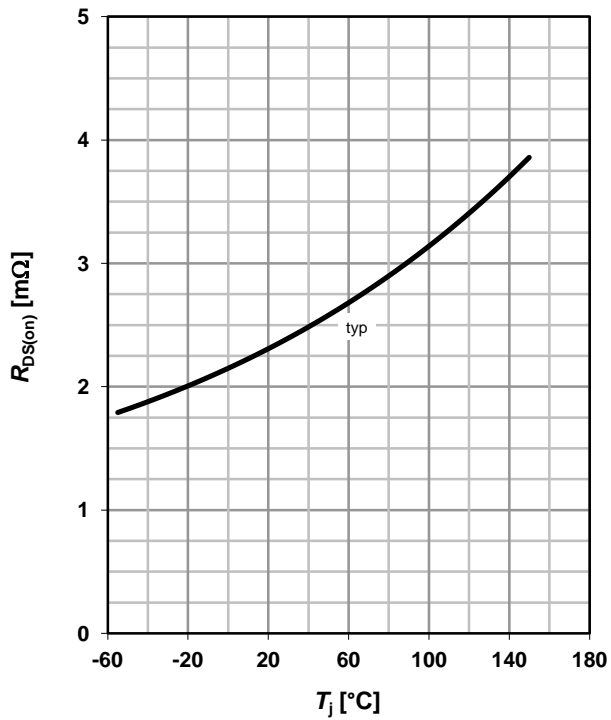
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ °C}$



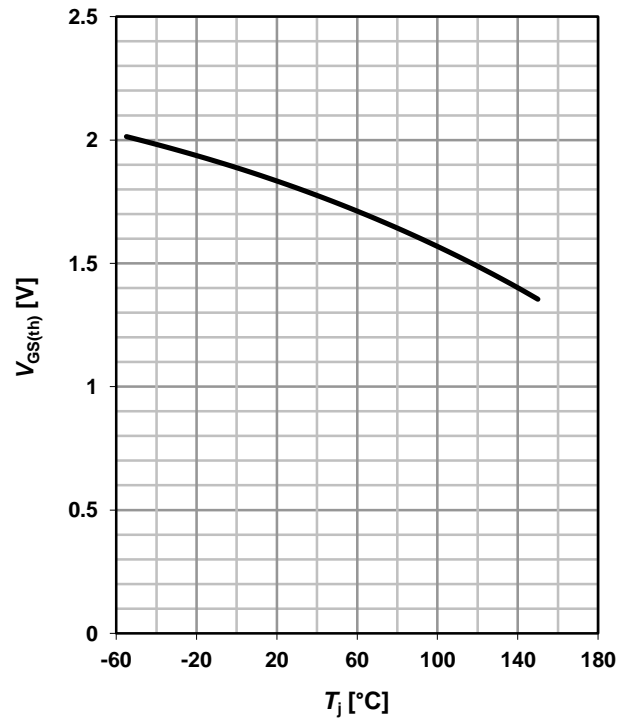
**9 Drain-source on-state resistance**

$R_{DS(on)}=f(T_j); I_D=30\text{ A}; V_{GS}=10\text{ V}$



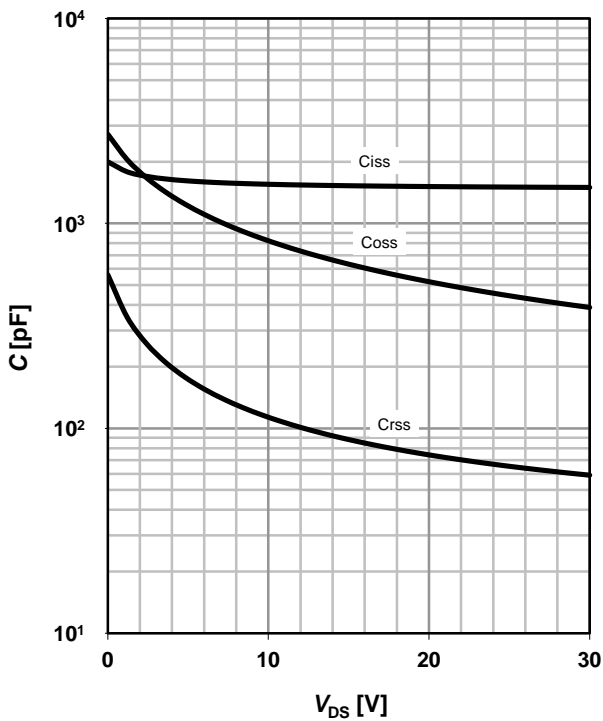
**10 Typ. gate threshold voltage**

$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}; I_D=10\text{ mA}$



**11 Typ. capacitances**

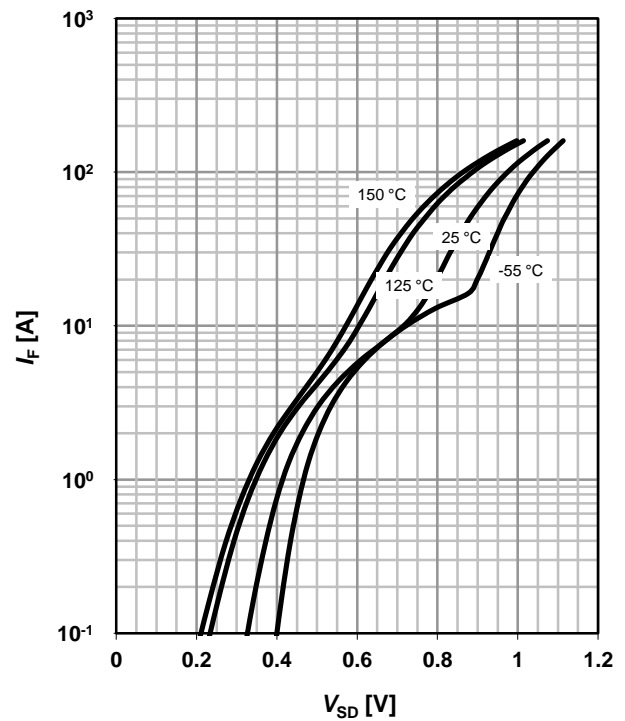
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$



**12 Forward characteristics of reverse diode**

$I_F=f(V_{SD})$

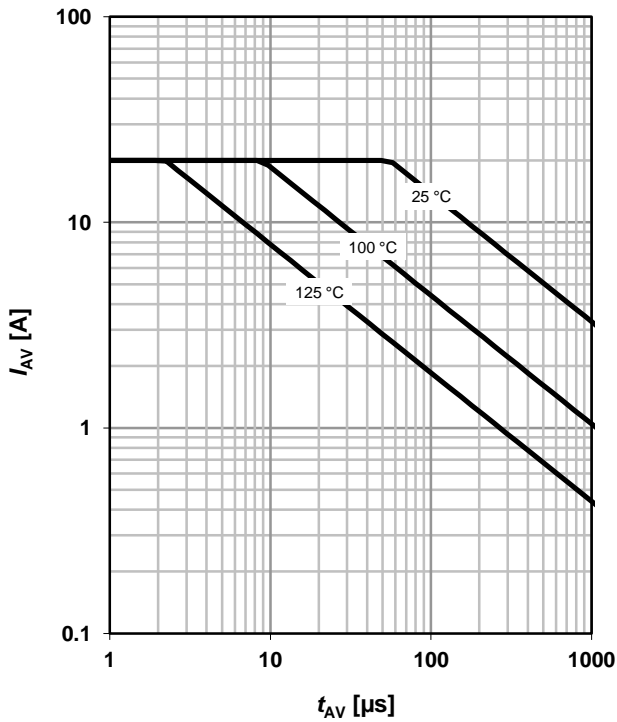
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

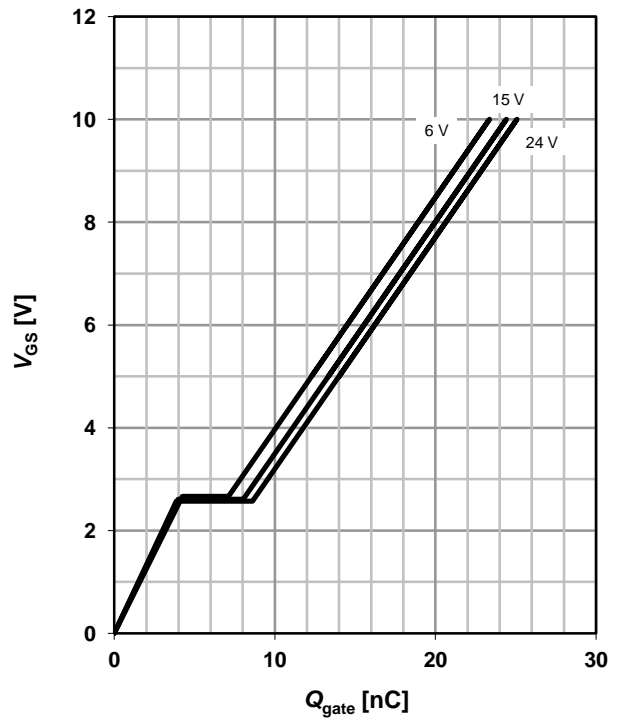
parameter:  $T_{j(\text{start})}$



**14 Typ. gate charge**

$V_{GS}=f(Q_{\text{gate}}); I_D=30 \text{ A pulsed}$

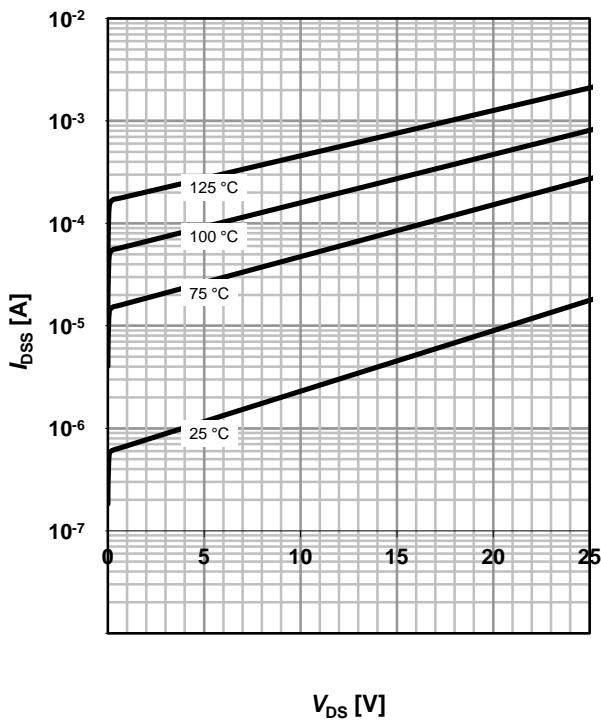
parameter:  $V_{DD}$



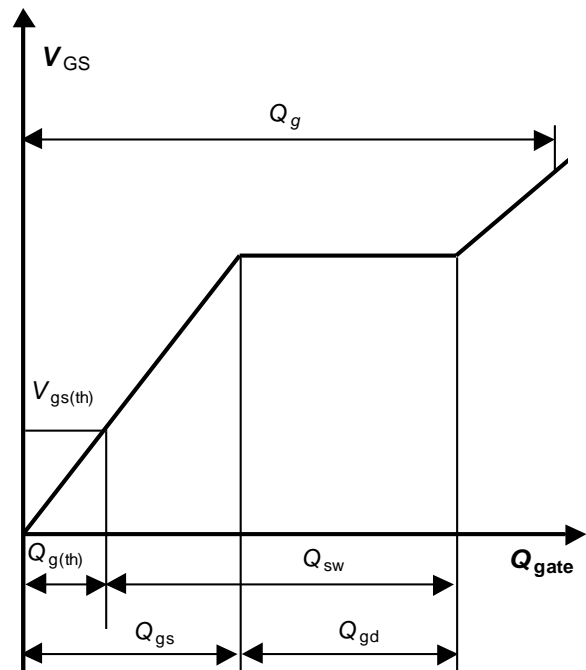
**15 Drain-source leakage current**

$I_{DSS}=f(V_{DS}); V_{GS}=0 \text{ V}$

parameter:  $T_j$



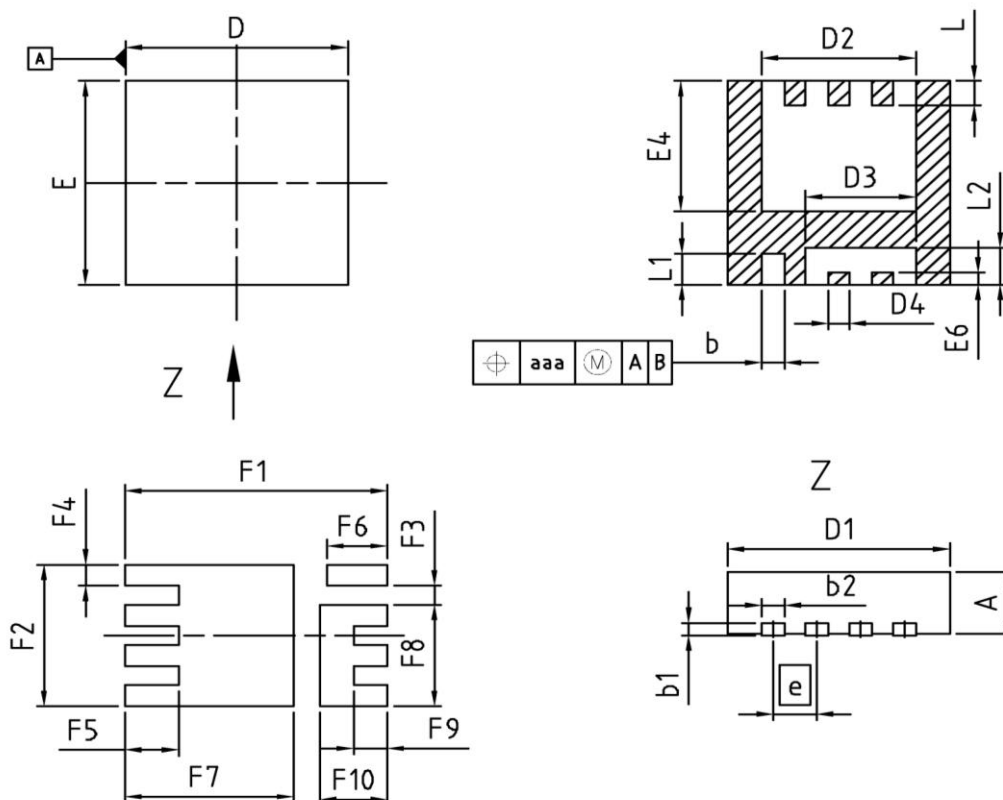
**16 Gate charge waveforms**



Package Outline

PG-TSDSON-8 (fused leads)

PG-TSDSON-8 (fused leads): Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.24	0.44	0.009	0.017
b1	0.10	0.30	0.004	0.012
b2	0.24	0.44	0.009	0.017
D=D1	3.20	3.40	0.126	0.134
D2	2.19	2.39	0.086	0.094
D3	1.54	1.74	0.061	0.069
D4	0.21	0.41	0.008	0.016
E	3.20	3.40	0.126	0.134
E4	2.01	2.21	0.079	0.087
E6	0.10	0.30	0.004	0.012
e	0.65 (BSC)		0.026 (BSC)	
N	8		8	
L	0.30	0.51	0.012	0.020
L1	0.40	0.60	0.016	0.024
L2	0.50	0.70	0.020	0.028
aaa	0.25		0.010	
F1	3.90		0.154	
F2	2.29		0.090	
F3	0.31		0.012	
F4	0.34		0.013	
F5	0.80		0.031	
F6	0.90		0.035	
F7	2.51		0.099	
F8	1.64		0.065	
F9	0.50		0.020	
F10	1.00		0.039	

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