



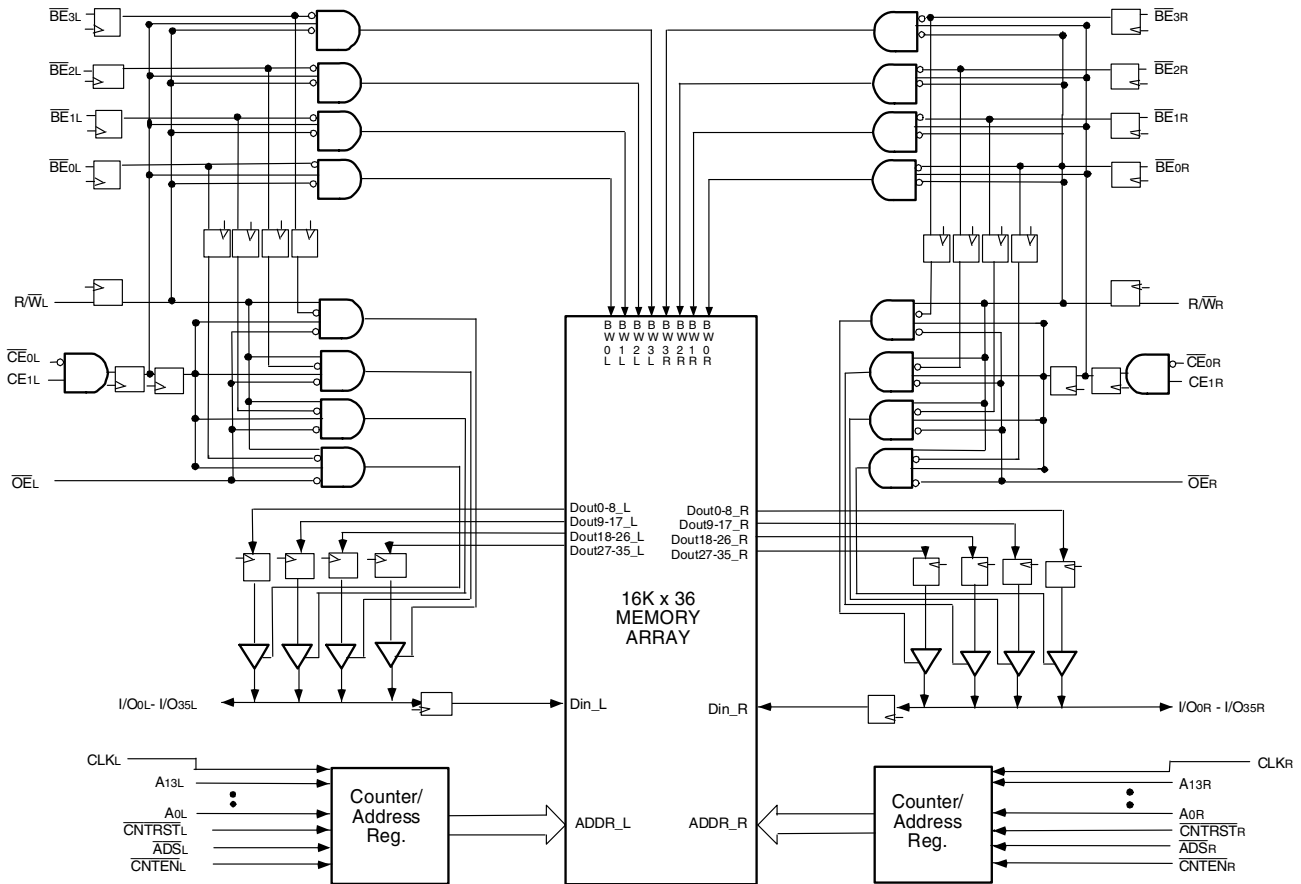
HIGH-SPEED 3.3V 16K x 36 SYNCHRONOUS PIPELINED DUAL-PORT STATIC RAM WITH 3.3V OR 2.5V INTERFACE

70V3569S

Features:

- ◆ True Dual-Port memory cells which allow simultaneous access of the same memory location
- ◆ High-speed clock to data access
 - Commercial: 4.2/5/6ns (max.)
 - Industrial: 5ns (max)
- ◆ Pipelined output mode
- ◆ Counter enable and reset features
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Full synchronous operation on both ports
 - 7.5ns cycle time, 133MHz operation (9.6 Gbps bandwidth)
 - Fast 4.2ns clock to data out
 - 1.8ns setup to clock and 0.7ns hold on all control, data, and address inputs @ 133MHz
- Data input, address, byte enable and control registers
- Self-timed write allows fast cycle time
- ◆ Separate byte controls for multiplexed bus and bus matching compatibility
- ◆ LVTTTL-compatible, single 3.3V ($\pm 150\text{mV}$) power supply for core
- ◆ LVTTTL-compatible, selectable 3.3V ($\pm 150\text{mV}$)/2.5V ($\pm 125\text{mV}$) power supply for I/Os and control signals on each port
- ◆ Industrial temperature range (-40°C to +85°C) is available for selected speeds
- ◆ Available in a 208-pin Plastic Quad Flatpack (PQFP), 208-ball fine-pitch Ball Grid Array, and 256-pin Ball Grid Array
- ◆ Green parts available, see ordering instructions

Functional Block Diagram



4831 tbi 01

AUGUST 2019

Description:

The IDT70V3569 is a high-speed 16K x 36 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70V3569 has been optimized for applications having unidirectional or bidirectional data flow

in bursts. An automatic power down feature, controlled by \overline{CE}_0 and CE_1 , permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70V3569 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (VDD) remains at 3.3V.

Pin Configuration^(1,2,3,4)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17
IO19L	IO18L	VSS	NC	NC	NC	A12L	A8L	\overline{BE}_{1L}	VDD	CLKL	\overline{CNTENL}	A4L	A0L	OPTL	IO17L	VSS
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17
IO20R	VSS	IO18R	VSS	NC	A13L	A9L	\overline{BE}_{2L}	\overline{CE}_{0L}	VSS	\overline{ADSL}	A5L	A1L	VSS	VDDQR	IO16L	IO15R
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16	C17
VDDQL	IO19R	VDDQR	VDD	NC	NC	A10L	\overline{BE}_{3L}	CE_{1L}	VSS	R/WL	A6L	A2L	VDD	IO16R	IO15L	VSS
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17
IO22L	VSS	IO21L	IO20L	NC	A11L	A7L	\overline{BE}_{0L}	VDD	\overline{OE}_L	$\overline{CNTRSTL}$	A3L	VDD	IO17R	VDDQL	IO14L	IO14R
E1	E2	E3	E4	<p style="text-align: center;">70V3569 BF208⁽⁵⁾ BFG208⁽⁵⁾ 208-Pin fpBGA Top View⁽⁶⁾</p>								E14	E15	E16	E17	
IO23L	IO22R	VDDQR	IO21R									IO12L	IO13R	VSS	IO13L	
F1	F2	F3	F4									F14	F15	F16	F17	
VDDQL	IO23R	IO24L	VSS									VSS	IO12R	IO11L	VDDQR	
G1	G2	G3	G4									G14	G15	G16	G17	
IO26L	VSS	IO25L	IO24R									IO9L	VDDQL	IO10L	IO11R	
H1	H2	H3	H4									H14	H15	H16	H17	
VDD	IO26R	VDDQR	IO25R									VDD	IO9R	VSS	IO10R	
J1	J2	J3	J4									J14	J15	J16	J17	
VDDQ	VDD	VSS	VSS									VSS	VDD	VSS	VDDQR	
K1	K2	K3	K4	K14	K15	K16	K17									
IO28R	VSS	IO27R	VSS	IO7R	VDDQ	IO8R	VSS									
L1	L2	L3	L4	L14	L15	L16	L17									
IO29R	IO28L	VDDQR	IO27L	IO6R	IO7L	VSS	IO8L									
M1	M2	M3	M4	M14	M15	M16	M17									
VDDQL	IO29L	IO30R	VSS	VSS	IO6L	IO5R	VDDQR									
N1	N2	N3	N4	N14	N15	N16	N17									
IO31L	VSS	IO31R	IO30L	IO3R	VDDQL	IO4R	IO5L									
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16	P17
IO32R	IO32L	VDDQR	IO35R	NC	NC	A12R	A8R	\overline{BE}_{1R}	VDD	CLKR	\overline{CNTENR}	A4R	IO2L	IO3L	VSS	IO4L
R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	R17
VSS	IO33L	IO34R	NC	NC	A13R	A9R	\overline{BE}_{2R}	\overline{CE}_{0R}	VSS	\overline{ADSR}	A5R	A1R	VSS	VDDQL	IO1R	VDDQR
T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	T17
IO33R	IO34L	VDDQL	VSS	NC	NC	A10R	\overline{BE}_{3R}	CE_{1R}	VSS	R/WR	A6R	A2R	VSS	IO0R	VSS	IO2R
U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17
VSS	IO35L	VDD	NC	NC	A11R	A7R	\overline{BE}_{0R}	VDD	\overline{OE}_R	$\overline{CNTRSTR}$	A3R	A0R	VDD	OPTR	IO0L	IO1L

NOTES:

- All VDD pins must be connected to 3.3V power supply.
- All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
- All VSS pins must be connected to ground supply.
- Package body is approximately 15mm x 15mm x 1.4mm, with 0.8mm ball pitch.
- This package code is used to reference the package diagram.
- This text does not indicate orientation of the actual part-marking.

4831 drw 02c

Pin Configuration^(1,2,3,4) (con't.)70V3569
BC256⁽⁵⁾256-Pin BGA
Top View⁽⁶⁾

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16
NC	NC	NC	NC	NC	A11L	A8L	\overline{BE}_{2L}	CE1L	\overline{OE}_{L}	CNTENL	A5L	A2L	A0L	NC	NC
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16
I/O18L	NC	NC	NC	NC	A12L	A9L	\overline{BE}_{3L}	\overline{CE}_{0L}	R/WL	CNTRST	A4L	A1L	VDD	I/O17L	NC
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16
I/O18R	I/O19L	VSS	NC	A13L	A10L	A7L	\overline{BE}_{1L}	\overline{BE}_{0L}	CLKL	\overline{ADS}_{L}	A6L	A3L	OPTL	I/O17R	I/O16L
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16
I/O20R	I/O19R	I/O20L	VDD	VDDQL	VDDQL	VDDQR	VDDQR	VDDQL	VDDQL	VDDQR	VDDQR	VDD	I/O15R	I/O15L	I/O16R
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	E16
I/O21R	I/O21L	I/O22L	VDDQL	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDDQR	I/O13L	I/O14L	I/O14R
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16
I/O23L	I/O22R	I/O23R	VDDQL	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDQR	I/O12R	I/O13R	I/O12L
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11	G12	G13	G14	G15	G16
I/O24R	I/O24L	I/O25L	VDDQR	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQL	I/O10L	I/O11L	I/O11R
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10	H11	H12	H13	H14	H15	H16
I/O26L	I/O25R	I/O26R	VDDQR	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQL	I/O9R	I/O9L	I/O10R
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
I/O27L	I/O28R	I/O27R	VDDQL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQR	I/O8R	I/O7R	I/O8L
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16
I/O29R	I/O29L	I/O28L	VDDQL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQR	I/O6R	I/O6L	I/O7L
L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L15	L16
I/O30L	I/O31R	I/O30R	VDDQR	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDQL	I/O5L	I/O4R	I/O5R
M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13	M14	M15	M16
I/O32R	I/O32L	I/O31L	VDDQR	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDDQL	I/O3R	I/O3L	I/O4L
N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16
I/O33L	I/O34R	I/O33R	VDD	VDDQR	VDDQR	VDDQL	VDDQL	VDDQR	VDDQR	VDDQL	VDDQL	VDD	I/O2L	I/O1R	I/O2R
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16
I/O35R	I/O34L	NC	NC	A13R	A10R	A7R	\overline{BE}_{1R}	\overline{BE}_{0R}	CLKR	\overline{ADS}_{R}	A6R	A3R	I/O0L	I/O0R	I/O1L
R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16
I/O35L	NC	NC	NC	NC	A12R	A9R	\overline{BE}_{3R}	\overline{CE}_{0R}	R/WR	CNTRSTR	A4R	A1R	OPTR	NC	NC
T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16
NC	NC	NC	NC	NC	A11R	A8R	\overline{BE}_{2R}	CE1R	\overline{OE}_{R}	CNTENR	A5R	A2R	A0R	NC	NC

4831 drw 02d

NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration^(1,2,3,4) (con't.)



NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 28mm x 28mm x 3.5mm.
5. This package code is used to reference the package diagram.

Pin Names

Left Port	Right Port	Names
\overline{CE}_{0L} , CE_{1L}	\overline{CE}_{0R} , CE_{1R}	Chip Enables
R/\overline{W}_L	R/\overline{W}_R	Read/Write Enable
\overline{OE}_L	\overline{OE}_R	Output Enable
A _{0L} - A _{13L}	A _{0R} - A _{13R}	Address
I/O _{0L} - I/O _{35L}	I/O _{0R} - I/O _{35R}	Data Input/Output
CLK _L	CLK _R	Clock
\overline{ADS}_L	\overline{ADS}_R	Address Strobe Enable
\overline{CNTEN}_L	\overline{CNTEN}_R	Counter Enable
\overline{CNTRST}_L	\overline{CNTRST}_R	Counter Reset
\overline{BE}_{0L} - \overline{BE}_{3L}	\overline{BE}_{0R} - \overline{BE}_{3R}	Byte Enables (9-bit bytes)
V _{DD0L}	V _{DD0R}	Power (I/O Bus) (3.3V or 2.5V) ⁽¹⁾
OPT _L	OPT _R	Option for selection V _{DD0x} ^(1,2)
V _{DD}		Power (3.3V) ⁽¹⁾
V _{SS}		Ground (0V)

NOTES:

- V_{DD}, OPT_x, and V_{DD0x} must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
- OPT_x selects the operating voltage levels for the I/Os and controls on that port. If OPT_x is set to VIH (3.3V), then that port's I/Os and controls will operate at 3.3V levels and V_{DD0x} must be supplied at 3.3V. If OPT_x is set to VIL (0V), then that port's I/Os and controls will operate at 2.5V levels and V_{DD0x} must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.

4831 tbl 01

Truth Table I—Read/Write and Enable Control^(1,2,3,4)

OE	CLK	\overline{CE}_0	CE ₁	\overline{BE}_3	\overline{BE}_2	\overline{BE}_1	\overline{BE}_0	R/ \overline{W}	Byte 3 I/O ₂₇₋₃₅	Byte 2 I/O ₁₈₋₂₆	Byte 1 I/O ₉₋₁₇	Byte 0 I/O ₀₋₈	MODE
X	↑	H	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected—Power Down
X	↑	X	L	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Deselected—Power Down
X	↑	L	H	H	H	H	H	X	High-Z	High-Z	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	H	H	L	L	High-Z	High-Z	High-Z	D _{IN}	Write to Byte 0 Only
X	↑	L	H	H	L	H	H	L	High-Z	High-Z	D _{IN}	High-Z	Write to Byte 1 Only
X	↑	L	H	H	L	H	H	L	High-Z	D _{IN}	High-Z	High-Z	Write to Byte 2 Only
X	↑	L	H	L	H	H	H	L	D _{IN}	High-Z	High-Z	High-Z	Write to Byte 3 Only
X	↑	L	H	H	H	L	L	L	High-Z	High-Z	D _{IN}	D _{IN}	Write to Lower 2 Bytes Only
X	↑	L	H	L	L	H	H	L	D _{IN}	D _{IN}	High-Z	High-Z	Write to Upper 2 bytes Only
X	↑	L	H	L	L	L	L	L	D _{IN}	D _{IN}	D _{IN}	D _{IN}	Write to All Bytes
L	↑	L	H	H	H	H	L	H	High-Z	High-Z	High-Z	D _{OUT}	Read Byte 0 Only
L	↑	L	H	H	H	L	H	H	High-Z	High-Z	D _{OUT}	High-Z	Read Byte 1 Only
L	↑	L	H	H	L	H	H	H	High-Z	D _{OUT}	High-Z	High-Z	Read Byte 2 Only
L	↑	L	H	L	H	H	H	H	D _{OUT}	High-Z	High-Z	High-Z	Read Byte 3 Only
L	↑	L	H	H	H	L	L	H	High-Z	High-Z	D _{OUT}	D _{OUT}	Read Lower 2 Bytes Only
L	↑	L	H	L	L	H	H	H	D _{OUT}	D _{OUT}	High-Z	High-Z	Read Upper 2 Bytes Only
L	↑	L	H	L	L	L	L	H	D _{OUT}	D _{OUT}	D _{OUT}	D _{OUT}	Read All Bytes
H	↑	L	H	L	L	L	L	X	High-Z	High-Z	High-Z	High-Z	Outputs Disabled

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- \overline{ADS} , \overline{CNTEN} , \overline{CNTRST} = X.
- OE is an asynchronous input signal.
- It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

4831 tbl 02

Truth Table II—Address Counter Control^(1,2)

Address	Previous Address	Addr Used	CLK ⁽⁶⁾	$\overline{\text{ADS}}$	$\overline{\text{CNTEN}}$	$\overline{\text{CNRST}}$	I/O ⁽³⁾	MODE
X	X	0	↑	X	X	L ⁽⁴⁾	D _{IO} (0)	Counter Reset to Address 0
An	X	An	↑	L ⁽⁴⁾	X	H	D _{IO} (n)	External Address Used
An	Ap	Ap	↑	H	H	H	D _{IO} (p)	External Address Blocked—Counter disabled (Ap reused)
X	Ap	Ap + 1	↑	H	L ⁽⁵⁾	H	D _{IO} (p+1)	Counter Enabled—Internal Address generation

4831 tbl 03

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- Read and write operations are controlled by the appropriate setting of R $\overline{\text{W}}$, $\overline{\text{CE}}_0$, CE₁, $\overline{\text{BE}}_n$ and $\overline{\text{OE}}$.
- Outputs are in Pipelined mode: the data out will be delayed by one cycle.
- $\overline{\text{ADS}}$ and $\overline{\text{CNRST}}$ are independent of all other memory control signals including $\overline{\text{CE}}_0$, CE₁ and $\overline{\text{BE}}_n$.
- The address counter advances if $\overline{\text{CNTEN}} = \text{V}_{\text{IL}}$ on the rising edge of CLK, regardless of all other memory control signals including $\overline{\text{CE}}_0$, CE₁, $\overline{\text{BE}}_n$.

Recommended Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature	GND	V _{DD}
Commercial	0°C to +70°C	0V	3.3V ± 150mV
Industrial	-40°C to +85°C	0V	3.3V ± 150mV

4831 tbl 04

NOTES:

- Industrial temperature: for specific speeds, packages and powers contact your sales office.

Recommended DC Operating Conditions with V_{DDQ} at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V _{DDQ}	I/O Supply Voltage ⁽³⁾	2.375	2.5	2.625	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage ⁽³⁾ (Address & Control Inputs)	1.7	—	V _{DDQ} + 125mV ⁽²⁾	V
V _{IH}	Input High Voltage - I/O ⁽³⁾	1.7	—	V _{DDQ} + 125mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.7	V

4831 tbl 05a

NOTES:

- V_{IL} ≥ -1.5V for pulse width less than 10 ns.
- V_{TERM} must not exceed V_{DDQ} + 125mV.
- To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IL} (0V), and V_{DDQX} for that port must be supplied as indicated above.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	50	mA

4831 tbl 06

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{DD} + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ V_{DD} + 150mV.

Recommended DC Operating Conditions with V_{DDQ} at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V _{DDQ}	I/O Supply Voltage ⁽³⁾	3.15	3.3	3.45	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage (Address & Control Inputs) ⁽³⁾	2.0	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IH}	Input High Voltage - I/O ⁽³⁾	2.0	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V

4831 tbl 05b

NOTES:

- V_{IL} ≥ -1.5V for pulse width less than 10 ns.
- V_{TERM} must not exceed V_{DDQ} + 150mV.
- To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IH} (3.3V), and V_{DDQX} for that port must be supplied as indicated above.

Capacitance⁽¹⁾

(TA = +25°C, F = 1.0MHz) PQFP ONLY

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	8	pF
C _{OUT} ⁽³⁾	Output Capacitance	V _{OUT} = 3dV	10.5	pF

4831 tbl 07

NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C_{OUT} also references C_{IO}.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Conditions	70V3569S		Unit
			Min.	Max.	
I _L	Input Leakage Current ⁽¹⁾	V _{DDQ} = Max., V _{IN} = 0V to V _{DDQ}	—	10	μA
I _O	Output Leakage Current	$\overline{CE}_0 = V_{IH}$ or $CE_1 = V_{IL}$, V _{OUT} = 0V to V _{DDQ}	—	10	μA
V _{OL} (3.3V)	Output Low Voltage ⁽²⁾	I _{OL} = +4mA, V _{DDQ} = Min.	—	0.4	V
V _{OH} (3.3V)	Output High Voltage ⁽²⁾	I _{OH} = -4mA, V _{DDQ} = Min.	2.4	—	V
V _{OL} (2.5V)	Output Low Voltage ⁽²⁾	I _{OL} = +2mA, V _{DDQ} = Min.	—	0.4	V
V _{OH} (2.5V)	Output High Voltage ⁽²⁾	I _{OH} = -2mA, V _{DDQ} = Min.	2.0	—	V

4831 tbl 08

NOTE:

- At V_{DD} ≤ -2.0V input leakages are undefined.
- V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to p.4 for details.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽³⁾ ($V_{DD} = 3.3V \pm 150mV$)

Symbol	Parameter	Test Condition	Version	70V3569S4 Com'l Only		70V3569S5 Com'l & Ind		70V3569S6 Com'l Only		Unit	
				Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.		
IDD	Dynamic Operating Current (Both Ports Active)	\overline{CE}_L and $\overline{CE}_R = V_{IL}$, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	375	460	285	360	245	310	mA
			IND	S	—	—	285	415	245	360	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	S	145	190	105	145	95	125	mA
			IND	S	—	—	105	175	95	150	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^{*A} = V_{IL}$ and $\overline{CE}^{*B} = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	265	325	190	260	175	225	mA
			IND	S	—	—	190	300	175	260	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{DDQ} - 0.2V$, $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(2)}$	COM'L	S	6	15	6	15	6	15	mA
			IND	S	—	—	6	30	6	30	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^{*A} \leq 0.2V$ and $\overline{CE}^{*B} \geq V_{DDQ} - 0.2V^{(5)}$ $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	265	325	180	260	170	225	mA
			IND	S	—	—	180	300	170	260	

4831 tbl 09

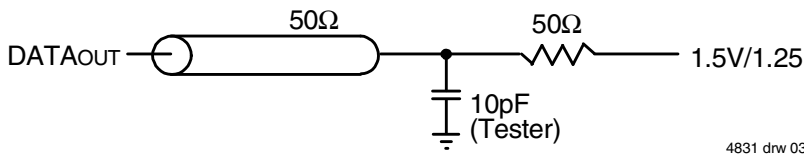
NOTES:

- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{cyc}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V$, $T_A = 25^\circ C$ for Typ, and are not production tested. $I_{DD} \text{ dc}(f=0) = 120\text{mA}$ (Typ).
- $\overline{CE}_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
 $\overline{CE}_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
 $\overline{CE}_X \leq 0.2V$ means $\overline{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{DDQ} - 0.2V$
 $\overline{CE}_X \geq V_{DDQ} - 0.2V$ means $\overline{CE}_{0X} \geq V_{DDQ} - 0.2V$ or $CE_{1X} \leq 0.2V$
"X" represents "L" for left port or "R" for right port.

AC Test Conditions

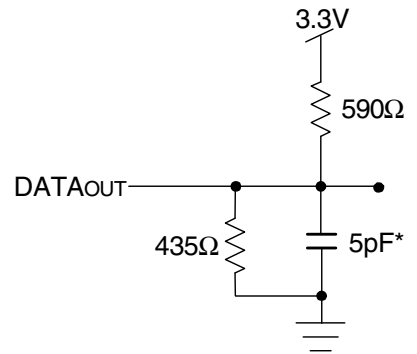
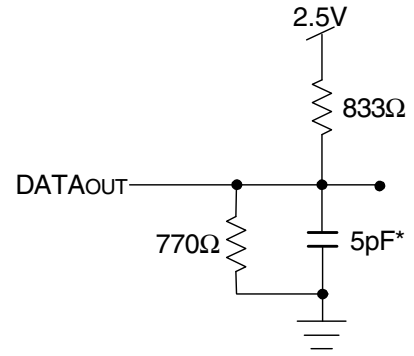
Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.35V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.35V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1, 2, and 3

4831 tbl 10



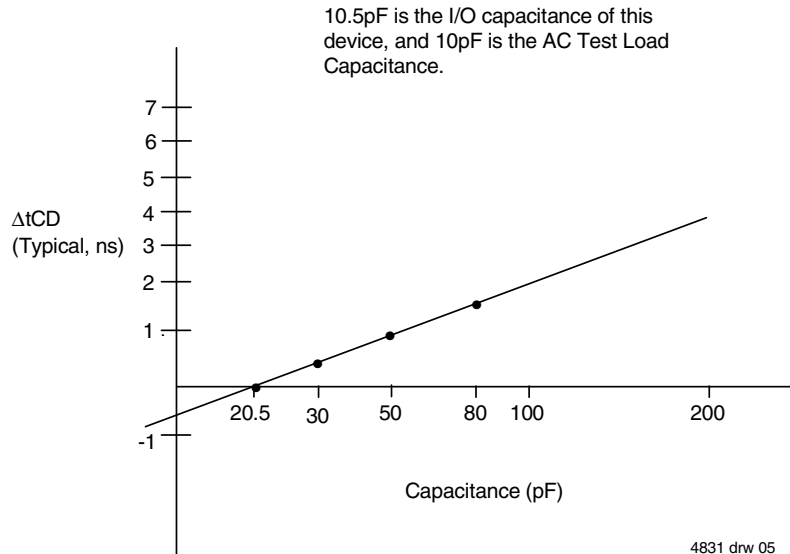
4831 drw 03

Figure 1. AC Output Test load.



4831 drw 04

Figure 2. Output Test Load
(For t_{CKLZ} , t_{CKHZ} , t_{OLZ} , and t_{OHZ}).
*Including scope and jig.



4831 drw 05

Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)^(1,2)

(V_{DD} = 3.3V ± 150mV, T_A = 0°C to +70°C)

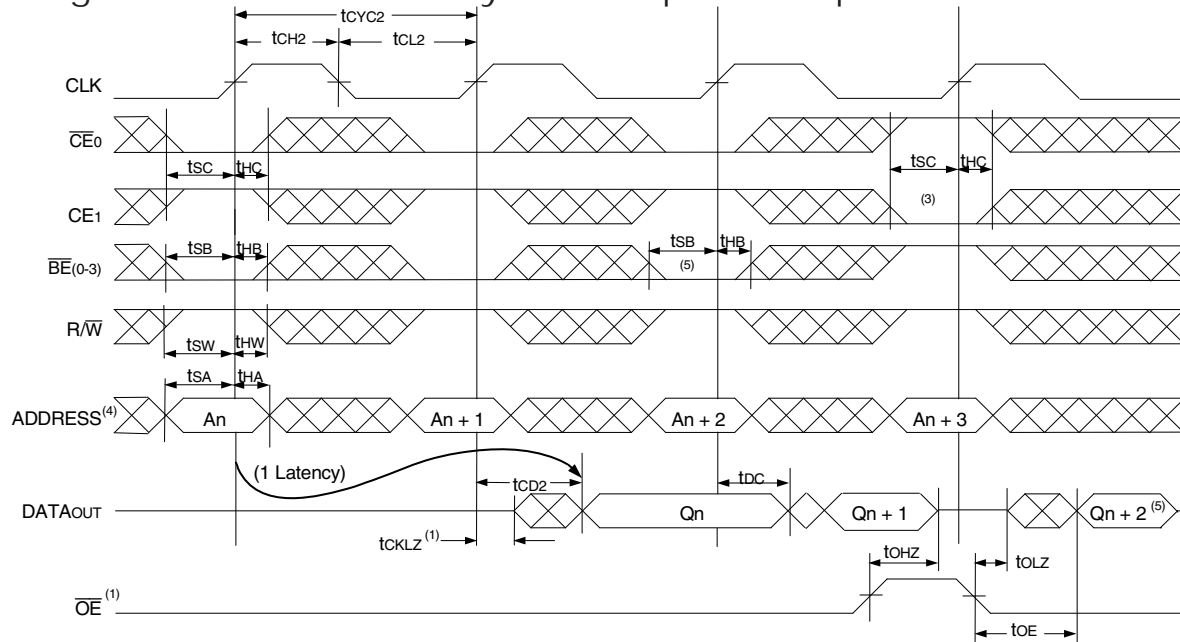
Symbol	Parameter	70V3569S4 Com'I Only		70V3569S5 Com'I & Ind		70V3569S6 Com'I Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC2}	Clock Cycle Time (Pipelined)	7.5	—	10	—	12	—	ns
t _{CH2}	Clock High Time (Pipelined)	3	—	4	—	5	—	ns
t _{CL2}	Clock Low Time (Pipelined)	3	—	4	—	5	—	ns
t _R	Clock Rise Time	—	3	—	3	—	3	ns
t _F	Clock Fall Time	—	3	—	3	—	3	ns
t _{SA}	Address Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HA}	Address Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SC}	Chip Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HC}	Chip Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SB}	Byte Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HB}	Byte Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SW}	R/W Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HW}	R/W Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SD}	Input Data Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HD}	Input Data Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SAD}	\overline{ADS} Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HAD}	\overline{ADS} Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SCN}	\overline{CNTEN} Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HCN}	\overline{CNTEN} Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SRST}	\overline{CNTRST} Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HRST}	\overline{CNTRST} Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{OE} ⁽¹⁾	Output Enable to Data Valid	—	4	—	5	—	6	ns
t _{OLZ}	Output Enable to Output Low-Z	0	—	0	—	0	—	ns
t _{OHZ}	Output Enable to Output High-Z	1	4	1	4.5	1	5	ns
t _{CD2}	Clock to Data Valid (Pipelined)	—	4.2	—	5	—	6	ns
t _{DC}	Data Output Hold After Clock High	1	—	1	—	1	—	ns
t _{CKHZ}	Clock High to Output High-Z	1	3	1	4.5	1.5	6	ns
t _{CKLZ}	Clock High to Output Low-Z	1	—	1	—	1	—	ns
Port-to-Port Delay								
t _{CO}	Clock-to-Clock Offset	6	—	8	—	10	—	ns

4831 tbl 11

NOTES:

1. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (\overline{OE}).
2. These values are valid for either level of V_{DDO} (3.3V/2.5V). See page 4 for details on selecting the desired I/O voltage levels for each port.

Timing Waveform of Read Cycle for Pipelined Operation⁽²⁾

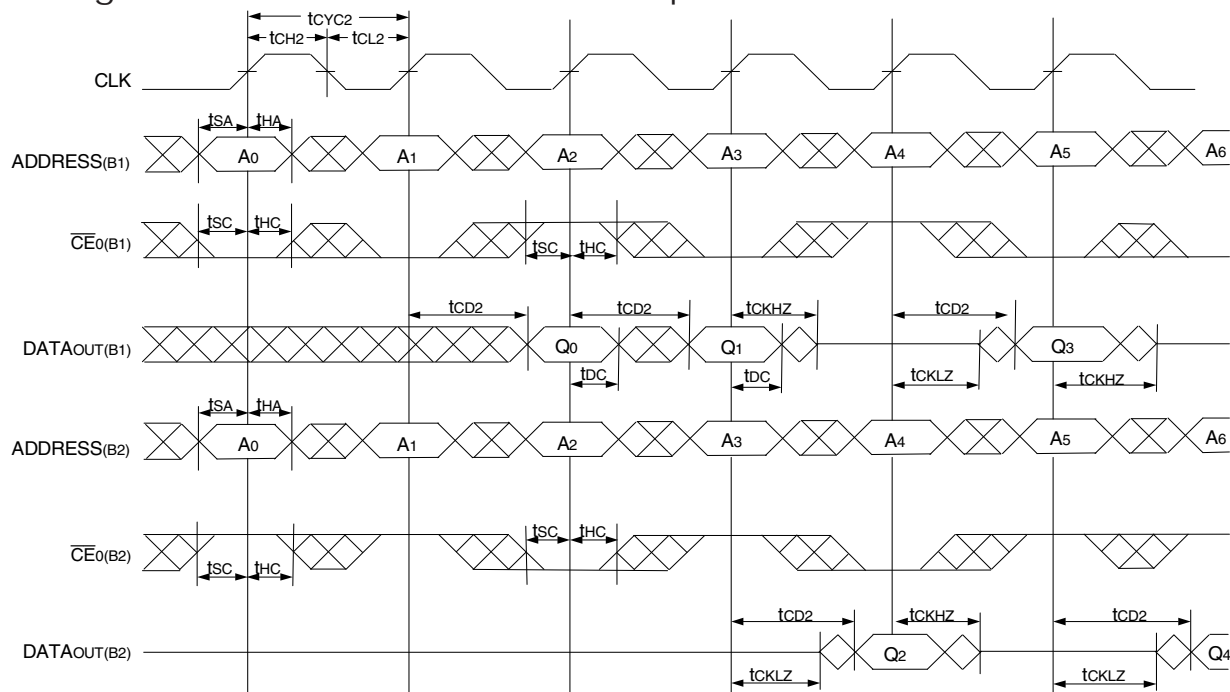


NOTES:

1. \overline{OE} is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2. $\overline{ADS} = V_{IL}$, \overline{CNTEN} and $\overline{CNRST} = V_{IH}$.
3. The output is disabled (High-Impedance state) by $\overline{CE}_0 = V_{IH}$, $CE_1 = V_{IL}$, $\overline{BE}_n = V_{IH}$ following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If \overline{BE}_n was HIGH, then the appropriate Byte of DATAout for $Q_n + 2$ would be disabled (High-Impedance state).

4831 drw 06

Timing Waveform of a Multi-Device Pipelined Read^(1,2)

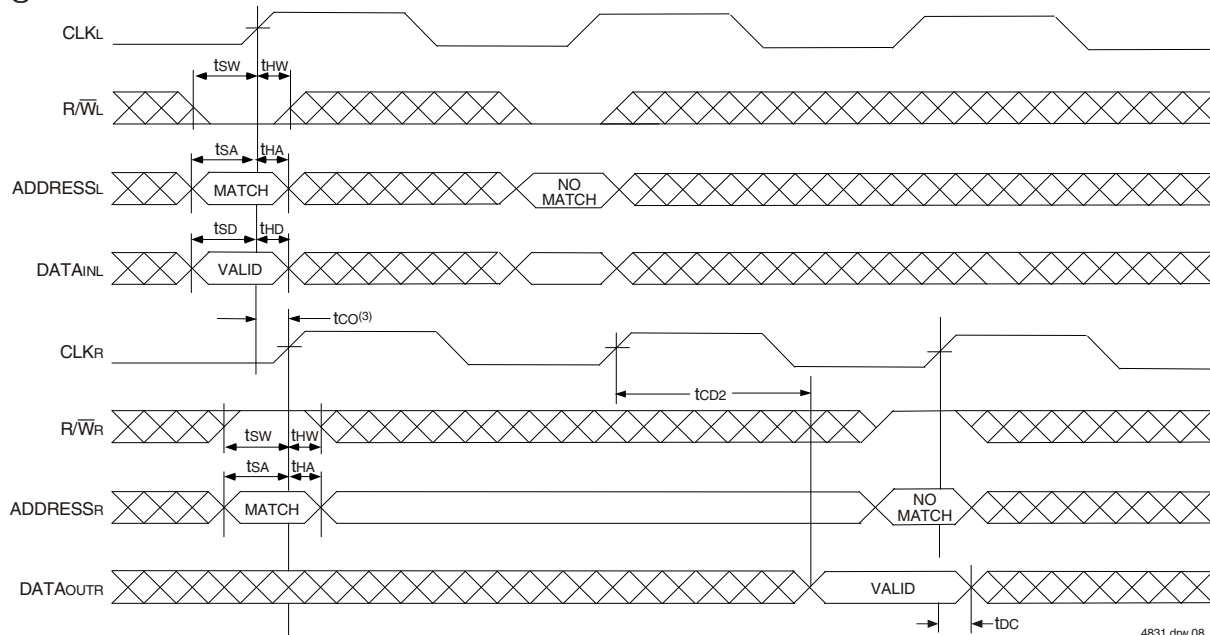


NOTES:

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V3569 for this waveform, and are setup for depth expansion in this example. $ADDRESS_{(B1)} = ADDRESS_{(B2)}$ in this situation.
2. \overline{BE}_n , \overline{OE} , and $\overline{ADS} = V_{IL}$; $CE_1(B_1)$, $CE_1(B_2)$, R/\overline{W} , \overline{CNTEN} , and $\overline{CNRST} = V_{IH}$.

4831 drw 07

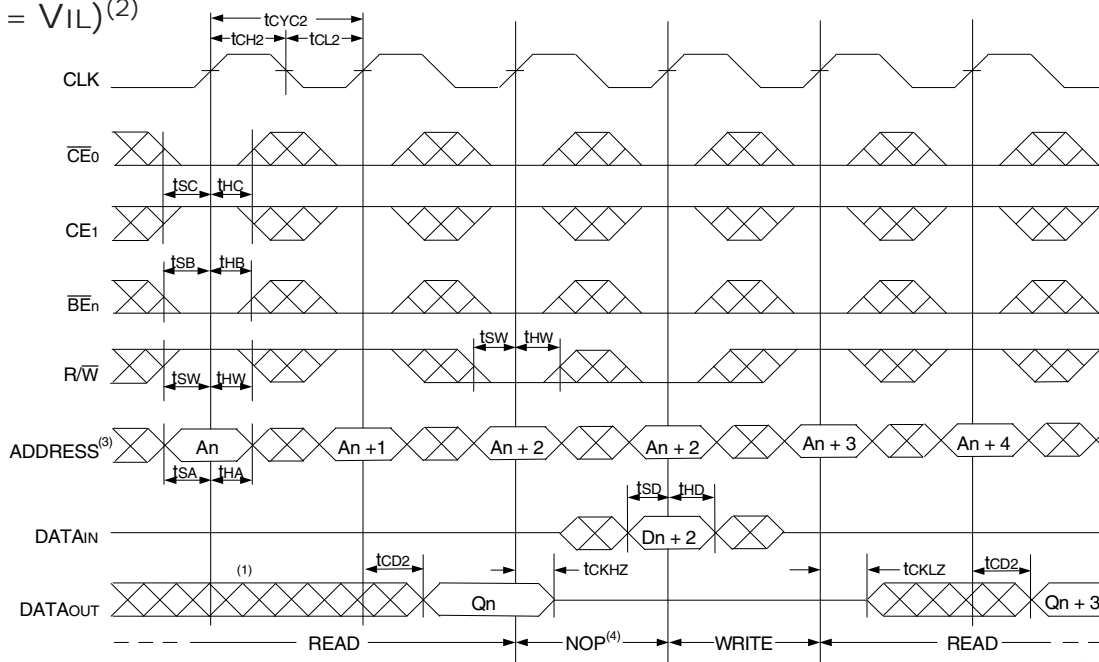
Timing Waveform of Left Port Write to Pipelined Right Port Read^(1,2)



NOTES:

- \overline{CE}_0 , \overline{BE}_n , and $\overline{ADS} = V_{IL}$; CE_1 , \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$.
- $\overline{OE} = V_{IL}$ for the Right Port, which is being read from. $\overline{OE} = V_{IH}$ for the Left Port, which is being written to.
- If $t_{CO} \leq$ minimum specified, then data from right port read is not valid until following right port clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + 2 t_{CYC2} + t_{CD2}$). If $t_{CO} >$ minimum, then data from right port read is available on first right port clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + t_{CYC} + t_{CD2}$).

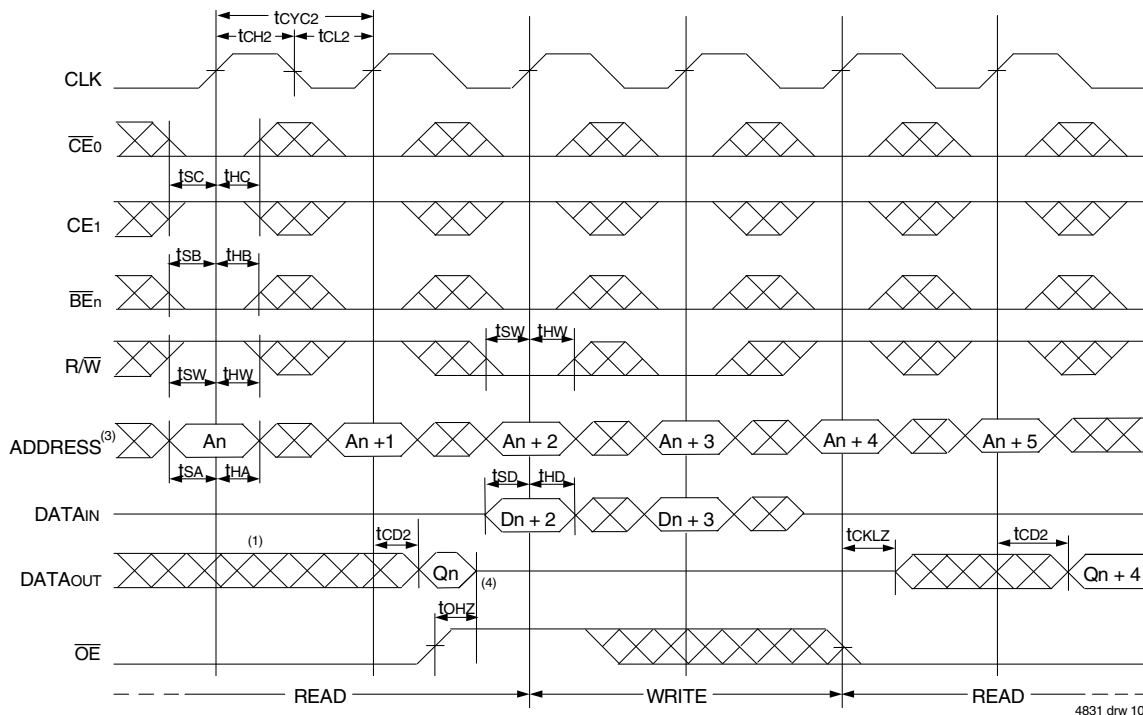
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽²⁾



NOTES:

- Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
- \overline{CE}_0 , \overline{BE}_n , and $\overline{ADS} = V_{IL}$; CE_1 , \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$. "NOP" is "No Operation".
- Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
- "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be rewritten to guarantee data integrity.

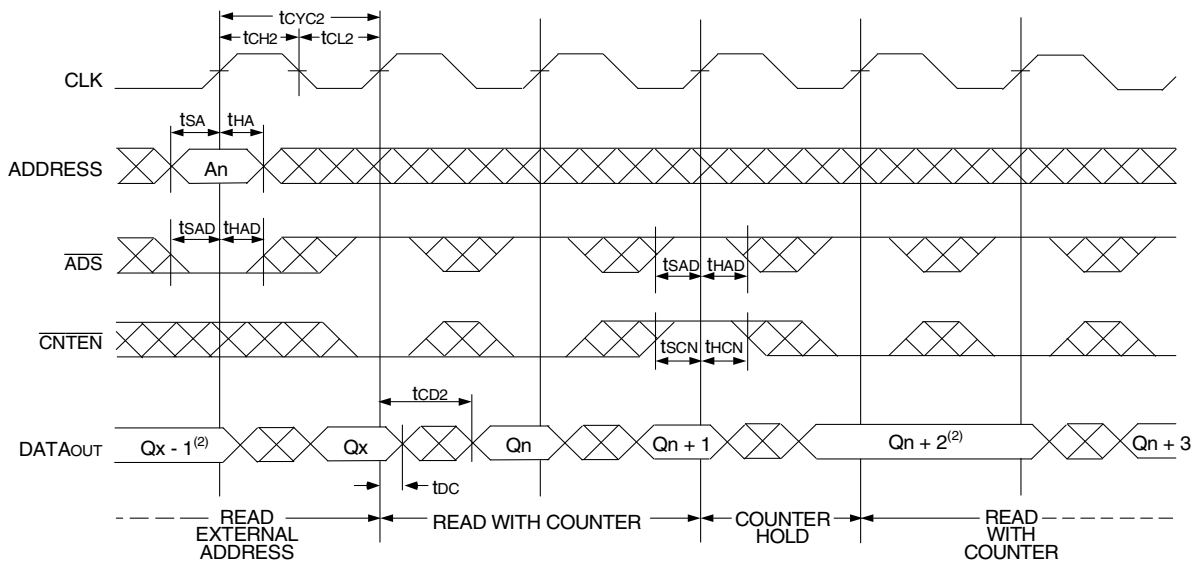
Timing Waveform of Pipelined Read-to-Write-to-Read (\overline{OE} Controlled)⁽²⁾



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. \overline{CE}_0 , \overline{BE}_n , and $\overline{ADS} = V_{IL}$; \overline{CE}_1 , \overline{CNTEN} , and $\overline{CNRST} = V_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

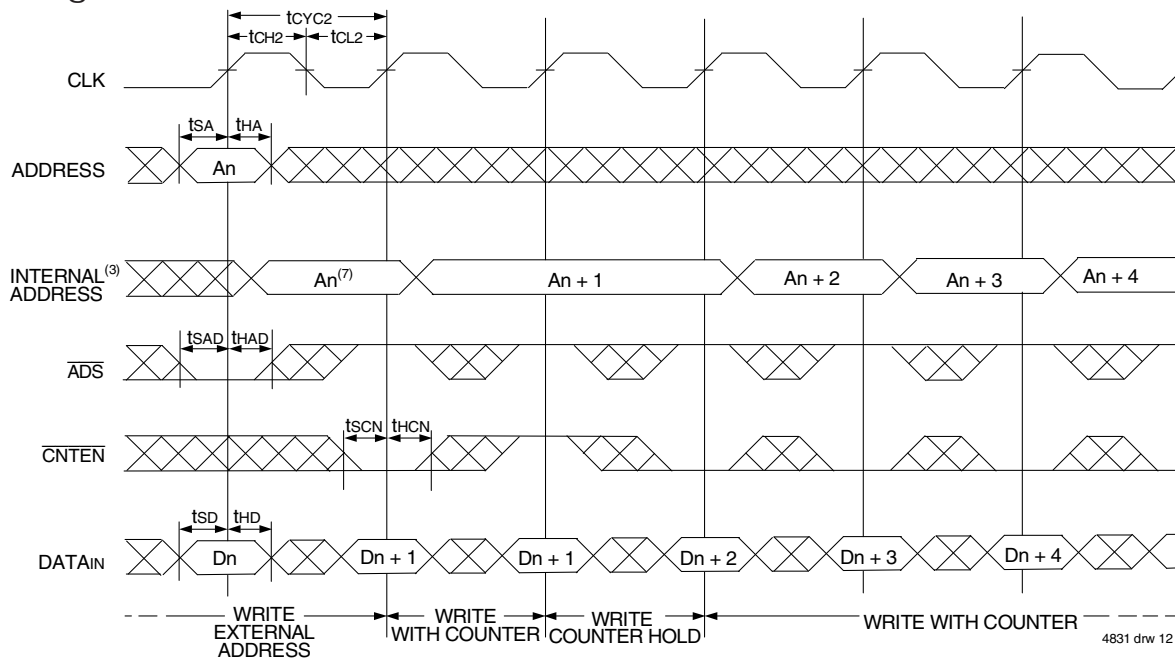
Timing Waveform of Pipelined Read with Address Counter Advance⁽¹⁾



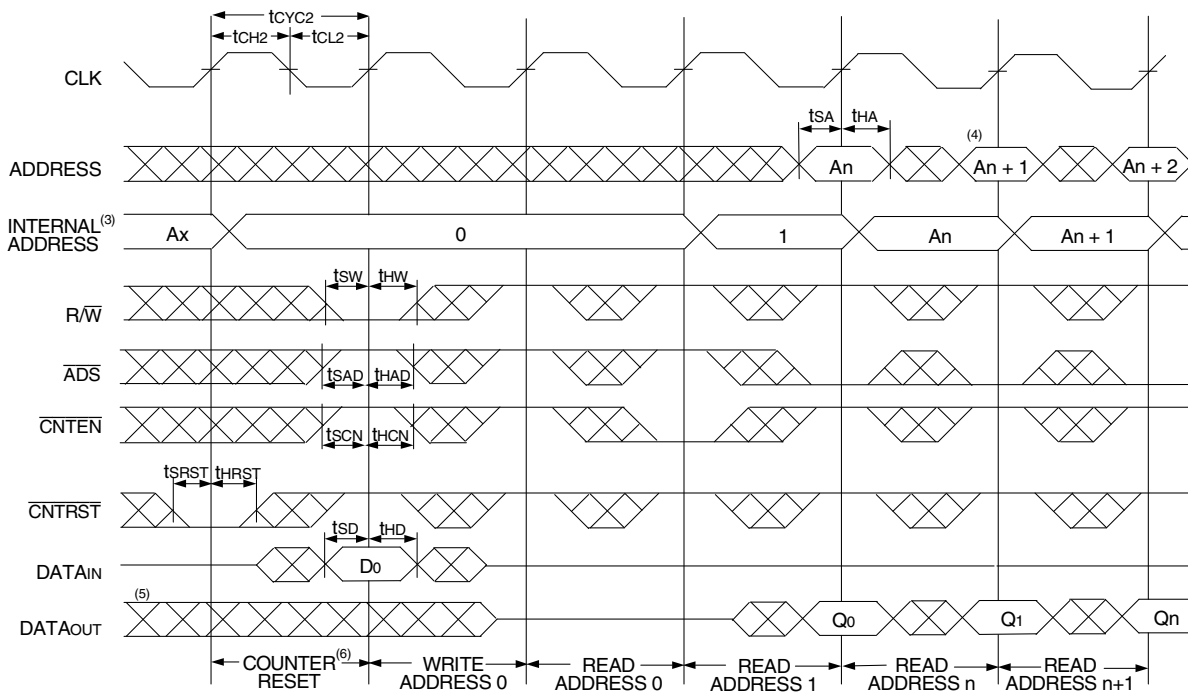
NOTES:

1. \overline{CE}_0 , \overline{OE} , $\overline{BE}_n = V_{IL}$; \overline{CE}_1 , $\overline{R/W}$, and $\overline{CNRST} = V_{IH}$.
2. If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance⁽¹⁾



Timing Waveform of Counter Reset⁽²⁾



NOTES:

1. \overline{CE}_0 , \overline{BE}_n , and $R/\overline{W} = V_{IL}$; CE_1 and $\overline{CNTRST} = V_{IH}$.
2. \overline{CE}_0 , $\overline{BE}_n = V_{IL}$; $CE_1 = V_{IH}$.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS} = V_{IL}$ and equals the counter output when $\overline{ADS} = V_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle: Addr 0 will be accessed. Extra cycles are shown here simply for clarification.
7. $\overline{CNTEN} = V_{IL}$ advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1' Address is written to during this cycle.

Functional Description

The IDT70V3569 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE_0}$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V3569s for depth expansion configurations. Two cycles are required with $\overline{CE_0}$ LOW and CE_1 HIGH to reactivate the outputs.

Depth and Width Expansion

The IDT70V3569 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V3569 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 72-bits or wider.

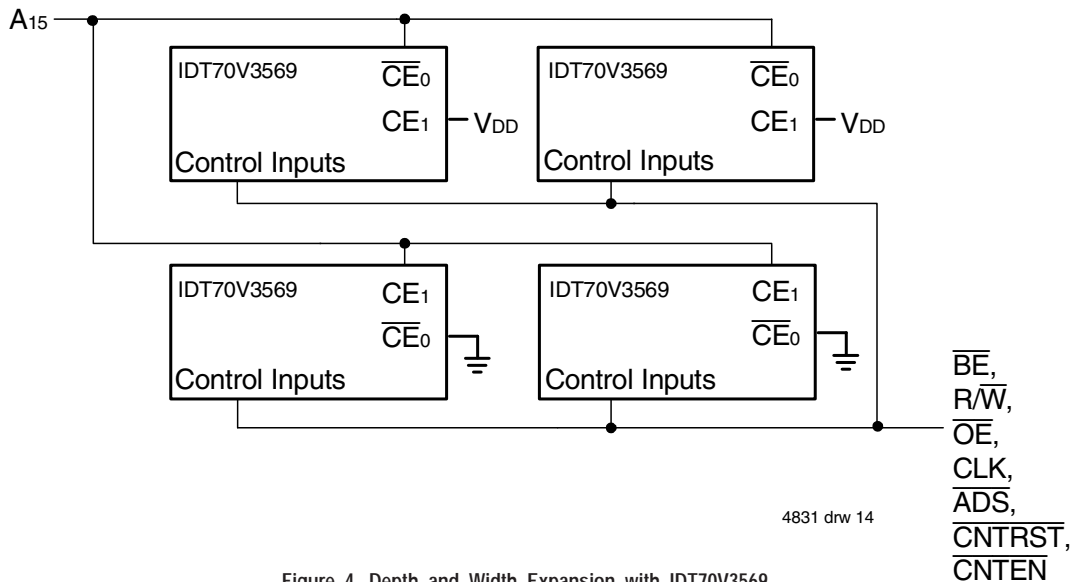
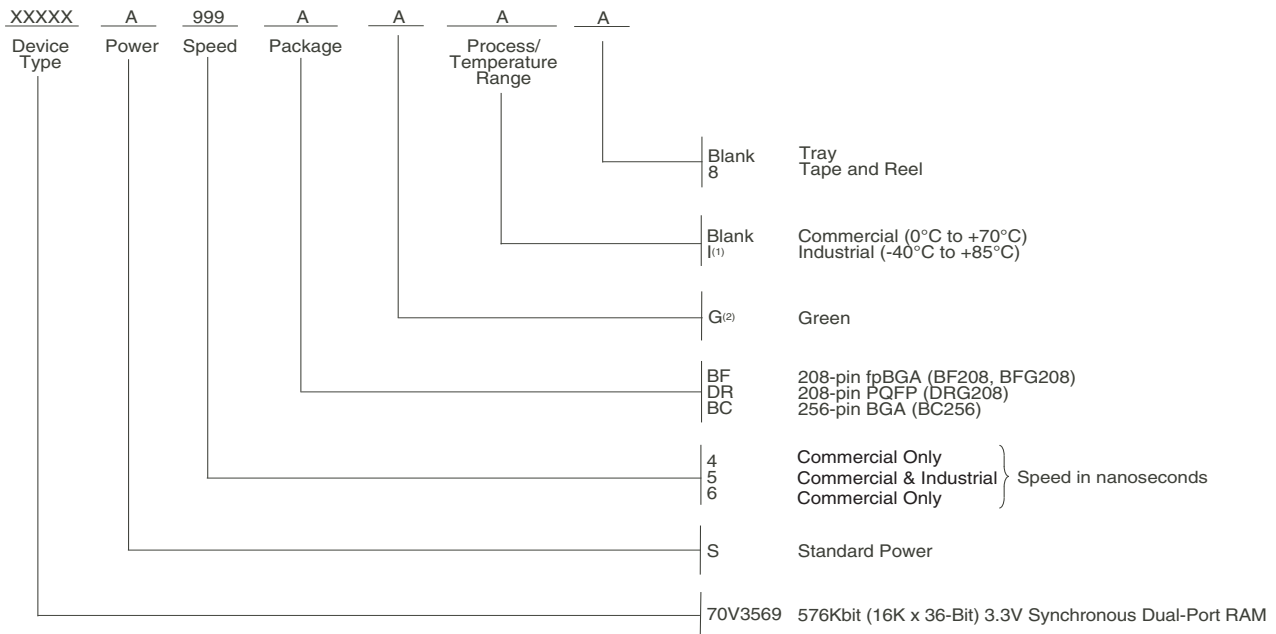


Figure 4. Depth and Width Expansion with IDT70V3569

Ordering Information



4831 drw 15

NOTES:

1. Contact your local sales office for Industrial temp range in other speeds, packages and powers.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

LEAD FINISH (SnPb) parts are Obsolete excluding BGA & fpBGA. Product Discontinuation Notice - PDN# SP-17-02
 Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
4	70V3569S4BC	BC256	CABGA	C
	70V3569S4BC8	BC256	CABGA	C
	70V3569S4BF	BF208	CABGA	C
	70V3569S4BF8	BF208	CABGA	C
	70V3569S4BFG	BFG208	CABGA	C
	70V3569S4BFG8	BFG208	CABGA	C
	70V3569S4DRG	DRG208	PQFP	C
5	70V3569S5BC	BC256	CABGA	C
	70V3569S5BC8	BC256	CABGA	C
	70V3569S5BCI	BC256	CABGA	I
	70V3569S5BCI8	BC256	CABGA	I
	70V3569S5BF	BF208	CABGA	C
	70V3569S5BF8	BF208	CABGA	C
	70V3569S5BFI	BF208	CABGA	I
70V3569S5BFI8	BF208	CABGA	I	
6	70V3569S6BC	BC256	CABGA	C
	70V3569S6BC8	BC256	CABGA	C
	70V3569S6BF	BF208	CABGA	C
	70V3569S6BF8	BF208	CABGA	C

Datasheet Document History

- 01/08/99: Initial Public Release
- 03/12/99: Added fpBGA package
- 04/28/99: Fixed typo on page 10
- 06/08/99: Changed drawing format
 - Page 2 Changed package body dimensions
 - Page 3 Fixed typo
- 06/15/99: Page 5 Deleted note 6 for Table II
- 08/04/99: Page 2 Fixed typographical error
 - Page 6 Improved power number
- 10/14/99: Upgraded speed to 133MHz, added 2.5V I/O capability
- 10/19/99: Page 4 Corrected I/O numbers in Truth Table I
- 11/12/99: Replaced IDT logo
- 04/10/00: Added new BGA packages, added full 2.5V interface capability
- 01/12/01: Page 6 Updated Truth Table II
 - Increased storage temperature parameter
 - Clarified TA Parameter

Page 8 DC Electrical parameters—changed wording from "open" to "disabled"

 - Removed note 7 on DC Electrical Characteristics table
 - Removed Preliminary status
- 04/10/01: Added Industrial Temperature Ranges and removed related notes
- 12/12/01: Page 2, 3 & 4 Added date revision to pin configurations
 - Page 6 Removed industrial temp footnote from table 04
 - Page 8 & 10 Removed industrial temp for 6ns from DC & AC Electrical Characteristics
 - Page 16 Removed industrial temp from 6ns in ordering information
 - Added industrial temp footnote
 - Page 1 & 17 Replaced TM logo with ® logo
- 03/23/05: Page 1 Added green availability to features
 - Page 16 Added green indicator to ordering information
 - Page 1 & 17 Replaced old IDT TM with new IDT TM logo
- 02/08/06: Page 5 Changed footnote 2 for Truth Table I from $\overline{\text{ADS}}, \overline{\text{CNTEN}}, \overline{\text{CNTRST}} = V_{\text{IH}}$ to $\overline{\text{ADS}}, \overline{\text{CNTEN}}, \overline{\text{CNTRST}} = X$
- 07/25/08: Page 8 Corrected a typo in the DC Chars table
- 10/23/08: Page 16 Removed "IDT" from orderable part number
- 10/08/14: Page 16 Added Tape and Reel to the Ordering Information
- 02/15/18: Product Discontinuation Notice - PDN# SP-17-02
Last time buy expires June 15, 2018
- 08/21/19: Page 2, 3 & 16 Updated package codes BF-208 to BF208, BFG208 and BC-256 to BC256
 - Page 4 Rotated DRG208 PQFP pin configuration to accurately reflect pin 1 orientation
 - Page 16 Added Orderable Part Information table



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[70V3569S5DR](#) [70V3569S5BF](#) [70V3569S5BC](#) [70V3569S6DR](#) [70V3569S6BF](#) [70V3569S6BC](#) [70V3569S4BFG](#)
[70V3569S4BFG8](#) [70V3569S6BF8](#) [70V3569S6BC8](#) [70V3569S5BFI](#) [70V3569S5DRI](#) [70V3569S5BCI](#) [70V3569S4BF8](#)
[70V3569S4BC8](#) [70V3569S4DRG](#)

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- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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