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74ABT573
Octal D-Type Latch with 3-STATE Outputs

Features

- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to ABT373
- 3-STATE outputs for bus interfacing
- Output sink capability of 64mA, source capability of 32mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50pF and 250pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High-impedance, glitch-free bus loading during entire power up and power down
- Nondestructive, hot insertion capability

General Description

The ABT573 is an octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

This device is functionally identical to the ABT373 but has broadside pinouts.

Ordering Information

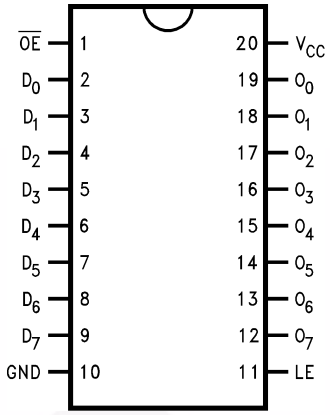
Order Number	Package Number	Package Description
74ABT573CSC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ABT573CSJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT573CMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74ABT573CMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

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Connection Diagram



Pin Descriptions

Pin Names	Descriptions
D_0–D_7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	3-STATE Output Enable Input (Active LOW)
O_0–O_7	3-STATE Latch Outputs

Functional Description

The ABT573 contains eight D-type latches with 3-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Function Table

Inputs			Outputs
$\overline{OE}$	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

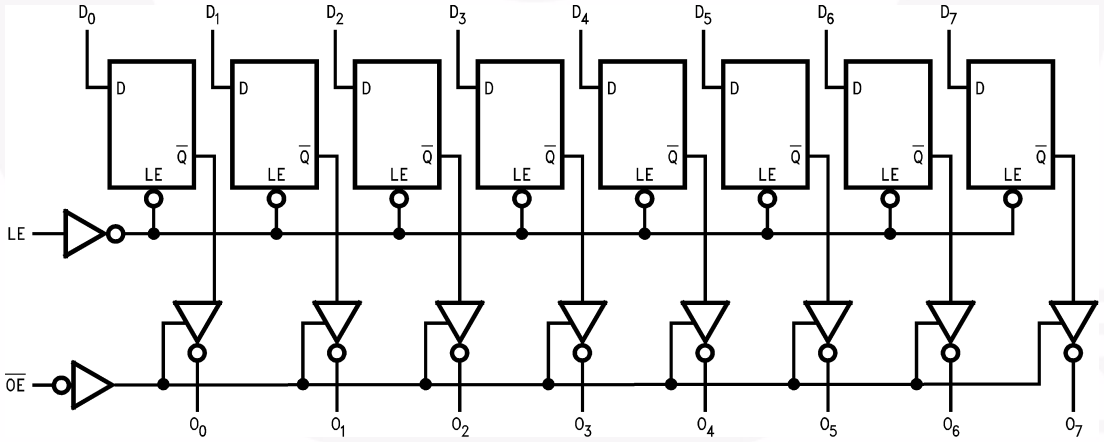
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

O_0 = Value stored from previous clock cycle

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
T_{STG}	Storage Temperature	–65°C to +150°C
T_A	Ambient Temperature Under Bias	–55°C to +125°C
T_J	Junction Temperature Under Bias	–55°C to +150°C
V_{CC}	V_{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
V_{IN}	Input Voltage(1)	–0.5V to +7.0V
I_{IN}	Input Current(1)	–30mA to +5.0mA
V_O	Voltage Applied to Any Output	
	Disabled or Power-Off State	–0.5V to 5.5V
	HIGH State	–0.5V to V_{CC}
	Current Applied to Output in LOW State (Max.)	twice the rated I_{OL} (mA)
	DC Latchup Source Current	–500mA
	Over Voltage Latchup (I/O)	10V

Note:

1. Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
T_A	Free Air Ambient Temperature	–40°C to +85°C
V_{CC}	Supply Voltage	+4.5V to +5.5V
$\Delta V / \Delta t$	Minimum Input Edge Rate	
	Data Input	50mV/ns
	Enable Input	20mV/ns

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DC Electrical Characteristics

Symbol	Parameter		V_{CC}	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage			Recognized HIGH Signal	2.0			V
V_{IL}	Input LOW Voltage			Recognized LOW Signal			0.8	V
V_{CD}	Input Clamp Diode Voltage		Min.	I_{IN} = –18mA			–1.2	V
V_{OH}	Output HIGH Voltage		Min.	I_{OH} = –3mA	2.5			V
				I_{OH} = –32mA	2.0			
V_{OL}	Output LOW Voltage		Min.	I_{OL} = 64mA			0.55	V
I_{IH}	Input HIGH Current		Max.	V_{IN} = 2.7V(3)			1	µA
				V_{IN} = V_{CC}			1	
I_{BVI}	Input HIGH Current Breakdown Test		Max.	V_{IN} = 7.0V			7	µA
I_{IL}	Input LOW Current		Max.	V_{IN} = 0.5V(3)			–1	µA
				V_{IN} = 0.0V			–1	
V_{ID}	Input Leakage Test		0.0	I_{ID} = 1.9 µA, All Other Pins Grounded	4.75			V
I_{OZH}	Output Leakage Current		0–5.5V	V_{OUT} = 2.7V, $\overline{OE}$ = 2.0V			10	µA
I_{OZL}	Output Leakage Current		0–5.5V	V_{OUT} = 0.5V, $\overline{OE}$ = 2.0V			–10	µA
I_{OS}	Output Short-Circuit Current		Max.	V_{OUT} = 0.0V	–100		–275	mA
I_{CEX}	Output HIGH Leakage Current		Max.	V_{OUT} = V_{CC}			50	µA
I_{ZZ}	Bus Drainage Test		0.0	V_{OUT} = 5.5V, All Others GND			100	µA
I_{CCH}	Power Supply Current		Max.	All Outputs HIGH			50	µA
I_{CCL}	Power Supply Current		Max.	All Outputs LOW			30	mA
I_{CCZ}	Power Supply Current		Max.	$\overline{OE}$ = V_{CC}, All Others at V_{CC} or GND			50	µA
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled	Max.	V_I = V_{CC} – 2.1V			2.5	mA
		Outputs 3-STATE		Enable Input V_I = V_{CC} – 2.1V			2.5	mA
		Outputs 3-STATE		Data Input V_I = V_{CC} – 2.1V, All Others at V_{CC} or GND			2.5	mA
I_{CCD}	Dynamic I_{CC} No Load(3)		Max.	Outputs Open, $\overline{OE}$ = GND, LE = V_{CC}(2), One-Bit Toggling, 50% Duty Cycle			0.12	mA/ MHz

Notes:

2. For 8-bits toggling, I_{CCD} < 0.8mA/MHz.
3. Guaranteed but not tested.

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DC Electrical Characteristics

SOIC package.

Symbol	Parameter	V_{CC}	Conditions $C_L = 50pF$, $R_L = 500\Omega$	Min.	Typ.	Max.	Units
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	$T_A = 25°C$[4]		0.7	1.0	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	$T_A = 25°C$[4]	–1.5	–1.2		V
V_{OHV}	Minimum HIGH Level Dynamic Output Voltage	5.0	$T_A = 25°C$[5]	2.5	3.0		V
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	$T_A = 25°C$[6]	2.2	1.8		V
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	$T_A = 25°C$[6]		1.0	0.7	V

Notes:

4. Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.
5. Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.
6. Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

AC Electrical Characteristics

SOIC and SSOP package.

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$			$T_A = –40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50pF$		Units
		Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, D_n to O_n	1.9	2.7	4.5	1.9	4.5	ns
t_{PHL}		1.9	2.8	4.5	1.9	4.5	
t_{PLH}	Propagation Delay, LE to O_n	2.0	3.1	5.0	2.0	5.0	ns
t_{PHL}		2.0	3.0	5.0	2.0	5.0	
t_{PZH}	Output Enable Time	1.5	3.1	5.3	1.5	5.3	ns
t_{PZL}		1.5	3.1	5.3	1.5	5.3	
t_{PHZ}	Output Disable Time	2.0	3.6	5.4	2.0	5.4	ns
t_{PLZ}		2.0	3.4	5.4	2.0	5.4	

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AC Operating Requirements

SOIC and SSOP package.

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$			$T_A = –40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50pF$		Units
		Min.	Typ.	Max.	Min.	Max.	
f_{TOGGLE}	Max Toggle Frequency		100				MHz
$t_S(H)$	Set Time, HIGH or LOW D_n to LE	1.5			1.5		ns
$t_S(L)$		1.5			1.5		
$t_H(H)$	Hold Time, HIGH or LOW D_n to LE	1.0			1.0		ns
$t_H(L)$		1.0			1.0		
$t_W(H)$	Pulse Width, LE HIGH	3.0			3.0		ns

Extended AC Electrical Characteristics

SOIC package.

Symbol	Parameter	$T_A = –40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50pF$, 8 Outputs Switching[7]		$T_A = –40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250pF$[8]		$T_A = –40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250pF$, 8 Outputs Switching[9]		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, D_n to O_n	1.5	5.2	2.0	6.8	2.0	9.0	ns
t_{PHL}		1.5	5.2	2.0	6.8	2.0	9.0	
t_{PLH}	Propagation Delay, LE to O_n	1.5	5.5	2.0	7.5	2.0	9.5	ns
t_{PHL}		1.5	5.5	2.0	7.5	2.0	9.5	
t_{PZH}	Output Enable Time	1.5	6.2	2.0	8.0	2.0	10.5	ns
t_{PZL}		1.5	6.2	2.0	8.0	2.0	10.5	
t_{PHZ}	Output Disable Time	1.0	5.5	(10)		(10)		ns
t_{PLZ}		1.0	5.5					

Notes:

7. This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).
8. This specification is guaranteed but not tested. The limits represent propagation delay with 250pF load capacitors in place of the 50pF load capacitors in the standard AC load. This specification pertains to single output switching only.
9. This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50pF load capacitors in the standard AC load.
10. The 3-STATE delay times are dominated by the RC network (500Ω, 250pF) on the output and has been excluded from the datasheet.

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Skew(11)

SOIC package.

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50pF$, 8 Outputs Switching(11)	$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250pF$, 8 Outputs Switching(12)	Units
		Max.	Max.	
t_{OSHL}(13)	Pin to Pin Skew, HL Transitions	1.0	1.5	ns
t_{OSLH}(13)	Pin to Pin Skew, LH Transitions	1.0	1.5	ns
t_{PS}(14)	Duty Cycle, LH–HL Skew	1.4	3.5	ns
t_{OST}(13)	Pin to Pin Skew, LH/HL Transitions	1.5	3.9	ns
t_{PV}(15)	Device to Device Skew LH/HL Transitions	2.0	4.0	ns

Notes:

11. This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.)
12. This specification is guaranteed but not tested. The limits represent propagation delays with 250pF load capacitors in place of the 50pF load capacitors in the standard AC load.
13. Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}), LOW-to-HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t_{OST}). This specification is guaranteed but not tested.
14. This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.
15. Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Capacitance

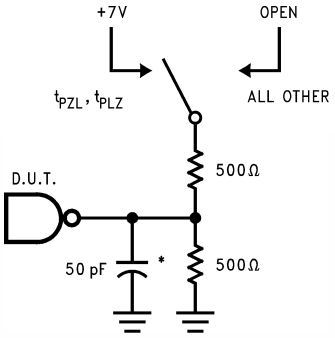
Symbol	Parameter	Conditions ($T_A = 25°C$)	Typ.	Units
C_{IN}	Input Capacitance	$V_{CC} = 0V$	5	pF
C_{OUT}(16)	Output Capacitance	$V_{CC} = 5.0V$	9	pF

Note:

16. C_{OUT} is measured at frequency f = 1MHz per MIL-STD-883B, Method 3012.

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AC Loading



*Includes jig and probe capacitance

Figure 1. Test Load

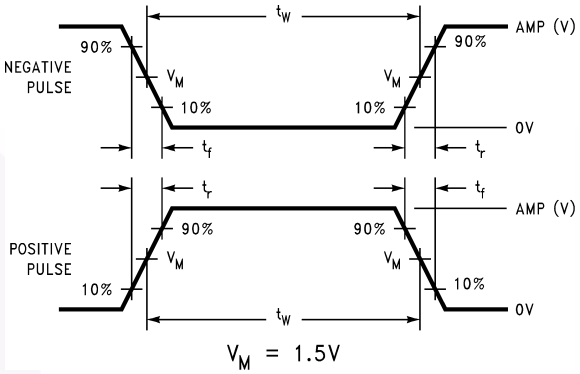


Figure 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1MHz	500ns	2.5ns	2.5ns

Figure 3. Test Input Signal Requirements

AC Waveforms

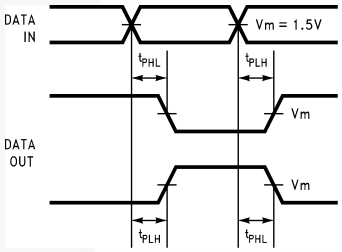


Figure 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

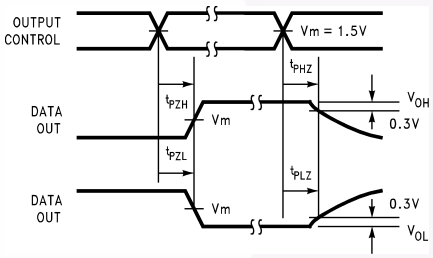


Figure 6. 3-STATE Output HIGH and LOW Enable and Disable Times

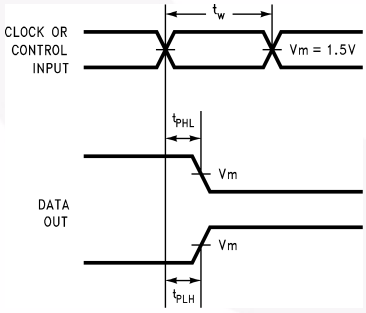


Figure 5. Propagation Delay, Pulse Width Waveforms

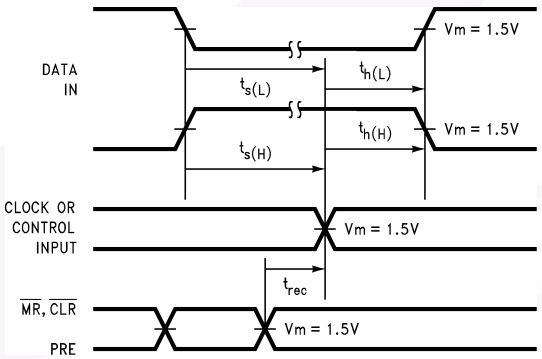


Figure 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions

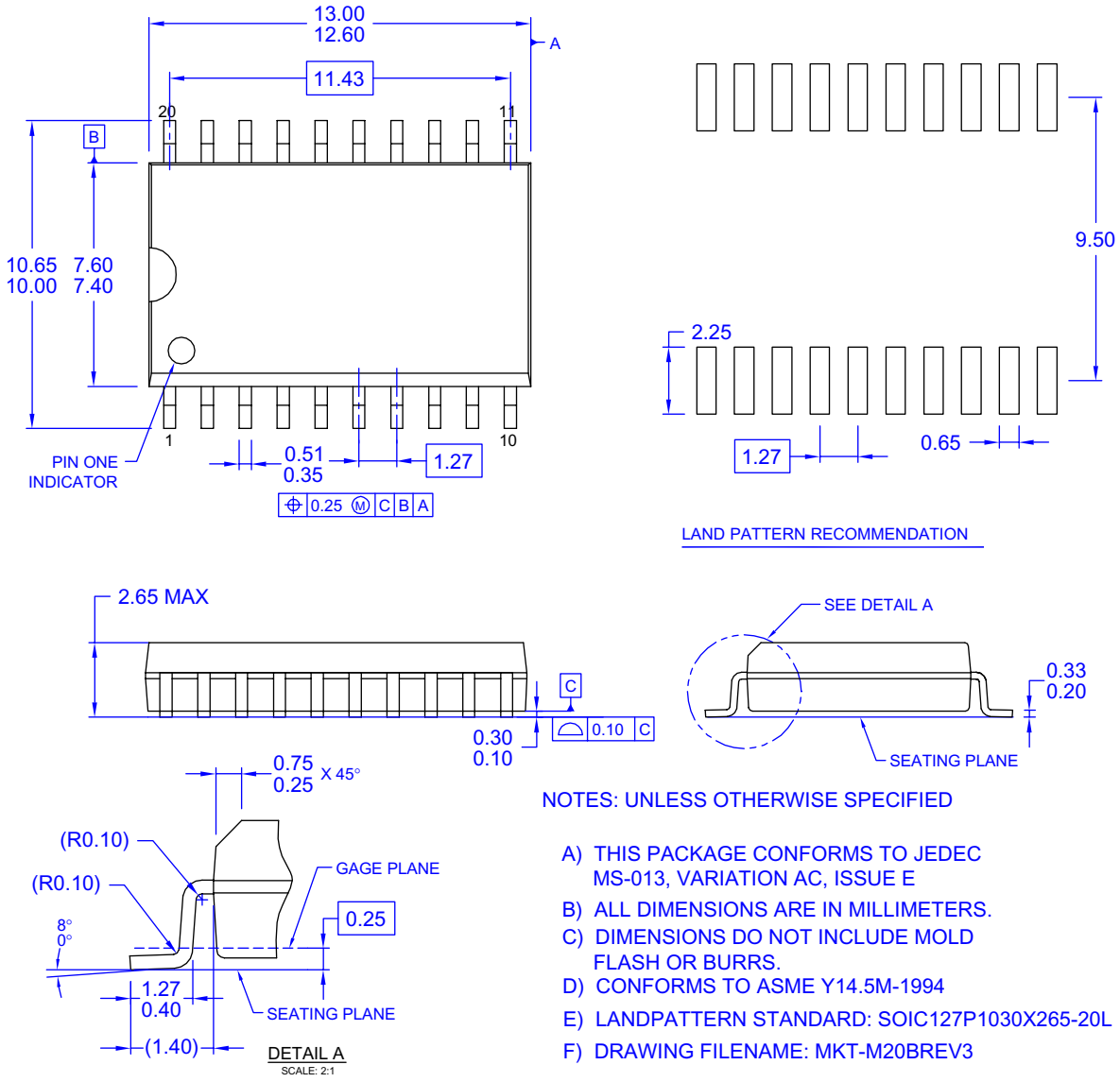


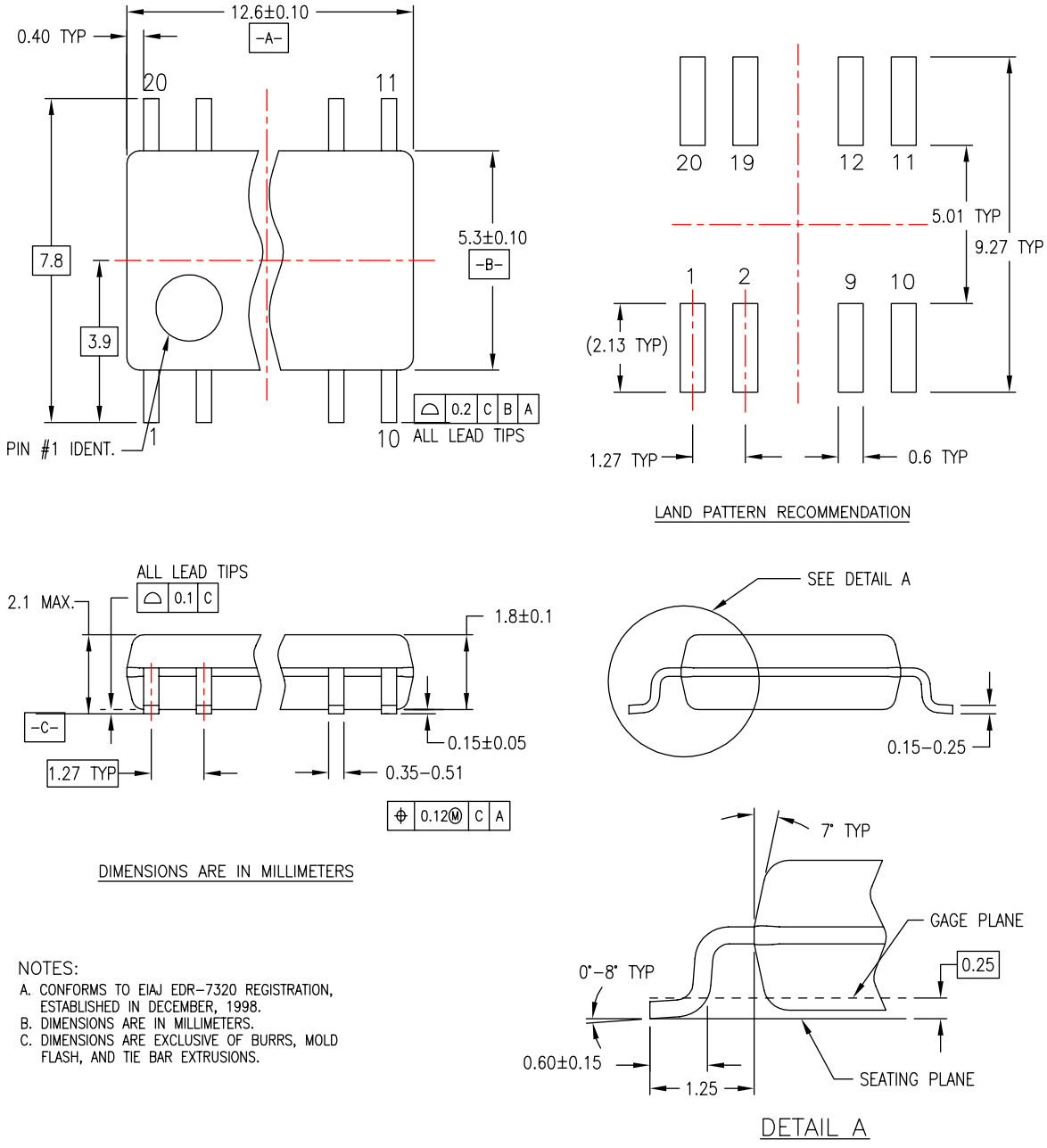
Figure 8. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide

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Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

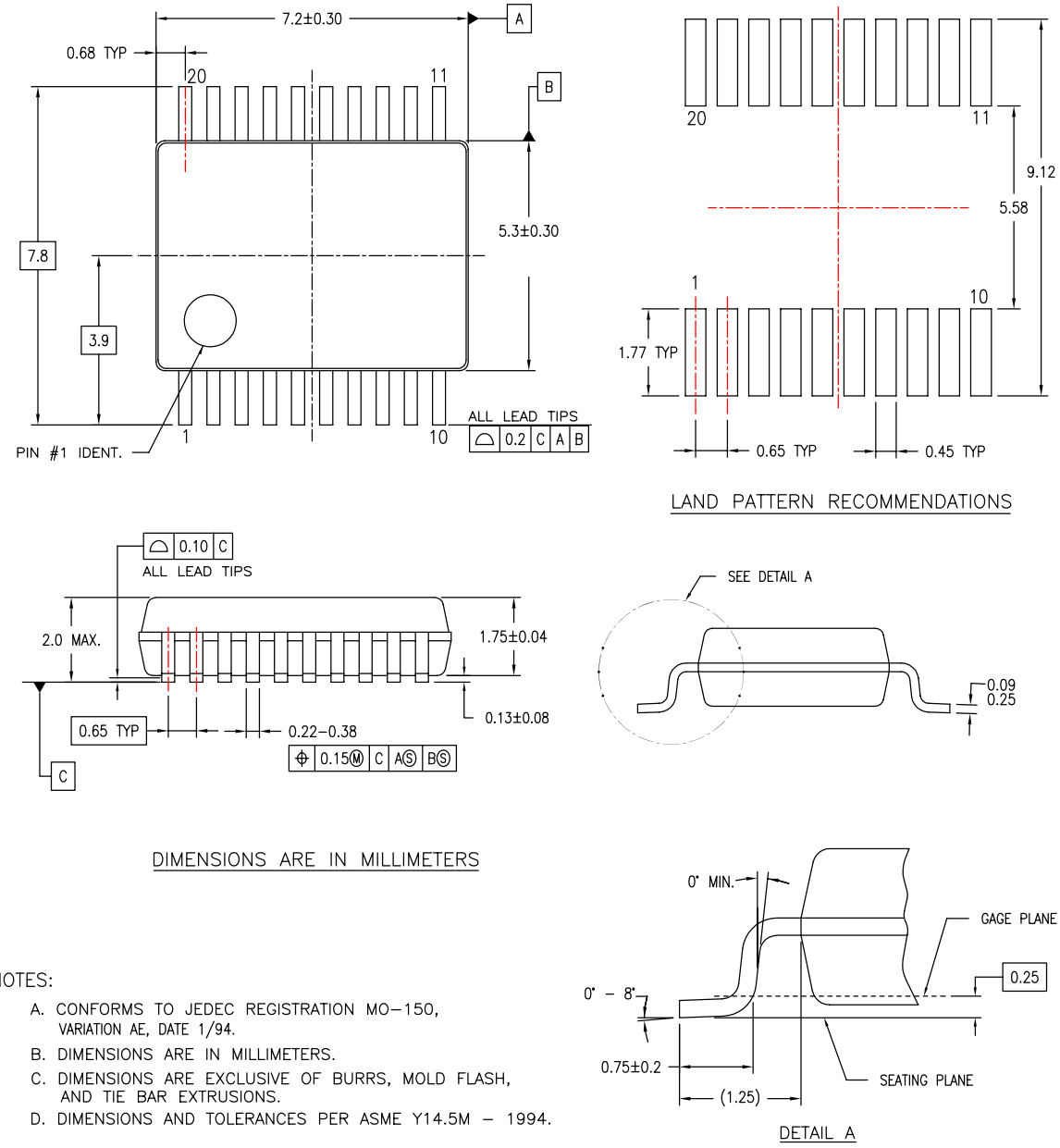
Figure 9. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–150, VARIATION AE, DATE 1/94.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M – 1994.

MSA20REVB

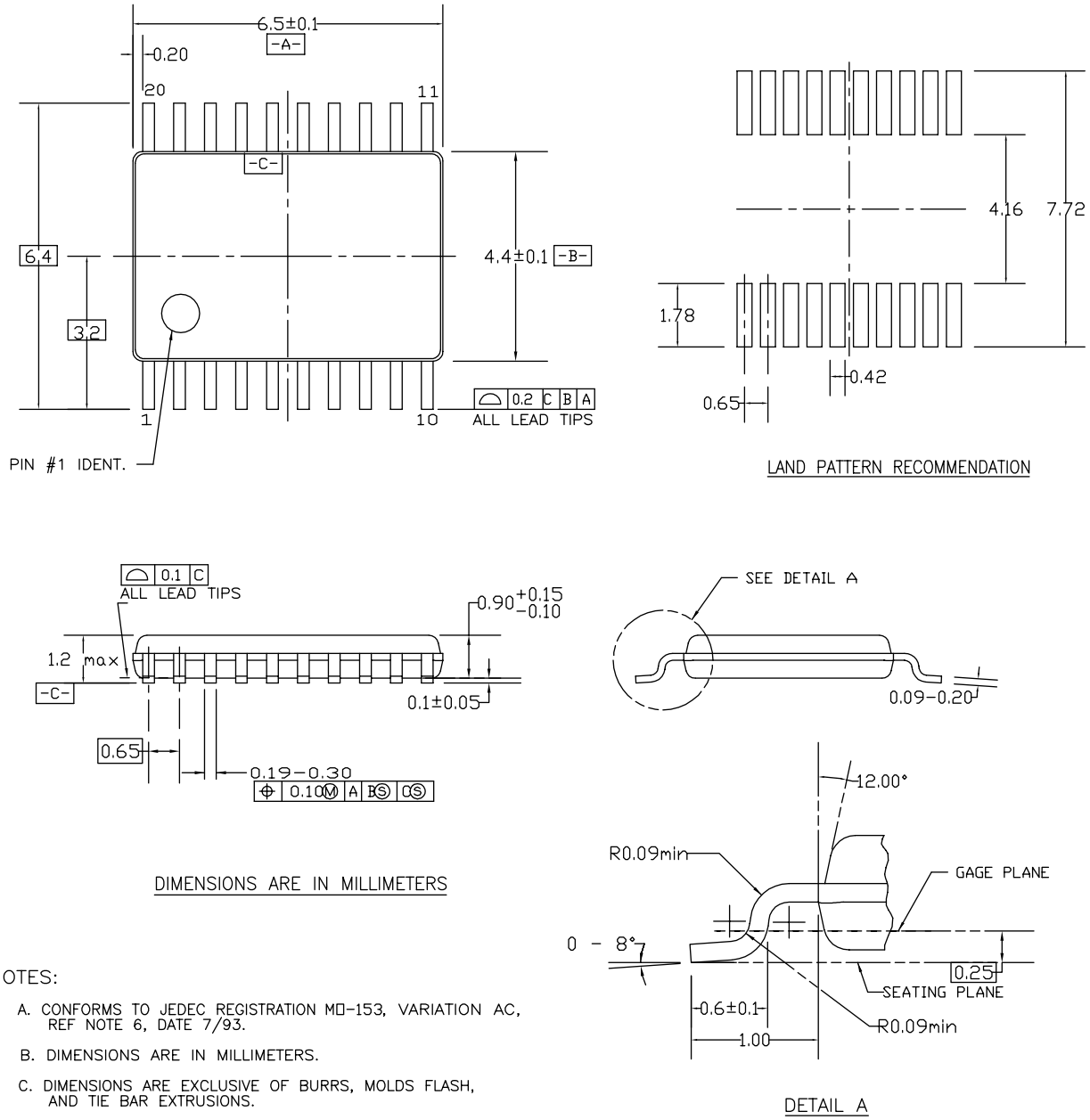
Figure 10. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

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Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

Figure 11. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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ISOPLANAR™
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PDP-SPM™
Power220®
Power247®
POWEREDGE®
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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LifeElectronics
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- *Тестирование поставляемой продукции.*
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- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

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- *Регистрацию проекта у производителя компонентов.*
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