RL78/H1D

RENESAS MCU

R01DS0318EJ0100
Rev. 1.00
Apr 13, 2018

Analog front-end (24-bit ΔΣA/D converter with programmable gain instrumentation amplifier, Amplifier unit and 12-bit D/A converter), External signal sampler/Sampling output timer detector and Integrated LCD controller/driver.
True Low Power Platform (as low as 70.8 µA/MHz, and 0.68 µA in Halt mode(RTC2 + LVD)), 1.8 V to 5.5V operation, 64 to 128 Kbyte Flash, 33 DMIPS at 24 MHz, for Healthcare and Flow meter applications.

1. OUTLINE

1.1 Features

○ Ultra-low power consumption technology
- V_{DD} = 2.4 to 5.5 V
  (10-bit SAR A/D converter: 2.4 to 5.5 V, operating voltage of the analog front-end (AFE): 2.7 to 5.5 V) Note 1,
  V_{DD} = 1.8 to 5.5 V Note 2
- HALT mode
- STOP mode
- SNOOZE mode

○ RL78 CPU core
- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.04167 µs: @ 24 MHz operation with high-speed on-chip oscillator clock) to ultra-low speed (30.5 µs: @ 32.768 kHz operation with subsystem clock)
- Multiply/divide and multiply/accumulate instructions are supported.
- Address space: 1 MB
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 5.5 KB Note 1, 8 KB Note 2

○ Code flash memory
- Code flash memory: 64 to 128 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

○ Data flash memory
- Data flash memory: 4 KB
- Background operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: V_{DD} = 2.4 to 5.5 V Note 1, 1.8 to 5.5 V Note 2

○ High-speed on-chip oscillator
- Select from 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy: ±1.0% (V_{DD} = 2.4 to 5.5 V, T_A = -20 to +85°C Note 1, V_{DD} = 1.8 to 5.5 V, T_A = -20 to +85°C Note 2)

○ Operating ambient temperature
- T_A = -40 to +85°C (A: Consumer applications Note 1, D: Industrial applications Note 2)

○ Power management and reset function
- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 9 Note 1 or 12 Note 2 levels)

○ Data transfer controller (DTC)
- Transfer modes: Normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources (35 sources).
- Chain transfer function

○ Event link controller (ELC)
- Event signals of 18 to 26 types can be linked to the specified peripheral function.

○ Serial interfaces
- CSI/CSI (SPI supported): 3 channels
- UART/UART (LIN-bus supported):3 channels
- I^2C/simplified I^2C: 4 channels
- Serial interface UARTMG (9600 bps @ 38.4 kHz): 1 channel (R5F11R only)

○ Timers
- 16-bit timer:
  Timer array unit (TAU): 8 channels,
  Timer RJ: 2 channels (R5F11R only)
- 8-bit timer:2 channels[Note 1], 6 channels[Note 2]
- 12-bit interval timer: 1 channel
- Real-time clock 2: 1 channel (calendar for 99 years, alarm function, and clock correction function)
- Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)
- External signal sampler: 1 channel (R5F11R only)
- Sampling output timer detector (SMOTD): 6 channels for input, 3 channels for output (R5F11R only)

○ LCD controller/driver
- Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.
- Segment signal output:
  27 (23) to 36 (32) [Note 3]
- Common signal output: 4 (8) [Note 3]

○ Analog front-end power supply circuit (R5F11N and R5F11P only)
- AFE reference power supply (ABGR)
- LDO for supplying power to internal circuits (REGA)
- LDO for supplying power to a sensor (SBIAS): 0.5 to 2.2 V

○ 24-bit ΔΣ A/D converter with programmable gain instrumentation amplifier (R5F11N and R5F11P only)
- 24-bit second-order ΔΣ A/D converter (AV_{DD} = 2.7 to 5.5 V)
  - SNDR: 85 dB (TYP.)
  - Output data rate: 488 sps to 15.625 ksps in normal mode
    61 sps to 1.953 ksps in low power mode
- Programmable gain instrumentation amplifier (PGA0)
  - Analog input: 1 to 5 channels (differential input mode or single-ended input mode)
  - D/A converter for offset adjustment
  - Variable gain: x1 to x64

○ Amplifier unit (R5F11N and R5F11P only)
- Programmable gain instrumentation amplifier (PGA1): 1 channel (R5F11NL, R5F11PL, and R5F11NG only)
  - Analog input: 1 or 2 channels
  - Variable gain: x12, x16, x20, x24
- Rail-to-rail operational amplifier (AMP0): 1 channel
- General-purpose operational amplifier (AMP1, AMP2): 2 channels (R5F11NL, R5F11PL, and R5F11NG only)

○ D/A converter (R5F11N and R5F11P only)
- 8-bit resolution R-2R resistor ladder D/A converter (DAC0) (AV_{DD} = 2.7 to 5.5 V): 1 channel
- 12-bit resolution R-2R resistor ladder D/A converter (DAC1) (AV_{DD} = 2.7 to 5.5 V): 1 channel (R5F11NL, R5F11PL, and R5F11NG only)

○ 10-bit SAR A/D converter
- 10-bit resolution A/D converter (V_{DD} = 2.4 to 5.5 V[Note 1], V_{DD} = 1.8 to 5.5 V[Note 2])
- Analog input: 3 channels
- Internal reference voltage (TYP. 1.45 V) [Note 4] and temperature sensor [Note 4]

○ I/O ports
- I/O ports: 29 to 63 (N-ch open drain I/O [withstand voltage of 6 V]: 2)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- On-chip clock output/buzzer output controller

○ Others
- On-chip BCD (binary-coded decimal) correction circuit

Note 1. In case of R5F11N and R5F11P.
Note 2. In case of R5F11R.
Note 3. The number in parentheses indicates the number of signal outputs when 8 coms are used.
Note 4. Selectable only in HS (high-speed main) mode.

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

○ ROM, RAM capacities

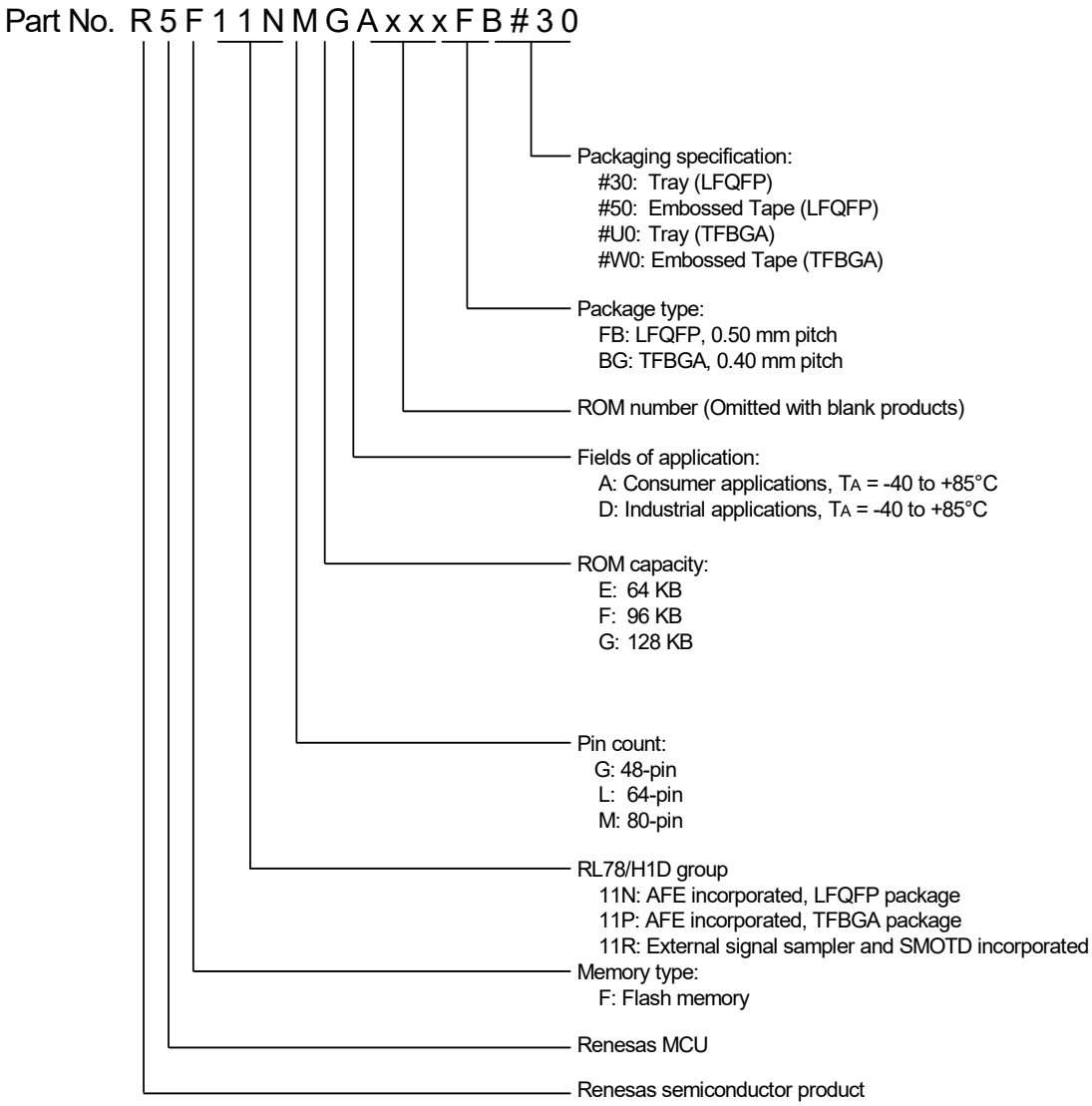
Flash ROM	Data Flash	RAM	RL78/H1D			
			80-pin LFQFP	64-pin LFQFP	64-pin TFBGA	48-pin LFQFP
128 KB	4 KB	5.5 KB	R5F11NMG	R5F11NLG	R5F11PLG	R5F11NGG
96 KB	4 KB	5.5 KB	R5F11NMF	R5F11NLF	R5F11PLF	R5F11NGF
64 KB	4 KB	5.5 KB	R5F11NME	—	—	—
128 KB	4 KB	8 KB	R5F11RMG	—	—	—

1.2 Ordering Information

Pin Count	Package	Fields of Application	Orderable Part Number
80 pins	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	A	R5F11NMGAFB#30, R5F11NMFAFB#30, R5F11NMEAFB#30 R5F11NMGAFB#50, R5F11NMFAFB#50, R5F11NMEAFB#50
64 pins	64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)	A	R5F11NLGAFB#30, R5F11NLFAFB#30 R5F11NLGAFB#50, R5F11NLFAFB#50
64 pins	64-pin plastic TFBGA (4 × 4 mm, 0.4 mm pitch)	A	R5F11PLGABG#U0, R5F11PLFABG#U0 R5F11PLGABG#W0, R5F11PLFABG#W0
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)	A	R5F11NGGAFB#30, R5F11NGFAFB#30 R5F11NGGAFB#50, R5F11NGFAFB#50
80 pins	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	D	R5F11RMGDFB#30, R5F11RMGDFB#50

Remark Products (R5F11PL) in 64-pin TFBGA have the same functionality as those (R5F11NG) in 48-pin LFQFP. The only difference is the package.

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/H1D

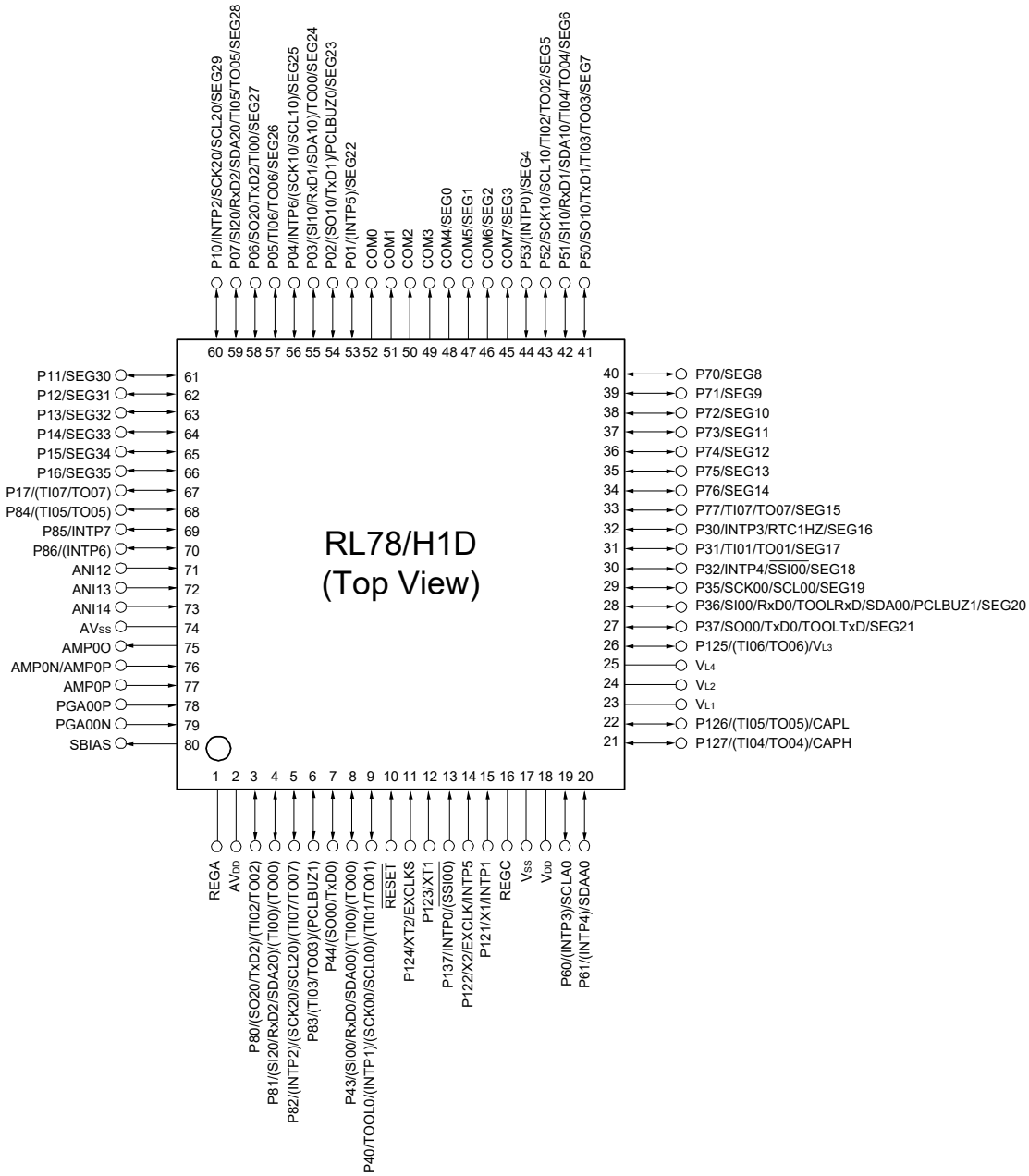


Caution Orderable part numbers are current as of when this manual was published.
Please make sure to refer to the relevant product page on the Renesas website for the latest part numbers.

1.3 Pin Configuration (Top View)

1.3.1 80-pin products (R5F11NM)

• 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)



Caution 1. Connect the REGC pin to VSS pin via a capacitor (0.47 to 1 μF).

Caution 2. Connect the REGA pin to AVSS pin via a capacitor (0.22 μF).

Caution 3. Make the AVSS pin the same potential as the VSS pin.

Caution 4. Make the AVDD pin the same potential as the VDD pin.

Caution 5. Connect the SBIAS pin to AVSS pin via a capacitor (0.22 μF).

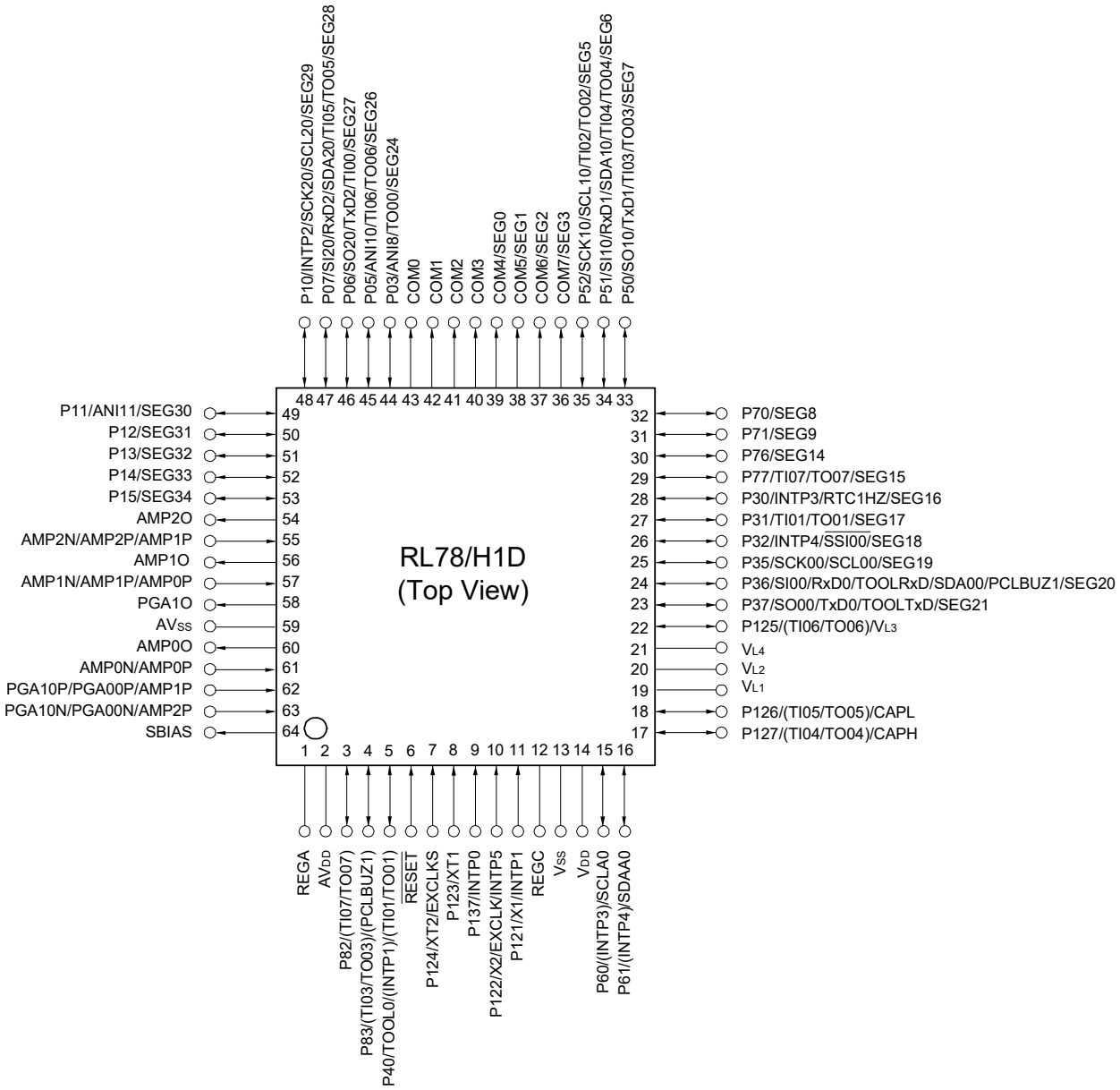
Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).

Remark 3. Set the AMP0P and AMP0N functions in the above figure by the amplifier unit 1 input select register (AMP0S).

1.3.2 64-pin products (R5F11NL)

• 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)

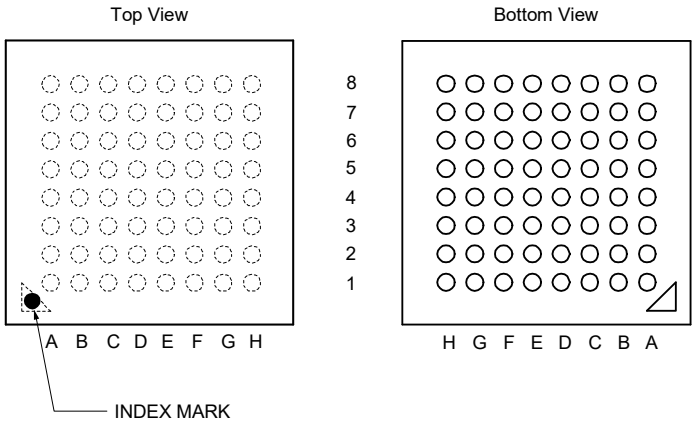


Caution 1. Connect the REGC pin to VSS pin via a capacitor (0.47 to 1 μF).
Caution 2. Connect the REGA pin to AVSS pin via a capacitor (0.22 μF).
Caution 3. Make the AVSS pin the same potential as the VSS pin.
Caution 4. Make the AVDD pin the same potential as the VDD pin.
Caution 5. Connect the SBIAS pin to AVSS pin via a capacitor (0.22 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).
Remark 3. Set the AMP0P and AMP0N functions in the above figure by the amplifier unit 1 input select register (AMP0S).
Set the AMP1P and AMP1N functions in the above figure by the amplifier unit 2 input select register (AMP1S).
Set the AMP2P and AMP2N functions in the above figure by the amplifier unit 3 input select register (AMP2S).

1.3.3 64-pin products (R5F11PL)

• 64-pin plastic TFBGA (4 × 4 mm, 0.4 mm pitch)



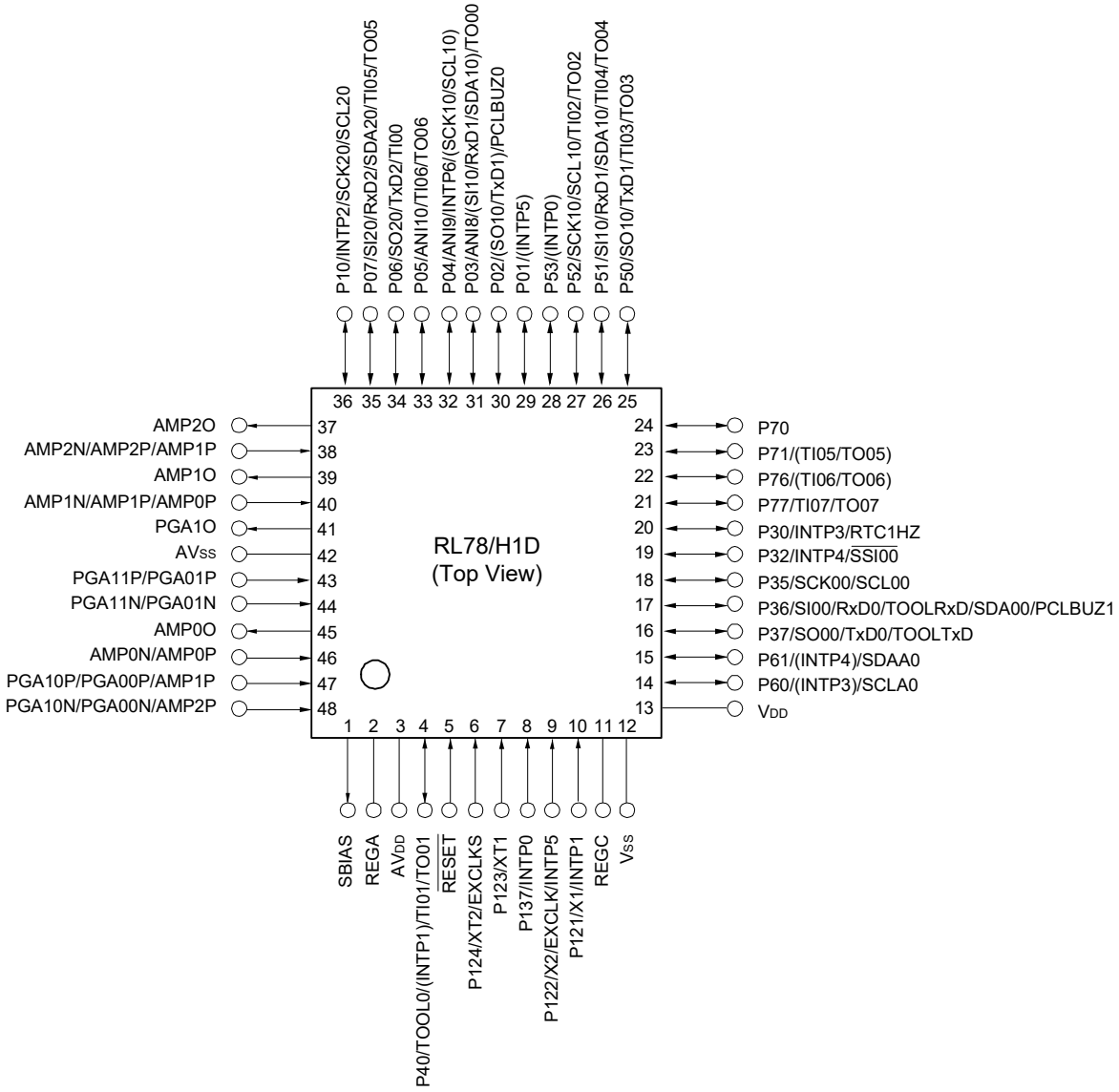
	A	B	C	D	E	F	G	H	
8	Vss	P71/(TI05/ TO05)	P77/TI07/ TO07	P35/SCK00/ SCL00	P36/SI00/ RxD0/ TOOLRxD/ SDA00/ PCLBUZ1	P61/(INTP4)/ SDAA0	VDD	Vss	8
7	P50/SO10/ TxD1/TI03/ TO03	P51/SI10/Rx D1/SDA10/ TI04/TO04	P76/(TI06/ TO06)	P32/INTP4/ $\overline{SSI00}$	P37/SO00/ TxD0/ TOOLTxD	P60/(INTP3)/ SCLA0	Vss	P121/X1/ INTP1	7
6	P53/(INTP0)	P52/SCK10/ SCL10/TI02/ TO02	P70	P30/INTP3/ RTC1HZ	Vss	$\overline{RESET}$	REGC	P122/X2/ EXCLK/ INTP5	6
5	P02/(SO10/ TxD1)/ PCLBUZ0	P03/ANI8/ (SI10/RxD1/ SDA10)/ TO00	P04/ANI9/IN TP6/(SCK10/ SCL10)	P01/(INTP5)	Vss	P40/TOOL0/ (INTP1)/TI01 /TO01	P137/INTP0	P123/XT1	5
4	P05/ANI10/ TI06/TO06	P07/SI20/ RxD2/ SDA20/ TI05/TO05	P06/SO20/ TxD2/TI00	P10/INTP2/ SCK20/ SCL20	Vss	Vss	Vss	P124/XT2/ EXCLKS	4
3	AMP1O	AVss	AVss	AVss	AVss	AVss	REGA	AVDD	3
2	AMP2O	AMP1N/ AMP1P/ AMP0P	PGA11P/ PGA01P	PGA11N/ PGA01N	AMP0N/ AMP0P	AVss	AVss	SBIAS	2
1	AVss	AMP2N/ AMP2P/ AMP1P	PGA1O	AVss	AMP0O	PGA10P/ PGA00P/ AMP1P	PGA10N/ PGA00N/ AMP2P	SBIAS	1
	A	B	C	D	E	F	G	H	

Caution 1. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 µF).
Caution 2. Connect the REGA pin to AVss pin via a capacitor (0.22 µF).
Caution 3. Make the AVss pin the same potential as the Vss pin.
Caution 4. Make the AVDD pin the same potential as the VDD pin.
Caution 5. Connect an SBIAS pin (either of two) to the AVss pin via a capacitor (0.22 µF).

Remark 1. For pin identification, see **1.4 Pin Identification**.
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0, 1, and 3 (PIOR0, PIOR1, and PIOR3).
Remark 3. Set the AMP0P and AMP0N functions in the above figure by the amplifier unit 1 input select register (AMP0S).
Set the AMP1P and AMP1N functions in the above figure by the amplifier unit 2 input select register (AMP1S).
Set the AMP2P and AMP2N functions in the above figure by the amplifier unit 3 input select register (AMP2S).

1.3.4 48-pin products (R5F11NG)

• 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)

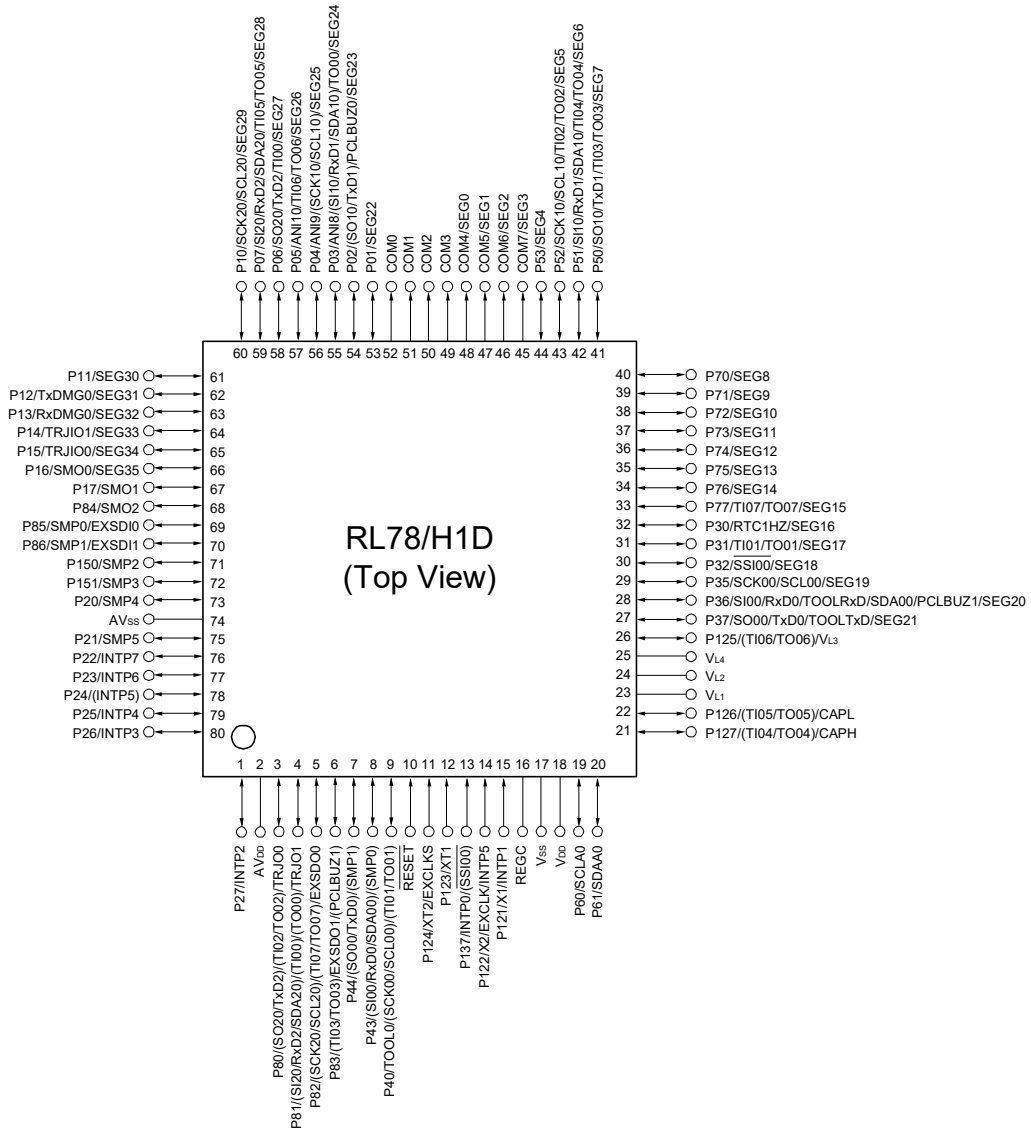


Caution 1. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 µF).
Caution 2. Connect the REGA pin to AVss pin via a capacitor (0.22 µF).
Caution 3. Make the AVss pin the same potential as the Vss pin.
Caution 4. Make the AVDD pin the same potential as the VDD pin.
Caution 5. Connect the SBIAS pin to AVss pin via a capacitor (0.22 µF).

Remark 1. For pin identification, see **1.4 Pin Identification**.
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0, 1, and 3 (PIOR0, PIOR1, and PIOR3).
Remark 3. Set the AMP0P and AMP0N functions in the above figure by the amplifier unit 1 input select register (AMP0S).
Set the AMP1P and AMP1N functions in the above figure by the amplifier unit 2 input select register (AMP1S).
Set the AMP2P and AMP2N functions in the above figure by the amplifier unit 3 input select register (AMP2S).

1.3.5 80-pin products (R5F11RM)

• 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)



Caution 1. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 µF).

Caution 2. Make the AVSS pin the same potential as the VSS pin.

Caution 3. Make the AVDD pin the same potential as the VDD pin.

Remark 1. For pin identification, see **1.4 Pin Identification**.

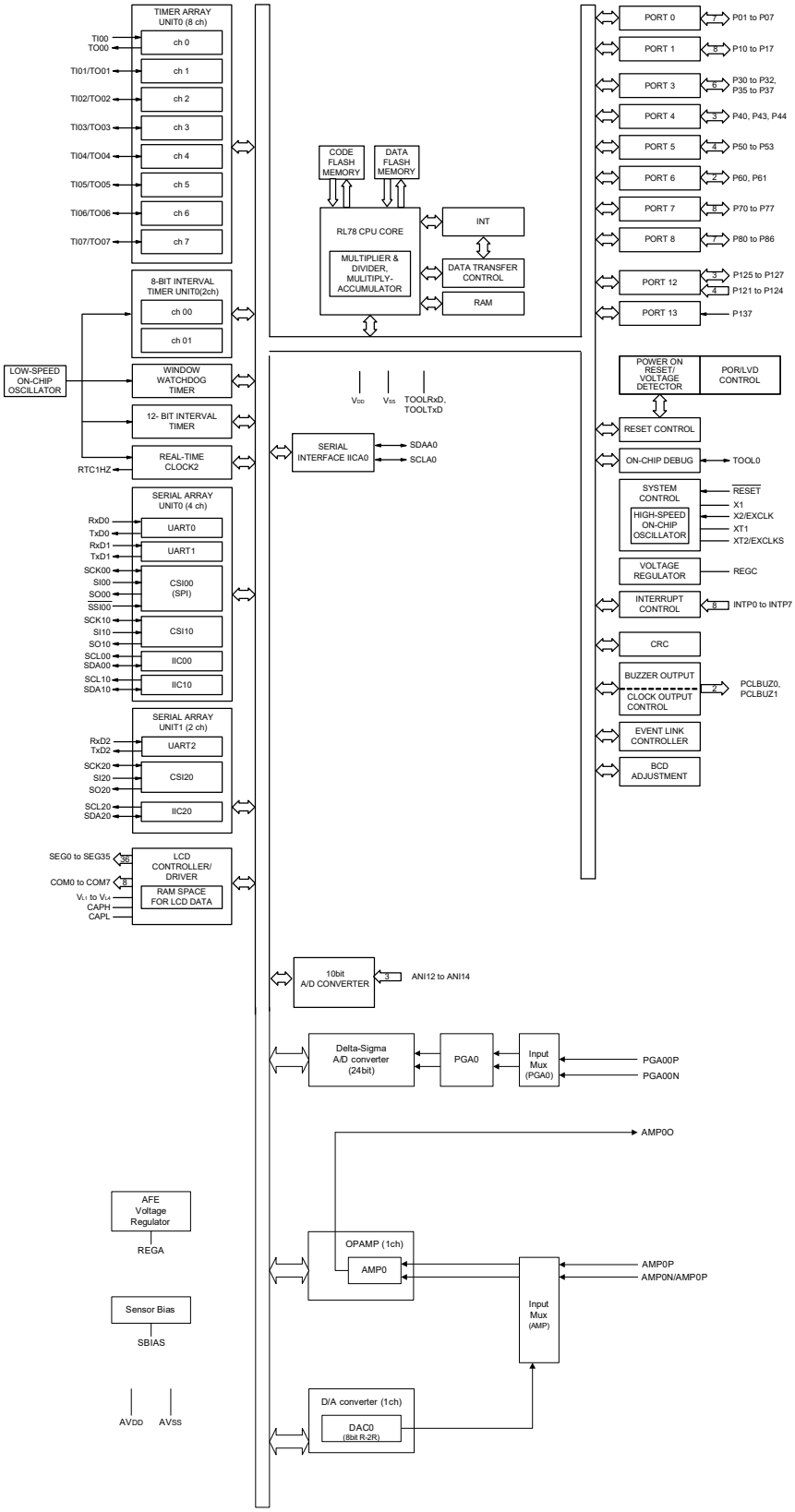
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 3 (PIOR0 to PIOR3).

1.4 Pin Identification

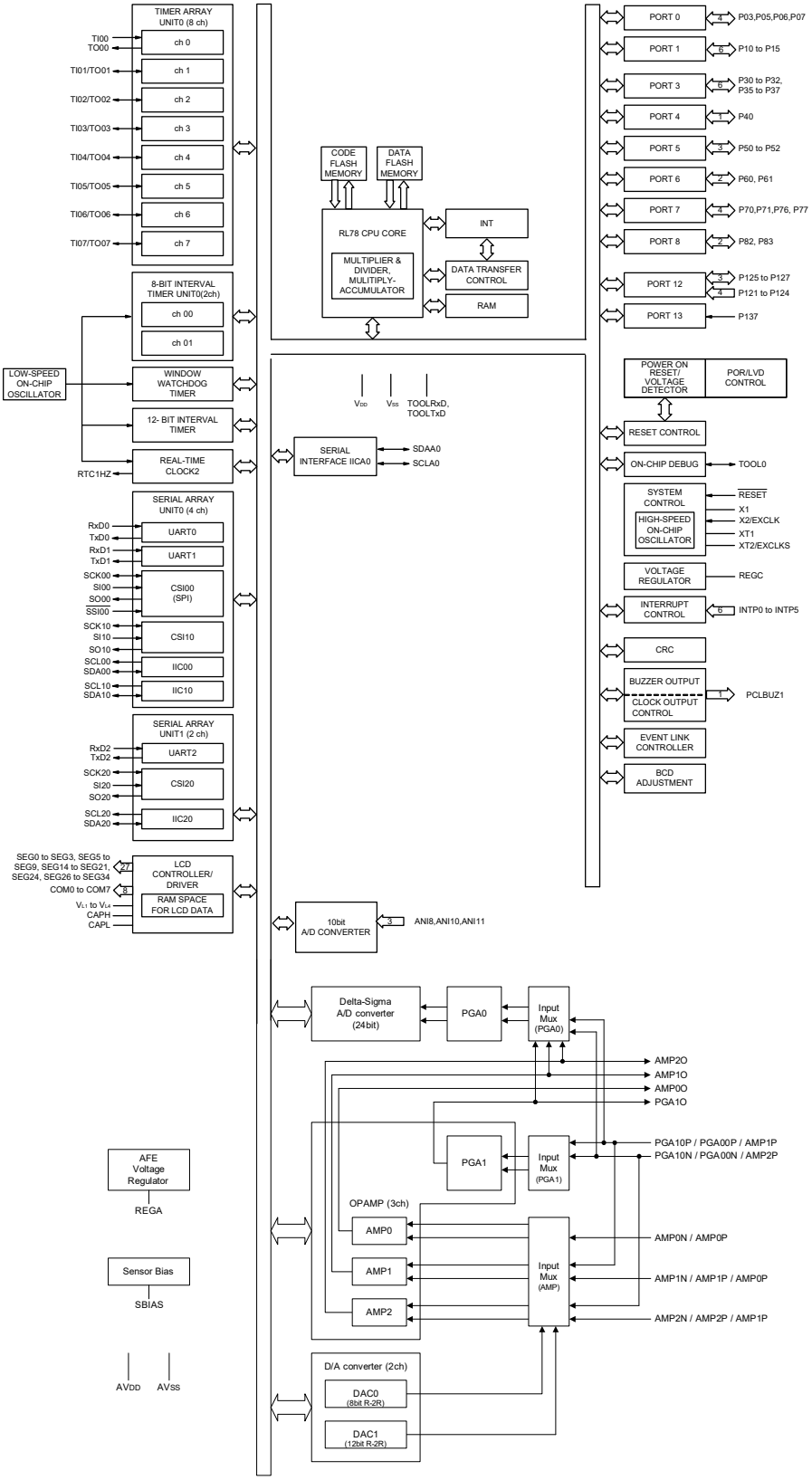
AMP0N to AMP2N :OP AMP Negative Input
AMP0P to AMP2P :OP AMP Positive Input
AMP0O to AMP2O :OP AMP Output
ANI8 to ANI14 :Analog Input
AV_{DD} :Analog Power Supply
AV_{SS} :Analog Ground
CAPH, CAPL :Capacitor for LCD
COM0 to COM7 :LCD Common Output
EXCLK :External Clock Input (Main System Clock)
EXCLKS :External Clock Input (Sub System Clock)
EXSDI0, EXSDI1 :External Sampling Input
EXSDO0, EXSDO1 :External Sampling Clock Output
INTP0 to INTP7 :External Interrupt Input
P01 to P07 :Port 0
P10 to P17 :Port 1
P20 to P27 :Port 2
P30 to P32, P35 to P37 :Port 3
P40, P43, P44 :Port 4
P50 to P53 :Port 5
P60 to P61 :Port 6
P70 to P77 :Port 7
P80 to P86 :Port 8
P121 to P127 :Port 12
P137 :Port 13
P150, P151 :Port 15
PCLBUZ0, PCLBUZ1 :Programmable Clock Output/ Buzzer Output
PGA00N, PGA01N PGA10N, PGA11N :PGA Negative Input
PGA00P, PGA01P PGA10P, PGA11P :PGA Positive Input
PGA1O :PGA Output
REGA :Regulator Capacitance for Analog
REGC :Regulator Capacitance
SBIAS :Reference Voltage Output
$\overline{RESET}$:Reset
RTC1HZ :Real-time Clock Correction
RxD0 to RxD2, RxDMG0 :Receive Data
SCK00, SCK10, SCK20, :Serial Clock Input/Output
SCLA0 :Serial Clock Input/Output
SCL00, SCL10, SCL20 :Serial Clock Output
SDAA0, SDA00, SDA10, SDA20 :Serial Data Input/Output
SEG0 to SEG35 :LCD Segment Output
SI00, SI10, SI20 :Serial Data Input
SO00, SO10, SO20 :Serial Data Output
SSI00 :Slave Select Input
SMP0 to SMP5 :Sampling Input
SMO0 to SMO2 :Sampling Clock Output
TI00 to TI07 :Timer Input
TO00 to TO07,TRJO0, TRJO1 :Timer Output
TOOL0 :Data Input/Output for Tool
TOOLRxD, TOOLTxD :Data Input/Output for External Device
TRJIO0, TRJIO1 :Timer Input/Output
TxD0 to TxD2, TxDMG0 :Transmit Data
V_{DD} :Power Supply
V_{L1} to V_{L4} :LCD Power Supply
V_{SS} :Ground
X1, X2 :Crystal Oscillator (Main System Clock)
XT1, XT2 :Crystal Oscillator (Subsystem Clock)

1.5 Block Diagram

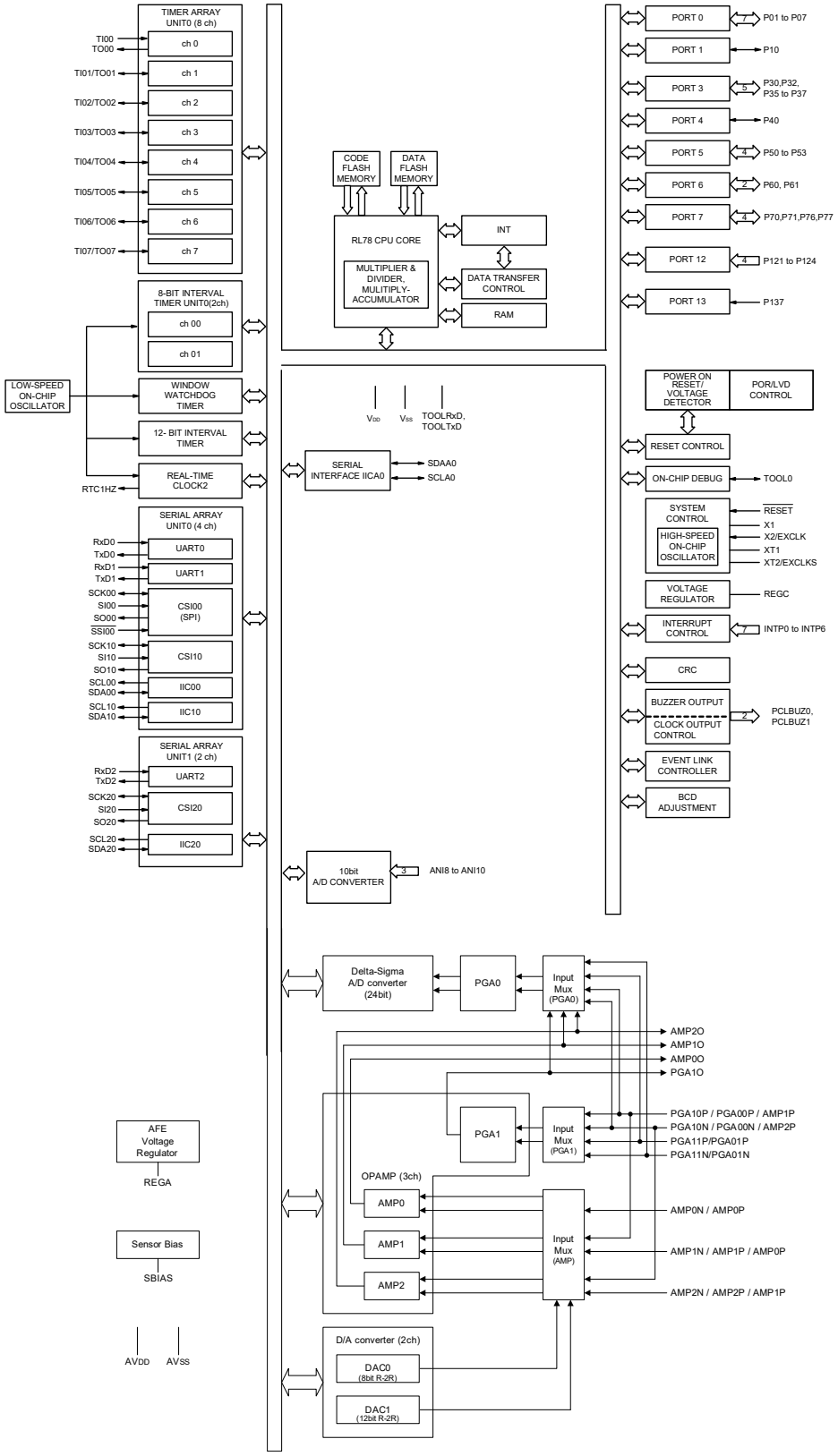
1.5.1 80-pin products (R5F11NM)



1.5.2 64-pin products (R5F11NL)

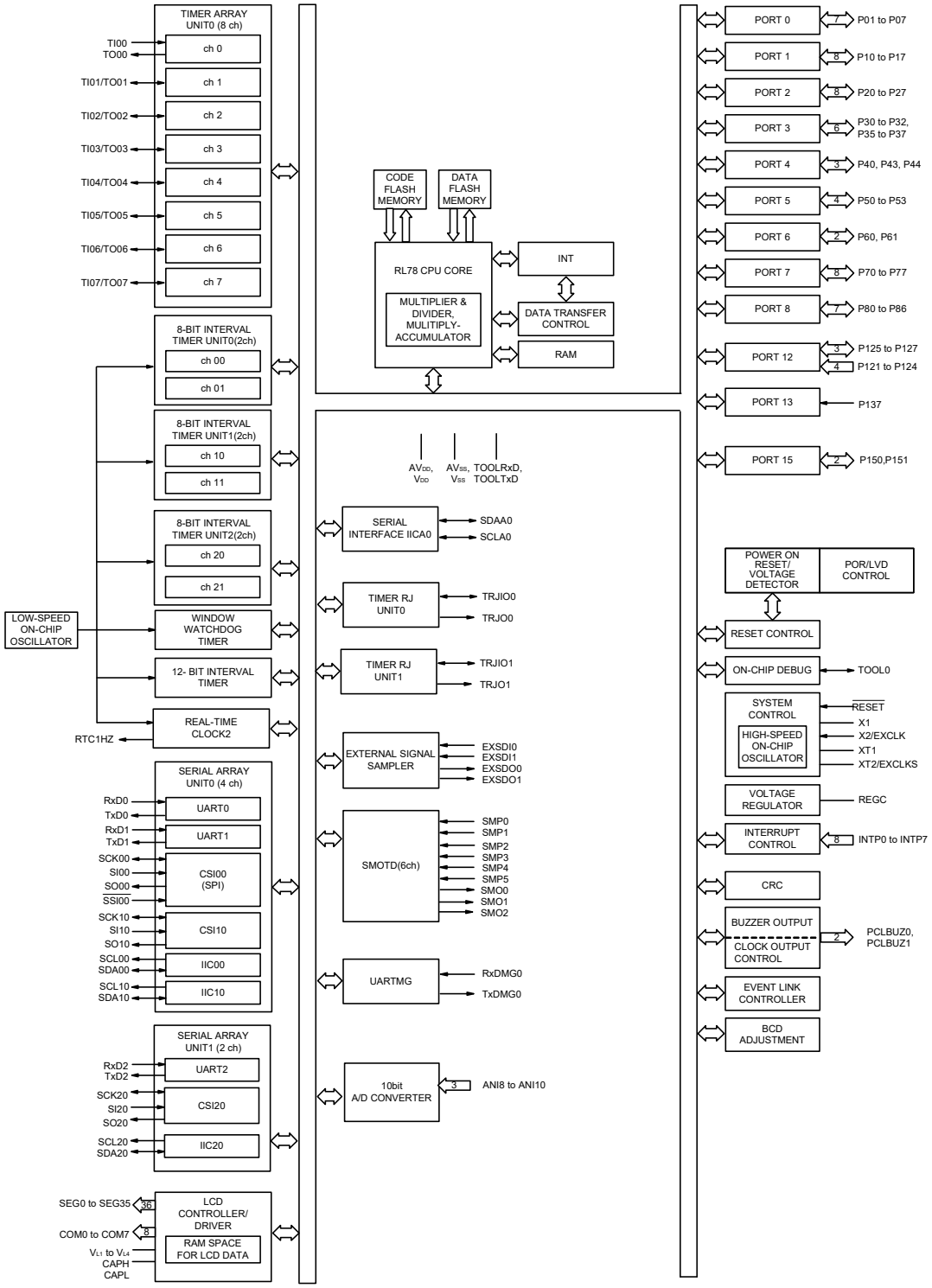


1.5.3 64-pin products (R5F11PL), 48-pin products (R5F11NG)



Remark 64-pin products (R5F11PL) have the same functionality as 48-pin products (R5F11NG). The only difference is the package.

1.5.4 80-pin products (R5F11RM)



1.6 Outline of Functions

(1/3)

Item		80-pin LFQFP	64-pin LFQFP	64-pin TFBGA 48-pin LFQFP	80-pin LFQFP
		R5F11NMx (x = E to G)	R5F11NLx (x = F, G)	R5F11PLx, R5F11NGx (x = F, G)	R5F11RMG
Code flash memory (KB)		64 to 128	96 to 128	96 to 128	128
Data flash memory (KB)		4	4	4	4
RAM (KB)		5.5	5.5	5.5	8
Memory space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)			
		1 to 20 MHz: VDD = 2.7 to 5.5 V, 1 to 8 MHz: VDD = 2.4 to 2.7 V			1 to 20 MHz: VDD = 2.7 to 5.5 V, 1 to 8 MHz: VDD = 1.8 to 2.7 V
	High-speed on-chip oscillator clock	HS (high-speed main) operation mode: 1 to 24 MHz (VDD = 2.7 to 5.5 V), HS (high-speed main) operation mode: 1 to 16 MHz (VDD = 2.4 to 5.5 V)			HS (high-speed main) operation mode: 1 to 24 MHz (VDD = 2.7 to 5.5 V), HS (high-speed main) operation mode: 1 to 16 MHz (VDD = 2.4 to 5.5 V), LS (low-speed main) operation mode: 1 to 8 MHz (VDD = 1.8 to 5.5 V)
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS)			
		32.768 kHz (TYP.): VDD = 2.4 to 5.5 V			32.768 kHz (TYP.): VDD = 1.8 to 5.5 V 38.4 kHz (TYP.): VDD = 1.8 to 5.5 V
Low-speed on-chip oscillator clock		15 kHz (TYP.): VDD = 2.4 to 5.5 V			15 kHz (TYP.): VDD = 1.8 to 5.5 V
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator clock: fIH = 24 MHz operation)			
		0.05 μs (High-speed system clock: fMX = 20 MHz operation)			
		30.5 μs (Subsystem clock: fSUB = 32.768 kHz operation)			
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	53	36	29	63
	CMOS I/O	46	29	22	56
	CMOS input	5	5	5	5
	CMOS output	—	—	—	—
	N-ch open-drain I/O (6 V tolerance)	2	2	2	2

(2/3)

Item		80-pin LFQFP R5F11NMx (x = E to G)	64-pin LFQFP R5F11NLx (x = F, G)	64-pin TFBGA 48-pin LFQFP R5F11PLx, R5F11NGx (x = F, G)	80-pin LFQFP R5F11RMG
Timer	16-bit timer TAU	8 channels (Timer outputs: 8, PWM outputs: 7 Note 1)			
	8-bit or 16-bit interval timer	2 channels (8 bits)/1 channel (16 bits)			6 channels (8 bits)/3 channels (16 bits)
	Watchdog timer	1 channel			
	12-bit interval timer	1 channel			
	Real-time clock 2	1 channel			
	RTC output	1 1 Hz (subsystem clock: fSUB = 32.768 kHz)			
	16-bit timer RJ	—			2 channels, timer outputs: 2
	External signal sampler	—			1 channel
	Sampling output timer detector (SMOTD)	—			Input: 6 channels Output: 3 channels
Clock output/buzzer output		2	1	2	2
		• 2.44 kHz, 4.88 kHz, 9.77 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: fMAIN = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: fSUB = 32.768 kHz operation)			
8/10-bit resolution A/D converter	Internal	3 channels			
	External	2 channels: Internal reference voltage (1.45 V), temperature sensor output voltage (only selectable in HS (high-speed main) mode)			
24-bit ΔΣ A/D converter with programmable gain instrumentation amplifier 0 (PGA0)		Analog input: 1 channel (differential or single-ended)	Analog input: 1 channel (differential or single-ended), 3 channels (single-ended)	Analog input: 2 channels (differential or single-ended), 3 channels (single-ended)	—
D/A converter	12-bit	—	1 channel (with an output amplifier but no external output pin)	1 channel (with an output amplifier but no external output pin)	—
	8-bit	1 channel (without an output amplifier and no external output pin)	1 channel (without an output amplifier and no external output pin)	1 channel (without an output amplifier and no external output pin)	—
Programmable gain instrumentation amplifier 1 (PGA1)		—	1 channel	1 channel	—
Rail-to-rail operational amplifier		1 channel	1 channel	1 channel	—
General-purpose operational amplifier		—	2 channels	2 channels	—
Serial interface		• CSI (SPI supported): 1 channel/UART (LIN-bus supported): 1 channel/simplified I2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I2C: 1 channel			
	I2C bus	1 channel			1 channel
	Serial interface UARTMG	—			1 channel

(3/3)

Item		80-pin LFQFP	64-pin LFQFP	64-pin TFBGA 48-pin LFQFP	80-pin LFQFP
		R5F11NMx (x = E to G)	R5F11NLx (x = F, G)	R5F11PLx, R5F11NGx (x = F, G)	R5F11RMG
LCD controller/driver		Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.			
	Segment signal output	36 (32) Note 2	27 (23) Note 2	—	36 (32) Note 2
	Common signal output	4 (8) Note 2	4 (8) Note 2	—	4 (8) Note 2
Data transfer controller (DTC)		26 sources	24 sources	25 sources	35 sources
Event link controller (ELC)		Event input: 20, Event trigger output: 7	Event input: 18, Event trigger output: 10	Event input: 19, Event trigger output: 10	Event input: 26, Event trigger output: 5
Vectored interrupt sources	Internal	29	29	29	43
	External	8	6	7	8
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note 3 • Internal reset by RAM parity error • Internal reset by illegal-memory access			
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V • Power-down-reset: 1.50 ±0.04 V			
Voltage detector		• Rising edge: 2.50 V to 4.06 V (9 stages) • Falling edge: 2.45 V to 3.98 V (9 stages)			• Rising edge: 1.88 V to 4.06 V (12 stages) • Falling edge: 1.84 V to 3.98 V (12 stages)
On-chip debug function		Provided			
Power supply voltage		V_{DD} = 2.4 to 5.5 V (10-bit SAR A/D converter: 2.4 to 5.5 V, operating voltage of the analog front-end (AFE): 2.7 to 5.5 V)			V_{DD} = 1.8 to 5.5 V
Operating ambient temperature		T_A = -40 to +85°C (A: Consumer applications)			T_A = -40 to +85°C (D: Industrial applications)

Note 1. The number of outputs depends on the setting of channels in use and the number of the master.

Note 2. The number in parentheses indicates the number of signal outputs when 8 coms are used.

Note 3. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS (R5F11N, R5F11P) (A: TA = -40 to +85°C)

This chapter describes the electrical specifications for the products A: Consumer applications (TA = -40 to +85°C).

Caution 1. The RL78 microcontroller has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2 Functions other than port pins in the User's Manual: Hardware.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings **(1/3)**

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +6.5	V
	AV_{DD}	AV_{DD} = V_{DD}	-0.5 to +6.5	V
	AV_{SS}	AV_{SS} = V_{SS}	-0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V_{DD} + 0.3 Note 1	V
REGA pin input voltage	V_{IREGA}	REGA	-0.3 to +2.8 and -0.3 to AV_{DD} + 0.3 Note 2	V
Input voltage	V_{I1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P121 to P124, P125 to P127, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to V_{DD} + 0.3 Note 3	V
	V_{I2}	P60, P61 (N-ch open-drain)	-0.3 to +6.5	V
Output voltage	V_{O1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P60, P61, P70 to P77, P80 to P86, P125 to P127	-0.3 to V_{DD} + 0.3 Note 3	V
Analog input voltage	V_{AI1}	ANI8 to ANI11	-0.3 to V_{DD} + 0.3 Note 3	V
	V_{AI2}	ANI12 to ANI14 PGA00P, PGA01P, PGA10P, PGA11P, PGA00N, PGA01N, PGA10N, PGA11N, AMP0P to AMP2P, AMP0N to AMP2N	-0.3 to AV_{DD} + 0.3 Note 3	V
Analog output voltage	V_{OA}	SBIAS, PGA1O, AMP0O to AMP2O	-0.3 to AV_{DD} + 0.3 Note 3	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Connect the REGA pin to AV_{SS} via a capacitor (0.22 μF). This value regulates the absolute maximum rating of the REGA pin. Do not use this pin with voltage applied to it.

Note 3. Must be 6.5 V or lower.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. The reference voltage is V_{SS} (for the V_{DD} systems) = AV_{SS} (for the AV_{DD} systems)

Absolute Maximum Ratings **(2/3)**

Parameter	Symbols	Conditions		Ratings	Unit
LCD voltage	V_{LI1}	V_{L1} input voltage Note 1		-0.3 to +2.8	V
	V_{LI2}	V_{L2} input voltage Note 1		-0.3 to +6.5	V
	V_{LI3}	V_{L3} input voltage Note 1		-0.3 to +6.5	V
	V_{LI4}	V_{L4} input voltage Note 1		-0.3 to +6.5	V
	V_{LI5}	CAPL, CAPH input voltage Note 1		-0.3 to +6.5	V
	V_{LO1}	V_{L1} output voltage		-0.3 to +2.8	V
	V_{LO2}	V_{L2} output voltage		-0.3 to +6.5	V
	V_{LO3}	V_{L3} output voltage		-0.3 to +6.5	V
	V_{LO4}	V_{L4} output voltage		-0.3 to +6.5	V
	V_{LO5}	CAPL, CAPH output voltage		-0.3 to +6.5	V
	V_{LO6}	COM0 to COM7 SEG0 to SEG35 output voltage	External resistance division method	-0.3 to V_{DD} + 0.3 Note 2	V
			Capacitor split method	-0.3 to V_{DD} + 0.3 Note 2	V
			Internal voltage boosting method	-0.3 to V_{LI4} + 0.3 Note 2	V

Note 1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 µF ± 30%) and connect a capacitor (0.47 µF ± 30%) between the CAPL and CAPH pins.

Note 2. Must be 6.5 V or lower.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Absolute Maximum Ratings **(3/3)**

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin		-40	mA
		Total of all pins -170 mA	P40, P43, P44, P80 to P83	-70	mA
			P01 to P07, P10 to P17, P30 to P32, P35 to P37, P50 to P53, P70 to P77, P84 to P86, P125 to P127	-100	mA
Output current, low	I_{OL1}	Per pin		40	mA
		Total of all pins 170 mA	P40, P43, P44, P80 to P83	70	mA
			P01 to P07, P10 to P17, P30 to P32, P35 to P37, P50 to P53, P60, P61, P70 to P77, P84 to P86, P125 to P127	100	mA
Operating ambient temperature	T_A	In normal operation mode		-40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1 and XT1 oscillator characteristics

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
XT1 clock oscillation frequency (f_{XT}) Note	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark When using the X1 and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the User's Manual: Hardware.

2.2.2 On-chip oscillator characteristics

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Oscillators	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}	2.7 V ≤ V_{DD} ≤ 5.5 V		1		24	MHz
		2.4 V ≤ V_{DD} < 2.7 V		1		16	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	2.4 V ≤ V_{DD} ≤ 5.5 V	-1.0		+1.0	%
		-40 to +85°C	2.4 V ≤ V_{DD} ≤ 5.5 V	-1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127				-10.0 Note 2	mA
		Total of P40, P43, P44, P80 to P83 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			-55	mA
			2.7 V ≤ V_{DD} < 4.0 V			-10	mA
			2.4 V ≤ V_{DD} < 2.7 V			-5	mA
		Total of P01 to P07, P10 to P17, P30 to P32, P35 to P37, P50 to P53, P70 to P77, P84 to P86, P125 to P127 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			-69	mA
			2.7 V ≤ V_{DD} < 4.0 V			-23	mA
			2.4 V ≤ V_{DD} < 2.7 V			-12	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4 V ≤ V_{DD} ≤ 5.5 V			-124	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin (I_{OH1}) to an output pin.

Note 2. However, do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –10.0 mA
Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P02 to P04, P06, P07, P10, P35 to P37, P40, P43, P44, P50 to P52, and P80 to P82 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127				20.0 Note 2	mA
		Per pin for P60 and P61				15.0 Note 2	mA
		Total of P40, P43, P44, P80 to P83 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			70	mA
			2.7 V ≤ V_{DD} < 4.0 V			15	mA
			2.4 V ≤ V_{DD} < 2.7 V			9	mA
		P01 to P07, P10 to P17, P30 to P32, P35 to P37, P50 to P53, P60, P61, P70 to P77, P84 to P86, P125 to P127 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			90	mA
			2.7 V ≤ V_{DD} < 4.0 V			35	mA
			2.4 V ≤ V_{DD} < 2.7 V			20	mA
		Total of all pins (When duty ≤ 70% Note 3)				160	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin (I_{OL1}).

Note 2. However, do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127	Normal input buffer	0.8 V_{DD}		V_{DD}	V
	V_{IH2}	For TTL mode supported ports	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			TTL input buffer 2.4 V ≤ V_{DD} < 3.3 V	1.50		V_{DD}	V
	V_{IH4}	P60, P61		0.7 V_{DD}		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P60, P61, P70 to P77, P80 to P86, P125 to P127	Normal input buffer	0		0.2 V_{DD}	V
	V_{IL2}	For TTL mode supported ports	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 2.4 V ≤ V_{DD} < 3.3 V	0		0.32	V
	V_{IL4}	P60, P61		0		0.3 V_{DD}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V

Caution The maximum value of V_{IH} of pins P02 to P04, P06, P07, P10, P35 to P37, P40, P43, P44, P50 to P52, and P80 to P82 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -10.0 mA	V_{DD} - 1.5			V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -3.0 mA	V_{DD} - 0.7			V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -2.0 mA	V_{DD} - 0.6			V
			2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -1.5 mA	V_{DD} - 0.5			V
Output voltage, low	V_{OL1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 20.0 mA			1.3	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 3.0 mA			0.6	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 1.5 mA			0.4	V
			2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 0.6 mA			0.4	V
	V_{OL3}	P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 15.0 mA			2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 5.0 mA			0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 3.0 mA			0.4	V
			2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 2.0 mA			0.4	V

Caution **P02 to P04, P06, P07, P10, P35 to P37, P40, P43, P44, P50 to P52, and P80 to P82 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P60, P61, P70 to P77, P80 to P86, P125 to P127, P137, $\overline{\text{RESET}}$	V_I = V_{DD}				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I = V_{DD}	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P60, P61, P70 to P77, P80 to P86, P125 to P127, P137, $\overline{\text{RESET}}$	V_I = V_{SS}				-1	μA
	I_{LIL3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I = V_{SS}	In input port or external clock input			-1	μA
				In resonator connection			-10	μA
On-chip pull-up resistance	R_{U1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127	V_I = V_{SS} or In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Notes 1, Note 6	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 5.0 V		1.7		mA
						V_{DD} = 3.0 V		1.7		
					Normal operation	V_{DD} = 5.0 V		3.7	6.2	
						V_{DD} = 3.0 V		3.7	6.2	
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.8	4.8	
						V_{DD} = 3.0 V		2.8	4.8	
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.1	5.2	mA
						Resonator connection		3.3	5.3	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.0	5.2	
						Resonator connection		3.3	5.3	
				f_{MX} = 16 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.6	4.5	
						Resonator connection		2.8	4.6	
				f_{MX} = 16 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.6	4.5	
						Resonator connection		2.8	4.6	
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		1.9	3.0	
						Resonator connection		1.9	3.0	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.9	3.0	
						Resonator connection		1.9	3.0	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		4.3	5.8	μA
						Resonator connection		4.6	5.8	
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.3	5.8	
						Resonator connection		4.6	5.8	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		4.5	7.6	
						Resonator connection		4.5	7.6	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		4.7	9.2	
						Resonator connection		5.1	9.2	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		5.2	12.6	
						Resonator connection		5.7	12.6	

Note 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.The current flowing into AFE is not included.

Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3. When high-speed system clock and subsystem clock are stopped.

Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and watchdog timer.

Note 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Note 6. I_{DD1} do not include the current flowing to the AFE.
The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and AFE current (AV_{DD} systems) when the AFE operates in the operating mode, HALT mode, or STOP mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C.

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Notes 1, Note 9	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.42	1.83	mA
					V_{DD} = 3.0 V		0.42	1.83	
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.39	1.38	
					V_{DD} = 3.0 V		0.39	1.38	
			HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.26	1.55	mA
					Resonator connection		0.40	1.68	
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.25	1.55	
					Resonator connection		0.40	1.68	
				f_{MX} = 16 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.23	1.22	
					Resonator connection		0.36	1.39	
				f_{MX} = 16 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.22	1.22	
					Resonator connection		0.35	1.39	
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.19	0.82	
					Resonator connection		0.29	0.90	
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.18	0.82	
					Resonator connection		0.28	0.90	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5 T_A = -40°C	Square wave input		0.32	0.69	µA
					Resonator connection		0.51	0.89	
				f_{SUB} = 32.768 kHz Note 5 T_A = +25°C	Square wave input		0.41	0.82	
					Resonator connection		0.62	1.00	
				f_{SUB} = 32.768 kHz Note 5 T_A = +50°C	Square wave input		0.52	1.40	
					Resonator connection		0.75	1.60	
				f_{SUB} = 32.768 kHz Note 5 T_A = +70°C	Square wave input		0.82	2.70	
					Resonator connection		1.08	2.90	
				f_{SUB} = 32.768 kHz Note 5 T_A = +85°C	Square wave input		1.38	4.95	
					Resonator connection		1.62	5.15	
	I_{DD3} Note 6	STOP mode Note 8	T_A = -40°C				0.20	0.59	µA
			T_A = +25°C				0.26	0.72	
			T_A = +50°C				0.33	1.30	
			T_A = +70°C				0.53	2.60	
			T_A = +85°C				0.93	4.85	

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.The current flowing into AFE is not included.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the real-time clock 2 is included. However, not including the current flowing into the 12-bit interval timer, 8-bit interval timer, and watchdog timer.

Note 6. Not including the current flowing into the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and watchdog timer.

Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz

2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Note 9. I_{DD2} and I_{DD3} do not include the current flowing to the AFE.

The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and AFE current (AV_{DD} systems) when the AFE operates in the operating mode, HALT mode, or STOP mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C.

• Peripheral functions

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1						0.20		μA
RTC2 operating current	I_{RTC} Notes 1, 3	f_{SUB} = 32.768 kHz					0.02		μA
12-bit interval timer operating current	I_{TMKA} Notes 1, 2, 4	f_{SUB} = 32.768 kHz, f_{MAIN} stopped					0.02		μA
8-bit interval timer operating current	I_{TMRT} Notes 1, 14	f_{SUB} = 32.768 kHz, f_{MAIN} stopped, per unit		8-bit counter mode × 2-channel operation			0.12		μA
				16-bit counter mode operation			0.10		μA
Watchdog timer operating current	I_{WDT} Notes 1, 5	f_{IL} = 15 kHz					0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed		Normal mode, V_{DD} = 5.0 V			1.3	1.7	mA
				Low-voltage mode, V_{DD} = 3.0 V			0.5	0.7	mA
Internal reference voltage (1.45 V) current	I_{ADREF} Notes 1, 7						85		μA
Temperature sensor operating current	I_{TMPS} Note 1						85		μA
LVD operating current	I_{LVI} Notes 1, 8						0.06		μA
Self-programming operating current	I_{FSP} Notes 1, 9						2.0	12.2	mA
BGO operating current	I_{BGO} Notes 1, 10						2.0	12.2	mA
SNOOZE operating current	I_{SNOZ} Notes 1, 11	A/D converter operation		The mode is performed			0.50	0.60	mA
				During A/D conversion, low-voltage mode, V_{DD} = 3.0 V			1.20	1.44	
		CSI/UART operation					0.70	0.84	mA
		DTC operation					3.1		mA
LCD operating current	I_{LCD1} Notes 12, 13	External resistance division method	f_{LCD} = f_{SUB} LCD clock = 128 Hz	1/3 bias 4-time slice	V_{DD} = 5.0 V, V_{L4} = 5.0 V		0.04	0.20	μA
	I_{LCD2} Note 12	Internal voltage boosting method	f_{LCD} = f_{SUB} LCD clock = 128 Hz	1/3 bias 4-time slice	V_{DD} = 3.0 V, V_{L4} = 3.0 V (VLCD = 04H)		0.85	2.20	μA
					V_{DD} = 5.0 V, V_{L4} = 5.1 V (VLCD = 04H)		1.55	3.70	μA
	I_{LCD3} Note 12	Capacitor split method	f_{LCD} = f_{SUB} LCD clock = 128 Hz	1/3 bias 4-time slice	V_{DD} = 3.0 V, V_{L4} = 3.0 V		0.20	0.50	μA

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Current flowing to V_{DD}.

Note 2. When high speed on-chip oscillator and high-speed system clock are stopped.

Note 3. Current flowing only to the real-time clock 2 (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock 2 operates in the operating mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock 2.

Note 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{TMKA}, when the 12-bit interval timer operates in the operating mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the 12-bit interval timer.

Note 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{WDT} when the watchdog timer operates in STOP mode.

Note 6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC}, I_{ADREF} when the A/D converter operates in the operating mode or the HALT mode.

Note 7. Operation current flowing to the internal reference voltage.

Note 8. Current flowing only to the LVD circuit. The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{LVI} when the LVD circuit operates in the operating mode, HALT mode, or STOP mode.

Note 9. Current flowing only during self-programming.

Note 10. Current flowing only during data flash rewrite.

Note 11. For shift time to the SNOOZE mode, see **27.3.3 SNOOZE mode** in the User's Manual: Hardware.

Note 12. Current flowing only to the LCD controller/driver (V_{DD} pin). The current value of the RL78 microcontrollers is the sum of the LCD operating current (I_{LCD1}, I_{LCD2}, or I_{LCD3}) and the supply current (I_{DD1} or I_{DD2}) when the LCD controller/driver operates in the operating mode or HALT mode. Not including the current that flows through the LCD panel.

Note 13. Not including the current that flows through the external divider resistor.

Note 14. Current flowing only to the 8-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 8-bit interval timer operates in the operating mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 3. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 4. Temperature condition of the TYP. value is T_A = 25°C

• AFE functions

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
24-bit ΔΣ A/D converter operating current	I_{DSAD}	Normal mode Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, VREFAMP, PGA0, 24-bit ΔΣ A/D converter, and digital filter Differential input mode, OSR = 256, SBIAS I_{OUT} = 0 mA		0.94	1.46	mA
		Low power mode Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, VREFAMP, PGA0, 24-bit ΔΣ A/D converter, and digital filter Differential input mode, OSR = 256, SBIAS I_{OUT} = 0 mA		0.60	0.91	mA
Amplifier operating current	I_{PGA1}	Low power mode Notes 1, 2 Circuits that operate: ABGR, PGA1, and DAC1 I_L = 0 mA		0.60	1.10	mA
		High-speed mode Notes 1, 2 Circuits that operate: ABGR, PGA1, and DAC1 I_L = 0 mA		1.10	1.80	mA
	I_{AMP0}	Low power mode Notes 1, 2 Circuits that operate: ABGR and AMP0 I_L = 0 mA		0.10	0.15	mA
		High-speed mode Notes 1, 2 Circuits that operate: ABGR and AMP0 I_L = 0 mA		0.30	0.48	mA
	I_{AMP1}, I_{AMP2}	Low power mode Notes 1, 2 Circuits that operate: ABGR and AMP1 or AMP2 I_L = 0 mA		0.10	0.14	mA
		High-speed mode Notes 1, 2 Circuits that operate: ABGR and AMP1 or AMP2 I_L = 0 mA		0.23	0.35	mA
8-bit D/A converter operating current	I_{DAC0}	SBIAS normal mode Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, and DAC0 Note 3 I_L = 0 mA, SBIAS I_{OUT} = 0 mA		1.00	1.50	mA
		SBIAS low-power mode Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, and DAC0 Note 3 I_L = 0 mA, SBIAS I_{OUT} = 0 mA		0.85	1.30	mA
12-bit D/A converter operating current	I_{DAC1}	When AV_{DD} is selected as the reference voltage Notes 1, 2 Circuits that operate: ABGR and DAC1 I_L = 0 mA		0.61	0.97	mA
		When SBIAS (normal mode) is selected as the reference voltage Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, and DAC1 Note 3 I_L = 0 mA, SBIAS I_{OUT} = 0 mA		1.06	1.62	mA
		When SBIAS (low-power mode) is selected as the reference voltage Notes 1, 2 Circuits that operate: ABGR, REGA, SBIAS, and DAC1 Note 3 I_L = 0 mA, SBIAS I_{OUT} = 0 mA		0.91	1.42	mA

Note 1. Current flowing to AV_{DD}. The typical conditions are the conditions when T_A = 25°C and AV_{DD} = 3.3 V.

Note 2. Current flowing only into the operating circuit indicated in the column for conditions.

Note 3. Including the static current of VREFAMP, PGA0, and 24-bit ΔΣ A/D converter.

Remark Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.

2.4 AC Characteristics

2.4.1 Basic operation

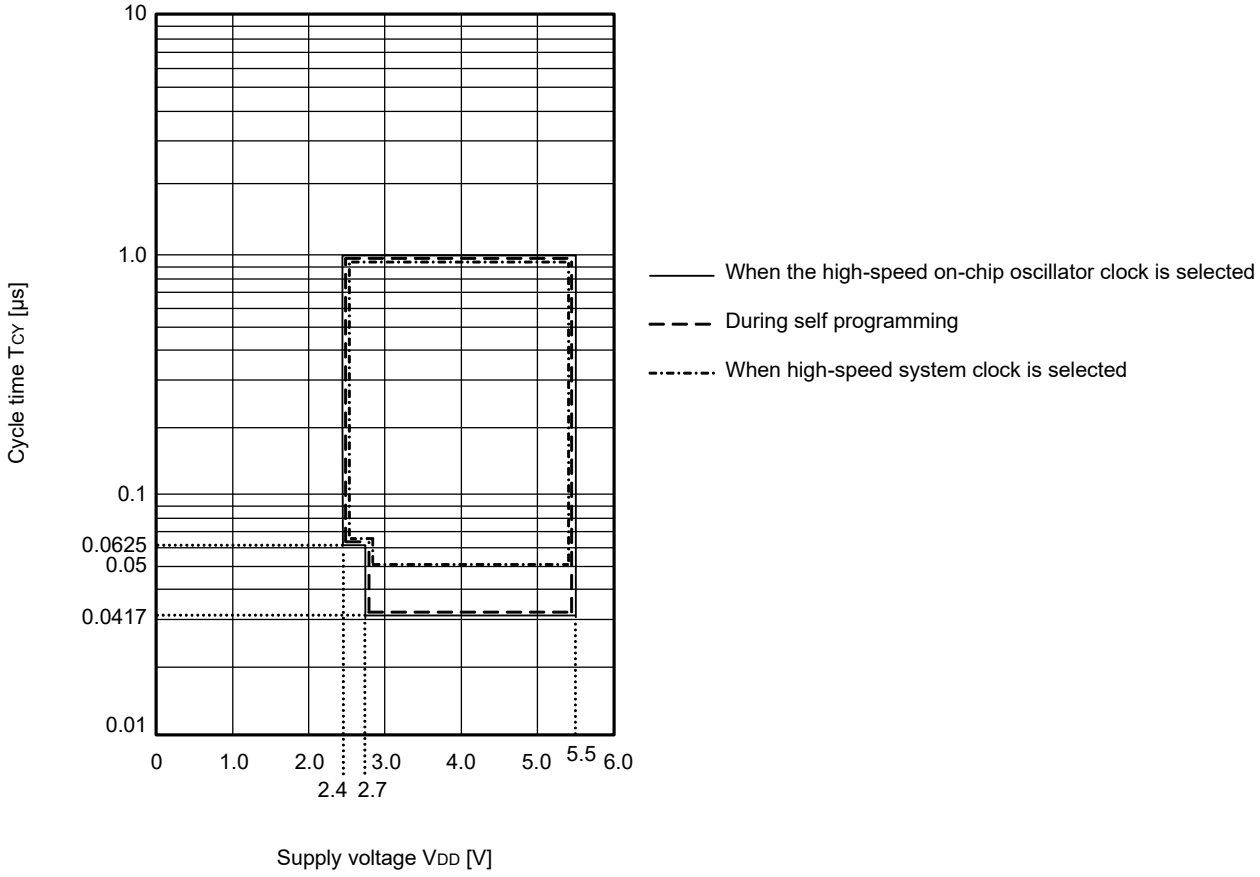
(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.0417		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
		Subsystem clock (f_{SUB}) operation	f_{XT} =32.768 kHz	2.4 V ≤ V_{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self-programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.0417		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
External main system clock frequency	f_{EX}	EXCLK		2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
				2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	MHz
	f_{EXT}	EXCLKS			32		35	kHz
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	EXCLK		2.7 V ≤ V_{DD} ≤ 5.5 V	24			ns
				2.4 V ≤ V_{DD} < 2.7 V	30			ns
	t_{EXHS}, t_{EXLS}	EXCLKS			13.7			μs
Timer input high-level width, low-level width	t_{TIH}, t_{TIL}	TI00 to TI07			1/f_{MCK} + 10			ns
Timer output frequency	f_{TO}	TO00 to TO07	HS (high-speed main) mode	4.0 V ≤ V_{DD} ≤ 5.5 V			12	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	MHz
				2.4 V ≤ V_{DD} < 2.7 V			4	MHz
Buzzer output frequency	f_{PCL}	PCLBUZ0, PCLBUZ1	HS (high-speed main) mode	4.0 V ≤ V_{DD} ≤ 5.5 V			12	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	MHz
				2.4 V ≤ V_{DD} < 2.7 V			4	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP7		2.4 V ≤ V_{DD} ≤ 5.5 V	1			μs
$\overline{RESET}$ low-level width	t_{RSL}				10			μs

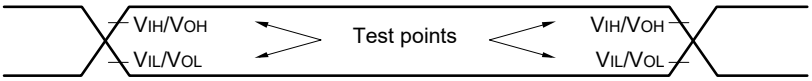
Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 7))

Minimum Instruction Execution Time during Main System Clock Operation

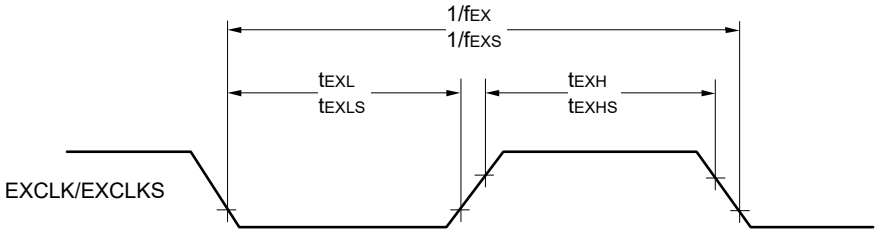
TCY vs VDD (HS (high-speed main) mode)



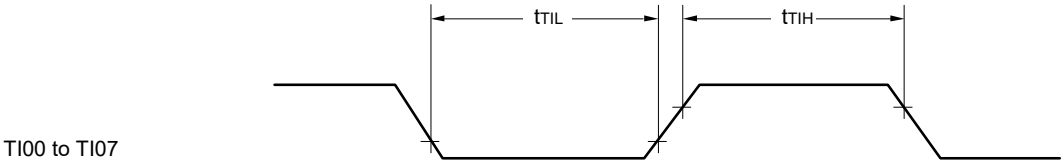
AC Timing Test Points

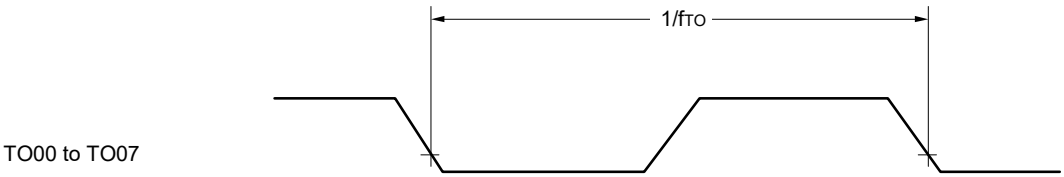


External System Clock Timing

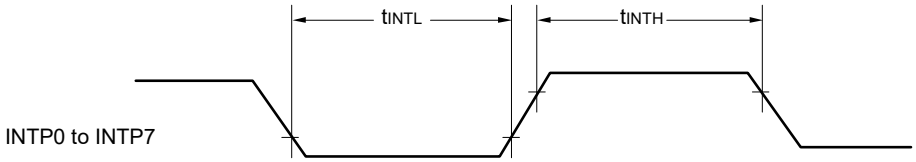


TI/TO Timing

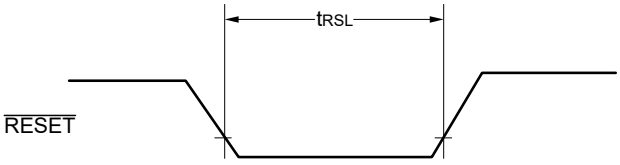




Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



2.5 Peripheral Functions Characteristics

2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate Note 1		2.4 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6 Note 2	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 3		4.0	Mbps

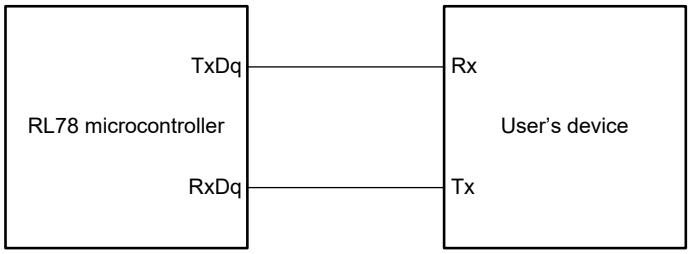
Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

Note 2. The following conditions are required for low voltage interface.
2.4 V ≤ V_{DD} < 2.7 V: MAX. 2.6 Mbps

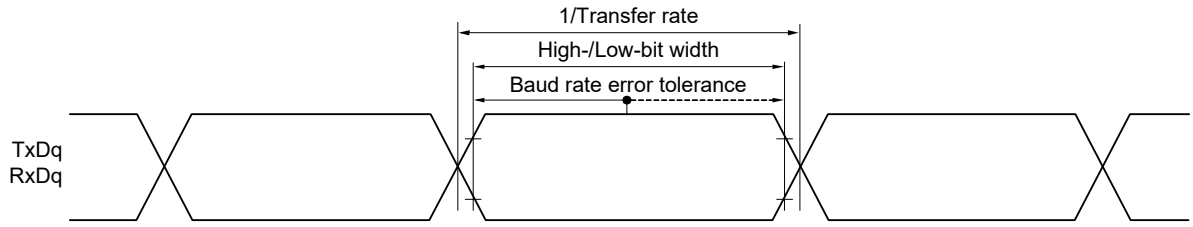
Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ f_{CLK}/4	2.7 V ≤ V_{DD} ≤ 5.5 V	167		ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	250		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 12		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 18		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 38		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		44		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		44		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		75		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}	2.4 V ≤ V_{DD} ≤ 5.5 V		19		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 20 pF Note 4	2.7 V ≤ V_{DD} ≤ 5.5 V		25	ns
			2.4 V ≤ V_{DD} ≤ 5.5 V		25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2),
g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 02, 10))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock output) (1/2)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}		ns
			f_{MCK} ≤ 20 MHz	8/f_{MCK}		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	f_{MCK} > 16 MHz	8/f_{MCK}		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 500		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 7		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 8		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 18		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 20		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}	2.4 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 44	ns
			2.4 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 75	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

Remark 2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock output) (2/2)

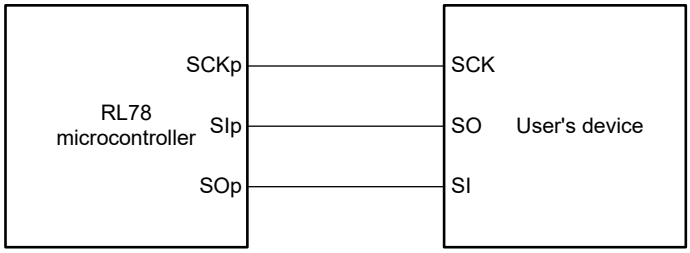
(TA = -40 to +85°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
$\overline{SSI00}$ setup time	tSSIK	DAPmn = 0	2.7 V ≤ VDD ≤ 5.5 V	120		ns
			2.4 V ≤ VDD ≤ 5.5 V	200		ns
		DAPmn = 1	2.7 V ≤ VDD ≤ 5.5 V	1/fMCK + 120		ns
			2.4 V ≤ VDD ≤ 5.5 V	1/fMCK + 200		ns
$\overline{SSI00}$ hold time	tKSSI	DAPmn = 0	2.7 V ≤ VDD ≤ 5.5 V	1/fMCK + 120		ns
			2.4 V ≤ VDD ≤ 5.5 V	1/fMCK + 200		ns
		DAPmn = 1	2.7 V ≤ VDD ≤ 5.5 V	120		ns
			2.4 V ≤ VDD ≤ 5.5 V	200		ns

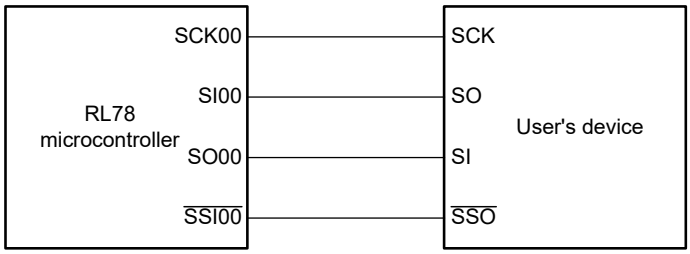
Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 4)

CSI mode connection diagram (during communication at same potential)

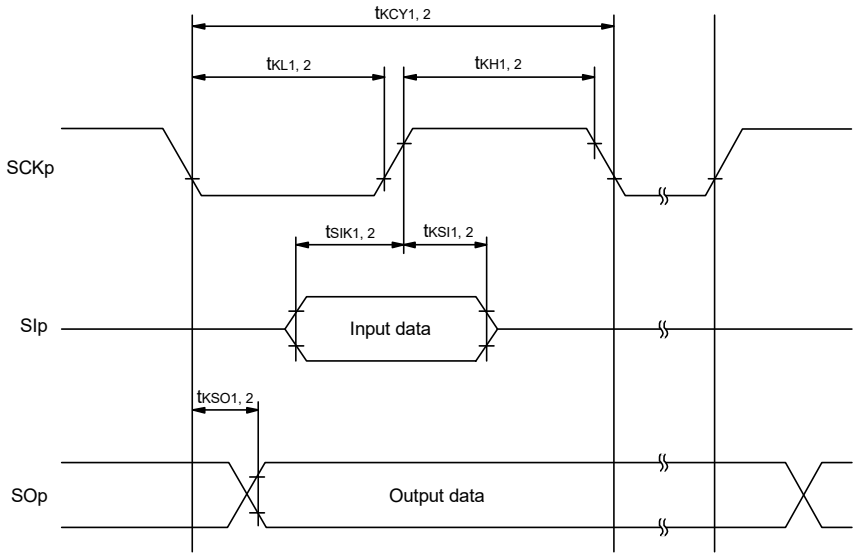


CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))

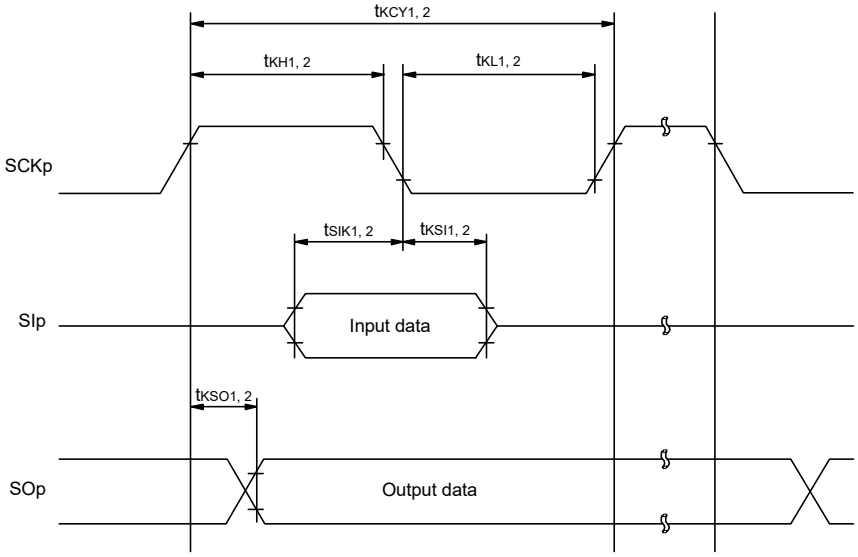


Remark p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

(4) During communication at same potential (simplified I^2C mode)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

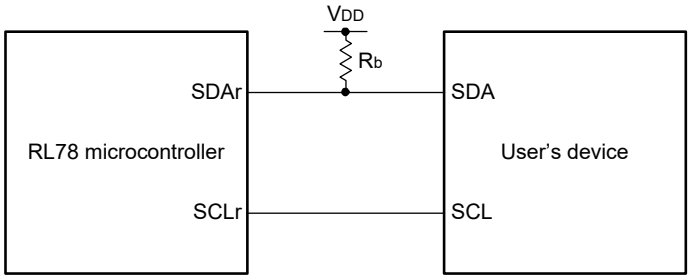
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1	kHz
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1	kHz
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		ns
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 85 Note 2		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 145 Note 2		ns
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 230 Note 2		ns
Data hold time (transmission)	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	ns
		2.4 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	355	ns
		2.4 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	405	ns

Note 1. The value must be equal to or less than f_{MCK}/4.

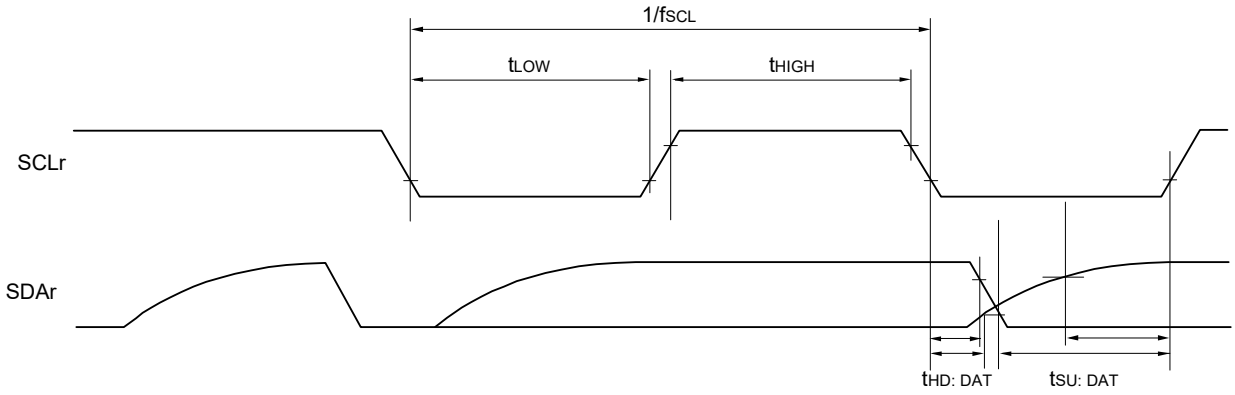
Note 2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remark 1. Rb[Ω]: Communication line (SDAr) pull-up resistance, Cb[F]: Communication line (SCLr, SDAr) load capacitance

Remark 2. r: IIC number (r = 00, 10, 20), g: PIM number (g = 0, 1, 3, 4, 5, 8),

Remark 3. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate		reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		4.0	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		4.0	Mbps
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		f_{MCK}/6 Notes 1, 2, 3	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		4.0	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4,800 bps only.

Note 2. Use it with V_{DD} ≥ V_b.

Note 3. The following conditions are required for low voltage interface.
2.4 V ≤ V_{DD} < 2.7 V: MAX. 2.6 Mbps

Note 4. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate		transmission	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		Note 1	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8 Note 2	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		Note 3	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 4	Mbps
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		Notes 5, 6	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 7	Mbps

Note 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} ≤ 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 4. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use it with $V_{DD} \geq V_b$.

Note 6. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.4 V ≤ V_{DD} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

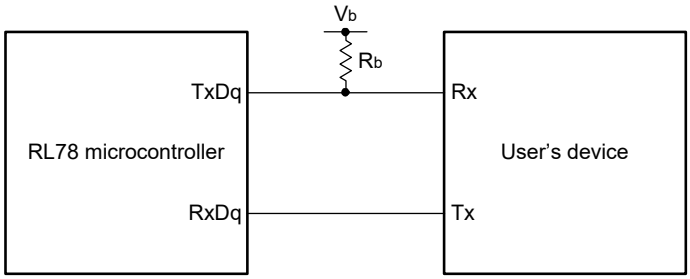
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

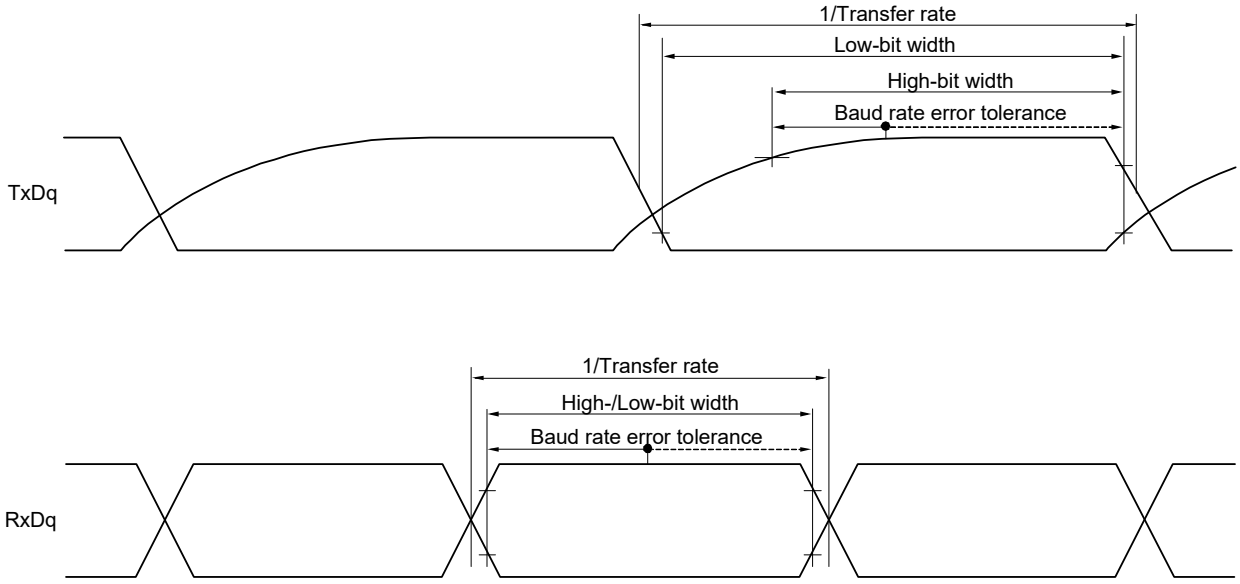
Note 7. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remark 1. Rb[Ω]: Communication line (TxDq) pull-up resistance, Cb[F]: Communication line (TxDq) load capacitance, Vb[V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/2)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500 Note		ns
			2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	1150 Note		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 75		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 170		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 458		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 12		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 18		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 50		ns

Note Use it with V_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the page after the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/2)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	81		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	479		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	19		ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		100	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		195	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ		483	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	110		ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ	19		ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		25	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 3, C_b = 30 pF, R_b = 5.5 kΩ		25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

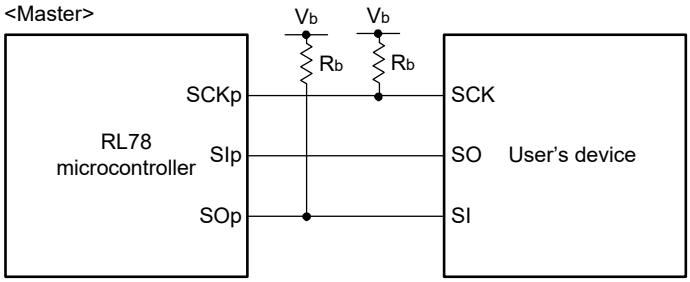
Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. Use it with V_{DD} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

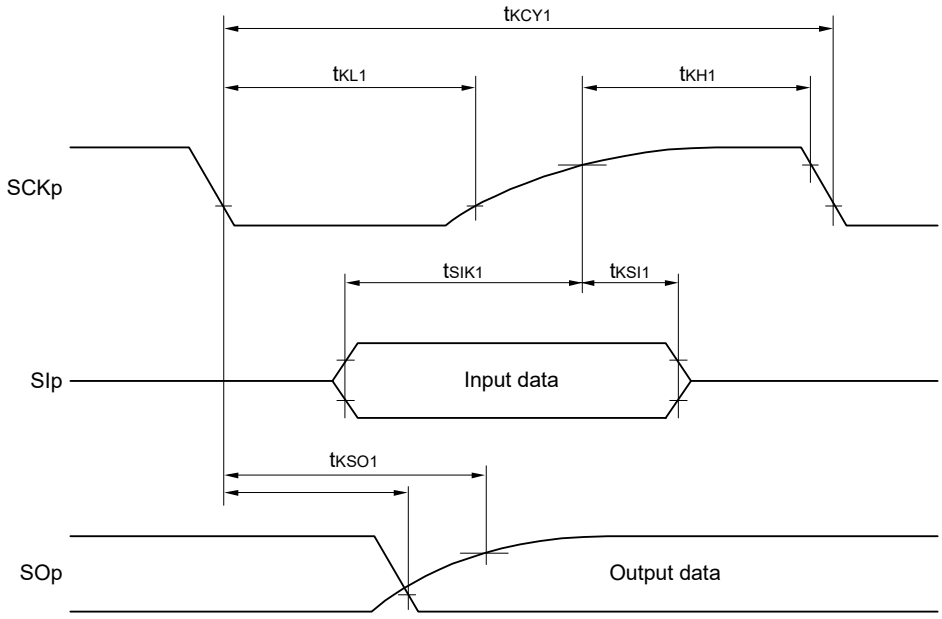


Remark 1. Rb[Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb[F]: Communication line (SCKp, SOp) load capacitance, Vb[V]: Communication line voltage

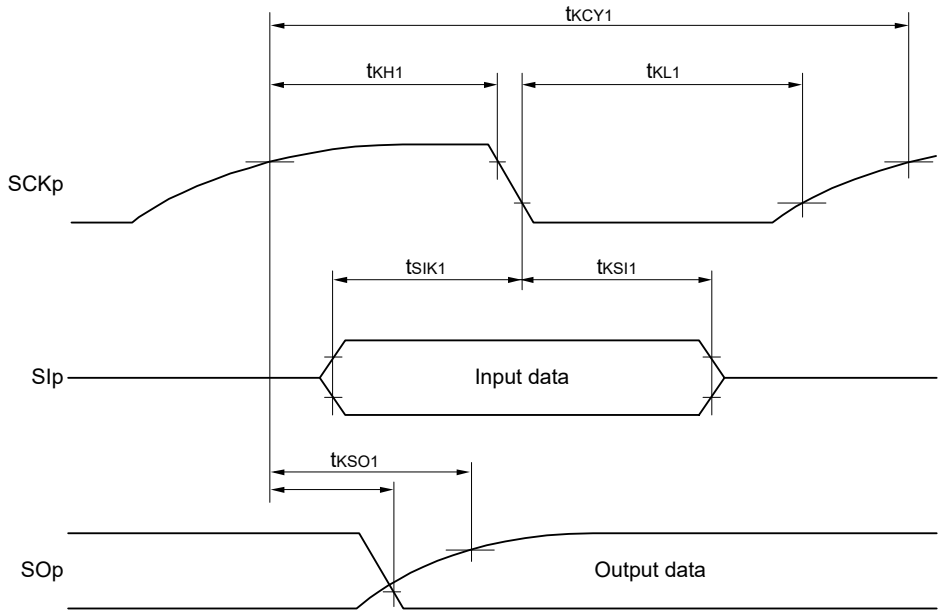
Remark 2. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10))

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2),
g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK}	12/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK}	16/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	20 MHz < f_{MCK}	36/f_{MCK}		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 - 12		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 - 18		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		t_{KCY2}/2 - 50		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 20		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 20		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 31		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 31		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 5	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} + 120	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 214	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2 C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} + 573	ns

Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Note 2. Use it with V_{DD} ≥ V_b.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

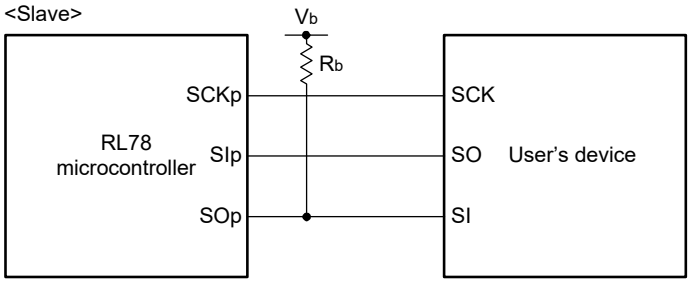
Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

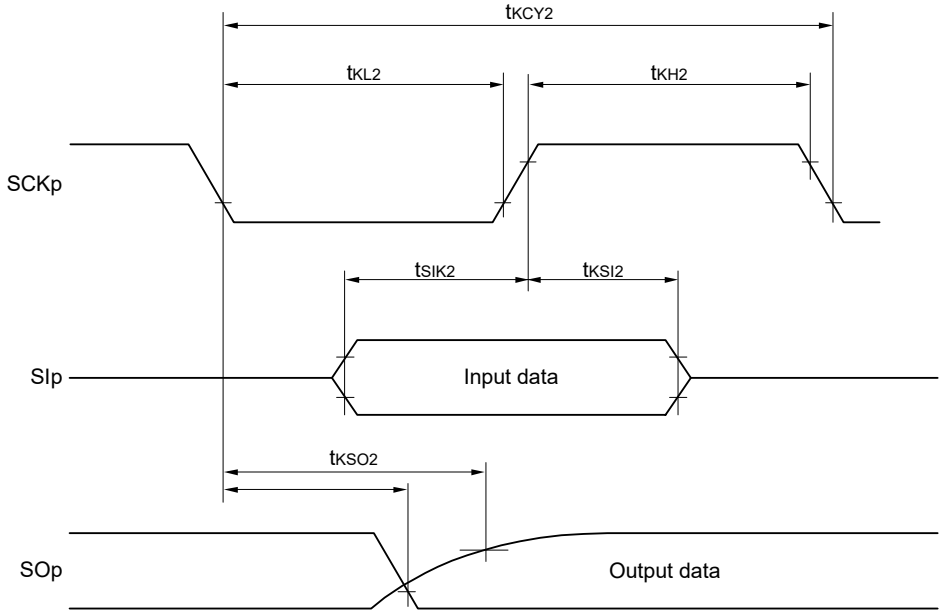


Remark 1. R_b[Ω]: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

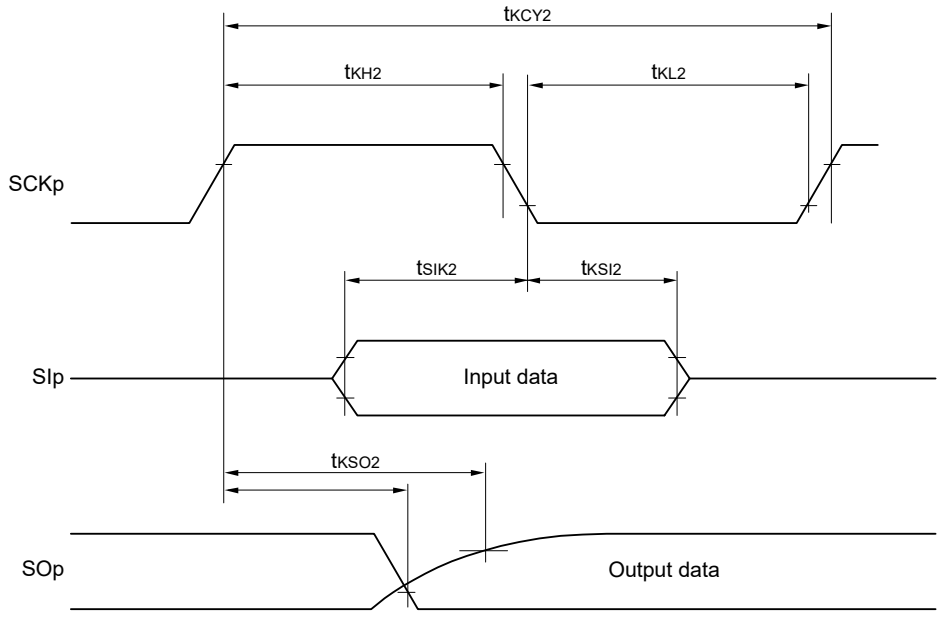
Remark 2. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10))

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1),
n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 3, 4, 5, 8)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode)

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1	kHz
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1	kHz
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		400 Note 1	kHz
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		400 Note 1	kHz
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ		400 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	475		ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	475		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1150		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1150		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1550		ns
Hold time when SCLr = “H”	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	245		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	200		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	675		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	600		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	610		ns
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 135 Note 3		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 135 Note 3		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1/f_{MCK} + 190 Note 3		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 190 Note 3		ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} + 190 Note 3		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	355	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	355	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	0	405	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.

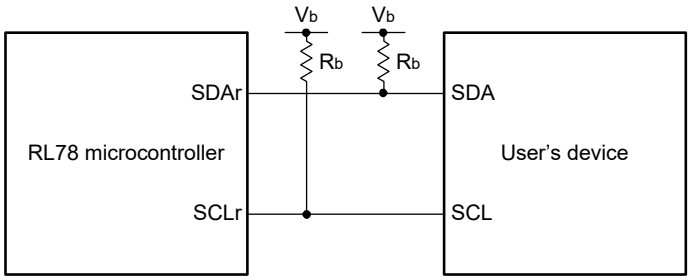
Note 2. Use it with V_{DD} ≥ V_b.

Note 3. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

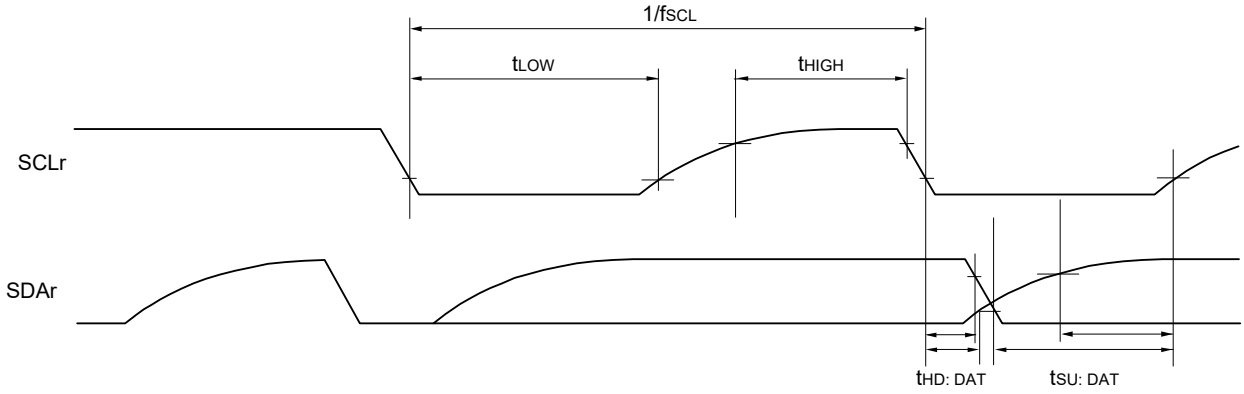
Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remark 1. Rb[Ω]: Communication line (SDAr, SCLr) pull-up resistance, Cb[F]: Communication line (SDAr, SCLr) load capacitance, Vb[V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 10, 20), g: PIM, POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10)

2.5.2 Serial interface IICA

(1) I²C standard mode

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	100	kHz
			2.4 V ≤ V_{DD} ≤ 5.5 V	0	100	kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.7		μs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.0		μs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.7		μs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.0		μs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		250		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		250		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	3.45	μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		0		μs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.0		μs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.7		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I^2C fast mode

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	400	kHz
			2.4 V ≤ V_{DD} ≤ 5.5 V	0	400	kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		0.6		μs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		0.6		μs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.3		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		1.3		μs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		0.6		μs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		100		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		100		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	0.9	μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		0		μs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		0.6		μs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.3		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		1.3		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(3) I^2C fast mode plus

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

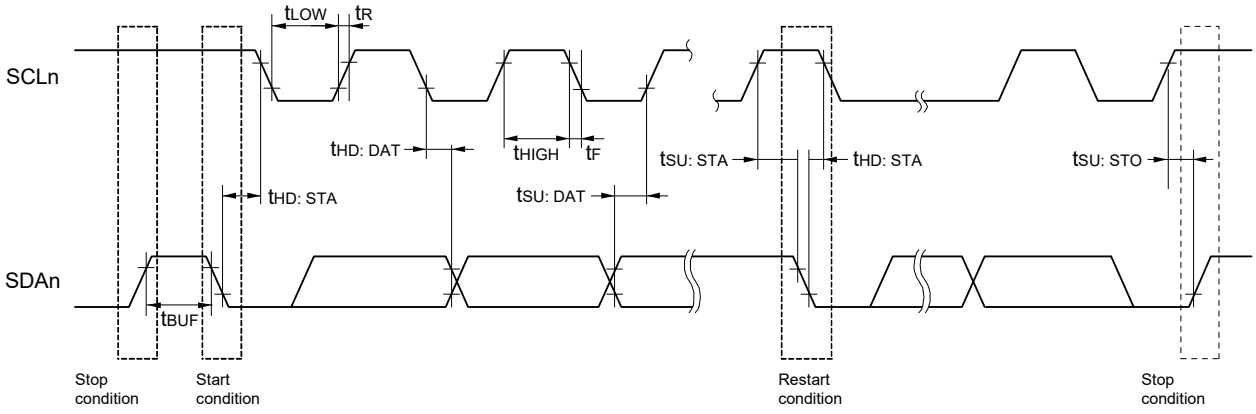
Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	1000	kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		µs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		µs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.5		µs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		µs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		50		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	0.45	µs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		µs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.5		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



2.6 Analog Characteristics

2.6.1 A/D converter characteristics

(1) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI8 to ANI14, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, reference voltage (+) = V_{DD}, reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	tCONV	10-bit resolution Target pin: ANI8 to ANI14	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: internal reference voltage and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5626		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	VAIN	ANI8 to ANI11		0		V_{DD}	V
		ANI12 to ANI14		0		AV_{DD}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{BGR} Note 3			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{TMPS25} Note 3			V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. Refer to **2.6.2 Temperature sensor/internal reference voltage output characteristics**.

(2) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI8 to ANI11, ANI12 to ANI14

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, reference voltage (+) = V_{BGR} Note 3, reference voltage (–) = V_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t_{CONV}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
Zero-scale error Notes 1, 2	E_{ZS}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±(0.60 + 0.35)	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±(2.0 + 0.5)	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±(1.0 + 0.2)	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} Note 3	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. Refer to **2.6.2 Temperature sensor/internal reference voltage output characteristics**.

2.6.2 Temperature sensor/internal reference voltage output characteristics

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}		1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	t_{AMP}	2.4 V ≤ V_{DD} ≤ 5.5 V	5			µs

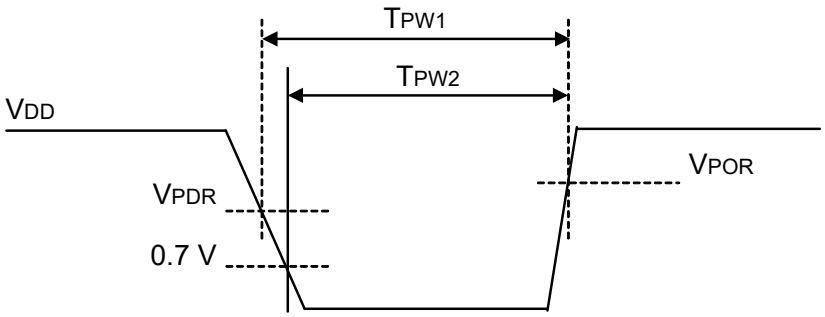
2.6.3 POR circuit characteristics

(TA = -40 to +85°C, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	VPOR	Power supply rise time	1.47	1.51	1.55	V
	VPDR	Power supply fall time Note 1	1.46	1.50	1.54	V
Minimum pulse width Note 2	TPW1	Other than STOP/SUB HALT/SUB RUN	300			μs
	TPW2	STOP/SUB HALT/SUB RUN	300			μs

Note 1. If the power supply voltage falls while the voltage detector is off, be sure to either shift to STOP mode or execute a reset by using the voltage detector or external reset pin before the power supply voltage falls below the minimum operating voltage specified in 2.4 AC Characteristics.

Note 2. Minimum time required for a POR reset when VDD falls below VPDR. This is also the minimum time required for a POR reset from when VDD exceeds below 0.7 V to when VDD exceeds VPOR while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.6.4 LVD circuit characteristics

(1) LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = -40 to +85°C, $V_{PDR} \le AV_{DD} = V_{DD} \le 5.5$ V, $AV_{SS} = V_{SS}$ = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		V_{LVD1}	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V_{LVD2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVD3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V_{LVD4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V_{LVD5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V_{LVD6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V_{LVD7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V_{LVD8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

Caution Set the detection voltage (V_{LVD}) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.
HS (high-speed main) mode: V_{DD} = 2.7 to 5.5 V @ 1 MHz to 24 MHz
V_{DD} = 2.4 to 5.5 V @ 1 MHz to 16 MHz

(2) LVD Detection Voltage of Interrupt & Reset Mode

(T_A = -40 to +85°C, $V_{PDR} \le AV_{DD} = V_{DD} \le 5.5$ V, $AV_{SS} = V_{SS}$ = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDC0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0, falling reset voltage: 2.4 V			2.40	2.45	2.50	V
	V_{LVDC1}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
				Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVDC2}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
				Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVDC3}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
				Falling interrupt voltage	3.60	3.67	3.74	V
	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage: 2.7 V			2.70	2.75	2.81	V
	V_{LVDD1}		LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDD2}		LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
				Falling interrupt voltage	2.90	2.96	3.02	V
	V_{LVDD3}		LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
				Falling interrupt voltage	3.90	3.98	4.06	V

2.6.5 Programmable gain instrumentation amplifier and 24-bit ΔΣ A/D converter

(1) Analog input in differential input mode

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksps, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sps, SBIAS = 2.1 V, $dOFR$ = 0 mV, V_{COM} = 1.0 V, external clock input used)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Full-scale differential input voltage range	V_{ID}	V_{ID} = (PGA0xP - PGA0xN) (x = 0, 1)	—	±800 /G_{TOTAL0}	—	mV
Input voltage range	V_I		0.2	—	1.8	V
Common mode input voltage range	V_{COM}	$dOFR$ = 0 mV	0.2+(|V_{ID}|x G_{SET01})/2	—	1.8-(|V_{ID}|x G_{SET01})/2	V
Input bias current	I_{IN}	V_I = 1.0 V			±50	nA
Input offset current	I_{INO}	V_I = 1.0 V			±20	nA

(2) Analog input in single-ended input mode

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksps, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sps, SBIAS = 2.1 V, $dOFR$ = 0 mV, V_{COM} = 1.0 V, external clock input used)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage range	V_I		0.2	—	1.8	V
Input bias current	I_{IN}	V_I = 1.0 V			±50	nA

(3) Programmable gain instrumentation amplifier and 24-bit ΔΣ A/D converter

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksps, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sps, SBIAS = 2.1 V, $dOFR$ = 0 mV, V_{COM} = 1.0 V, external clock input used, in differential input mode) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES				24	bit
Sampling frequency	fs1	Normal mode		1		MHz
	fs2	Low-power mode		0.125		MHz
Output data rate	f_{DATA1}	Normal mode	0.488		15.625	ksps
	f_{DATA2}	Low-power mode	61.035		1953.125	sps
Gain setting range	G_{TOTAL0}	G_{TOTAL0} = G_{SET01} x G_{SET02}	1		64	V/V
1st gain setting range	G_{SET01}			1, 2, 3, 4, 8		V/V
2nd gain setting range	G_{SET02}			1, 2, 4, 8		V/V
Offset adjustment bit range	$dOFFB$			5		bit
Offset adjustment range	$dOFR$	Referred to input	- 164/G_{SET01}		+ 164/G_{SET01}	mV
Offset adjustment steps	$dOFS$	Referred to input		11/G_{SET01}		mV

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, normal mode: fs1 = 1 MHz, FDATA1 = 3.90625 ksps, low-power mode: fs2 = 0.125 MHz, FDATA2 = 488.28125 sps, SBIAS = 2.1 V, dO_{FR} = 0 mV, V_{COM} = 1.0 V, external clock input used, in differential input mode) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Gain error	E_{G0}	T_A = 25°C G_{SET01} = 1, G_{SET02} = 1 Excluding SBIAS error		±0.2	±2.7	%
		T_A = 25°C G_{SET01} = 8, G_{SET02} = 4 Excluding SBIAS error		±0.1		%
Gain drift Note	dE_{G0}	G_{SET01} = 1, G_{SET02} = 1 Excluding SBIAS drift		(5.6)	(22.0)	ppm/°C
		G_{SET01} = 8, G_{SET02} = 4 Excluding SBIAS drift		(9.1)		ppm/°C
Offset error	E_{OS0}	T_A = 25°C G_{SET01} = 1, G_{SET02} = 1 Referred to input		±0.32	±2.90	mV
		T_A = 25°C G_{SET01} = 8, G_{SET02} = 4 Referred to input		±0.03		mV
Offset drift Note	dE_{OS}	G_{SET01} = 1, G_{SET02} = 1 Referred to input		(±0.02)	(±6.00)	µV/°C
		G_{SET01} = 8, G_{SET02} = 4 Referred to input		(±0.02)		µV/°C
SND ratio	SNDR	G_{SET01} = 1, G_{SET02} = 1, fin = 50 Hz Normal mode, Pin = -1 dBFS	(82)	(85)		dB
		G_{SET01} = 8, G_{SET02} = 4, fin = 50 Hz Normal mode, Pin = -1 dBFS	(73)	(80)		dB
Noise	Vn	G_{SET01} = 1, G_{SET02} = 1, OSR = 2048		(13)		µVRms
		G_{SET01} = 8, G_{SET02} = 4, OSR = 2048		(0.6)		µVRms
Integral non-linearity error	INL	G_{SET01} = 1, G_{SET02} = 1, OSR = 2048		(±10)		ppmFS
Common mode rejection ratio	CMRR0	V_{COM} = 1.0±0.8 V, fin = 50 Hz G_{SET01} = 1, G_{SET02} = 1	(72)	(90)		dB
Power supply rejection ratio	PSRR0	AV_{DD} = 2.7 to 5.5 V, G_{SET01} = 1, G_{SET02} = 1	(60)	(85)		dB
ΔΣ A/D converter input clock frequency	f_{ADC}		3.8	4.0	4.2	MHz

Note Calculate the gain drift and offset drift by using the following expression (for 85°C products):
For gain drift: (MAX(EG(T(-40) to T(85))) - MIN(EG(T(-40) to T(85)))) / (85°C -(-40°C))
For offset drift: (MAX(EOS(T(-40) to T(85))) - MIN(EOS(T(-40) to T(85)))) / (85°C -(-40°C))
MAX(EG(T(-40) to T(85))): The maximum value of gain error when the temperature range is -40°C to 85°C
MIN(EG(T(-40) to T(85))): The minimum value of gain error when the temperature range is -40°C to 85°C
MAX(EOS(T(-40) to T(85))): The maximum value of offset error when the temperature range is -40°C to 85°C
MIN(EOS(T(-40) to T(85))):The minimum value of offset error when the temperature range is -40°C to 85°C

Remark 1. Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.
Remark 2. The typical conditions are the conditions when T_A = 25°C and AV_{DD} = 3.3 V.

2.6.6 Sensor power supply (SBIAS)

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, C_{OUT} = 0.22 µF, V_{OUT} = 1.0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage range	V_{OUT}		0.5		2.2	V
Output voltage adjustment steps	V_{STEP}			0.1		V
Output voltage precision	V_A	I_{OUT} = 1 mA	(- 3)		(+ 3)	%
Maximum output current	I_{OUT}		5			mA
Short circuit current	I_{SHORT}	V_{OUT} = 0 V		40	65	mA
Load regulation	L_R	1 mA ≤ I_{OUT} ≤ 5 mA			(15)	mV
Power supply rejection ratio	PSRR	AV_{DD} = 5.0 V + 0.1 Vpp ripple f = 100 Hz, I_{OUT} = 2.5 mA, V_{OUT} = 2.1 V	(45)	(70)		dB

Remark 1. Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.
Remark 2. The typical conditions are the conditions when T_A = 25°C and AV_{DD} = 3.3 V.

2.6.7 Internal BIAS power supply

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage	V_{BIAS}		0.95	1.00	1.05	V

Remark The typical conditions are the conditions when T_A = 25°C and AV_{DD} = 3.3 V.

2.6.8 Programmable gain instrumentation amplifier (PGA1)

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Differential input voltage range	V_{ID}	V_{ID} = (PGA1xP - PGA1xN) (x = 0, 1)		±800 /G_{TOTAL1}		mV
Input voltage range	V_{IN}		0.3		AV_{DD} - 0.6	V
Common mode input voltage range	V_{COM}		0.3+ (($\|V_{ID}\|$+$\|E_{OS}\|$) ×G_{SET11})/2		AV_{DD}-0.6+ (($\|V_{ID}\|$+$\|E_{OS}\|$) ×G_{SET11})/2	V
Output voltage range	V_{OUT}		0.1		AV_{DD} - 0.1	V
Maximum output current	I_{OUT}		-0.1		+0.1	mA
Input bias current	I_{IN}				±50	nA
Input bias offset current	I_{OS}				±20	nA
Gain setting range	G_{TOTAL1}			G_{SET11} × G_{SET12}		V/V
1st gain setting range	G_{SET11}			12, 16, 20, 24		V/V
2nd gain setting range	G_{SET12}			Note		V/V
Gain error	E_{G1}	T_A = 25°C G_{SET11} = 24, G_{SET12} = 1			±2.7	%
Gain drift	dE_{G1}	G_{SET11} = 24, G_{SET12} = 1		(5.6)	(22.0)	ppm/°C
Offset error	E_{OS1}	T_A = 25°C G_{SET11} = 24, G_{SET12} = 1 Referred to input	-10		+10	mV
Bandwidth	BW11	Low-power mode G_{SET11} = 24, G_{SET12} = 1		(1.5)		kHz
	BW12	High-speed mode G_{SET11} = 24, G_{SET12} = 1		(67)		kHz
Slew rate	SR11	Low-power mode		(6)		mV/µs
	SR12	High-speed mode		(220)		mV/µs
Peak-to-peak voltage noise	Enb11	0.1 Hz to 10 Hz Low-power mode		(3.0)		µVrms
	Enb12	0.1 Hz to 10 Hz High-speed mode		(2.6)		µVrms

Note See the setting of PGA1GC3 to PGA1GC0.

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input-referred noise	En11	f = 1 kHz Low-power mode		(210)		nV/√Hz
	En12	f = 1 kHz High-speed mode		(110)		nV/√Hz
	En13	f = 10 Hz Low-power mode		(460)		nV/√Hz
	En14	f = 10 Hz High-speed mode		(410)		nV/√Hz
Common mode rejection ratio	CMRR1	G_{SET11} = 24, G_{SET12} = 1 f = 50 Hz		(100)		dB
Power supply rejection ratio	PSRR1	2.7 V ≤ AV_{DD} ≤ 5.5 V f = 50 Hz When SBIAS is selected as the reference voltage of the 12-bit D/A converter.		(80)		dB

Remark 1. Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.

Remark 2. The typical conditions are the conditions when T_A = 25°C and AV_{DD} = 3.3 V.

Remark 3. Unless otherwise specified, values are for operation in high-speed mode.

2.6.9 Operational amplifier 0 (AMP0)

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Common mode input voltage range	V_{CM}		0.1		AV_{DD} - 0.1	V
Output voltage range	V_{OUT}	I_{OUT}= ±1 mA	0.07		AV_{DD} - 0.15	V
Maximum output current	I_{OUT}		(-2)		(+2)	mA
Input bias current	I_{IN}				±50	nA
Input offset voltage	V_{OS1}	Low-power mode	-10		+10	mV
	V_{OS2}	High-speed mode	-7		+7	mV
Slew rate	SR1	Low-power mode		(0.04)		V/µs
	SR2	High-speed mode		(0.7)		V/µs
Gain bandwidth	GBW1	Low-power mode		(0.06)		MHz
	GBW2	High-speed mode		(1)		MHz
Phase margin	PM1	Low-power mode		(70)		deg
	PM2	High-speed mode		(60)		deg
Settling time	Tset1	Low-power mode CL = 50 pF, RL = 10 kΩ			(300)	µs
	Tset2	High-speed mode CL = 50 pF, RL = 10 kΩ			(14)	µs
Stabilization wait time	Tstaw1	AMPEn = 0 → 1, Low-power mode CL = 50 pF, RL = 10 kΩ			(300)	µs
	Tstaw2	AMPEn = 0 → 1, High-speed mode CL = 50 pF, RL = 10 kΩ			(14)	µs
Input-referred noise	En1	f = 1 kHz Low-power mode		(200)		nV/√Hz
	En2	f = 1 kHz High-speed mode		(80)		nV/√Hz
Common mode rejection ratio	CMRR	DC		(70)		dB
Power supply rejection ratio	PSRR	DC		(90)		dB

Remark 1. Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.

Remark 2. The typical conditions are the conditions when T_A = 25°C and AV_{DD} = 3.3 V.

Remark 3. Unless otherwise specified, values are for operation in high-speed mode.

2.6.10 Operational amplifiers 1 and 2 (AMP1, AMP2)

(T_A = -40 to +85°C, 2.7 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Common mode input voltage range	V_{CM1}	Low-power mode	0.2		AV_{DD} - 0.5	V
	V_{CM2}	High-speed mode	0.3		AV_{DD} - 0.6	V
Output voltage range	V_{OUT}		0.1		AV_{DD} - 0.1	V
Maximum output current	I_{OUT}	2.7 V ≤ AV_{DD} ≤ 5.5 V	-100		+100	μA
Input bias current	I_{IN}				±50	nA
Input offset voltage	V_{OS1}	Low-power mode	-10		+10	mV
	V_{OS2}	High-speed mode	-10		+10	mV
Slew rate	SR1	Low-power mode		(0.02)		V/μs
	SR2	High-speed mode		(1.1)		V/μs
Gain bandwidth	GBW1	Low-power mode		(0.04)		MHz
	GBW2	High-speed mode		(1.7)		MHz
Phase margin	PM1	Low-power mode		(70)		deg
	PM2	High-speed mode		(60)		deg
Settling time	Tset1	Low-power mode CL = 50 pF, RL = 10 kΩ			(750)	μs
	Tset2	High-speed mode CL = 50 pF, RL = 10 kΩ			(13)	μs
Stabilization wait time	Tstaw1	AMPEn = 0 → 1, Low-power mode CL = 50 pF, RL = 10 kΩ			(800)	μs
	Tstaw2	AMPEn = 0 → 1, High-speed mode CL = 50 pF, RL = 10 kΩ			(13)	μs
Input-referred noise	En1	f = 1 kHz Low-power mode		(230)		nV/√Hz
	En2	f = 1 kHz High-speed mode		(90)		nV/√Hz
Common mode rejection ratio	CMRR	DC		(90)		dB
Power supply rejection ratio	PSRR	DC		(90)		dB

Remark 1. Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.

Remark 2. The typical conditions are the conditions when T_A = 25°C and AV_{DD} = 3.3 V.

Remark 3. Unless otherwise specified, values are for operation in high-speed mode.

2.6.11 8-bit D/A converter (DAC0)

(TA = -40 to +85°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, reference voltage (+) = 2.1 V (SBIAS))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	DARES0				8	bit
Absolute accuracy	LE	Note			±2.5	LSB
Differential non-linearity error	DADLE0				±2.0	LSB
Settling time	DAtset0	CL = 50 pF, RL = 10 kΩ			(6)	μs

Note Errors of the SBIAS output voltage are not included.

Remark 1. Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.
Remark 2. The 8-bit D/A converter characteristics are the values obtained with the amplifier unit connected.

2.6.12 12-bit D/A converter (DAC1)

(1) When reference voltage (+) = 2.1 V (SBIAS)

(TA = -40 to +85°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, reference voltage (+) = 2.1 V (SBIAS))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	DARES1				(12)	bit
Output voltage range	DAOUT	12-bit resolution	0.35		SBIAS	V
Integral non-linearity error	DAILE	12-bit resolution			±4.0	LSB
Differential non-linearity error	DADLE1	12-bit resolution			±1.0	LSB
Offset error	DAErr	12-bit resolution			±30	mV
Gain error	DAEG	12-bit resolution Note			±20	mV
Settling time	DAtset1	12-bit resolution CL = 50 pF, RL = 10 kΩ			(60)	μs

Note Errors of the SBIAS output voltage are not included.

Remark 1. Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.
Remark 2. The 12-bit D/A converter characteristics are the values obtained with the amplifier unit connected.

(2) When reference voltage (+) = AVDD

(TA = -40 to +85°C, 2.7 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, reference voltage (+) = AVDD)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	DARES1				(12)	bit
Output voltage range	DAOUT	12-bit resolution	0.35		AVDD - 0.47	V
Integral non-linearity error	DAILE	12-bit resolution			±4.0	LSB
Differential non-linearity error	DADLE1	12-bit resolution			±1.0	LSB
Offset error	DAErr	12-bit resolution			±30	mV
Gain error	DAEG	12-bit resolution			±20	mV
Settling time	DAtset1	12-bit resolution CL = 50 pF, RL = 10 kΩ			(60)	μs

Remark 1. Values in parentheses are target design values (i.e. not guaranteed) and therefore are not tested for shipment.
Remark 2. The 12-bit D/A converter characteristics are the values obtained with the amplifier unit connected.

2.7 Power supply voltage rising slope characteristics

(T_A = -40 to +85°C, V_{SS} = 0 V)

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SV_{DD}			54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

2.8 LCD Characteristics

2.8.1 Resistance division method

(1) Static display mode

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.0		V_{DD}	V

(2) 1/2 bias method, 1/4 bias method

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.7		V_{DD}	V

(3) 1/3 bias method

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.5		V_{DD}	V

2.8.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C4 Note 1 = 0.47 µF Note 2	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V_{L2}	C1 to C4 Note 1 = 0.47 µF		2 V_{L1} - 0.1	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L4}	C1 to C4 Note 1 = 0.47 µF		3 V_{L1}- 0.15	3 V_{L1}	3 V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C4 Note 1 = 0.47 µF		500			ms

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 µF±30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

(2) 1/4 bias method

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C5 Note 1 = 0.47 μF Note 2	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
Doubler output voltage	V_{L2}	C1 to C5 Note 1 = 0.47 μF		2 V_{L1} - 0.08	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L3}	C1 to C5 Note 1 = 0.47 μF		3 V_{L1} - 0.12	3 V_{L1}	3 V_{L1}	V
Quadruply output voltage	V_{L4}	C1 to C5 Note 1 = 0.47 μF		4 V_{L1} - 0.16	4 V_{L1}	4 V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C5 Note 1 = 0.47μF		500			ms

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L3} and GND
C5: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = C5 = 0.47 μF±30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

2.8.3 Capacitor split method

(1) 1/3 bias method

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{L4} voltage	V_{L4}	C1 to C4 = 0.47 µF Note 2		V_{DD}		V
V_{L2} voltage	V_{L2}	C1 to C4 = 0.47 µF Note 2	2/3 V_{L4} - 0.1	2/3 V_{L4}	2/3 V_{L4} + 0.1	V
V_{L1} voltage	V_{L1}	C1 to C4 = 0.47 µF Note 2	1/3 V_{L4} - 0.1	1/3 V_{L4}	1/3 V_{L4} + 0.1	V
Capacitor split wait time Note 1	t_{VWAIT}		100			ms

Note 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

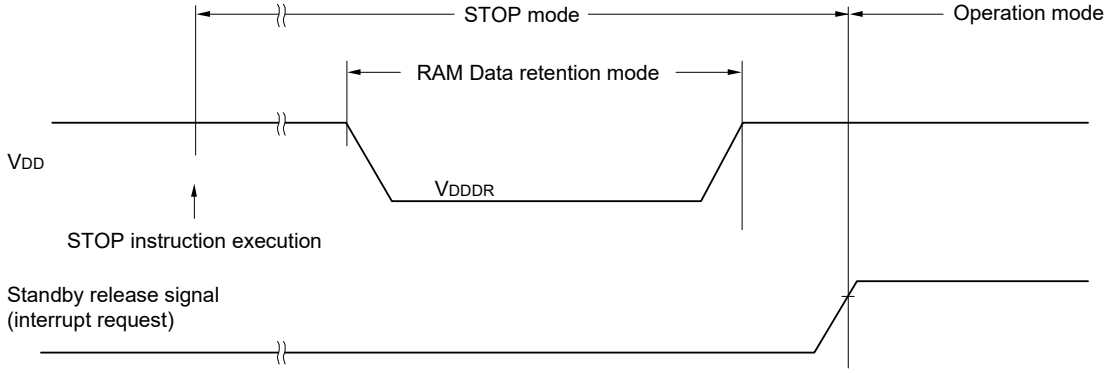
Note 2. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 µF±30%

2.9 RAM data retention characteristics

(TA = -40 to +85°C, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.46 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



2.10 Flash Memory Programming Characteristics

(TA = -40 to +85°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK	2.4 V ≤ VDD ≤ 5.5 V		1		24	MHz
Number of code flash rewrites Notes 1, 2, 3	Cerwr	Retained for 20 years	TA = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year	TA = 25°C		1,000,000		
		Retained for 5 years	TA = 85°C	100,000			
		Retained for 20 years	TA = 85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.11 Dedicated Flash Memory Programmer Communication (UART)

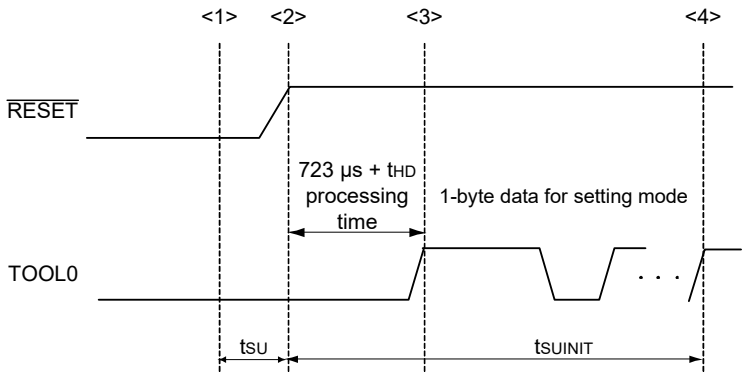
(TA = -40 to +85°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.12 Timing of Entry to Flash Memory Programming Modes

(T_A = -40 to +85°C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
Time to hold the TOOL0 pin at the low level after an external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.
t_{SU}: How long from when the TOOL0 pin is placed at the low level until an external reset ends
t_{HD}: Time to hold the TOOL0 pin at the low level after an external reset is released (excluding the processing time of the firmware to control the flash memory)

3. ELECTRICAL SPECIFICATIONS (R5F11R) (D: TA = -40 to +85°C)

This chapter describes the electrical specifications for the products “D: Industrial applications (TA = -40 to +85°C)”.

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2 Functions other than port pins in the User’s Manual: Hardware.

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings **(1/3)**

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +6.5	V
	AV_{DD}	$AV_{DD} = V_{DD}$	-0.5 to +6.5	V
	AV_{SS}	$AV_{SS} = V_{SS}$	-0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V_{DD} + 0.3 Note 1	V
Input voltage	V_{I1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P121 to P124, P125 to P127, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to V_{DD} +0.3 Note 2	V
	V_{I2}	P60, P61 (N-ch open-drain)	-0.3 to +6.5	V
	V_{I3}	P20 to P27, P150, P151	-0.3 to AV_{DD} + 0.3 Note 2	V
Output voltage	V_{O1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P60, P61, P70 to P77, P80 to P86, P125 to P127	-0.3 to V_{DD} + 0.3 Note 2	V
	V_{O2}	P20 to P27, P150, P151	-0.3 to AV_{DD} + 0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI8 to ANI10	-0.3 to V_{DD} + 0.3 Note 2	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. The reference voltage is V_{SS} (for the V_{DD} systems) = AV_{SS} (for the AV_{DD} systems).

Absolute Maximum Ratings **(2/3)**

Parameter	Symbol	Conditions		Ratings	Unit
LCD voltage	V_{LI1}	V_{L1} input voltage Note 1		-0.3 to +2.8	V
	V_{LI2}	V_{L2} input voltage Note 1		-0.3 to +6.5	V
	V_{LI3}	V_{L3} input voltage Note 1		-0.3 to +6.5	V
	V_{LI4}	V_{L4} input voltage Note 1		-0.3 to +6.5	V
	V_{LI5}	CAPL, CAPH input voltage Note 1		-0.3 to +6.5	V
	V_{LO1}	V_{L1} output voltage		-0.3 to +2.8	V
	V_{LO2}	V_{L2} output voltage		-0.3 to +6.5	V
	V_{LO3}	V_{L3} output voltage		-0.3 to +6.5	V
	V_{LO4}	V_{L4} output voltage		-0.3 to +6.5	V
	V_{LO5}	CAPL, CAPH output voltage		-0.3 to +6.5	V
	V_{LO6}	COM0 to COM7 SEG0 to SEG35 output voltage	External resistance division method	-0.3 to V_{DD} + 0.3 Note 2	V
			Capacitor split method	-0.3 to V_{DD} + 0.3 Note 2	V
			Internal voltage boosting method	-0.3 to V_{LI4} + 0.3 Note 2	V

Note 1. This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 µF ± 30%) and connect a capacitor (0.47 µF ± 30%) between the CAPL and CAPH pins.

Note 2. Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Absolute Maximum Ratings **(3/3)**

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin		-40	mA
		Total of all pins -170 mA	P40, P43, P44, P80 to P83	-70	mA
			P01 to P07, P10 to P17, P30 to P32, P35 to P37, P50 to P53, P70 to P77, P84 to P86, P125 to P127	-100	mA
	I_{OH2}	Per pin		-40	mA
		Total of all pins -140 mA	P21 to P27	-70	mA
			P20, P150, P151	-70	mA
Output current, low	I_{OL1}	Per pin		40	mA
		Total of all pins 170 mA	P40, P43, P44, P80 to P83	70	mA
			P01 to P07, P10 to P17, P30 to P32, P35 to P37, P50 to P53, P60, P61, P70 to P77, P84 to P86, P125 to P127	100	mA
	I_{OL2}	Per pin		40	mA
		Total of all pins 140 mA	P21 to P27	70	mA
			P20, P150, P151	70	mA
Operating ambient temperature	T_A	In normal operation mode		-40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.2 Oscillator Characteristics

3.2.1 X1 and XT1 characteristics

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X) Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
		1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	
X1 clock oscillation frequency (f_{XT}) Note	Crystal resonator		32	32.768	35	kHz
			31	38.4	39	

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the User's Manual: Hardware.

3.2.2 On-chip oscillator characteristics

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{IH}	2.7 V ≤ V_{DD} ≤ 5.5 V		1		24	MHz
		2.4 V ≤ V_{DD} < 2.7 V		1		16	MHz
		1.8 V ≤ V_{DD} < 2.4 V		1		8	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.0		+1.0	%
		-40 to -20°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

3.3 DC Characteristics

3.3.1 Pin characteristics

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/5)**

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127				-10.0 Note 2	mA
		Total of P40, P43, P44, P80 to P83 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			-55	mA
			2.7 V ≤ V_{DD} < 4.0 V			-10	mA
			1.8 V ≤ V_{DD} < 2.7 V			-5	mA
		Total of P01 to P07, P10 to P17, P30 to P32, P35 to P37, P50 to P53, P70 to P77, P84 to P86, P125 to P127 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			-69	mA
			2.7 V ≤ V_{DD} < 4.0 V			-23	mA
			1.8 V ≤ V_{DD} < 2.7 V			-12	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.8 V ≤ V_{DD} ≤ 5.5 V			-124	mA
	I_{OH2}	Per pin for P20 to P27, P150, P151	1.8 V ≤ AV_{DD} ≤ 5.5 V			-10.0 Note 2	mA
		Total of P21 to P27 (When duty ≤ 70% Note 3)	4.0 V ≤ AV_{DD} ≤ 5.5 V			-50	mA
			2.7 V ≤ AV_{DD} < 4.0 V			-10	mA
			1.8 V ≤ AV_{DD} < 2.7 V			-5	mA
		Total of P20, P150, P151 (When duty ≤ 70% Note 3)	4.0 V ≤ AV_{DD} ≤ 5.5 V			-21	mA
			2.7 V ≤ AV_{DD} < 4.0 V			-5	mA
			1.8 V ≤ AV_{DD} < 2.7 V			-3	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.8 V ≤ AV_{DD} ≤ 5.5 V			-71	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin (I_{OH1}) and AV_{DD} pin (I_{OH2}) to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = −10.0 mA
Total output current of pins = (−10.0 × 0.7)/(80 × 0.01) ≅ −8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution **P02 to P04, P06, P07, P10, P12, P35 to P37, P40, P43, P44, P50 to P52, and P80 to P82 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(2/5)**

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P121 to P127				20.0 Note 2	mA
		Per pin for P60, P61				15.0 Note 2	mA
		Total of P40, P43, P44, P80 to P83 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			70	mA
			2.7 V ≤ V_{DD} < 4.0 V			15	mA
			1.8 V ≤ V_{DD} < 2.7 V			9	mA
		Total of P01 to P07, P10 to P17, P30 to P32, P35 to P37, P50 to P53, P60, P61, P70 to P77, P84 to P86, P125 to P127 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			90	mA
			2.7 V ≤ V_{DD} < 4.0 V			35	mA
			1.8 V ≤ V_{DD} < 2.7 V			20	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.8 V ≤ V_{DD} ≤ 5.5 V			160	mA
	I_{OL2}	Per pin for P20 to P27, P150, P151	1.8 V ≤ AV_{DD} ≤ 5.5 V			20	mA
		Total of P21 to P27 (When duty ≤ 70% Note 3)	4.0 V ≤ AV_{DD} ≤ 5.5 V			60	mA
			2.7 V ≤ AV_{DD} < 4.0 V			10	mA
			1.8 V ≤ AV_{DD} < 2.7 V			5	mA
		Total of P20, P150, P151 (When duty ≤ 70% Note 3)	4.0 V ≤ AV_{DD} ≤ 5.5 V			25	mA
			2.7 V ≤ AV_{DD} < 4.0 V			8	mA
			1.8 V ≤ AV_{DD} < 2.7 V			5	mA
		Total of all pins (When duty ≤ 70% Note 3)	1.8 V ≤ AV_{DD} ≤ 5.5 V			85	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{SS} pin (I_{OL1}) and AV_{SS} pin (I_{OL2}) to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(3/5)**

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127	Normal input buffer	0.8 V_{DD}		V_{DD}	V
	V_{IH2}	For TTL mode supported ports	TTL input buffer, 4.0 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	V
			TTL input buffer, 3.3 V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			TTL input buffer, 1.8 V ≤ V_{DD} < 3.3 V	1.5		V_{DD}	V
	V_{IH3}	P20 to P27, P150, P151		0.8 AV_{DD}		AV_{DD}	V
	V_{IH4}	P60, P61		0.7 V_{DD}		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127	Normal input buffer	0		0.2 V_{DD}	V
	V_{IL2}	For TTL mode supported ports	TTL input buffer, 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer, 3.3 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer, 1.8 V ≤ V_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P27, P150, P151		0		0.2 AV_{DD}	V
	V_{IL4}	P60, P61		0		0.3 V_{DD}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V

Caution **The maximum V_{IH} value on P02 to P04, P06, P07, P10, P12, P35 to P37, P40, P43, P44, P50 to P52, and P80 to P82 is V_{DD}, even in the N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (4/5)

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -10.0 mA	V_{DD} - 1.5			V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -3.0 mA	V_{DD} - 0.7			V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -2.0 mA	V_{DD} - 0.6			V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = -1.5 mA	V_{DD} - 0.5			V
	V_{OH2}	P20 to P27, P150, P151	4.0 V ≤ AV_{DD} ≤ 5.5 V, I_{OH} = -10.0 mA	AV_{DD} - 1.5			V
			4.0 V ≤ AV_{DD} ≤ 5.5 V, I_{OH} = -3.0 mA	AV_{DD} - 0.7			V
			2.7 V ≤ AV_{DD} ≤ 5.5 V, I_{OH} = -2.0 mA	AV_{DD} - 0.6			V
			1.8 V ≤ AV_{DD} ≤ 5.5 V, I_{OH} = -1.5 mA	AV_{DD} - 0.5			V
Output voltage, low	V_{OL1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P70 to P77, P80 to P86, P125 to P127	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 20.0 mA			1.3	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 3.0 mA			0.6	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 1.5 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 0.6 mA			0.4	V
	V_{OL2}	P20 to P27, P150, P151	4.0 V ≤ AV_{DD} ≤ 5.5 V, I_{OL} = 20.0 mA			1.3	V
			4.0 V ≤ AV_{DD} ≤ 5.5 V, I_{OL} = 8.5 mA			0.7	V
			2.7 V ≤ AV_{DD} ≤ 5.5 V, I_{OL} = 3.0 mA			0.6	V
			2.7 V ≤ AV_{DD} ≤ 5.5 V, I_{OL} = 1.5 mA			0.4	V
			1.8 V ≤ AV_{DD} ≤ 5.5 V, I_{OL} = 0.6 mA			0.4	V
	V_{OL3}	P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 15.0 mA			2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 5.0 mA			0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 3.0 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL} = 2.0 mA			0.4	V

Caution The maximum V_{IH} value on P02 to P04, P06, P07, P10, P12, P35 to P37, P40, P43, P44, P50 to P52, and P80 to P82 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(5/5)**

Item	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P60, P61, P70 to P77, P80 to P86, P125 to P127, P137, $\overline{\text{RESET}}$	V_I = V_{DD}				1	μA
	I_{LIH2}	P20 to P27, P150, P151	V_I = AV_{DD}				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I = V_{DD}	In input port mode or when using external clock input			1	μA
				When a resonator is connected			10	μA
Input leakage current, low	I_{LIL1}	P01 to P07, P10 to P17, P30 to P32, P35 to P37, P40, P43, P44, P50 to P53, P60, P61, P70 to P77, P80 to P86, P125 to P127, P137, $\overline{\text{RESET}}$	V_I = V_{SS}				-1	μA
	I_{LIL2}	P20 to P27, P150, P151	V_I = AV_{SS}				-1	μA
	I_{LIL3}	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I = V_{SS}	In input port mode or when using external clock input			-1	μA
				When a resonator is connected			-10	μA
On-chip pull-up resistance	R_{U1}	P01 to P07, P10 to P16, P30 to P32, P35 to P37, P50 to P53, P70 to P77, P125 to P127	V_I = V_{SS}, in input port mode	2.4 V ≤ V_{DD} ≤ 5.5 V	10	20	100	kΩ
				1.8 V ≤ V_{DD} < 2.4 V	10	30	100	kΩ
	R_{U2}	P17, P40, P43, P44, P80 to P86,	V_I = V_{SS}, in input port mode		10	20	100	kΩ
	R_{U3}	P20 to P27, P150 and P151	V_I = AV_{SS}, in input port mode		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) Mode Note 5	f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 5.0 V		1.7		mA
						V_{DD} = 3.0 V		1.7		
					Normal operation	V_{DD} = 5.0 V		3.7	6.4	
						V_{DD} = 3.0 V		3.7	6.4	
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.8	5.0	
						V_{DD} = 3.0 V		2.8	5.0	
			LS (low-speed main) Mode Note 5	f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.2	2.1	mA
						V_{DD} = 2.0 V		1.2	2.1	
			HS (high-speed main) Mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.1	5.4	mA
						Resonator connection		3.3	5.5	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.0	5.4	
						Resonator connection		3.3	5.5	
				f_{MX} = 16 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.6	4.7	
						Resonator connection		2.8	4.8	
				f_{MX} = 16 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.6	4.7	
						Resonator connection		2.8	4.8	
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		1.9	3.1	
						Resonator connection		1.9	3.1	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.9	3.1	
						Resonator connection		1.9	3.1	
			LS (low-speed main) Mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.1	2.1	mA
						Resonator connection		1.1	2.1	
				f_{MX} = 8 MH Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		1.1	2.1	
						Resonator connection		1.1	2.1	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		4.3	5.8	µA
						Resonator connection		4.6	5.8	
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.3	5.8	
						Resonator connection		4.6	5.8	
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		4.5	7.6	
						Resonator connection		4.5	7.6	
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		4.7	9.2	
						Resonator connection		5.1	9.2	
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		5.2	12.6	
						Resonator connection		5.7	12.6	
				f_{SUB} = 38.4 kHz Note 4 T_A = -40°C	Normal operation	Square wave input		5.0	6.8	µA
						Resonator connection		5.4	6.8	
				f_{SUB} = 38.4 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		5.0	6.8	
						Resonator connection		5.4	6.8	
				f_{SUB} = 38.4 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		5.3	8.9	
						Resonator connection		5.3	8.9	
				f_{SUB} = 38.4 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		5.5	10.8	
						Resonator connection		6.0	10.8	
				f_{SUB} = 38.4 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		6.1	14.8	
						Resonator connection		6.7	14.8	

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Total current flowing into VDD and AVDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD, I/O ports, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3. When high-speed system clock and subsystem clock are stopped.

Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and watchdog timer.

Note 5. Relationship between operation voltage width, operation frequency of CPU, and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ VDD ≤ 5.5 V @ 1 MHz to 24 MHz
2.4 V ≤ VDD ≤ 5.5 V @ 1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ VDD ≤ 5.5 V @ 1 MHz to 8 MHz

Remark 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. fIH: High-speed on-chip oscillator clock frequency

Remark 3. fSUB: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 4. Except subsystem clock operation, temperature condition for the TYP. value is TA = 25°C.

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) Mode Note 7	f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.42	2.03	mA
					V_{DD} = 3.0 V		0.42	2.03	
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.39	1.58	
					V_{DD} = 3.0 V		0.39	1.58	
			LS (low-speed main) Mode Note 7	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		0.25	0.81	mA
					V_{DD} = 2.0 V		0.25	0.81	
			HS (high-speed main) Mode Note 7	f_{MX} = 20 MHz Note 3 V_{DD} = 5.0 V	Square wave input		0.26	1.75	mA
					Resonator connection		0.40	1.88	
				f_{MX} = 20 MHz Note 3 V_{DD} = 3.0 V	Square wave input		0.25	1.75	
					Resonator connection		0.40	1.88	
				f_{MX} = 16 MHz Note 3 V_{DD} = 5.0 V	Square wave input		0.23	1.42	
					Resonator connection		0.36	1.59	
				f_{MX} = 16 MHz Note 3 V_{DD} = 3.0 V	Square wave input		0.22	1.42	
					Resonator connection		0.35	1.59	
				f_{MX} = 10 MHz Note 3 V_{DD} = 5.0 V	Square wave input		0.19	0.92	
					Resonator connection		0.29	1.00	
				f_{MX} = 10 MHz Note 3 V_{DD} = 3.0 V	Square wave input		0.18	0.92	
					Resonator connection		0.28	1.00	
			LS (low-speed main) Mode Note 7	f_{MX} = 8 MHz Note 3 V_{DD} = 3.0 V	Square wave input		0.09	0.61	mA
					Resonator connection		0.15	0.66	
				f_{MX} = 8 MHz Note 3 V_{DD} = 2.0 V	Square wave input		0.10	0.62	
					Resonator connection		0.15	0.67	
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5 T_A = -40°C	Square wave input		0.32	0.69	µA
					Resonator connection		0.51	0.89	
				f_{SUB} = 32.768 kHz Note 5 T_A = +25°C	Square wave input		0.41	0.82	
					Resonator connection		0.62	1.00	
				f_{SUB} = 32.768 kHz Note 5 T_A = +50°C	Square wave input		0.52	1.40	
					Resonator connection		0.75	1.60	
				$_{SUB}$ = 32.768 kHz Note 5 T_A = +70°C	Square wave input		0.82	2.70	
					Resonator connection		1.08	2.90	
				f_{SUB} = 32.768 kHz Note 5 T_A = +85°C	Square wave input		1.38	4.95	
					Resonator connection		1.62	5.15	
				f_{SUB} = 38.4 kHz Note 5 T_A = -40°C	Square wave input		0.38	0.81	µA
					Resonator connection		0.60	1.04	
				f_{SUB} = 38.4 kHz Note 5 T_A = +25°C	Square wave input		0.48	0.96	
					Resonator connection		0.73	1.17	
				f_{SUB} = 38.4 kHz Note 5 T_A = +50°C	Square wave input		0.61	1.64	
					Resonator connection		0.88	1.88	
				$_{SUB}$ = 38.4 kHz Note 5 T_A = +70°C	Square wave input		0.96	3.16	
					Resonator connection		1.27	3.40	
				f_{SUB} = 38.4 kHz Note 5 T_A = +85°C	Square wave input		1.62	5.80	
					Resonator connection		1.90	6.04	
	I_{DD3} Note 6	STOP mode Note 8	T_A = -40°C				0.20	0.59	µA
			T_A = +25°C				0.26	0.72	
			T_A = +50°C				0.33	1.30	
			T_A = +70°C				0.53	2.60	
			T_A = +85°C				0.93	4.85	

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Total current flowing into V_{DD} and AV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD, I/O ports, and on-chip pull-up/pull-down resistors and the current flowing during writing to the data flash.

Note 2. During HALT instruction execution from flash memory

Note 3. When the high-speed on-chip oscillator and the subsystem clock are stopped

Note 4. When the high-speed system clock and the subsystem clock are stopped

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the real-time clock 2 is included. However, not including the current flowing into the 12-bit interval timer, 8-bit interval timer, and watchdog timer.

Note 6. Not including the current flowing into the real-time clock 2, 12-bit interval timer, 8-bit interval timer, and watchdog timer.

Note 7. Relationship between operation voltage width, operation frequency of CPU, and operation mode is as below.

HS (high-speed main) Mode: 2.7 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 16 MHz
LS (low-speed main) Mode: 1.8 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 8 MHz

Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C.

• Peripheral functions

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
RTC2 operating current	I_{RTC} Notes 1, 3	f_{SUB} = 32.768 kHz			0.02		μA
12-bit Interval timer operating current	I_{TMKA} Notes 1, 2, 4	f_{SUB} = 38.4 kHz, f_{MAIN} stopped			0.02		μA
		f_{SUB} = 32.768 kHz, f_{MAIN} stopped			0.02		μA
8-bit Interval timer operating current	I_{TMRT} Notes 1, 14	f_{SUB} = 38.4 kHz, f_{MAIN} stopped, per unit	8-bit counter mode × 2-channel operation		0.14		μA
			16-bit counter mode operation		0.12		μA
		f_{SUB} = 32.768 kHz, f_{MAIN} stopped, per unit	8-bit counter mode × 2-channel operation		0.12		μA
			16-bit counter mode operation		0.10		μA
Watchdog timer operating current	I_{WDT} Notes 1, 5	f_{IL} = 15 kHz			0.22		μA
10-bit A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, V_{DD} = 5.0 V		1.3	1.7	mA
			Low-voltage mode, V_{DD} = 3.0 V		0.5	0.7	mA
Internal reference voltage (1.45 V) current	I_{ADREF} Notes 1, 7				85		μA
Temperature sensor operating current	I_{TMPS} Note 1				85		μA
LVD operating current	I_{LVI} Notes 1, 8				0.06		μA
Self-programming operating current	I_{FSP} Notes 1, 9				2.0	12.2	mA
BGO operating current	I_{BGO} Notes 1, 10				2.0	12.2	mA
SNOOZE operating current	I_{SNOZ} Notes 1, 11	A/D converter operation	The mode is performed		0.50	0.60	mA
			During A/D conversion, low-voltage mode, V_{DD} = 3.0 V		1.20	1.44	
		CSI/UART operation			0.70	0.84	
		DTC operation			3.1		

(**Notes** and **Remarks** are listed on the page after the next page.)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
LCD operating current	I_{LCD1} Notes 12, 13	External resistance division method	f_{LCD} = f_{SUB} (32.768 kHz) LCD clock = 128 Hz	1/3 bias 4-time slice	V_{DD} = 5.0 V V_{L4} = 5.0 V		0.04	0.20	μA
			f_{LCD} = f_{SUB} (38.4 kHz) LCD clock = 75 Hz				0.08	0.40	
	I_{LCD2} Note 12	Internal voltage boosting method	f_{LCD} = f_{SUB} (32.768 kHz) LCD clock = 128 Hz	1/3 bias 4-time slice	V_{DD} = 3.0 V V_{L4} = 3.0 V (VLCD = 04H)		0.85	2.20	μA
			f_{LCD} = f_{SUB} (38.4 kHz) LCD clock = 75 Hz				0.50	2.20	
			f_{LCD} = f_{SUB} (32.768 kHz) LCD clock = 128 Hz		V_{DD} = 5.0 V V_{L4} = 5.1 V (VLCD = 12H)		1.55	3.70	μA
			f_{LCD} = f_{SUB} (38.4 kHz) LCD clock = 75 Hz				0.91	3.70	
	I_{LCD3} Note 12	Capacitor split method	f_{LCD} = f_{SUB} (32.768 kHz) LCD clock = 128 Hz	1/3 bias 4-time slice	V_{DD} = 3.0 V V_{L4} = 3.0 V		0.20	0.50	μA
			f_{LCD} = f_{SUB} (38.4 kHz) LCD clock = 75 Hz				0.13	0.50	
Operating currents of the meter-dedicated macro	I_{TMRJ} Note 15	f_{SUB} = 38.4 kHz, f_{MAIN} stopped, per unit					0.10		μA
	I_{UARTMG} Note 15	f_{SUB} = 38.4 kHz, f_{MAIN} stopped					0.12		μA
	I_{SMOTD} Note 15	f_{SUB} = 38.4 kHz, f_{MAIN} stopped					0.10		μA
	I_{EXSD} Note 15	f_{SUB} = 38.4 kHz, f_{MAIN} stopped					0.02		μA

(**Notes** and **Remarks** are listed on the next page.)

Note 1. Current flowing to V_{DD}.

Note 2. When the high-speed on-chip oscillator and high-speed system clock are stopped.

Note 3. Current flowing only to the real-time clock 2 (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock 2 is operating in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock 2.

Note 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{TMKA}, when the 12-bit interval timer operates in the operating mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the 12-bit interval timer.

Note 5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is operating.

Note 6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2}, I_{ADC}, and I_{ADREF} when the A/D converter operates in the operating mode or the HALT mode.

Note 7. Operation current flowing to the internal reference voltage.

Note 8. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and ILVI when the LVD circuit operates in the operating mode, HALT mode, or STOP mode.

Note 9. Current flowing during self-programming

Note 10. Current flowing during writing to the data flash

Note 11. For time required to shift to the SNOOZE mode, see **27.3.3 SNOOZE mode** in the User's Manual: Hardware.

Note 12. Current flowing only to the LCD controller/driver (V_{DD} pin). The current value of the RL78 microcontrollers is the sum of the LCD operating current (I_{LCD1}, I_{LCD2}, or I_{LCD3}) and the supply current (I_{DD1} or I_{DD2}) when the LCD controller/driver operates in the operating mode or HALT mode. Not including the current that flows through the LCD panel.

Note 13. Not including the current that flows through the external divider resistor.

Note 14. Current flowing only to the 8-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and IIT, when the 8-bit interval timer operates in the operating mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

Note 15. The current value of the RL78 microcontrollers is the sum of I_{DD2} or I_{DD3} and I_{TMRJ}, I_{UARTMG}, I_{SMOTD}, or I_{EXSD} when each module operates in the sub-HALT mode or STOP mode.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 3. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 4. The temperature condition for the TYP. value is T_A = 25°C.

3.4 AC Characteristics

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/2)**

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) Mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.0417		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) Mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
		Subsystem clock (f_{SUB}) operation	f_{XT} = 38.4 kHz	1.8 V ≤ V_{DD} ≤ 5.5 V		26.04		μs
			f_{XT} = 32.768 kHz	1.8 V ≤ V_{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self-programming mode	HS (high-speed main) Mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.0417		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) Mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
External system clock frequency	f_{EX}	EXCLK		2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
				2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	MHz
				1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	MHz
	f_{EXT}	EXCLKS			32		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	EXCLK		2.7 V ≤ V_{DD} ≤ 5.5 V	24			ns
				2.4 V ≤ V_{DD} < 2.7 V	30			ns
				1.8 V ≤ V_{DD} < 2.4 V	60			ns
	t_{EXHS}, t_{EXLS}	EXCLKS			13.7			μs
Timer input high-level width, low-level width	t_{TIH}, t_{TIL}	TI00 to TI07			1/f_{MCK} + 10			ns
Timer RJ input cycle	t_C	TRJIO0, TRJIO1		2.7 V ≤ V_{DD} ≤ 5.5 V	100			ns
				1.8 V ≤ V_{DD} < 2.7 V	300			ns
Timer RJ input high-level width, low-level width	t_{TJIH}, t_{TJIL}	TRJIO0, TRJIO1		2.7 V ≤ V_{DD} ≤ 5.5 V	40			ns
				1.8 V ≤ V_{DD} < 2.7 V	120			ns
Timer output frequency	f_{TO}	TO00 to TO07 TRJIO0, TRJIO1, TRJO0, TRJO1	HS (high-speed main) Mode	4.0 V ≤ V_{DD} ≤ 5.5 V			12	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	MHz
				2.4 V ≤ V_{DD} < 2.7 V			4	MHz
			LS (low-speed main) Mode	1.8 V ≤ V_{DD} ≤ 5.5 V			4	MHz
Buzzer output frequency	f_{PCL}	PCLBUZ0, PCLBUZ1	HS (high-speed main) Mode	4.0 V ≤ V_{DD} ≤ 5.5 V			12	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	MHz
				2.4 V ≤ V_{DD} < 2.7 V			4	MHz
			LS (low-speed main) Mode	1.8 V ≤ V_{DD} ≤ 5.5 V			4	MHz

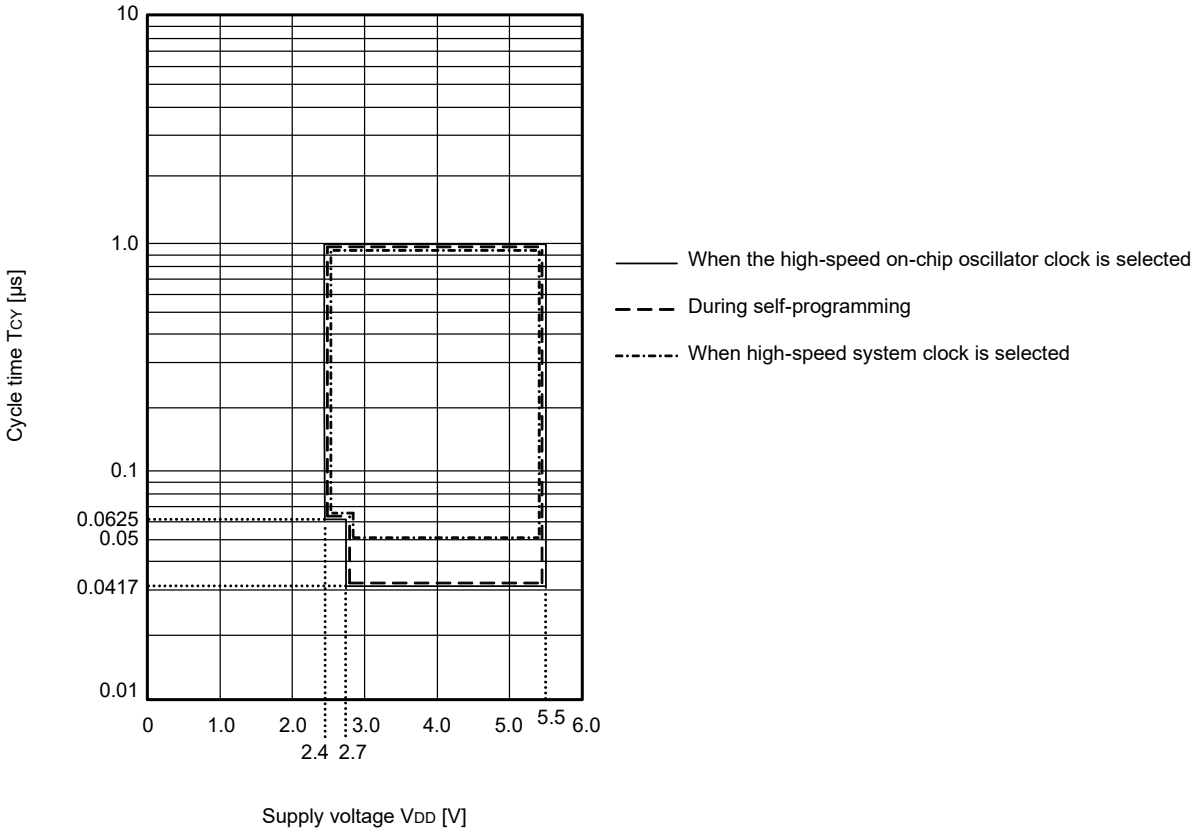
(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V) **(2/2)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt input high-level width, low-level width	tINTH, tINTL	INTP0 to INTP7 (when the pin on which the function is in use is multiplexed with pin functions other than P27 to P22)	1.8 V ≤ VDD ≤ 5.5 V	1			μs
		INTP2 to INTP7 (when the pin on which the function is in use is multiplexed with a pin function from among P27 to P22)	1.8 V ≤ AVDD ≤ 5.5 V	1			μs
$\overline{\text{RESET}}$ low-level width	tRSL			10			μs

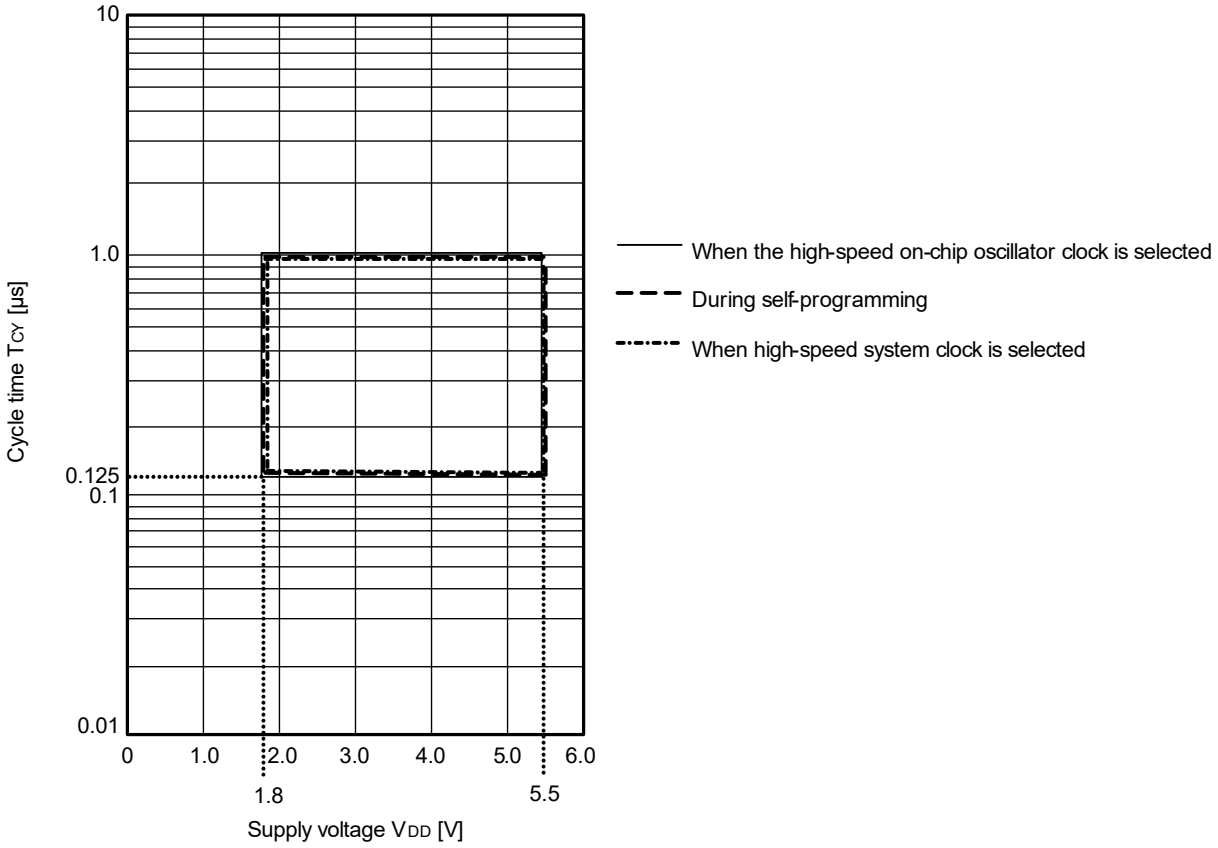
Remark fMCK: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 7))

Minimum Instruction Execution Time During Main System Clock Operation

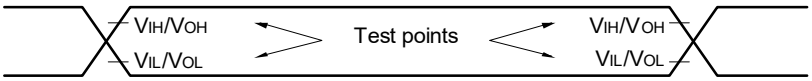
TCY vs VDD (HS (high-speed main) mode)



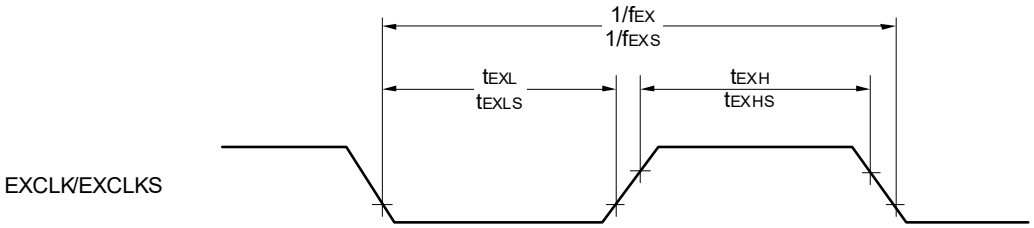
TCY vs VDD (LS (low-speed main) mode)



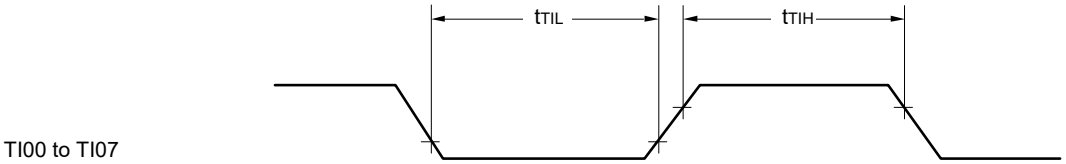
AC Timing Test Points

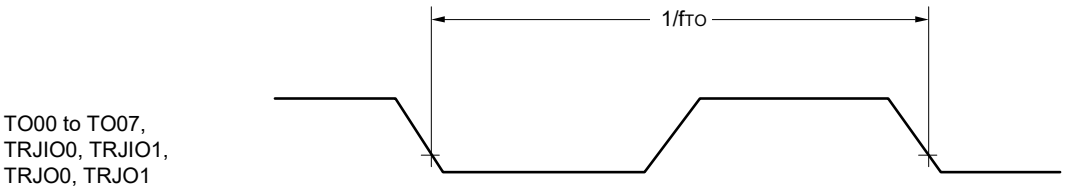


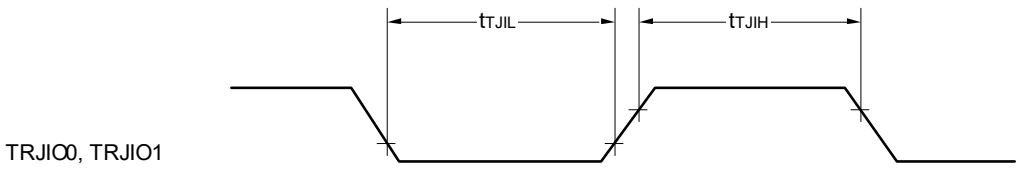
External System Clock Timing



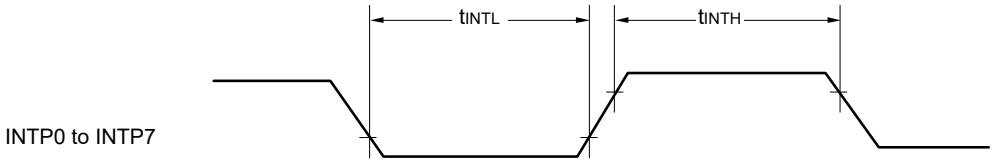
TI/TO Timing



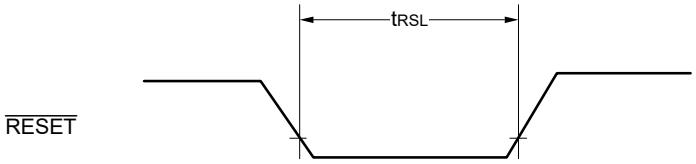




Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



3.5 Peripheral Functions Characteristics

3.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 1		2.4 V ≤ VDD ≤ 5.5 V		fMCK/6 Note 2		fMCK/6 Note 2	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 3		4.0		1.3	Mbps
		1.8 V ≤ VDD ≤ 5.5 V	—			fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 3	—			1.3	Mbps

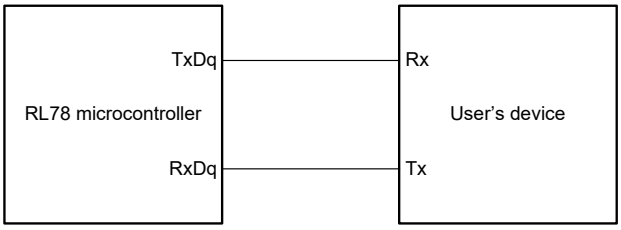
Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

Note 2. The following conditions are required for low voltage interface.
2.4 V ≤ VDD < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ VDD < 2.4 V: MAX. 1.3 Mbps

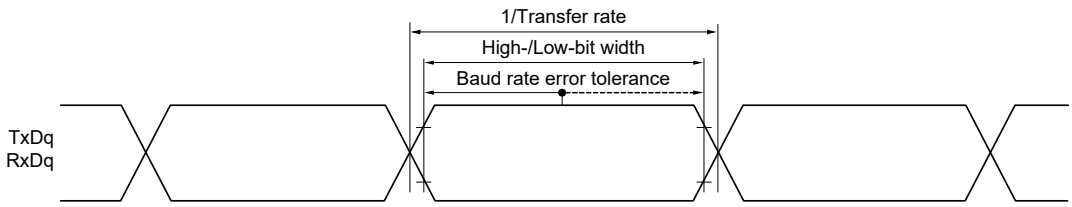
Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ VDD ≤ 5.5 V)
16 MHz (2.4 V ≤ VDD ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ VDD ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 0 to 2), g: PIM or POM number (g = 0, 1, 3, 4, 5, 8)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tKCY1	tKCY1 ≥ 4/fCLK	2.7 V ≤ VDD ≤ 5.5 V	167		500		ns
			2.4 V ≤ VDD ≤ 5.5 V	250		500		ns
			1.8 V ≤ VDD ≤ 5.5 V	—		500		ns
SCKp high-/low-level width	tKH1, tKL1	4.0 V ≤ VDD ≤ 5.5 V		tKCY1/2 - 12		tKCY1/2 - 50		ns
		2.7 V ≤ VDD ≤ 5.5 V		tKCY1/2 - 18		tKCY1/2 - 50		ns
		2.4 V ≤ VDD ≤ 5.5 V		tKCY1/2 - 38		tKCY1/2 - 50		ns
		1.8 V ≤ VDD ≤ 5.5 V		—		tKCY1/2 - 50		ns
SIp setup time (to SCKp↑) Note 1	tSIK1	4.0 V ≤ VDD ≤ 5.5 V		44		110		ns
		2.7 V ≤ VDD ≤ 5.5 V		44		110		ns
		2.4 V ≤ VDD ≤ 5.5 V		75		110		ns
		1.8 V ≤ VDD ≤ 5.5 V		—		110		ns
SIp hold time (from SCKp↑) Note 2	tKSI1	2.4 V ≤ VDD ≤ 5.5 V		19		19		ns
		1.8 V ≤ VDD ≤ 5.5 V		—		19		ns
Delay time from SCKp↓ to SOp output Note 3	tKSO1	C = 30 pF Note 4	2.7 V ≤ VDD ≤ 5.5 V		25		50	ns
			2.4 V ≤ VDD ≤ 5.5 V		25		50	ns
			1.8 V ≤ VDD ≤ 5.5 V		—		50	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2),
g: PIMand POM number (g = 0, 1, 3, 4, 5, 8)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00, 02, 10))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}		—		ns
			f_{MCK} ≤ 20 MHz	8/f_{MCK}		6/f_{MCK}		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	16 MHz > f_{MCK}	8/f_{MCK}		—		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 500		6/f_{MCK} and 500		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		—		6/f_{MCK} and 750		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		—		t_{KCY2}/2 - 18		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 20		1/f_{MCK} + 30		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		—		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}	2.4 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		—		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 44		2/f_{MCK} + 110	ns
			2.4 V ≤ V_{DD} ≤ 5.5 V		2/f_{MCK} + 75		2/f_{MCK} + 110	ns
			1.8 V ≤ V_{DD} ≤ 5.5 V		—		2/f_{MCK} + 110	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), g: PIM number (g = 0, 1, 3, 4, 5, 8)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

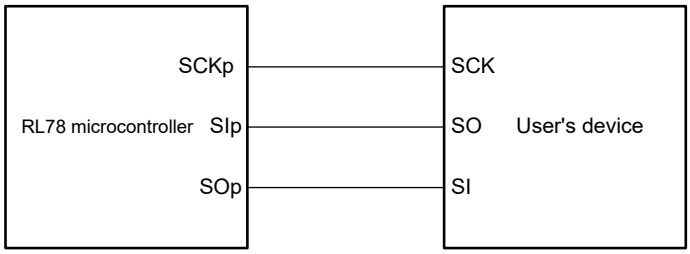
(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V) **(2/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
$\overline{SSI00}$ setup time	tSSIK	DAPmn = 0	2.7 V ≤ VDD ≤ 5.5 V	120		120		ns
			2.4 V ≤ VDD ≤ 5.5 V	200		200		ns
			1.8 V ≤ VDD ≤ 5.5 V	—		200		ns
		DAPmn = 1	2.7 V ≤ VDD ≤ 5.5 V	1/fMCK + 120		1/fMCK + 120		ns
			2.4 V ≤ VDD ≤ 5.5 V	1/fMCK + 200		1/fMCK + 200		ns
			1.8 V ≤ VDD ≤ 5.5 V	—		1/fMCK + 200		ns
$\overline{SSI00}$ hold time	tKSSI	DAPmn = 0	2.7 V ≤ VDD ≤ 5.5 V	1/fMCK + 120		1/fMCK + 120		ns
			2.4 V ≤ VDD ≤ 5.5 V	1/fMCK + 200		1/fMCK + 200		ns
			1.8 V ≤ VDD ≤ 5.5 V	—		1/fMCK + 200		ns
		DAPmn = 1	2.7 V ≤ VDD ≤ 5.5 V	120		120		ns
			2.4 V ≤ VDD ≤ 5.5 V	200		200		ns
			1.8 V ≤ VDD ≤ 5.5 V	—		200		ns

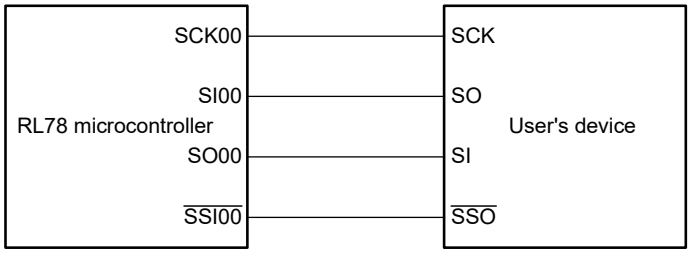
Caution **Select the normal input buffer for the SIp and SCKp pins and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 4)

CSI mode connection diagram (during communication at same potential)

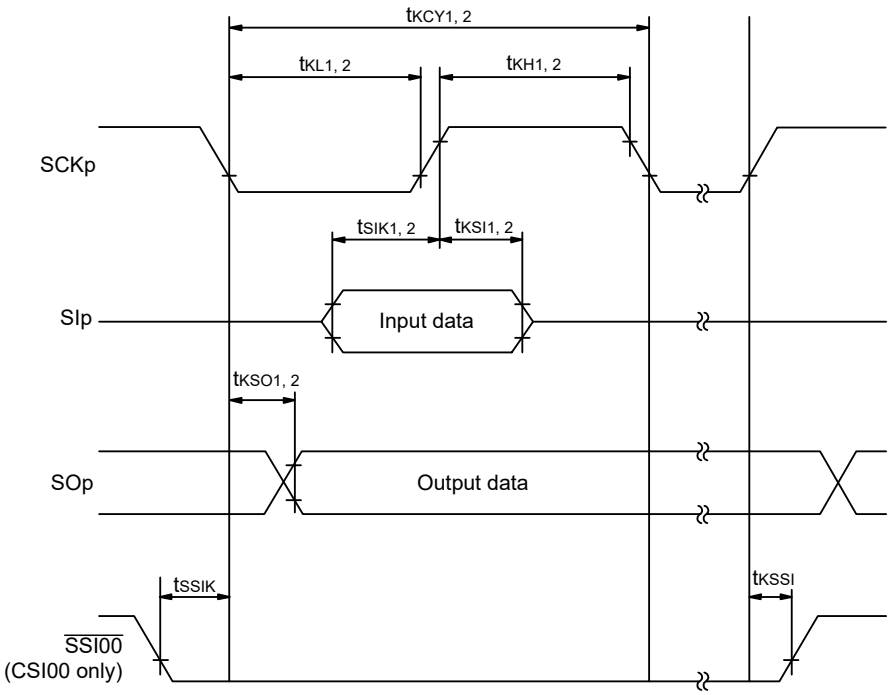


CSI mode connection diagram (during communication at same potential)
(Slave transmission of slave select input function (CSI00))

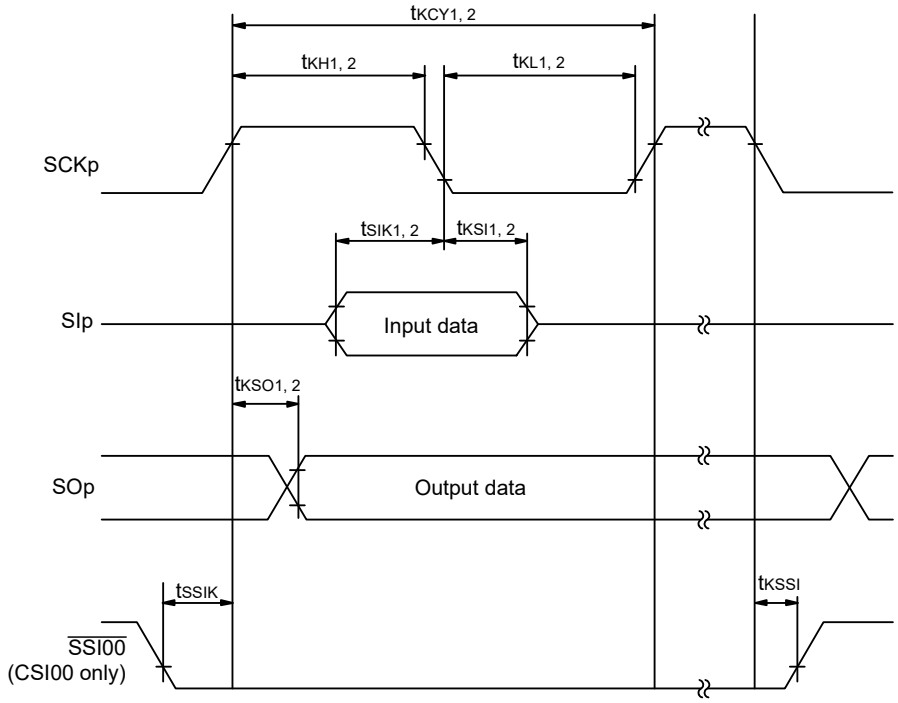


Remark p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

(4) During communication at same potential (simplified I²C mode)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		400 Note 1	kHz
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1		400 Note 1	kHz
		1.8 V (2.4 V Note 3) ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 85 Note 2		1/f_{MCK} + 145 Note 2		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 145 Note 2		1/f_{MCK} + 145 Note 2		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 230 Note 2		1/f_{MCK} + 230 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	355	0	355	ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	ns

Note 1. The value must be equal to or less than f_{MCK}/4.

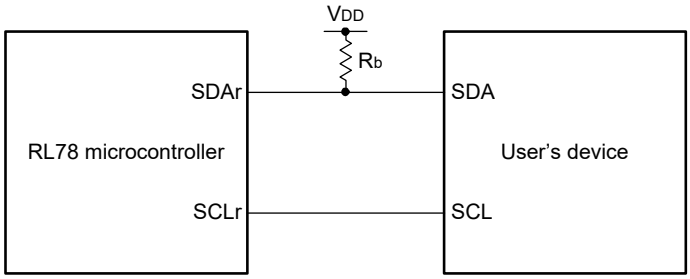
Note 2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Note 3. Condition in the HS (high-speed main) mode

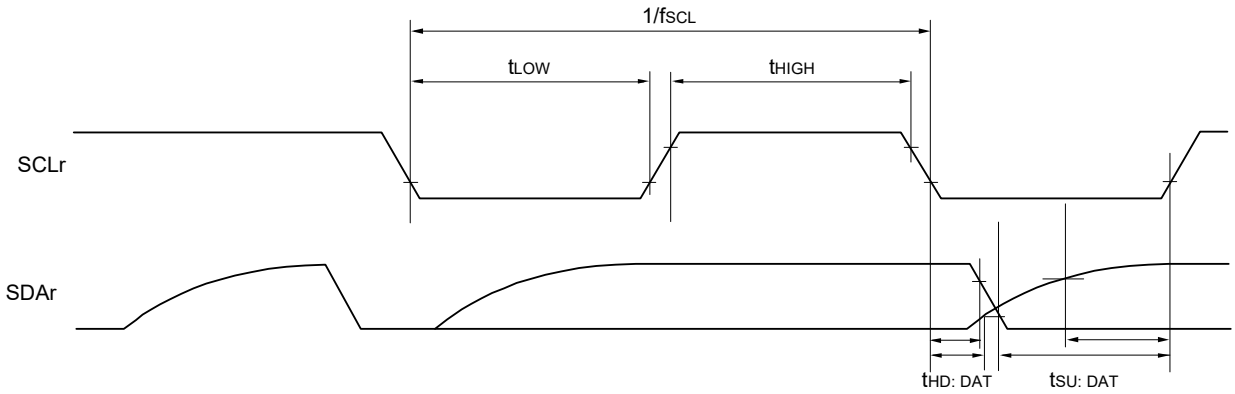
Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(**Remarks** are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remark 1. Rb [Ω]: Communication line (SDAr) pull-up resistance, Cb [F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 10, 20), g: PIM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		4.0		1.3	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		4.0		1.3	Mbps
			1.8 V (2.4 V Note 5) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		f_{MCK}/6 Notes 1, 2, 3		f_{MCK}/6 Notes 1, 2, 3	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		4.0		1.3	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

Note 2. Use it with $V_{DD} \geq V_b$

Note 3. The following conditions are required for low voltage interface.
2.4 V ≤ V_{DD} < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ V_{DD} < 2.4 V: MAX. 1.3 Mbps

Note 4. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) Mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)
LS (low-speed main) Mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)

Note 5. Condition in the HS (high-speed main) mode

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. V_b [V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 2), g: PIM or POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		Note 3		Note 3	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 4		1.2 Note 4	Mbps
			1.8 V (2.4 V Note 8) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		Notes 5, 6		Notes 5, 6	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 7		0.43 Note 7	Mbps

Note 1. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ V_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 4. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use it with V_{DD} ≥ V_b

Note 6. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8 V ≤ V_{DD} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

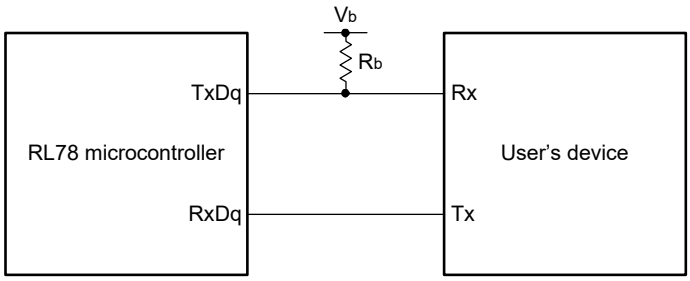
* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 7. This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

Note 8. Condition in the HS (high-speed main) mode

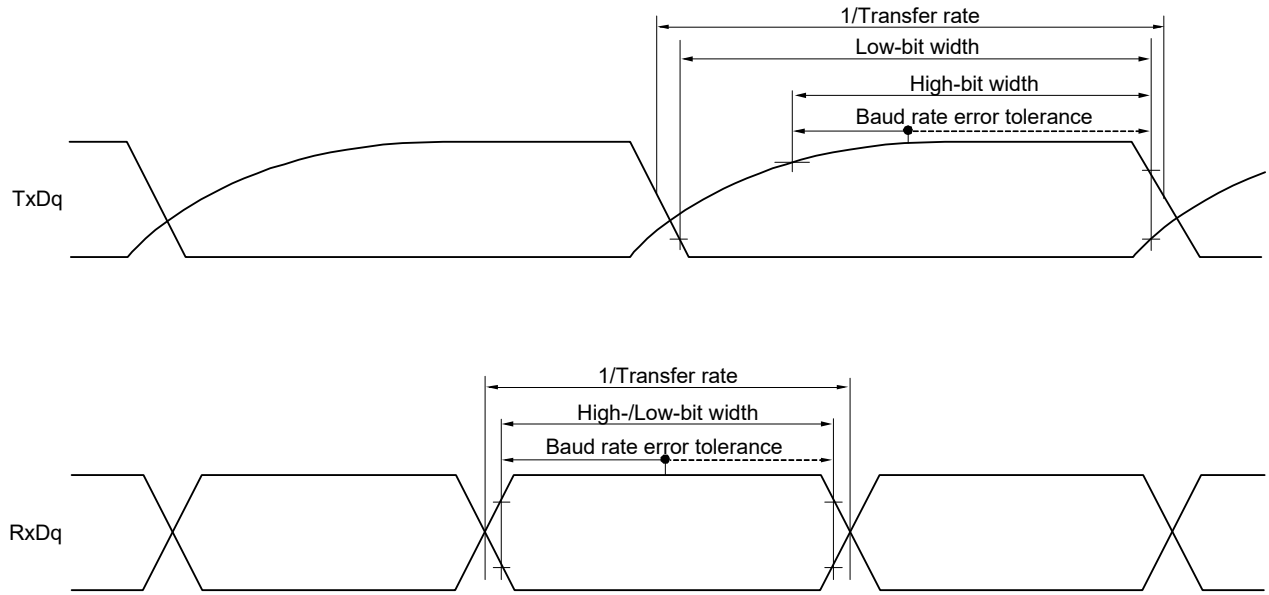
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



(**Remarks** are listed on the next page.)

UART mode bit width (during communication at different potential) (reference)



Remark 1. R_b [Ω]: Communication line (TxDq) pull-up resistance,
C_b [F]: Communication line (TxDq) load capacitance, V_b [V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 2), g: PIM or POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		1150		ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500 Note 1		1150		ns
			1.8 V (2.4 V Note 2) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	1150 Note 1		1150		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 75		t_{KCY1}/2 - 75		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 170		t_{KCY1}/2 - 170		ns
		1.8 V (2.4 V Note 2) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 458		t_{KCY1}/2 - 458		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 12		t_{KCY1}/2 - 50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 18		t_{KCY1}/2 - 50		ns
		1.8 V (2.4 V Note 2) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns

Note 1. Use it with V_{DD} ≥ V_b

Note 2. Condition in the HS (high-speed main) mode

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed two pages after the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V) (2/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) Note 1	tSIK1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	81		479		ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	177		479		ns
		1.8 V (2.4 V Note 4) ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	479		479		ns
SIp hold time (from SCKp↓) Note 1	tKSI1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		ns
		1.8 V (2.4 V Note 4) ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	19		19		ns
Delay time from SCKp↑ to SOp output Note 1	tKSO1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		100		100	ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		195		195	ns
		1.8 V (2.4 V Note 4) ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ		483		483	ns
SIp setup time (to SCKp↓) Note 2	tSIK1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	44		110		ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	44		110		ns
		1.8 V (2.4 V Note 4) ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	110		110		ns
SIp hold time (from SCKp↓) Note 2	tKSI1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		ns
		1.8 V (2.4 V Note 4) ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ	19		19		ns
Delay time from SCKp↑ to SOp output Note 2	tKSO1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		25		25	ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		25		25	ns
		1.8 V (2.4 V Note 4) ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 3, Cb = 30 pF, Rb = 5.5 kΩ		25		25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

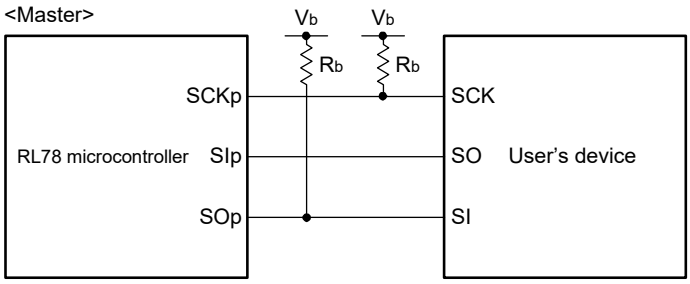
Note 3. Use it with VDD ≥ Vb

Note 4. Condition in the HS (high-speed main) mode

(**Caution** and remarks are listed on the next page.)

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

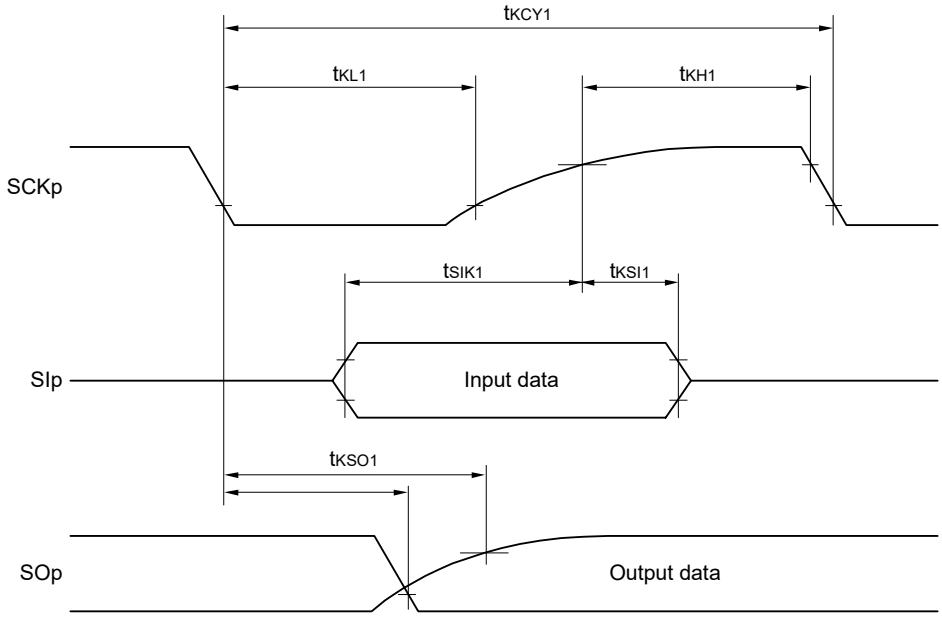


Remark 1. R_b [Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b [F]: Communication line (SCKp, SOp) load capacitance, V_b [V]: Communication line voltage

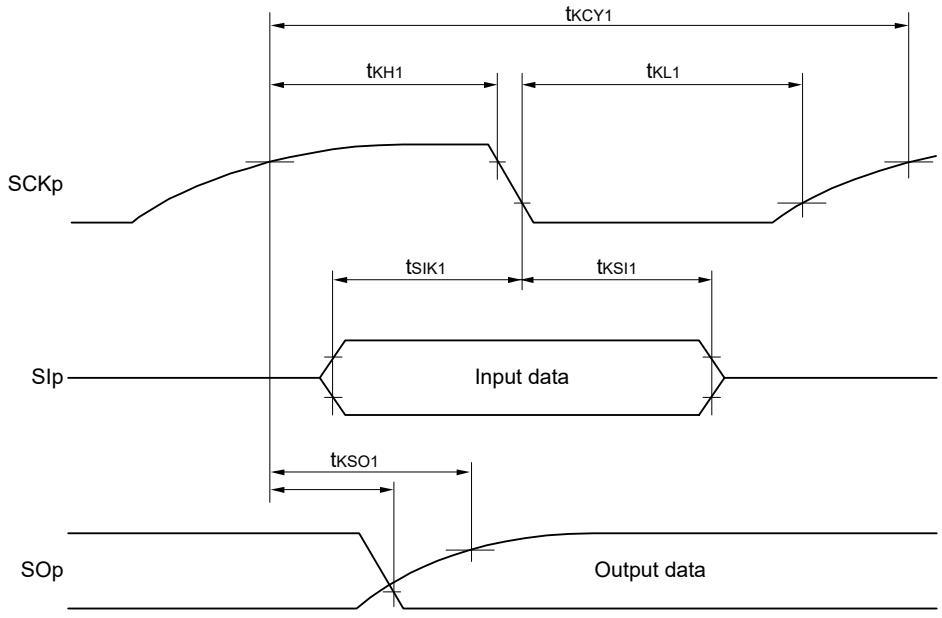
Remark 2. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), g: PIM or POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 02, 10))

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2),
g: PIM or POM number (g = 0, 1, 3, 4, 5, 8)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK}	12/f_{MCK}		—		ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		—		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK}	16/f_{MCK}		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		ns
		1.8 V (2.4 V Note 6) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	20 MHz < f_{MCK}	36/f_{MCK}		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}		ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 - 12		t_{KCY2}/2 - 50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 - 18		t_{KCY2}/2 - 50		ns
		1.8 V (2.4 V Note 6) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 20		1/f_{MCK} + 30		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 20		1/f_{MCK} + 30		ns
		1.8 V (2.4 V Note 6) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		1.8 V (2.4 V Note 6) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 5	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} + 120		2/f_{MCK} + 573	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 214		2/f_{MCK} + 573	ns
		1.8 V (2.4 V Note 6) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} + 573		2/f_{MCK} + 573	ns

(**Notes**, **Cautions**, and **Remarks** are listed on the next page.)

Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Note 2. Use it with $V_{DD} \geq V_b$.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

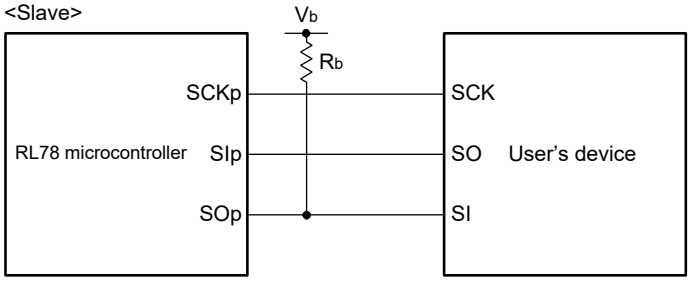
Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 0.

Note 5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 6. Condition in the HS (high-speed main) mode

Caution **Select the TTL input buffer for the SIp and SCKp pins, and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

CSI mode connection diagram (during communication at different potential)

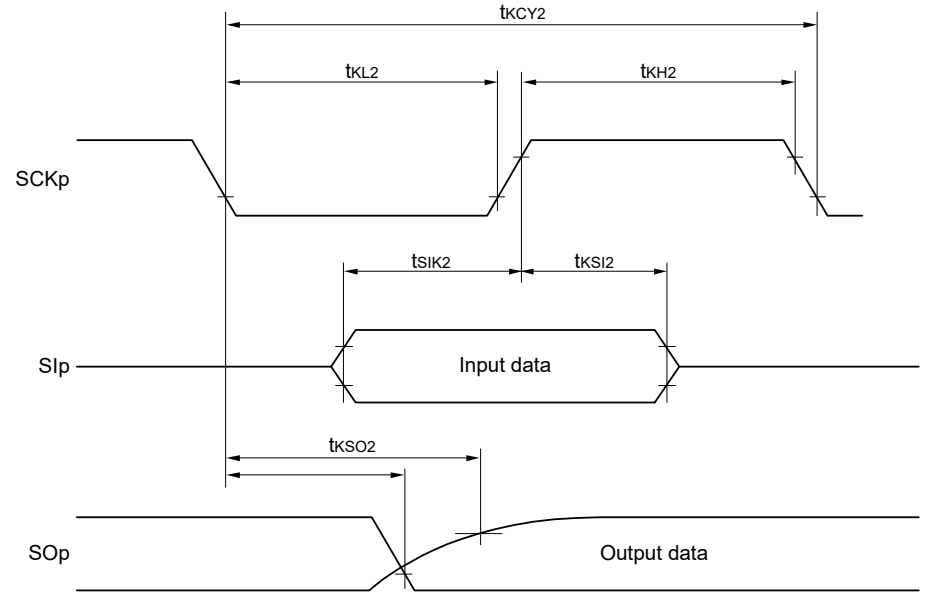


Remark 1. R_b [Ω]: Communication line (SOp) pull-up resistance, C_b [F]: Communication line (SOp) load capacitance, V_b [V]: Communication line voltage

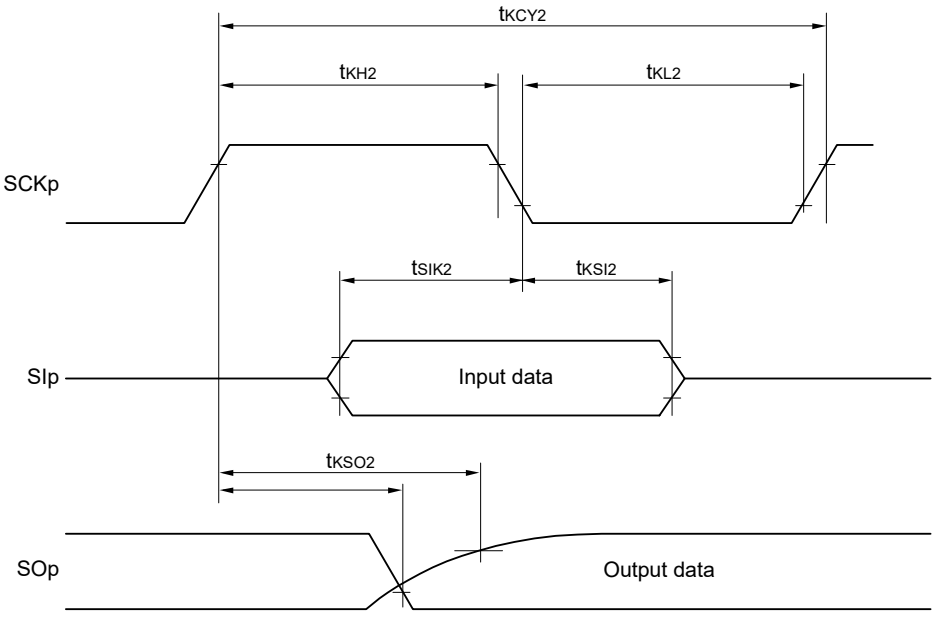
Remark 2. p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0 , 2), g: PIM or POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02, 10))

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark p: CSI number (p = 00, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 0, 2),
g: PIM or POM number (g = 0, 1, 3, 4, 5, 8)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		300 Note 1	kHz
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		300 Note 1	kHz
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		400 Note 1		300 Note 1	kHz
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		400 Note 1		300 Note 1	kHz
		1.8 V (2.4 V Note 4) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ		400 Note 1		300 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1550		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1550		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1150		1550		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1150		1550		ns
		1.8 V (2.4 V Note 4) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1550		1550		ns
Hold time when SCLr = “H”	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	245		610		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	200		610		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	675		610		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	600		610		ns
		1.8 V (2.4 V Note 4) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	610		610		ns

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode)

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 135 Note 3		1/f_{MCK} + 190 Note 2		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 135 Note 3		1/f_{MCK} + 190 Note 2		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		ns
		1.8 V (2.4 V Note 4) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	355	0	355	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	355	0	355	ns
		1.8 V (2.4 V Note 4) ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	0	405	0	405	ns

Note 1. The value must be equal to or less than f_{MCK}/4.

Note 2. Use it with V_{DD} ≥ V_b

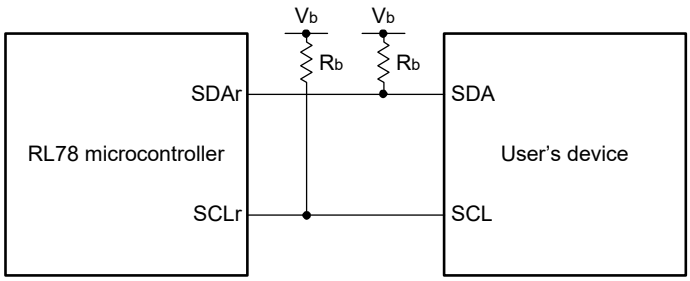
Note 3. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

Note 4. Condition in the HS (high-speed main) mode

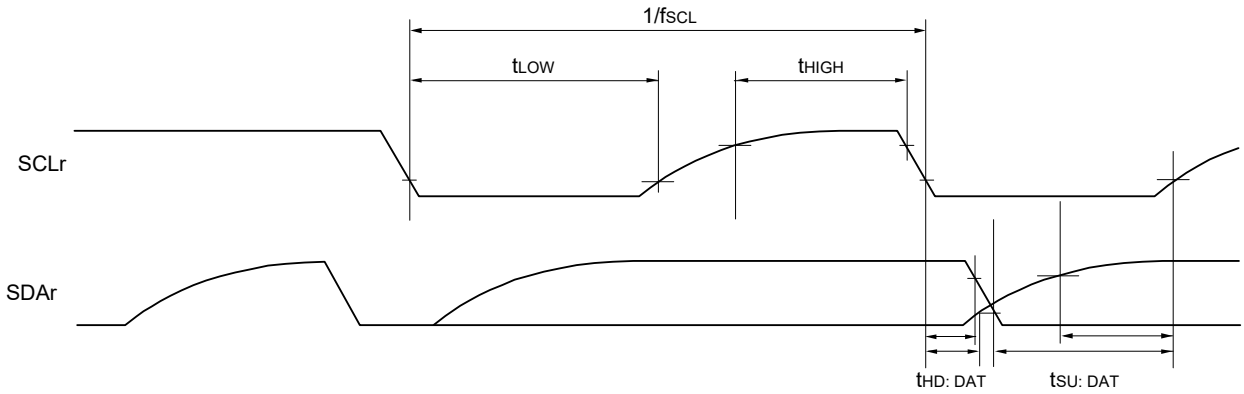
Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remark 1. Rb [Ω]: Communication line (SDAr, SCLr) pull-up resistance, Cb [F]: Communication line (SDAr, SCLr) load capacitance, Vb [V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 10, 20), g: PIM, POM number (g = 0, 1, 3, 4, 5, 8)

Remark 3. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0, 2), mn = 00, 02, 10)

3.5.2 Serial Interface UARTMG

(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		fSUB = 38.4 kHz	200		9600	bps
		fSUB = 38.4 kHz (when the clock doubler is in use)	200		19200	bps

3.5.3 Serial interface IICA

(1) I²C standard mode

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	100	0	100	kHz
			1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V	0	100	0	100	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		4.7		μs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		4.7		4.7		μs
Hold time Note 1	$t_{HD:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		4.0		μs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		4.0		4.0		μs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		4.7		μs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		4.7		4.7		μs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		4.0		μs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		4.0		4.0		μs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		250		250		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		250		250		ns
Data hold time (transmission) Note 2	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	3.45	0	3.45	μs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		0		0	3.45	μs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		4.0		μs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		4.0		4.0		μs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		4.7		μs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		4.7		4.7		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Note 3. Condition in the HS (high-speed main) mode

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I^2C fast mode

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	400	0	400	kHz
			1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V	0	400	0	400	kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		0.6		μs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		0.6		0.6		μs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		0.6		μs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		0.6		0.6		μs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.3		1.3		μs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		1.3		1.3		μs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		0.6		μs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		0.6		0.6		μs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		100		100		ns
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		100		100		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	0.9	0	0.9	μs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		0		0	0.9	μs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.6		0.6		μs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		0.6		0.6		μs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.3		1.3		μs
		1.8 V (2.4 V Note 3) ≤ V_{DD} ≤ 5.5 V		1.3		1.3		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Note 3. Condition in the HS (high-speed main) mode

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(3) I²C fast mode plus

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

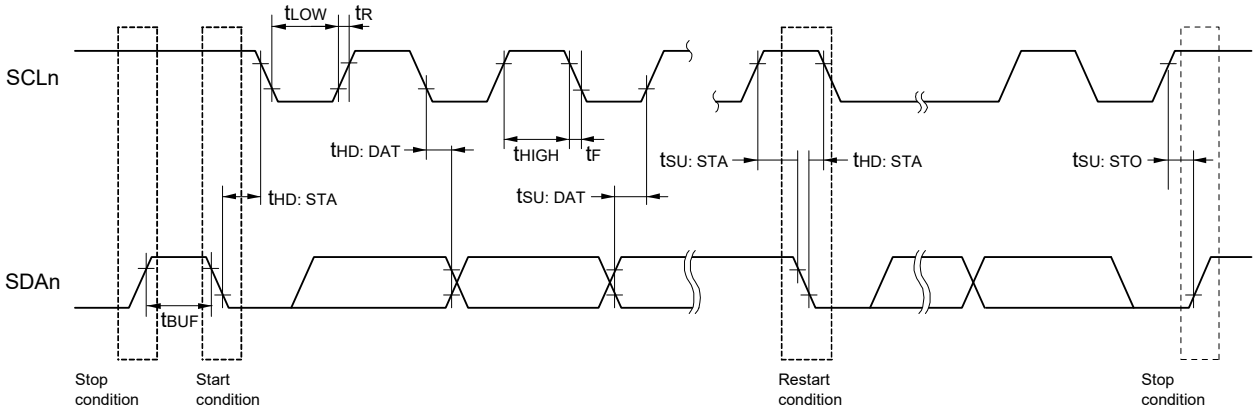
Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	1000	—		kHz
Setup time of restart condition	$t_{SU: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		—		µs
Hold time Note 1	$t_{HD: STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		—		µs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.5		—		µs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		—		µs
Data setup time (reception)	$t_{SU: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		50		—		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	0.45	—		µs
Setup time of stop condition	$t_{SU: STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0.26		—		µs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		0.5		—		µs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



3.6 Analog Characteristics

3.6.1 A/D converter Characteristics

(1) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI8 to ANI10, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V, reference voltage (+) = V_{DD}, reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI8 to ANI10	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	µs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
		10-bit resolution Target pin: internal reference voltage and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	µs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5626		39	µs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	µs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI8 to ANI10		0		V_{DD}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{BGR} Note 3			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{TMPS25} Note 3			V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. Refer to **3.6.2 Temperature sensor/internal reference voltage output characteristics**.

(2) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = VSS (ADREFM = 0), target pin: ANI8 to ANI10

(TA = -40 to +85°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, reference voltage (+) = VBGR Note 3, reference voltage (–) = VSS = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	tCONV	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2,	EZS	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±(0.60+0.35)	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±(2.0+0.5)	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±(1.0+0.2)	LSB
Analog input voltage	VAIN			0		VBGR Note 3	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. Refer to **3.6.2 Temperature sensor/internal reference voltage output characteristics**.

3.6.2 Temperature sensor/internal reference voltage output characteristics

(TA = -40 to +85°C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V, HS (high-speed main) Mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	VTEMP	TA = +25°C		1.05		V
Internal reference voltage	VBGR		1.38	1.45	1.5	V
Temperature coefficient	FVTMPS	Temperature sensor output voltage that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	tAMP	2.4 V ≤ VDD ≤ 5.5 V	5			μs

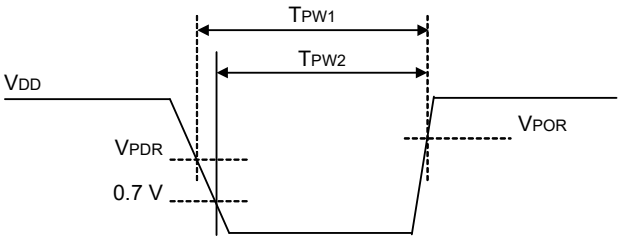
3.6.3 POR circuit characteristics

(TA = -40 to +85°C, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	VPOR	Power supply rise time	1.47	1.51	1.55	V
	VPDR	Power supply fall time Note 1	1.46	1.50	1.54	V
Minimum pulse width Note 2	TPW1	Other than STOP/SUB HALT/SUB RUN	300			μs
	TPW2	STOP/SUB HALT/SUB RUN	300			μs

Note 1. If the power supply voltage falls while the voltage detector is off, be sure to either shift to STOP mode or execute a reset by using the voltage detector or external reset pin before the power supply voltage falls below the minimum operating voltage specified in **3.4 AC Characteristics**.

Note 2. Minimum time required for a POR reset when VDD falls below VPDR. This is also the minimum time required for a POR reset from when VDD exceeds below 0.7 V to when VDD exceeds VPOR while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



3.6.4 LVD circuit characteristics

(1) LVD detection voltage in reset mode and interrupt mode

(T_A = -40 to +85°C, $V_{PDR} \le AV_{DD} = V_{DD} \le 5.5$ V, $AV_{SS} = V_{SS}$ = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Rising edge	3.98	4.06	4.14	V
			Falling edge	3.90	3.98	4.06	V
		V_{LVD1}	Rising edge	3.68	3.75	3.82	V
			Falling edge	3.60	3.67	3.74	V
		V_{LVD2}	Rising edge	3.07	3.13	3.19	V
			Falling edge	3.00	3.06	3.12	V
		V_{LVD3}	Rising edge	2.96	3.02	3.08	V
			Falling edge	2.90	2.96	3.02	V
		V_{LVD4}	Rising edge	2.86	2.92	2.97	V
			Falling edge	2.80	2.86	2.91	V
		V_{LVD5}	Rising edge	2.76	2.81	2.87	V
			Falling edge	2.70	2.75	2.81	V
		V_{LVD6}	Rising edge	2.66	2.71	2.76	V
			Falling edge	2.60	2.65	2.70	V
		V_{LVD7}	Rising edge	2.56	2.61	2.66	V
			Falling edge	2.50	2.55	2.60	V
		V_{LVD8}	Rising edge	2.45	2.50	2.55	V
			Falling edge	2.40	2.45	2.50	V
		V_{LVD9}	Rising edge	2.05	2.09	2.13	V
			Falling edge	2.00	2.04	2.08	V
		V_{LVD10}	Rising edge	1.94	1.98	2.02	V
			Falling edge	1.90	1.94	1.98	V
		V_{LVD11}	Rising edge	1.84	1.88	1.91	V
			Falling edge	1.80	1.84	1.87	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

Caution Set the detection voltage (V_{LVD}) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.

HS (high-speed main) mode: V_{DD} = 2.7 to 5.5 V @ 1 MHz to 24 MHz

V_{DD} = 2.4 to 5.5 V @ 1 MHz to 16 MHz

LS (low-speed main) mode: V_{DD} = 1.8 to 5.5 V @ 1 MHz to 8 MHz

(2) LVD Detection Voltage of Interrupt & Reset Mode

(T_A = -40 to +85°C, $V_{PDR} \le AV_{DD} = V_{DD} \le 5.5$ V, $AV_{SS} = V_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDB0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1, falling reset voltage: 1.8 V		1.80	1.84	1.87	V
	V_{LVDB1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVDB2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVDB3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVDC0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0, falling reset voltage: 2.4 V		2.40	2.45	2.50	V
	V_{LVDC1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVDC2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVDC3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
			Falling interrupt voltage	3.60	3.67	3.74	V
	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage: 2.7 V		2.70	2.75	2.81	V
	V_{LVDD1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDD2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V
	V_{LVDC3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
			Falling interrupt voltage	3.90	3.98	4.06	V

3.7 Power supply voltage rising slope characteristics

(T_A = -40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SV_{DD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.

3.8 LCD Characteristics

3.8.1 Resistance division method

(1) Static display mode

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.0		V_{DD}	V

(2) 1/2 bias method, 1/4 bias method

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.7		V_{DD}	V

(3) 1/3 bias method

(T_A = -40 to +85°C, V_{L4} (MIN.) ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.5		V_{DD}	V

3.8.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C4 Note 1 = 0.47 µF Note 2	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V_{L2}	C1 to C4 Note 1 = 0.47 µF		2 V_{L1} - 0.1	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L4}	C1 to C4 Note 1 = 0.47 µF		3 V_{L1}- 0.15	3 V_{L1}	3 V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C4 Note 1 = 0.47µF		500			ms

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 µF±30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

(2) 1/4 bias method

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C5 Note 1 = 0.47 μF Note 2	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
Doubler output voltage	V_{L2}	C1 to C5 Note 1 = 0.47 μF		2 V_{L1} - 0.08	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L3}	C1 to C5 Note 1 = 0.47 μF		3 V_{L1} - 0.12	3 V_{L1}	3 V_{L1}	V
Quadruply output voltage	V_{L4}	C1 to C5 Note 1 = 0.47 μF		4 V_{L1} - 0.16	4 V_{L1}	4 V_{L1}	V
Reference voltage setup time Note 2	t_{VWAIT1}			5			ms
Voltage boost wait time Note 3	t_{VWAIT2}	C1 to C5 Note 1 = 0.47μF		500			ms

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L3} and GND
C5: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = C5 = 0.47 μF±30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

3.8.3 Capacitor split method

(1) 1/3 bias method

(T_A = -40 to +85°C, 2.2 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{L4} voltage	V_{L4}	C1 to C4 = 0.47 μF Note 2		V_{DD}		V
V_{L2} voltage	V_{L2}	C1 to C4 = 0.47 μF Note 2	2/3 V_{L4} - 0.1	2/3 V_{L4}	2/3 V_{L4} + 0.1	V
V_{L1} voltage	V_{L1}	C1 to C4 = 0.47 μF Note 2	1/3 V_{L4} - 0.1	1/3 V_{L4}	1/3 V_{L4} + 0.1	V
Capacitor split wait time Note 1	t_{VWAIT}		100			ms

Note 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

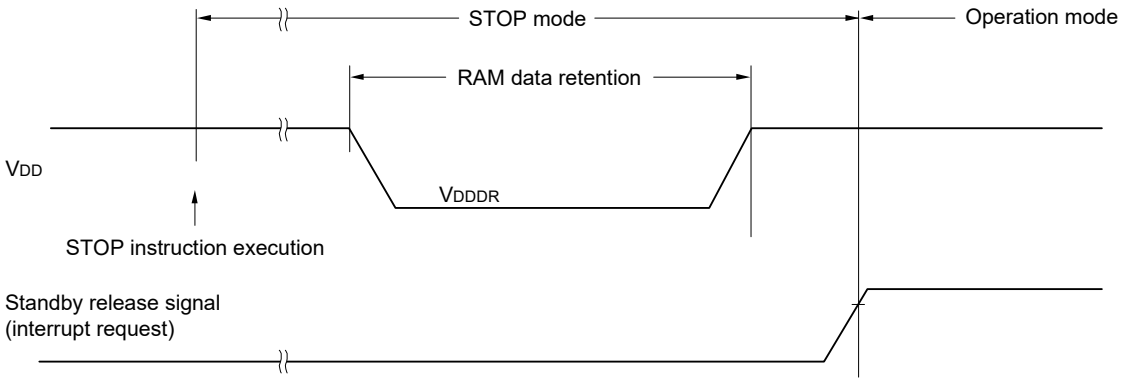
Note 2. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 μF±30%

3.9 RAM Data Retention Characteristics

(TA = -40 to +85°C, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.46 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



3.10 Flash Memory Programming Characteristics

(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK	1.8 V ≤ VDD ≤ 5.5 V		1		24	MHz
Number of code flash rewrites Notes 1, 2, 3	Cerwr	Retained for 20 years	TA = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year	TA = 25°C		1,000,000		
		Retained for 5 years	TA = 85°C	100,000			
		Retained for 20 years	TA = 85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

3.11 Dedicated Flash Memory Programmer Communication (UART)

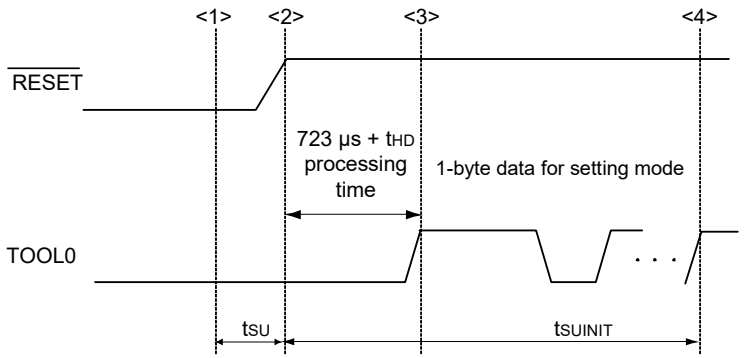
(TA = -40 to +85°C, 1.8 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3.12 Timing of Entry to Flash Memory Programming Modes

(T_A = -40 to +85°C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.
t_{SU}: How long from when the TOOL0 pin is placed at the low level until a pin reset ends
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

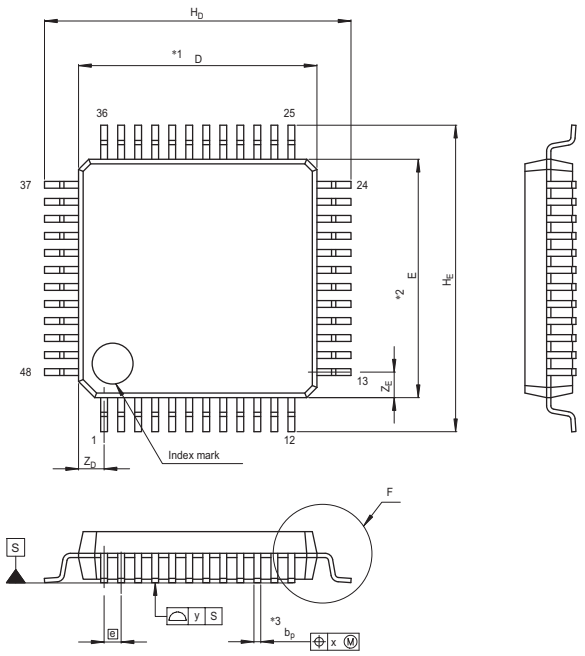
Remark

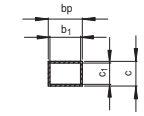
4. PACKAGE DRAWINGS

4.1 48-pin products

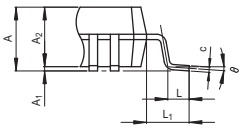
R5F11NGGAFB, R5F11NGFAFB

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g





Terminal cross section



Detail F

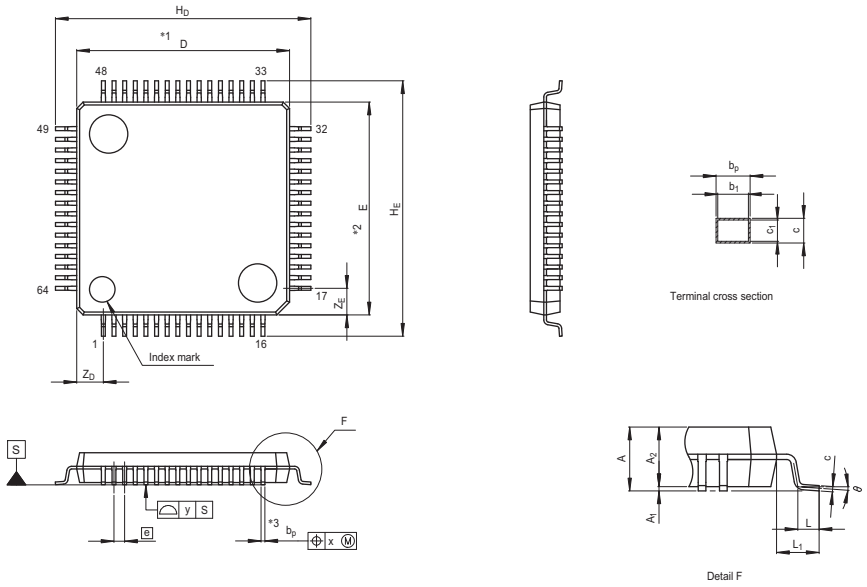
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

4.2 64-pin products

R5F11NLGAFB, R5F11NLFAFB

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g

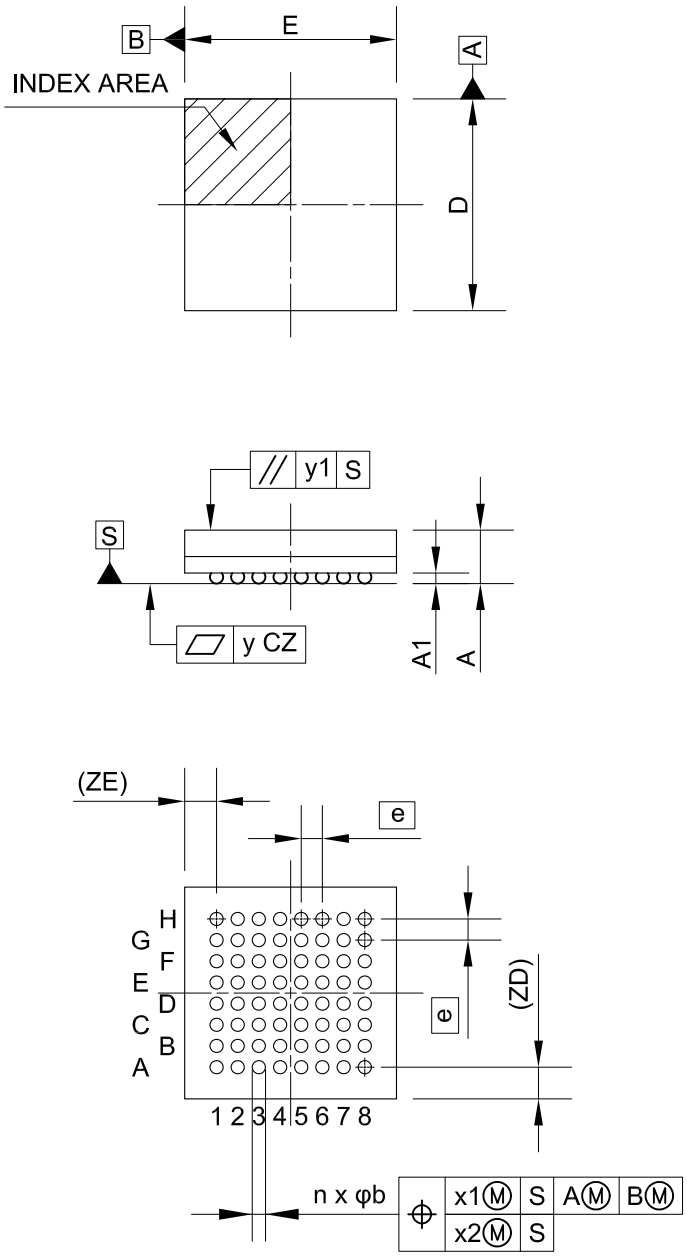


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

R5F11PLGABG, R5F11PLFABG

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-TFBGA64-4x4-0.40	PTBG0064LA-A	0.03

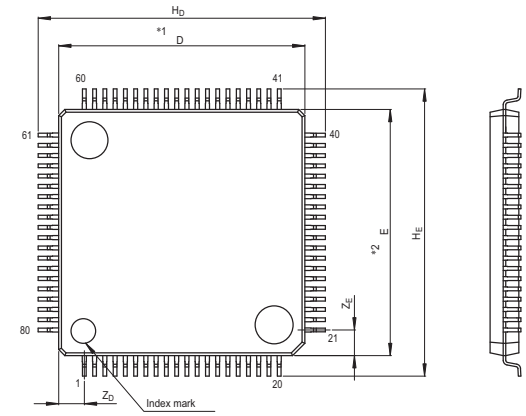


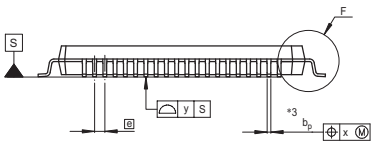
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	3.9	4.0	4.1
E	3.9	4.0	4.1
A	—	—	1.10
A1	0.15	0.20	0.25
b	0.20	0.25	0.30
e	—	0.40	—
x1	—	—	0.15
x2	—	—	0.05
y	—	—	0.08
y1	—	—	0.20
n	—	64	—
ZD	—	0.60	—
ZE	—	0.60	—

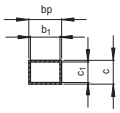
4.3 80-pin products

R5F11NMGAFB, R5F11NMFAFB, R5F11NMEAFB
R5F11RMGDFB

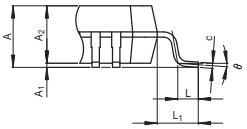
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g







Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

REVISION HISTORY	RL78/H1D Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Apr 13 2018	—	First Edition issued

SuperFlash is a registered trademark of Silicon Storage Technology, Inc. in several countries including the United States and Japan.

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

All trademarks and registered trademarks are the property of their respective owners.

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

RENESAS

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

© 2018 Renesas Electronics Corporation. All rights reserved.

Colophon 7.0

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Renesas Electronics:

R5F11NMFAFB#30 R5F11NMEAFB#30 R5F11PLGABG#U0 R5F11NGFAFB#30 R5F11NGGAFB#30 R5F11PLFABG#U0 R5F11NMGAFB#30 R5F11NLFAFB#30 R5F11RMGDFB#30 R5F11NGFAFB#50 R5F11NGGAFB#50 R5F11NLFAFB#50 R5F11NLGAFB#30 R5F11NLGAFB#50 R5F11NMEAFB#50 R5F11NMFAFB#50 R5F11NMGAFB#50 R5F11RMGDFB#50

LifeElectronics
Живое партнерство

ООО «ЛайфЭлектроникс» **“LifeElectronics” LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru