Neo-Iso™ TS13103
Solid State Relay with Diagnostics and Power Transfer Output (PTO)

TRIUNE PRODUCTS

Features

- Low Quiescent Operating Currents
  2µA in OFF state
  5µA in ON state
- Supports galvanically-isolated I/O
- Galvanic power transfer from load supply
- Addressable for minimum GPIO usage
  Supports four physical address configurations
- Single control signal for on/off input (CLK)
  Microcontroller-compatible 1.7V to 5.5V input levels
  Configurable switching options
- Switch Characteristics:
  Bi-directional blocking in OFF state
  Single switch device
  60V switch and 290mΩ on-resistance
  Up to 2.5A operating current
- Package Options
  16 lead QFN package – 3x3mm, 1.0mm max height
- Operating Modes
  Zero-cross ON / OFF
  Immediate ON / OFF
  Dithering Mode for system power sharing
  Switch state polling

Summary Specification

- Junction operating temperature -40°C to 125°C
- Packaged in a 16 pin QFN (3x3)
- Product is lead-free, Halogen Free, RoHS / WEEE compliant

Description

The TS13103 is a galvanically isolated 60V power switch device with bi-directional blocking. The device includes an integrated 290mΩ high voltage switch allowing high efficiency switching of power loads or other high current applications. CLK input pin control sequences support switching options, including immediate on/off, zero-volt switch-on, zero-current switch-off, dither modes, as well as latching and non-latching behavior.

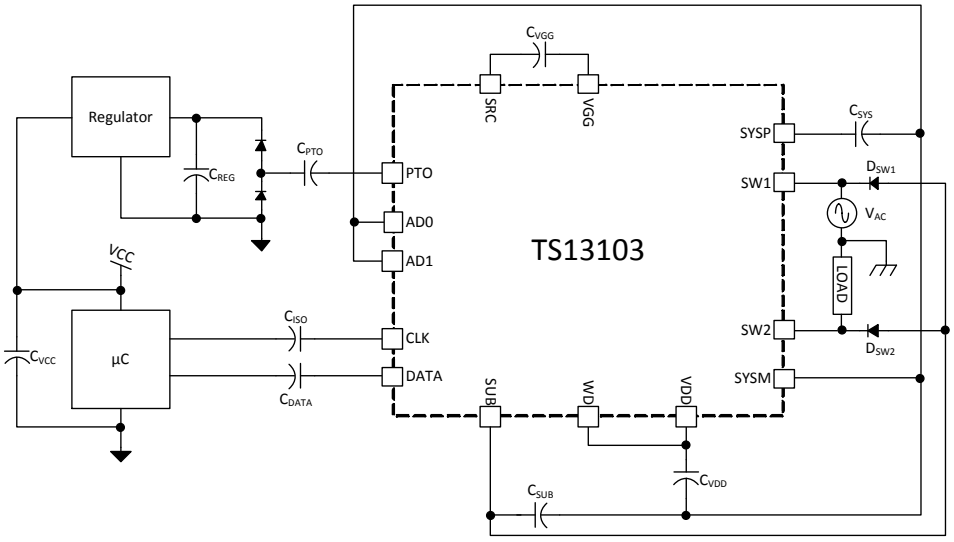
The TS13103 offers galvanic power transfer from the system AC supply to provide power to the low-voltage controller domain.

The TS13103 includes an integrated over-current protection to prevent device damage during short-circuit or other unusually high load conditions which opens the switch until the CLK turn on sequence is given.

Applications

- Power load / rail switching
- Input supply multiplexing
- Isolated power supplies
- Solid state relays
- HVAC control
- Sprinkler control
- Internet of Things (IoT)

Typical Application Circuit



Pin Description

Pin Symbol	Pin #	Function	Description
SYSP	1	Positive System Voltage	Connect C_{SYS} to SYSM
SYSM	2	Negative System Voltage	
SUB	3	IC Substrate Bias	Connect C_{SUB} Capacitor to SYSM
SRC	4	Switch Driver Supply Return	Local common supply return
VGG	5	Internal Switch Driver Supply	Connect Bypass Capacitor C_{VGG} to SRC
SW2	6	Switch Output Node 2	
SW2	7	Switch Output Node 2	
DATA	8	Data Output	AC Coupled Data Output
CLK	9	Clock Input	AC Coupled Clock Input
WD	10	Watch Dog	Control input for latching vs non-latching Switch
VDD	11	Internal Supply 1	Connect Bypass Capacitor C_{VDD} to SYSM
AD0	12	Address Select 0	For logic 0, must be tied to SYSM on PCB For logic 1, must be tied to VDD on PCB
AD1	13	Address Select 1	
PTO	14	Power Transfer Output	Connect to Power Transfer Capacitor C_{PTO}
SW1	15	Switch Output Node 1	
SW1	16	Switch Output Node 1	
PAD	PAD	Power PAD	Must be floating or connected to SUB

Functional Block Diagram

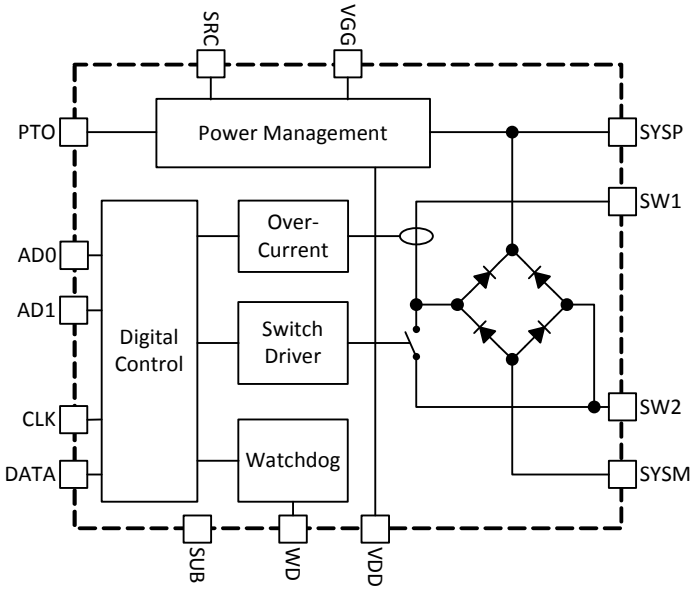


Figure 1: TS13103 Block Diagram

Absolute Maximum Ratings

Over operating free–air temperature range unless otherwise noted[1, 4]

Parameter	Range	Unit
SW1, SW2[2]	-1 to 60	V
SYSP, PTO[3]	-1 to 60	V
CLK , DATA, VDD, AD1, AD0, WD[3]	-0.3 to 5.5	V
VGG[2]	-0.3 to 5.5	V
SUB[2]	-55 to 0.3	V
Maximum Junction Temperature, $T_{J\,MAX}$	150	°C
Storage Temperature Range, T_{STG}	-65 to 150	°C
Electrostatic Discharge – Human Body Model	±2k	V
Electrostatic Discharge – Charged Device Model	±1.5k	V
Lead Temperature (soldering, 10 seconds)	260	°C

Notes:

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) Voltage values are with respect to SRC terminal.

(3) Voltage values are with respect to SYSM terminal.

(4) ESD testing is performed according to the respective JESD22 JEDEC standard.

Thermal Characteristics

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance Junction to Air [1]	50	°C/W
T_J	Operating Junction Temperature Range	-40 to 125	°C

Notes:

(1) Assumes 16 LD 3x3 QFN with hi-K JEDEC board and 13.5 inch^2 of 1 oz Cu and 4 thermal vias connected to PAD

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{SW}	AC Switch Voltage	18	24	36	V_{RMS}
F_{SYS}	System Supply Voltage Frequency	DC		60	Hz
C_{DATA}	Data Isolation Capacitor		100		pF
C_{ISO}	Clock Isolation Capacitor		220		pF
C_{PTO}	Power Transfer Capacitor		10		nF
C_{VDD}	VDD Bypass Capacitor		470		nF
C_{VGG}	VGG Bypass Capacitor		470		nF
C_{SUB}	Sub Capacitor		100		nF
C_{WD}	Watch Dog Capacitor		22		nF
C_{SYS}	VSYS Capacitor		10		nF
R_{WD}	Watch Dog Resistor		1		MΩ
$D_{SW1/2}$	SW 1/2 Schottky Diode (Forward Voltage)		0.3		V
CLK Drive					
V_{CLK}	Clock Drive Voltage	1.7		5.5	V
T_{CLK}	Clock Period	0.9	1	1.2	µs
T_{BIT}	Bit Period	7	8	10	µs
T_{RESET}	Reset Time	25			µs

Electrical Characteristics

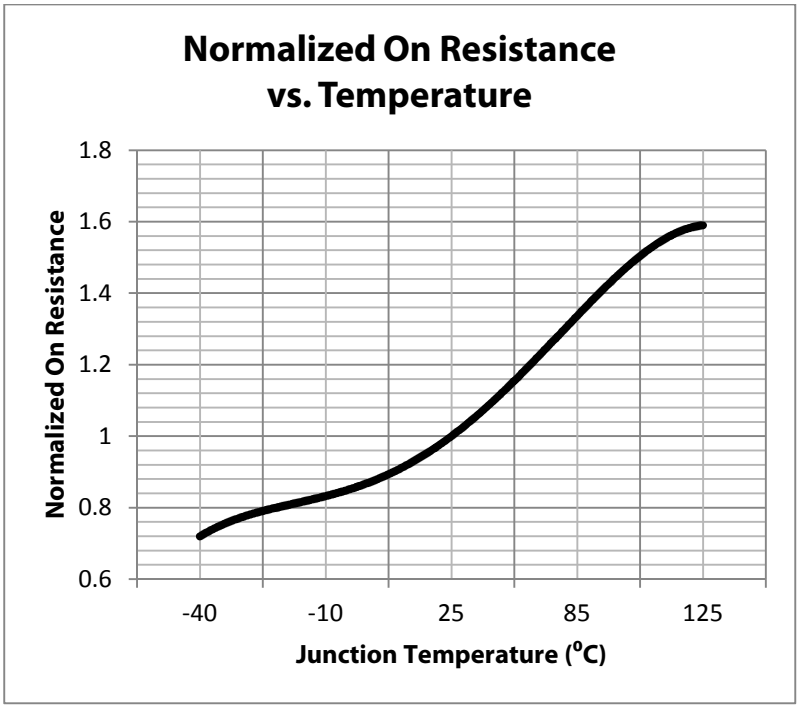
Electrical Characteristics, T_J = -40°C to 125°C (unless otherwise noted)

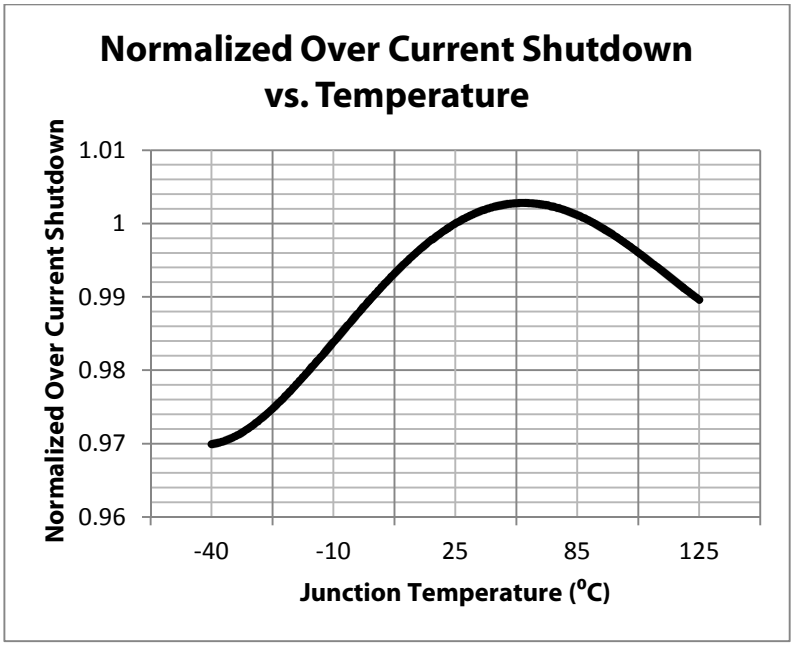
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply and Power Management						
$I_{CLK-STBY}$	Quiescent current Disable Mode or Latch Mode	V_{CLK} = 0V, C_{ISO}=220pF, F_{SYS} = 60Hz V_{SW} = 24V		3		µA
I_{SYSP}	System Supply Current	Latch Mode		8	15	µA
VDD	VDD Supply Voltage	With respect to VSYS	4	5.0	5.5	V
VGG	VGG Supply Voltage	With respect to SRC	4	5.0	5.5	V
T_{DOFF}	Dither Off Period			25		µs
T_{DRTY}	Dither Retry Interval			4		ms
V_{DON}	Dither Voltage ON Threshold			12		V
V_{DOFF}	Dither Voltage OFF Threshold			13		V
Communication Parameters						
T_{HB}	Heartbeat Pulse-width			20		µs
Output Switch						
R_{ON}	Switch On Resistance	T_J=25°C	230	290	350	mΩ
I_{OFF}	Off State Leakage	T_J<85°C			3	µA
$IOUT_{OC}$	Output Over Current Shutdown	T_J=25°C		2.5		A
OC_{FILT}	Output Over Current Deglitch			25		µs
$I_{TURN-OFF}$	Switch Current for Zero Cross Turn-Off		-150		150	mA
Watch Dog						
WD_{TO}	Turn-Off Threshold Voltage		500	700	900	mV
WD_{RC}	WD Recharge Voltage		VDD-1.1	VDD-0.8	VDD-0.5	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Power Transfer						
F_{PTO}	Power Transfer Output Frequency	V_{SYSP}-V_{SYSM} = 24V	40	70	110	kHz
R_{HS_PTO}	Power Transfer High Side Driver Resistance	V_{SYSP}-V_{SYSM} = 24V(1)		50		Ω
R_{LS_PTO}	Power Transfer Low Side Driver Resistance	V_{SYSP}-V_{SYSM} = 24V		50		Ω

Notes:
(1) This parameter is not tested in production.

Product Characteristics





Detailed Description

Communication Protocol

The TS13103 device supports a proprietary single-wire interface that is compact and allows support of systems where galvanic isolation is required with a minimum number of external components.

Bit Signaling

The MCU can generate three signals on the CLK pin: Reset, Zero, and One. The Zero and One signals are digital bits and form a command word. Each command word is preceded by a Reset signal.

Reset Signal (R)
The Reset signal is a zero logic level that is kept low for longer than T_{RESET}.

Zero Signal (0)
The Zero signal is two pulses of period T_{CLK} during a bit period T_{BIT}.

One Signal (1)
The One signal is four pulses of period T_{CLK} during a bit period T_{BIT}.

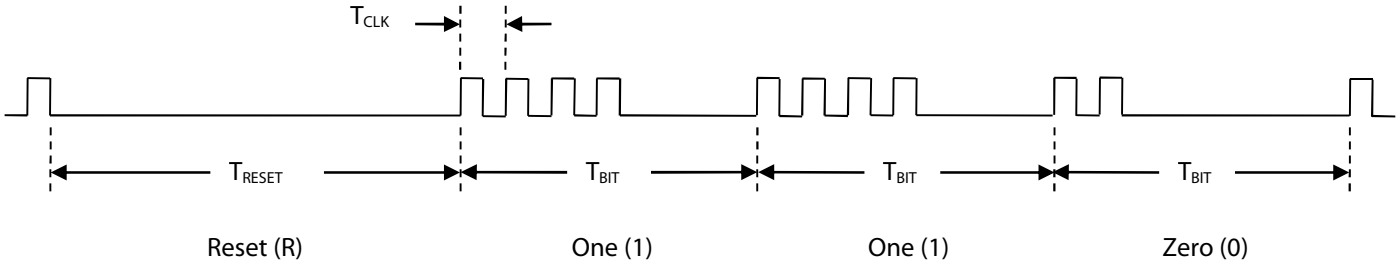


Figure 2: Communication Protocol

		Preamble					Address			Command								
CLK:	ANY	R	1	1	0	A2	A1	A0	C3	C2	C1	C0	1	1	1	1	1	ANY
Switch State:	Old State																	New State
DATA:	High Impedance												0	S2	S1	S0	0	High Impedance
														Status				

Table 1: Communication Sequence

Device Addressing

Figure 2 shows the beginning of a command sequence. This pattern appears at the CLK input and forms the Preamble, as shown in Table 1, a sequence of a low period for duration of T_{RESET} or greater, followed by a bit sequence of (1 1 0). The following three bits designate the address of the device being selected. These three bits (A2 A1 A0) correspond to the device with AD1 and AD0 pins connected as in the Address Configuration Table shown in Figure 5. In the TS13103 device, A2 must be equal to A1 resulting in the shaded area in the table. See the Multi-channel Application section for more information.

Switch Commands

The (C3 C2 C1 C0) field sent using the CLK pin determines the command sent to the switch. The following commands are defined:

C3	C2	C1	C0	Command
0	0	0	0	Not allowed (No Operation)
0	0	0	1	OFF, Immediate
0	0	1	0	OFF, Zero Crossing
0	0	1	1	ON, Immediate
0	1	0	0	ON, Zero Crossing
0	1	0	1	ON, Immediate, with Dithering
0	1	1	0	ON, Zero Crossing, with Dithering
0	1	1	1	Heartbeat
1	0	0	0	Not allowed (No Operation)
1	0	0	1	Send Power (PTO), 8 pulses
1	0	1	0	Send Power (PTO), 16 pulses
1	0	1	1	Send Power (PTO), 32 pulses
1	1	0	0	Send Power (PTO), 64 pulses
1	1	0	1	Not allowed (No Operation)
1	1	1	0	Not allowed (No Operation)
1	1	1	1	Poll State (No Operation)

Table 2: Valid Commands

Each switch monitors the CLK line regardless of the address; however only the device with the (AD1 AD0) pins configured to match the (A2 A1 A0) field sent via the CLK pin will respond to the Command bits (C3 C2 C1 C0). If two or more devices on the CLK bus have address pins wired alike, those devices will all respond to the same command. However, doing this may lead to DATA bus conflicts when the device Status Values are reported.

The command is executed after the status values are shifted out to avoid interference on the status values caused by transients in the system.

ON Commands

Four modes of closing the switch are available:

1. ON, Immediate: When this command sequence is sent, the switch will be closed after the status values are shifted out. The system must comprehend the time it takes to complete the sequence in order to place the switch in the closed state at the desired time.
2. ON, Zero Crossing: When this command sequence is sent, the switch will close on the first occurrence of a polarity change in the voltage across the switch (V_{SW1}-V_{SW2} changes sign to indicate a voltage zero-crossing) after the switch receives the command and the status values are shifted out. This should not be used for DC applications.
3. ON, Immediate with Dithering: This command closes the switch as in ON, Immediate, above, but puts the device into Dither mode as well. Dithering opens the switch after an interval of T_{DRTY} for a period of time, T_{DOFF} when the system voltage drops below V_{DON}. This allows the C_{SYS} capacitor to be re-charged. See the Dither Functionality section for more details.
4. ON, Zero Crossing with Dithering: This command closes the switch as in ON, Zero Crossing, but enables the Dither mode as described above.

OFF Commands

Two modes of opening the switch are available:

1. OFF, Immediate: When the OFF, Immediate sequence is sent, the switch will transition to the open state after the status values are shifted out.
2. OFF, Zero Crossing: When the OFF, Zero-Crossing sequence is received, the switch will open on the first occurrence of the load-current dropping within I_{TURN_OFF} after the status values are shifted out.

Poll Command

A Poll State command may be sent to the device when no change of operation is desired, but the state of the Status Values is needed by the microcontroller. In non-latched operation, this command will also serve to recharge the Watchdog Timer. See the Latching Configuration section for details.

Status Values

The (S2 S1 S0) field received using the DATA pin provides the status of the switch before the command has been executed. Each of the S2, S1 or the S0 bits is generated by the switch in the following way:

- For zero: the DATA pin is pulsed for first 2 clock pulses matching the protocol (the pulses corresponding to the Zero signal).
- For one: the DATA pin duplicates the signal available at the CLK pin (the pulses corresponding to the One signal).

The following status values are defined:

S2	S1	S0	Status
0	0	0	Reserved
0	0	1	OFF
0	1	0	Reserved
0	1	1	Reserved
1	0	0	ON, Dithering disabled
1	0	1	ON, Dithering enabled
1	1	0	Reserved
1	1	1	Over Current

Table 3: Valid Status Values

DATA Bus Contention

Note that if more than one device is wired to the same address, the devices will all report their status values at the same time. Since the status of each device may be different (for example, an over-current event was recorded on one device and it has disabled itself), the status values (S2 S1 S0) can possibly be different, leading to the DATA pins of two (or more) devices to transmit different data. This will lead to high supply current draw which may damage the device, reset the system (due to voltage drop), or other undesirable events. If sharing addresses is desired, the DATA pins of those devices must have a separate C_{DATA} capacitor wired to a dedicated GPIO on the microcontroller.

Latching Configuration

The Switch can be configured for latching or non-latching functionality via external interconnect. When the WD pin is tied to VDD, the Switch state is latched after each command (CMD) sequence. When the WD pin is tied to an RC circuit, the device is configured for non-latching behavior. If a CMD sequence is not received before the WD pin voltage decays to WD_{TO}, the Switch will be turned off. A CMD sequence received by the device before the WD pin voltage decays to WD_{TO} will cause the WD pin to recharge to WD_{RC}, and the switch will remain closed. In order to recharge, the CMD address must be for the corresponding device address configuration. Typical waveforms for non-latching behavior are shown below.

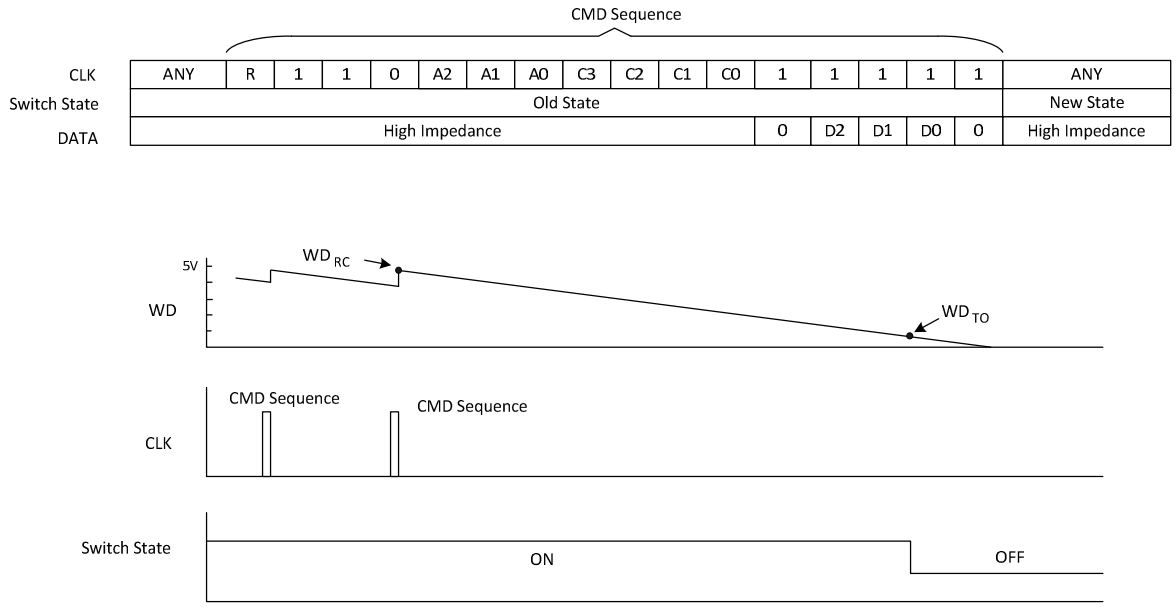


Figure 3: Latching Functionality

The time between the last CMD sequence and the switch opening (in a non-latching configuration) can be computed by the following equation:

$$t_{OFF} = -R_{WD} C_{WD} \ln\left(\frac{WD_{TO}}{WD_{RC}}\right)$$

Where:
t_{OFF} is the time from the last CMD sequence until the switch opens
R_{WD} is the WD pin resistor
C_{WD} is the WD pin capacitor
WD_{TO} is the WD pin turn-off voltage threshold
WD_{RC} is the WD pin re-charge voltage

It should be noted that the WD capacitor, C_{WD}, is recommended to be 22nF. The reason for this is that charge proportional to C_{WD} is drawn from the C_{SYS} capacitor in every re-charge cycle, thereby elevating the average current, and forcing the device to switch off more frequently in order to re-charge C_{SYS} (see Dither Functionality, below). C_{WD} can be made smaller, but this will necessitate a larger value of R_{WD} to be used to define a given t_{OFF} time. R_{WD} has its practical limits due to leakage within the components attached to the WD pin and possible leakage on the circuit board due to contamination. The system designer should consider all these issues when selecting R_{WD} and C_{WD}. Device 2 in Figure 5 shows R_{WD} and C_{WD} being used to create a non-latching channel. Device 1 is shown in latching mode.

Dither Functionality

Dithering is provided as a mode of operation for applications where a single device per system is used. It enables powering the TS13103 from the AC waveform. The device monitors the system voltage, (V_{SYSP}-V_{SYSM}), and if it falls below V_{DON}, the Switch is shut off for approximately T_{DOFF}. This causes energy stored in the load to be transferred into the C_{SYS} capacitor. When the device is in dither mode, this event occurs at T_{DRTY} intervals until the system voltage reaches V_{DOFF}.

Heartbeat Functionality

When the Switch is off and the Heartbeat Command Sequence has been transmitted, the DATA pin provides a pulse synchronous with the zero crossings of the AC waveform. A single pulse or "Heartbeat" for each crossing will be present with a pulse-width of T_{HB} as shown in the figure below. This is useful for monitoring load presence and for evaluating the phase of the AC waveform.

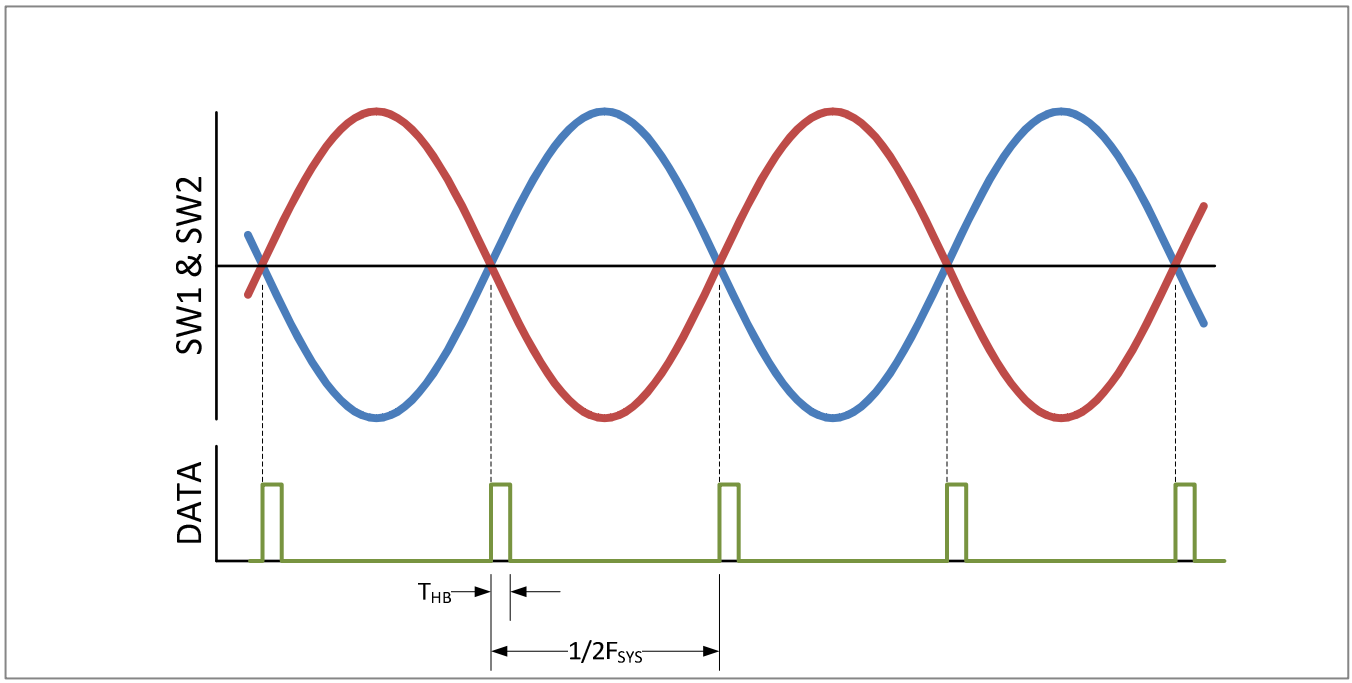


Figure 4: Heartbeat Functionality

Multi-channel Application

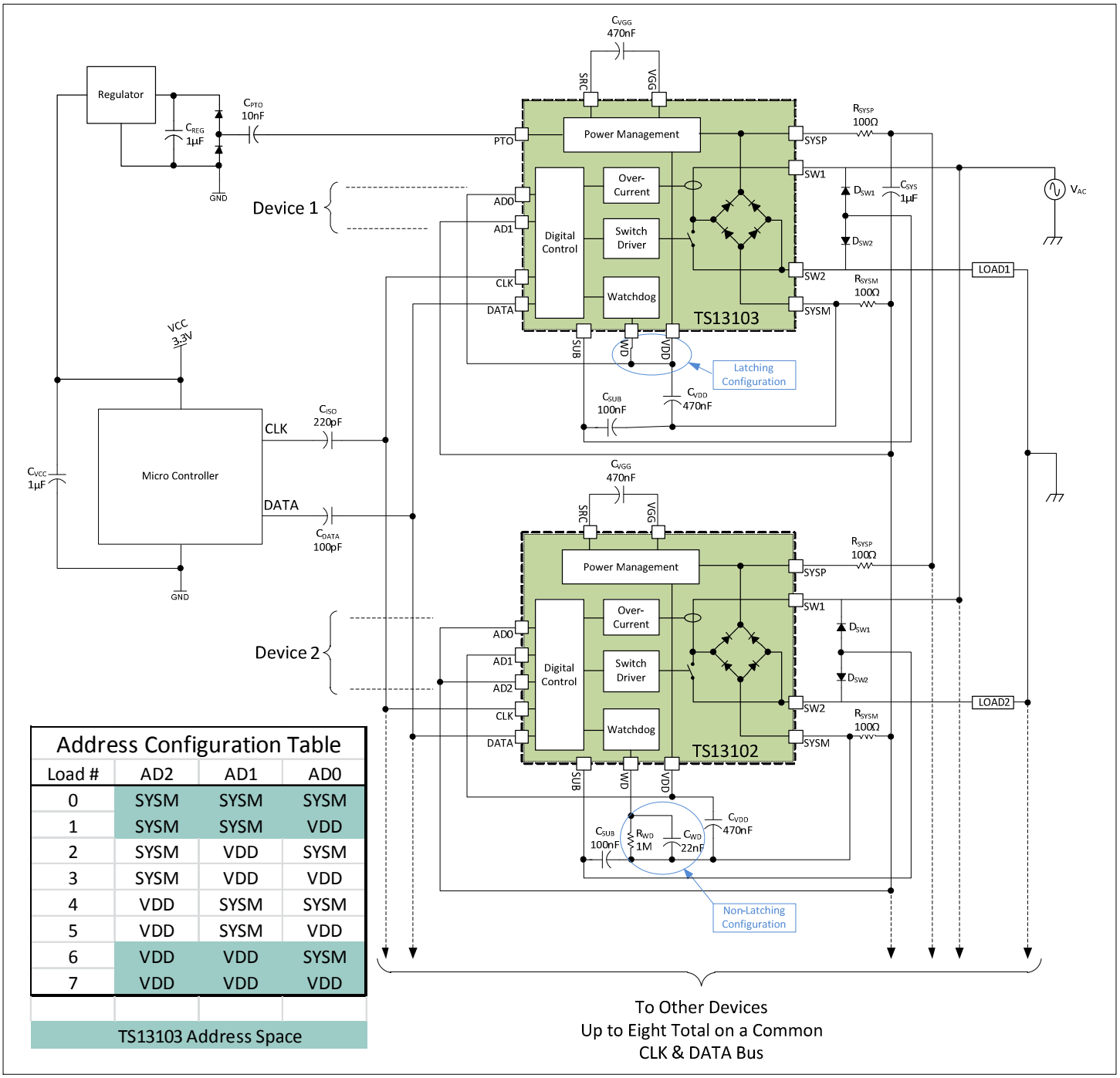
In a multi-channel application, dithering is unnecessary as long as one device is switched off. As long as the device address pins are wired uniquely for each channel, a single pair of GPIO pins on the microcontroller can control each device by matching the address in the CMD sequence with the hardwired address. If all devices must be on simultaneously, one device can be configured for dithering mode to maintain system supply.

The SYSP net should be tied to the SYSM net through the C_{SYS} capacitor as shown in the Figure 5 below. For a single transformer system, only one is necessary. If additional transformers are used in a given system, then the SYSP and SYSM pins for those TS13103 devices will need an additional C_{SYS} capacitor for each additional transformer.

Current limit resistors are needed for each SYSP pin and each SYSM pin as shown below (R_{SYSP} and R_{SYSM} respectively). These are typically 100 Ω, ¼ W.

A pair of GPIO pins can manage the command and control for up to 4 loads as long as each TS13103 has a unique address. The TS13103 address space is shown in the Address Configuration Table shown in Figure 5. The AD2 and AD1 are internally connected within the device (they share the AD1 pin), resulting in the shaded region in the table. Pins AD1 and AD0 are set using hard wired connections on the board to define the device's address. The TS13103 device is fully-compatible with the TS13102, which supports a wider address range of up to eight loads. As an example, Figure 5 shows a system with a mixture of TS13102 and TS13103 devices. The TS13103 is shown to be wired to respond to a command addressing Load 1 and a TS13102 is configured as Load 2.

Also note that some devices can be wired in non-latching mode and others in latching mode.



Address Configuration Table			
Load #	AD2	AD1	AD0
0	SYSM	SYSM	SYSM
1	SYSM	SYSM	VDD
2	SYSM	VDD	SYSM
3	SYSM	VDD	VDD
4	VDD	SYSM	SYSM
5	VDD	SYSM	VDD
6	VDD	VDD	SYSM
7	VDD	VDD	VDD
TS13103 Address Space			

Figure 5: System Configuration with Multiple Switches

Package Information

Product Marking

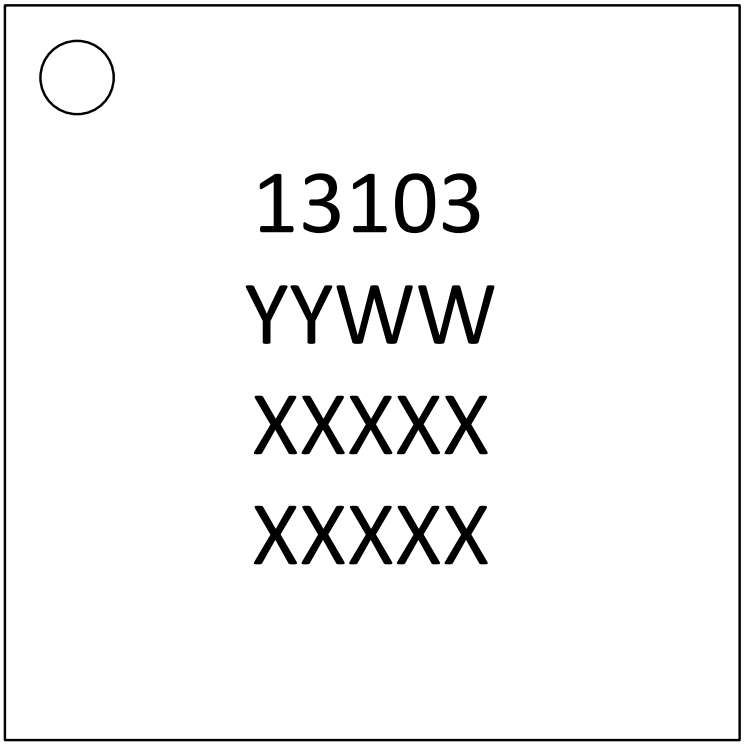
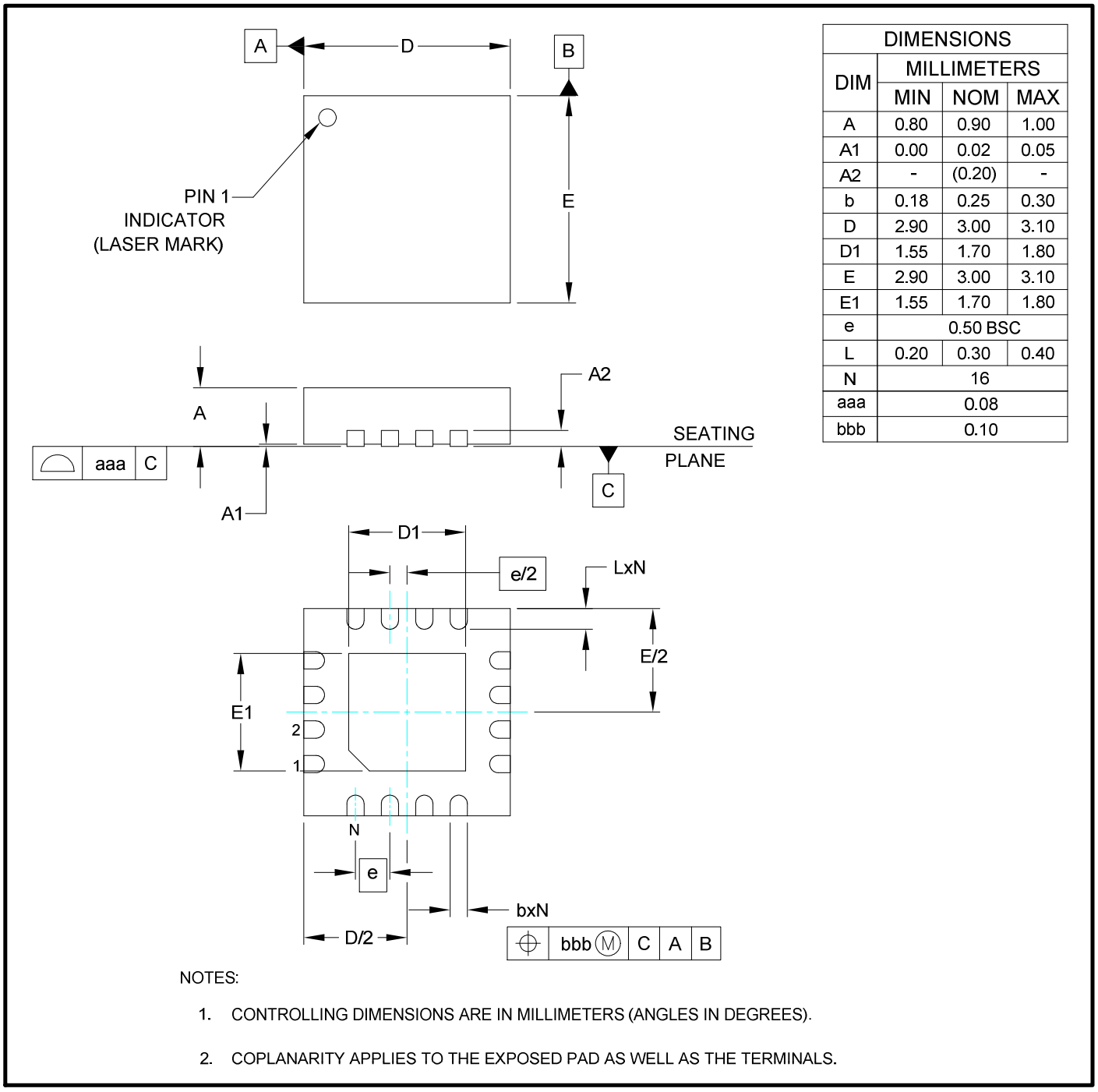


Figure 6: Device Symbolization

Notes:
YYWW = Year Calendar Week
XXXXX = Semtech Lot Number
XXXXX = Lot Number (Continued)

Package Outline Drawing



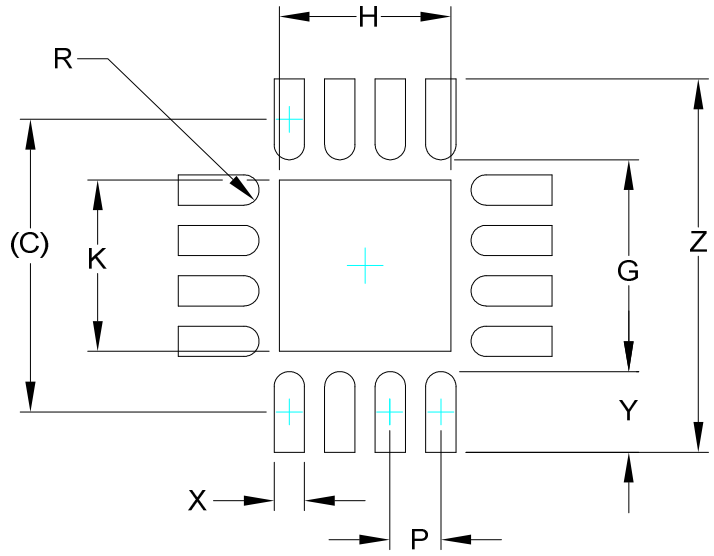
DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2	-	(0.20)	-
b	0.18	0.25	0.30
D	2.90	3.00	3.10
D1	1.55	1.70	1.80
E	2.90	3.00	3.10
E1	1.55	1.70	1.80
e	0.50 BSC		
L	0.20	0.30	0.40
N	16		
aaa	0.08		
bbb	0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Figure 7: Package Outline Drawing

Board Land Pattern



DIMENSIONS	
DIM	MILLIMETERS
C	(2.90)
G	2.10
H	1.70
K	1.70
P	0.50
R	0.15
X	0.30
Y	0.80
Z	3.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Figure 8: Recommended Board Layout Land Pattern

Ordering Information

Device Part Number	Description	Package
TS13103-QFNR	60V Power Load Switch	MLPQ-16 3.0 x 3.0 Tape & Reel (3,300 parts/reel)
TS13103EVB	Evaluation Board	

IMPORTANT NOTICE

Information relating to this product and the application or design described herein is believed to be reliable, however such information is provided as a guide only and Semtech assumes no liability for any errors in this document, or for the application or design described herein. Semtech reserves the right to make changes to the product or this document at any time without notice. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. Semtech warrants performance of its products to the specifications applicable at the time of sale, and all sales are made in accordance with Semtech's standard terms and conditions of sale.

SEMTECH PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS, OR IN NUCLEAR APPLICATIONS IN WHICH THE FAILURE COULD BE REASONABLY EXPECTED TO RESULT IN PERSONAL INJURY, LOSS OF LIFE OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. INCLUSION OF SEMTECH PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE UNDERTAKEN SOLELY AT THE CUSTOMER'S OWN RISK. Should a customer purchase or use Semtech products for any such unauthorized application, the customer shall indemnify and hold Semtech and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs damages and attorney fees which could arise.

Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com

LifeElectronics
Живое партнерство

ООО «ЛайфЭлектроникс» **“LifeElectronics” LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru