CAT24C164

16 kb CMOS Serial EEPROM, Cascadable

Description

The CAT24C164 is a 16 kb CMOS cascadable Serial EEPROM device organized internally as 128 pages of 16 bytes each, for a total of 2048 x 8 bits. The device supports both the Standard (100 kHz) as well as Fast (400 kHz) I^2C protocol.

Data is written by providing a starting address, then loading 1 to 16 contiguous bytes into a Page Write Buffer, and then writing all data to non−volatile memory in one internal write cycle. Data is read by providing a starting address and then shifting out data serially while automatically incrementing the internal address count.

External address pins make it possible to address up to eight CAT24C164 devices on the same bus.

Features

- Supports Standard and Fast I^2C Protocol
- 1.8 V to 5.5 V Supply Voltage Range
- 16−Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Schmitt Triggers and Noise Suppression Filters on I^2C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial Temperature Range
- PDIP, SOIC, TSSOP and TDFN 8−lead Packages
- This Device is Pb−Free, Halogen Free/BFR Free, and RoHS Compliant

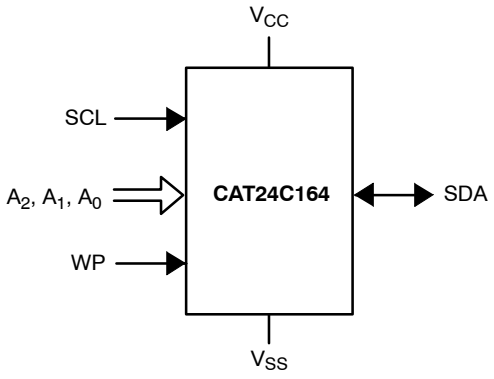


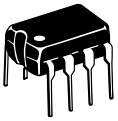
Figure 1. Functional Symbol

ON Semiconductor®

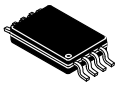
http://onsemi.com

SOIC−8
W SUFFIX
CASE 751BD

TDFN−8
VP2 SUFFIX
CASE 511AK

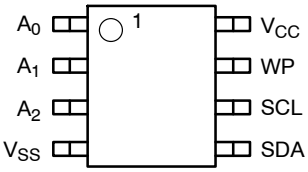


PDIP−8
L SUFFIX
CASE 646AA



TSSOP−8
Y SUFFIX
CASE 948AL

PIN CONFIGURATION



PDIP (L), SOIC (W),
TSSOP (Y), TDFN (VP2)
(Top View)

For the location of Pin 1, please consult the corresponding package drawing.

PIN FUNCTION

Pin Name	Function
A_0, A_1, A_2	Device Address Inputs
SDA	Serial Data Input/Output
SCL	Serial Clock Input
WP	Write Protect Input
V_{CC}	Power Supply
V_{SS}	Ground

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

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Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Storage Temperature	–65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	–0.5 to +6.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The DC input voltage on any pin should not be lower than –0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than –1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END} (Note 3)	Endurance	1,000,000	Program/Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC–Q100 and JEDEC test methods.
3. Page Mode, V_{CC} = 5 V, 25°C.

Table 3. D.C. OPERATING CHARACTERISTICS (V_{CC} = 1.8 V to 5.5 V, T_A = –40°C to +85°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CCR}	Read Current	Read, f_{SCL} = 400 kHz		1	mA
I_{CCW}	Write Current	Write, f_{SCL} = 400 kHz		1	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}		1	μA
I_L	I/O Pin Leakage	Pin at GND or V_{CC}		1	μA
V_{IL}	Input Low Voltage		–0.5	V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	$V_{CC} \geq$ 2.5 V, I_{OL} = 3.0 mA		0.4	V
V_{OL2}	Output Low Voltage	V_{CC} < 2.5 V, I_{OL} = 1.0 mA		0.2	V

Table 4. PIN IMPEDANCE CHARACTERISTICS (V_{CC} = 1.8 V to 5.5 V, T_A = –40°C to +85°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Max	Units
C_{IN} (Note 4)	SDA I/O Pin Capacitance	V_{IN} = 0 V	8	pF
C_{IN} (Note 4)	Input Capacitance (other pins)	V_{IN} = 0 V	6	pF
I_{WP} (Note 5)	WP Input Current	$V_{IN} < V_{IH}$, V_{CC} = 5.5 V	200	μA
		$V_{IN} < V_{IH}$, V_{CC} = 3.3 V	150	
		$V_{IN} < V_{IH}$, V_{CC} = 1.8 V	100	
		$V_{IN} > V_{IH}$	1	

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC–Q100 and JEDEC test methods.
5. When not driven, the WP pin is pulled down to GND internally. For improved noise immunity, the internal pull–down is relatively strong; therefore the external driver must be able to supply the pull–down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull–down reverts to a weak current source.

Table 5. A.C. CHARACTERISTICS (V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +85°C.) (Note 6)

Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1000		300	ns
t_F (Note 7)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		μs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9	μs
t_{DH}	Data Out Hold Time	100		100		ns
T_i (Note 7)	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns
$t_{SU:WP}$	WP Setup Time	0		0		μs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		μs
t_{WR}	Write Cycle Time		5		5	ms
t_{PU} (Notes 7, 8)	Power-up to Ready Mode		1		1	ms

6. Test conditions according to “A.C. Test Conditions” table.
7. Tested initially and after a design or process change that affects this parameter.
8. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

Table 6. A.C. TEST CONDITIONS

Input Levels	0.2 x V_{CC} to 0.8 x V_{CC}
Input Rise and Fall Times	≤ 50 ns
Input Reference Levels	0.3 x V_{CC}, 0.7 x V_{CC}
Output Reference Levels	0.5 x V_{CC}
Output Load	Current Source: I_{OL} = 3 mA (V_{CC} ≥ 2.5 V); I_{OL} = 1 mA (V_{CC} < 2.5 V); C_L = 100 pF

Power-On Reset (POR)

CAT24C164 incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state.

A CAT24C164 device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi−directional POR feature protects the device against 'brown−out' failure following a temporary loss of power.

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A_0, A_1 and A_2: The Address inputs set the device address when cascading multiple devices. When not driven, these pins are pulled LOW internally.

The CAT24C164 can be made compatible with the CAT24C16 by tying A_2, A_1 and A_0 to V_{SS} or by leaving A_2, A_1 and A_0 float.

WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. When not driven, this pin is pulled LOW internally.

Functional Description

The CAT24C164 supports the Inter−Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT24C164 acts as a Slave device. Master and Slave alternate as either transmitter or receiver.

I^2C Bus Protocol

The I^2C bus consists of two 'wires', SCL and SDA. The two wires are connected to the V_{CC} supply via pull−up resistors. Master and Slave devices connect to the 2−wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 2). The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake−up' call to all receivers. Absent a START, a Slave will not respond to commands. The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH.

Device Addressing

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular Slave device it is requesting. The most significant bit of the 8−bit slave address is fixed as 1. (see Figure 3). The next three significant bits (A_2, A_1, A_0) are the device address bits and define which device or which part of the device the Master is accessing (The A_1 bit must be the compliment of the A_1 input pin signal). Up to eight CAT24C164 devices may be individually addressed by the system. The next three bits are used as the three most significant bits of the data word address. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9^{th} clock cycle (Figure 4). The Slave will also acknowledge the address byte and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9^{th} clock cycle. As long as the Master acknowledges the data, the Slave will continue transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by issuing a STOP condition. Bus timing is illustrated in Figure 5.

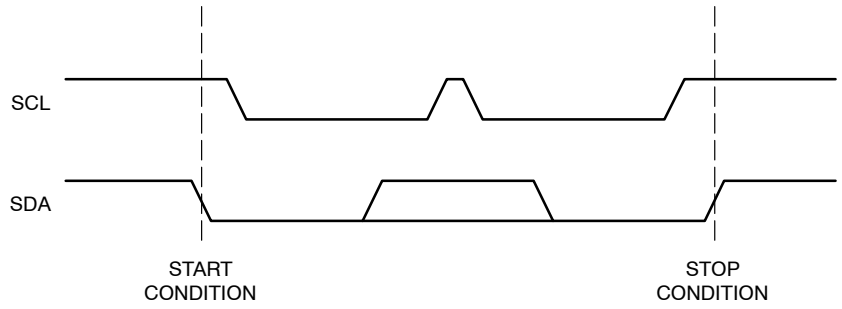


Figure 2. START/STOP Conditions

1	A2	$\overline{A1}$	A0	a_{10}	a_9	a_8	R/$\overline{W}$	CAT24C164

Figure 3. Slave Address Bits

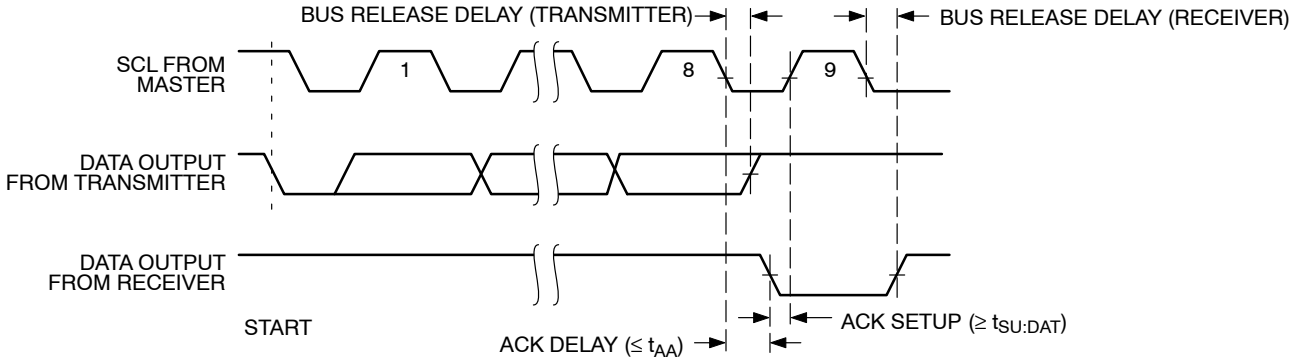


Figure 4. Acknowledge Timing

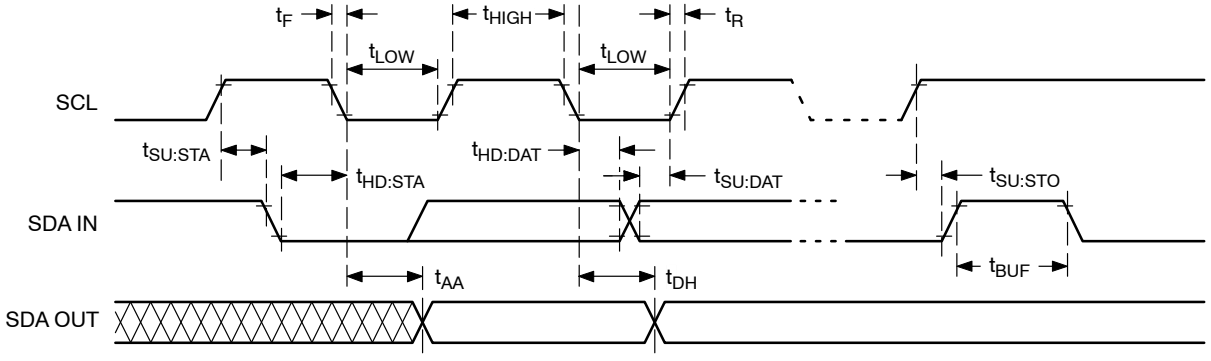


Figure 5. Bus Timing

WRITE OPERATIONS

Byte Write

In Byte Write mode, the Master sends the START condition and the Slave address with the R/$\overline{W}$ bit set to zero to the Slave. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24C164. After receiving another acknowledge from the Slave, the Master transmits the data byte to be written into the addressed memory location. The CAT24C164 device will acknowledge the data byte and the Master generates the STOP condition, at which time the device begins its internal Write cycle to nonvolatile memory (Figure 6). While this internal cycle is in progress (t_{WR}), the SDA output will be tri−stated and the CAT24C164 will not respond to any request from the Master device (Figure 7).

Page Write

The CAT24C164 writes up to 16 bytes of data in a single write cycle, using the Page Write operation (Figure 8). The Page Write operation is initiated in the same manner as the Byte Write operation, however instead of terminating after the data byte is transmitted, the Master is allowed to send up to fifteen additional bytes. After each byte has been transmitted the CAT24C164 will respond with an acknowledge and internally increments the four low order address bits. The high order bits that define the page address remain unchanged. If the Master transmits more than sixteen bytes prior to sending the STOP condition, the address counter ‘wraps around’ to the beginning of page and previously transmitted data will be overwritten. Once all sixteen bytes are received and the STOP condition has been sent by the Master, the internal Write cycle begins. At this point all received data is written to the CAT24C164 in a single write cycle.

Acknowledge Polling

The acknowledge (ACK) polling routine can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host’s write operation, the CAT24C164 initiates the internal write cycle. The ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24C164 is still busy with the write operation, NoACK will be returned. If the CAT24C164 has completed the internal write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAT24C164. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the CAT24C164 will not acknowledge the data byte and the Write request will be rejected.

Delivery State

The CAT24C164 is shipped erased, i.e., all bytes are FFh.

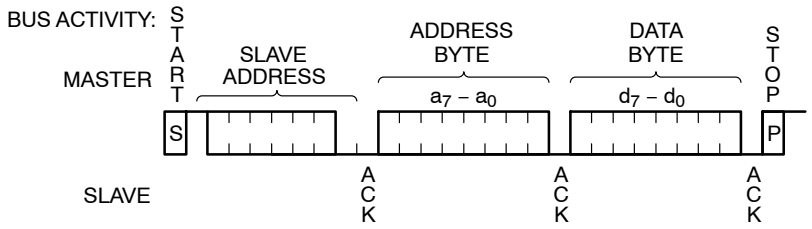


Figure 6. Byte Write Sequence

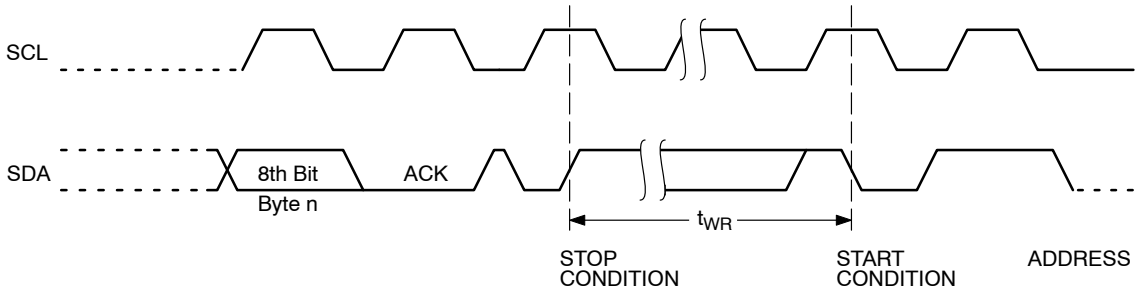


Figure 7. Write Cycle Timing

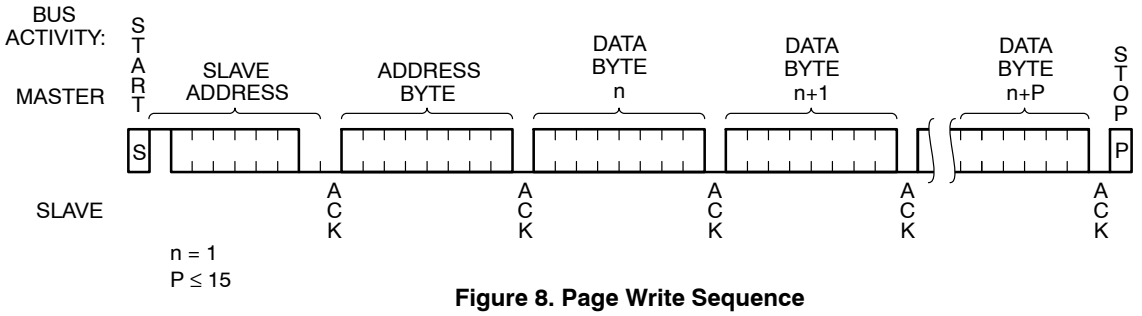


Figure 8. Page Write Sequence

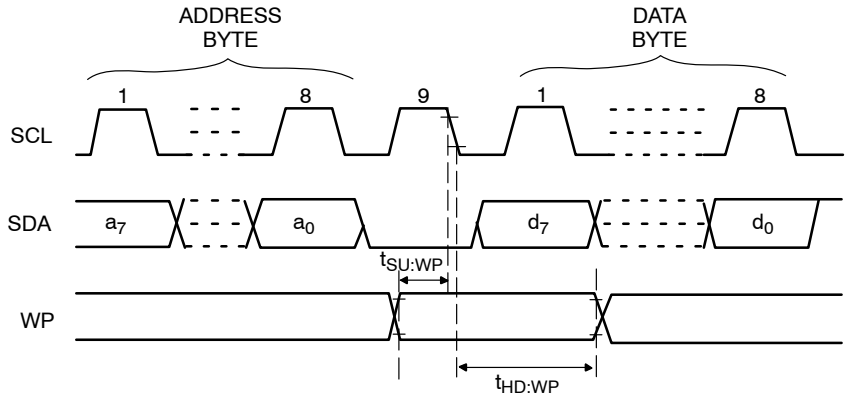


Figure 9. WP Timing

READ OPERATIONS

Immediate Read

Upon receiving a Slave address with the R/$\overline{W}$ bit set to '1', the CAT24C164 will interpret this as a request for data residing at the current byte address in memory. The CAT24C164 will acknowledge the Slave address, will immediately shift out the data residing at the current address, and will then wait for the Master to respond. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 10), the CAT24C164 returns to Standby mode.

Selective Read

Selective Read operations allow the Master device to select at random any memory location for a read operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24C164 acknowledges the byte address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24C164 then responds with its acknowledge and sends the requested data byte. The Master device does not acknowledge the data (NoACK) but will generate a STOP condition (Figure 11).

Sequential Read

If during a Read session, the Master acknowledges the 1st data byte, then the CAT24C164 will continue transmitting data residing at subsequent locations until the Master responds with a NoACK, followed by a STOP (Figure 12). In contrast to Page Write, during Sequential Read the address count will automatically increment to and then wrap−around at end of memory (rather than end of page).

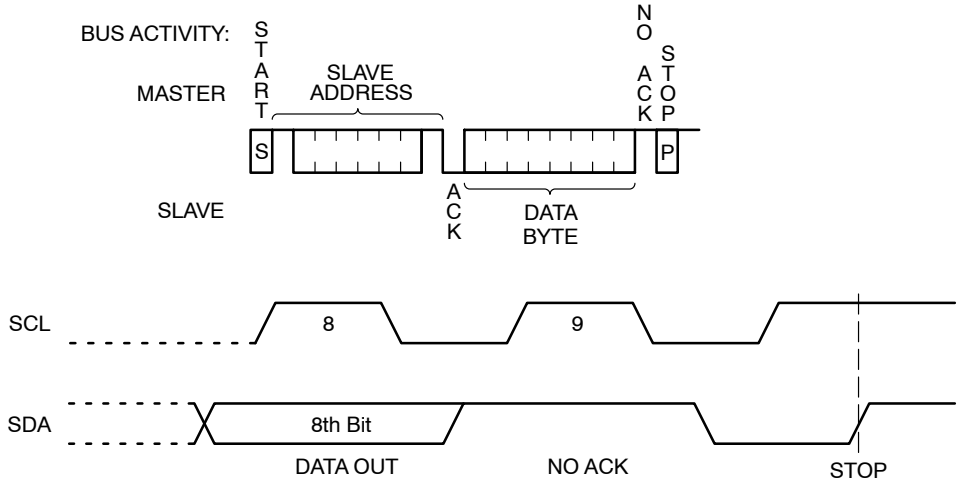


Figure 10. Immediate Read Sequence and Timing

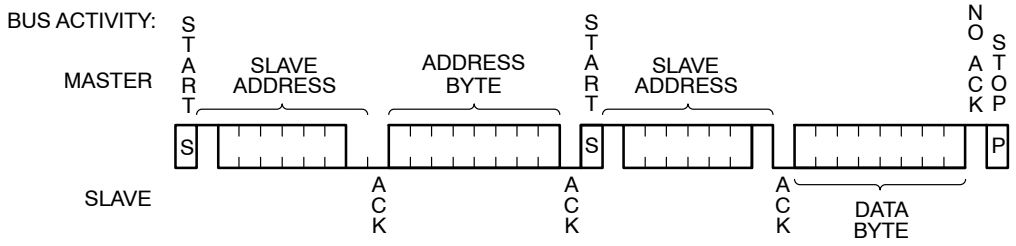


Figure 11. Selective Read Sequence

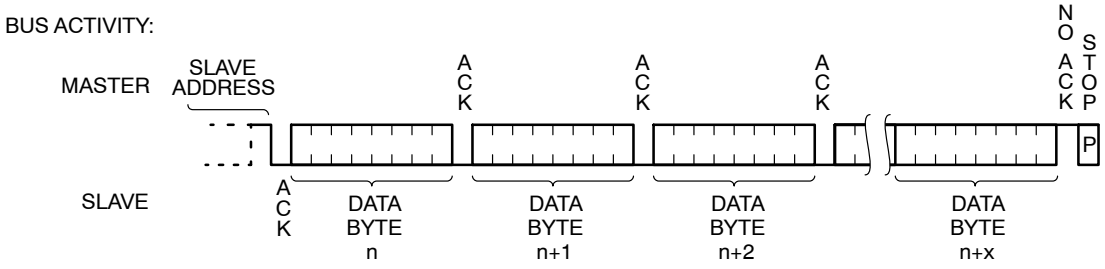
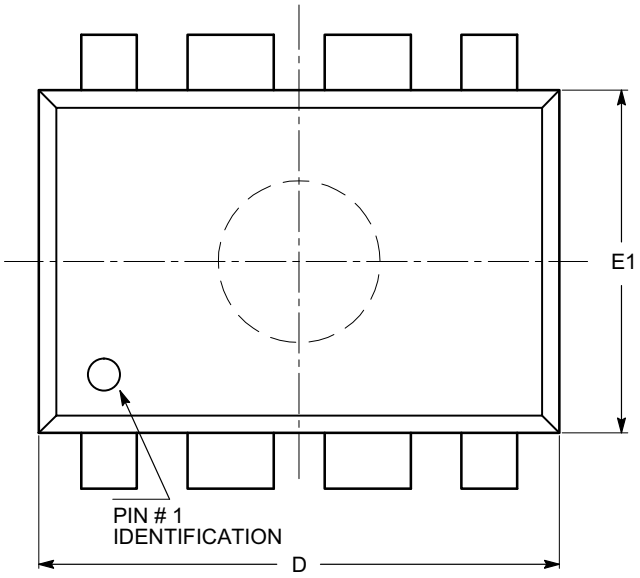


Figure 12. Sequential Read Sequence

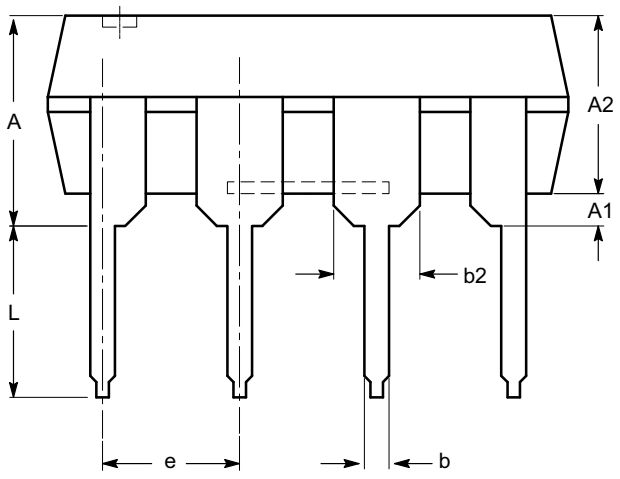
PACKAGE DIMENSIONS

PDIP−8, 300 mils
CASE 646AA−01
ISSUE A

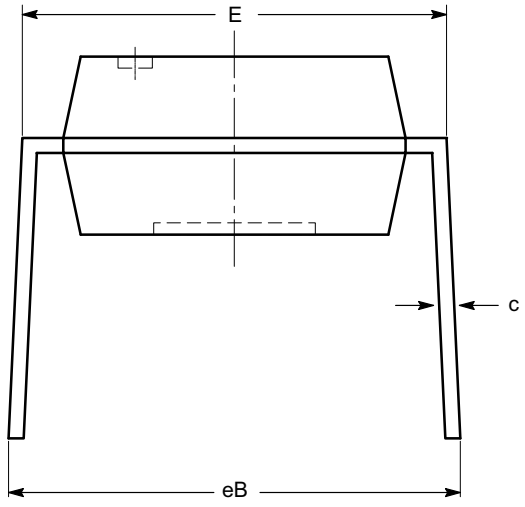


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e		2.54 BSC	
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW

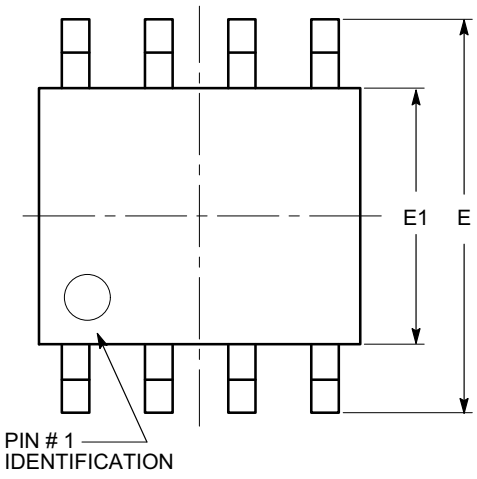


END VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

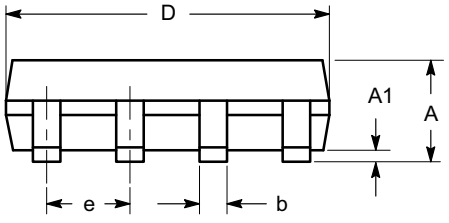
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

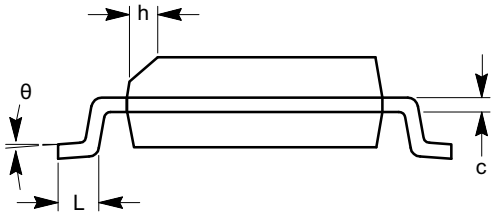


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW

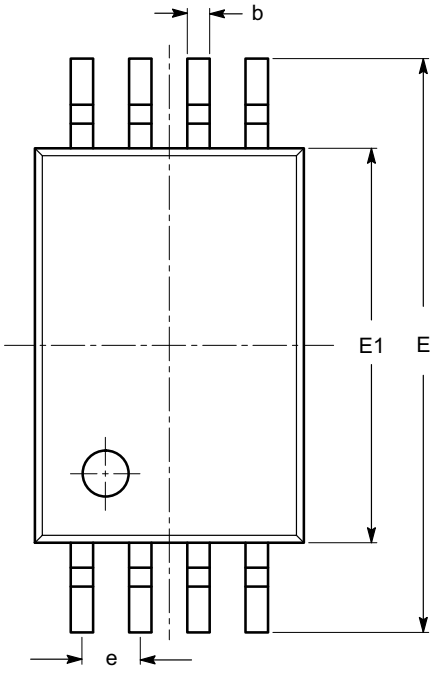


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

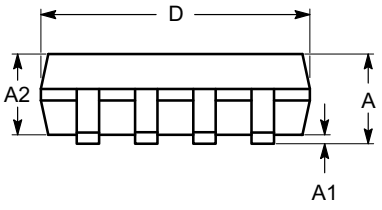
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

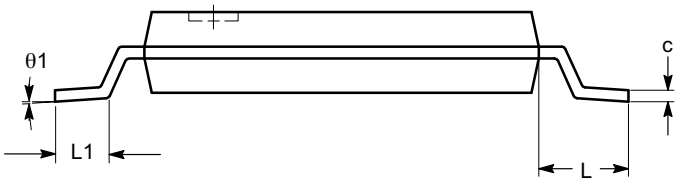


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°



SIDE VIEW

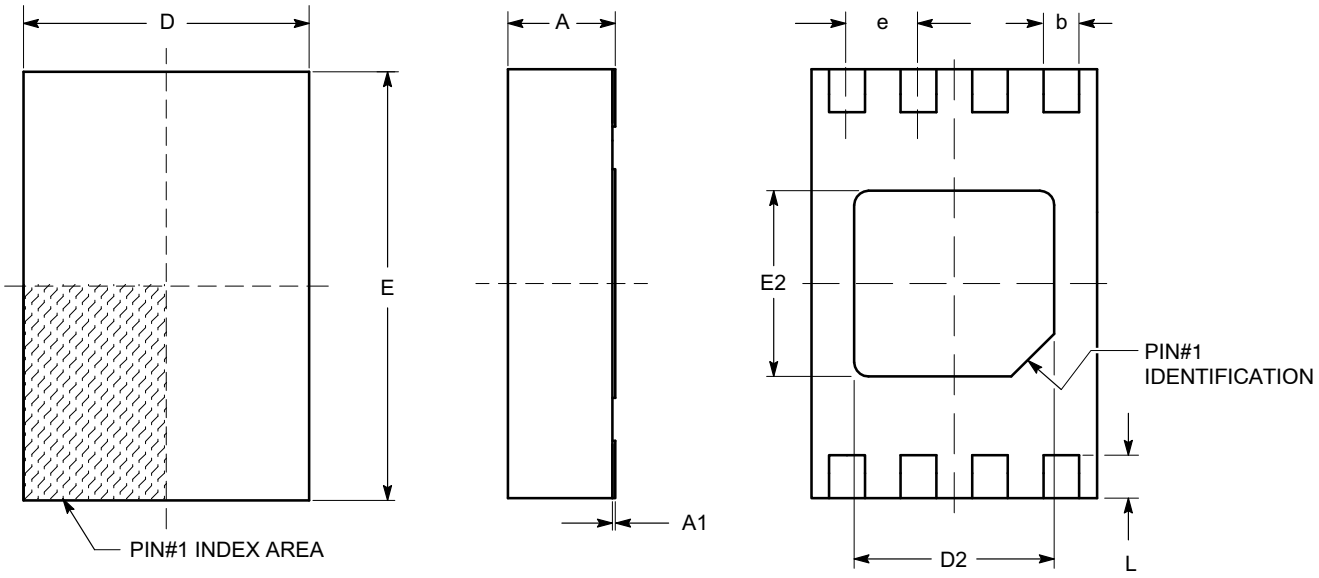


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

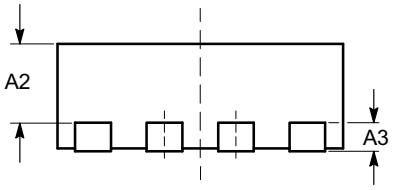
PACKAGE DIMENSIONS

TDFN8, 2x3
CASE 511AK−01
ISSUE A



TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.45	0.55	0.65
A3		0.20 REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.20	1.30	1.40
e		0.50 TYP	
L	0.20	0.30	0.40

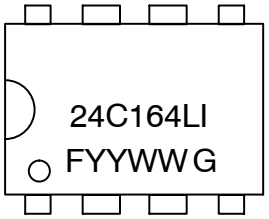


FRONT VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-229.

Package Marking

8−Lead PDIP

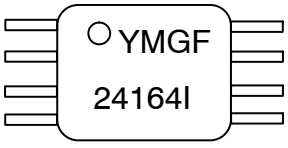


I = Temperature Range
YY = Production Year
WW = Production Week
G = Product Revision
F = Lead Finish
4 = NiPdAu

8−Lead SOIC

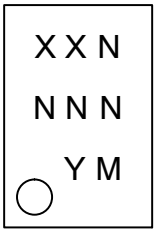
I = Temperature Range
YY = Production Year
WW = Production Week
G = Product Revision
F = Lead Finish
4 = NiPdAu

8−Lead TSSOP



Y = Production Year
M = Production Month
G = Die Revision
I = Temperature Range
F = Lead Finish
4 = NiPdAu

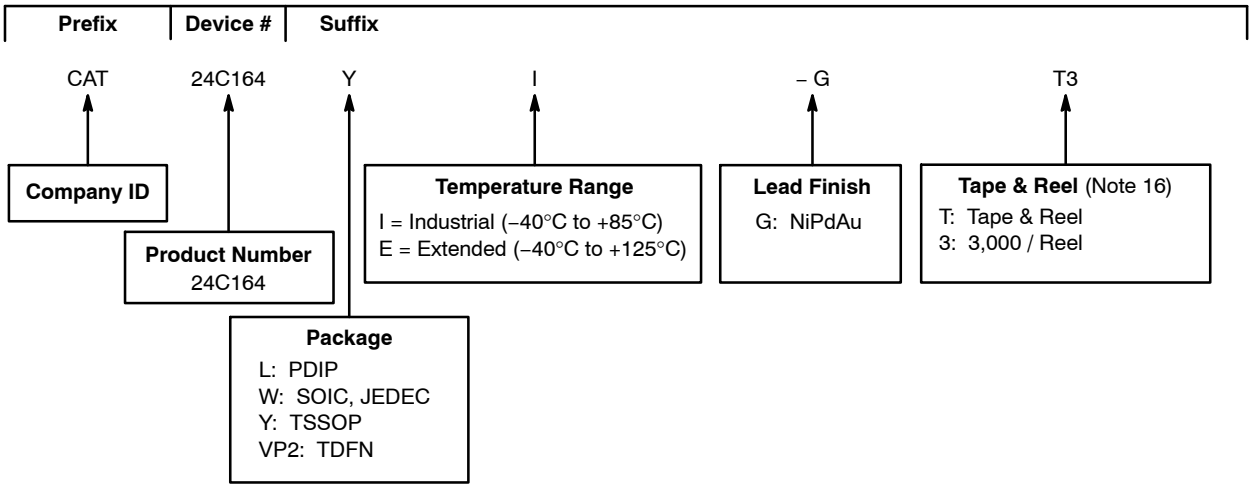
8−Pad TDFN



XX = Device Code
FR = NiPdAu
N = Traceable Code
Y = Production Year
M = Production Month

9. The circle on the package marking indicates the location of Pin 1.
10. For TDFN package, the Product Revision marking is included in the Device Code (XX).

Example of Ordering Information



ORDERING INFORMATION

Orderable Part Numbers	
CAT24C164LI–G	CAT24C164LE–G
CAT24C164WI–GT3	CAT24C164WE–GT3
CAT24C164YI–GT3	CAT24C164YE–GT3
CAT24C164VP2IGT3 (Note 15)	CAT24C164VP2EGT3 (Note 15)

11. All packages are RoHS-compliant (Lead-free, Halogen-free).
12. The standard lead finish is NiPdAu.
13. The device used in the above example is a CAT24C164YI–GT3 (TSSOP, Industrial Temperature, NiPdAu, Tape & Reel, 3,000/Reel).
14. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
15. Part number is not exactly the same as the “Example of Ordering Information” shown above. For the part numbers indicated there are NO hyphens in the orderable part numbers.
16. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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