Low Voltage, 1.15 V to 5.5 V, 4-Channel, Bidirectional Logic Level Translator

Data Sheet

ADG3304

FEATURES

- Bidirectional level translation
- Operates from 1.15 V to 5.5 V
- Low quiescent current < 5 µA
- No direction pin
- Qualified for automotive applications

APPLICATIONS

- SPI®, MICROWIRE™ level translation
- Low voltage ASIC level translation
- Smart card readers
- Cell phones and cell phone cradles
- Portable communications devices
- Telecommunications equipment
- Network switches and routers
- Storage systems (SAN/NAS)
- Computing/server applications
- GPS
- Portable POS systems
- Low cost serial interfaces

FUNCTIONAL BLOCK DIAGRAM

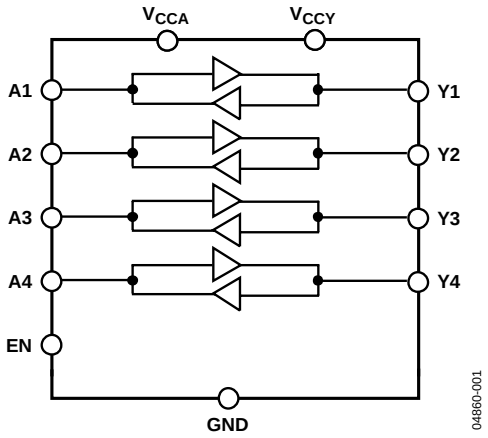


Figure 1.

GENERAL DESCRIPTION

The ADG3304 is a bidirectional logic level translator that contains four bidirectional channels. It can be used in multivoltage digital system applications, such as data transfer, between a low voltage digital signal processing controller and a higher voltage device using SPI and MICROWIRE interfaces. The internal architecture allows the device to perform bidirectional logic level translation without an additional signal to set the direction in which the translation takes place.

The voltage applied to V_{CCA} sets the logic levels on the A side of the device, while V_{CCY} sets the levels on the Y side. For proper operation, V_{CCA} must always be less than V_{CCY}. The V_{CCA}-compatible logic signals applied to the A side of the device appear as V_{CCY}-compatible levels on the Y side. Similarly, V_{CCY}-compatible logic levels applied to the Y side of the device appear as V_{CCA}-compatible logic levels on the A side.

The enable pin (EN) provides three-state operation on both the A side and the Y side pins. When the EN pin is pulled low, the terminals on both sides of the device are in the high impedance state. The EN pin is referred to the V_{CCA} supply voltage and driven high for normal operation.

The ADG3304 is available in compact 14-lead TSSOP, 12-ball WLCSP, and 20-lead LFCSP. It is guaranteed to operate over the 1.15 V to 5.5 V supply voltage range.

PRODUCT HIGHLIGHTS

1. Bidirectional level translation.
2. Fully guaranteed over the 1.15 V to 5.5 V supply range.
3. No direction pin.
4. Available in 14-lead TSSOP, 12-ball WLCSP, and 20-lead LFCSP.

Rev. D
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REVISION HISTORY

4/13—Rev. C to Rev. D
Changes to Figure 3 and Table 4 ... 7

12/12—Rev. B to Rev. C
Changes to Table 1 ... 3
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Changes to V_{CCY} Description, Table 3 and Table 4 ... 7
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Added Automotive Products Section ... 20

12/05—Rev. A to Rev. B
Changes to Table 1 ... 3
Changes to Table 2 ... 6
Changes to Figure 3 and Table 4 ... 7
Updated Outline Dimensions ... 19
Changes to Ordering Guide ... 21

6/05—Rev. 0 to Rev. A
Added LFCSP Package ... Universal

1/05—Revision 0: Initial Version

SPECIFICATIONS

V_{CCY} = 1.65 V to 5.5 V, V_{CCA} = 1.15 V to V_{CCY}, GND = 0 V, T_A = 25°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	B Version[1] Min	Typ	Max	Unit
LOGIC INPUTS/OUTPUTS						
A Side						
Input High Voltage[2]	V_{IHA}	V_{CCA} = 1.2 V + 0.1 V/−0.05 V	$V_{CCA} \times 0.88$			V
		V_{CCA} = 1.8 V ± 0.15 V	$V_{CCA} \times 0.72$			V
		V_{CCA} = 2.5 V ± 0.2 V	1.7			V
		V_{CCA} = 3.3 V ± 0.3 V	2.2			V
		V_{CCA} = 5 V ± 0.5 V	$V_{CCA} \times 0.7$			V
Input Low Voltage[2]	V_{ILA}	V_{CCA} = 1.2 V + 0.1 V/−0.05 V			$V_{CCA} \times 0.35$	V
		V_{CCA} = 1.8 V ± 0.15 V			$V_{CCA} \times 0.35$	V
		V_{CCA} = 2.5 V ± 0.2 V			0.7	V
		V_{CCA} = 3.3 V ± 0.3 V			0.8	V
		V_{CCA} = 5 V ± 0.5 V			$V_{CCA} \times 0.3$	V
Output High Voltage	V_{OHA}	$V_Y = V_{CCY}$, I_{OH} = 20 µA, see Figure 29	V_{CCA} − 0.4			V
Output Low Voltage	V_{OLA}	V_Y = 0 V, I_{OL} = 20 µA, see Figure 29			0.4	V
Capacitance[2]	C_A	f = 1 MHz, EN = 0, see Figure 34		9		pF
Leakage Current	$I_{LA, Hi-Z}$	V_A = 0 V/V_{CCA}, EN = 0, see Figure 31			±1	µA
Y Side						
Input High Voltage[2]	V_{IHY}	V_{CCY} = 1.8 V ± 0.15 V	$V_{CCY} \times 0.67$			V
		V_{CCY} = 2.5 V ± 0.2 V	1.7			V
		V_{CCY} = 3.3 V ± 0.3 V	2			V
		V_{CCY} = 5 V ± 0.5 V	$V_{CCY} \times 0.7$			V
Input Low Voltage[2]	V_{ILY}	V_{CCY} = 1.8 V ± 0.15 V			$V_{CCY} \times 0.35$	V
		V_{CCY} = 2.5 V ± 0.2 V			0.7	V
		V_{CCY} = 3.3 V ± 0.3 V			0.8	V
		V_{CCY} = 5 V ± 0.5 V			$V_{CCY} \times 0.25$	V
Output High Voltage	V_{OHY}	$V_A = V_{CCA}$, I_{OH} = 20 µA, see Figure 30	V_{CCY} − 0.4			V
Output Low Voltage	V_{OLY}	V_A = 0 V, I_{OL} = 20 µA, see Figure 30			0.4	V
Capacitance[2]	C_Y	f = 1 MHz, EN = 0, see Figure 35		6		pF
Leakage Current	$I_{LY, Hi-Z}$	V_Y = 0 V/V_{CCY}, EN = 0, see Figure 32			±1	µA
Enable (EN)						
Input High Voltage[2]	V_{IHEN}	V_{CCA} = 1.2 V + 0.1 V/−0.05 V	$V_{CCA} \times 0.88$			V
		V_{CCA} = 1.8 V ± 0.15 V	$V_{CCA} \times 0.72$			V
		V_{CCA} = 2.5 V ± 0.2 V	1.7			V
		V_{CCA} = 3.3 V ± 0.3 V	2.2			V
		V_{CCA} = 5 V ± 0.5 V	$V_{CCA} \times 0.7$			V
Input Low Voltage[2]	V_{ILEN}	V_{CCA} = 1.2 V + 0.1 V/−0.05 V			$V_{CCA} \times 0.35$	V
		V_{CCA} = 1.8 V ± 0.15 V			$V_{CCA} \times 0.35$	V
		V_{CCA} = 2.5 V ± 0.2 V			0.7	V
		V_{CCA} = 3.3 V ± 0.3 V			0.8	V
		V_{CCA} = 5 V ± 0.5 V			$V_{CCA} \times 0.3$	V
Leakage Current	I_{LEN}	V_{EN} = 0 V/V_{CCA}, V_A = 0 V, see Figure 33			±1	µA
Capacitance[2]	C_{EN}			3		pF
Enable Time[2]	t_{EN}	$R_S = R_T$ = 50 Ω, V_A = 0 V/V_{CCA} (A→Y), V_Y = 0 V/V_{CCY} (Y→A), see Figure 36		1	1.8	µs

Parameter	Symbol	Test Conditions/Comments	B Version[1] Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS[2]						
3.3 V ± 0.3 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 5 V ± 0.5 V						
A→Y Level Translation		$R_S = R_T = 50\ \Omega$, $C_L = 50$ pF, see Figure 37				
Propagation Delay	$t_{P, A\rightarrow Y}$			6	10	ns
Rise Time	$t_{R, A\rightarrow Y}$			2	3.5	ns
Fall Time	$t_{F, A\rightarrow Y}$			2	3.5	ns
Maximum Data Rate	$D_{MAX, A\rightarrow Y}$		50			Mbps
Channel-to-Channel Skew	$t_{SKEW, A\rightarrow Y}$			2	4	ns
Part-to-Part Skew	$t_{PPSKEW, A\rightarrow Y}$				3	ns
Y→A Level Translation		$R_S = R_T = 50\ \Omega$, $C_L = 15$ pF, see Figure 38				
Propagation Delay	$t_{P, Y\rightarrow A}$			4	7	ns
Rise Time	$t_{R, Y\rightarrow A}$			1	3	ns
Fall Time	$t_{F, Y\rightarrow A}$			3	7	ns
Maximum Data Rate	$D_{MAX, Y\rightarrow A}$		50			Mbps
Channel-to-Channel Skew	$t_{SKEW, Y\rightarrow A}$			2	3.5	ns
Part-to-Part Skew	$t_{PPSKEW, Y\rightarrow A}$				2	ns
1.8 V ± 0.15 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 3.3 V ± 0.3 V						
A→Y Translation		$R_S = R_T = 50\ \Omega$, $C_L = 50$ pF, see Figure 37				
Propagation Delay	$t_{P, A\rightarrow Y}$			8	11	ns
Rise Time	$t_{R, A\rightarrow Y}$			2	5	ns
Fall Time	$t_{F, A\rightarrow Y}$			2	5	ns
Maximum Data Rate	$D_{MAX, A\rightarrow Y}$		50			Mbps
Channel-to-Channel Skew	$t_{SKEW, A\rightarrow Y}$			2	4	ns
Part-to-Part Skew	$t_{PPSKEW, A\rightarrow Y}$				4	ns
Y→A Translation		$R_S = R_T = 50\ \Omega$, $C_L = 15$ pF, see Figure 38				
Propagation Delay	$t_{P, Y\rightarrow A}$			5	8	ns
Rise Time	$t_{R, Y\rightarrow A}$			2	3.5	ns
Fall Time	$t_{F, Y\rightarrow A}$			2	3.5	ns
Maximum Data Rate	$D_{MAX, Y\rightarrow A}$		50			Mbps
Channel-to-Channel Skew	$t_{SKEW, Y\rightarrow A}$			2	3	ns
Part-to-Part Skew	$t_{PPSKEW, Y\rightarrow A}$				3	ns
1.15 V to 1.3 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 3.3 V ± 0.3 V						
A→Y Translation		$R_S = R_T = 50\ \Omega$, $C_L = 50$ pF, see Figure 37				
Propagation Delay	$t_{P, A\rightarrow Y}$			9	18	ns
Rise Time	$t_{R, A\rightarrow Y}$			3	5	ns
Fall Time	$t_{F, A\rightarrow Y}$			2	5	ns
Maximum Data Rate	$D_{MAX, A\rightarrow Y}$		40			Mbps
Channel-to-Channel Skew	$t_{SKEW, A\rightarrow Y}$			2	5	ns
Part-to-Part Skew	$t_{PPSKEW, A\rightarrow Y}$				10	ns
Y→A Translation		$R_S = R_T = 50\ \Omega$, $C_L = 15$ pF, see Figure 38				
Propagation Delay	$t_{P, Y\rightarrow A}$			5	9	ns
Rise Time	$t_{R, Y\rightarrow A}$			2	4	ns
Fall Time	$t_{F, Y\rightarrow A}$			2	4	ns
Maximum Data Rate	$D_{MAX, Y\rightarrow A}$		40			Mbps
Channel-to-Channel Skew	$t_{SKEW, Y\rightarrow A}$			2	4	ns
Part-to-Part Skew	$t_{PPSKEW, Y\rightarrow A}$				4	ns

Parameter	Symbol	Test Conditions/Comments	B Version[1] Min	Typ	Max	Unit
1.15 V to 1.3 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 1.8 V ± 0.3 V						
A→Y Translation		R_S = R_T = 50 Ω, C_L = 50 pF, see Figure 37				
Propagation Delay	$t_{P, A→Y}$			12	25	ns
Rise Time	$t_{R, A→Y}$			7	12	ns
Fall Time	$t_{F, A→Y}$			3	5	ns
Maximum Data Rate	$D_{MAX, A→Y}$		25			Mbps
Channel-to-Channel Skew	$t_{SKEW, A→Y}$			2	5	ns
Part-to-Part Skew	$t_{PPSKEW, A→Y}$				15	ns
Y→A Translation		R_S = R_T = 50 Ω, C_L = 15 pF, see Figure 38				
Propagation Delay	$t_{P, Y→A}$			14	35	ns
Rise Time	$t_{R, Y→A}$			5	16	ns
Fall Time	$t_{F, Y→A}$			2.5	6.5	ns
Maximum Data Rate	$D_{MAX, Y→A}$		25			Mbps
Channel-to-Channel Skew	$t_{SKEW, Y→A}$			3	6.5	ns
Part-to-Part Skew	$t_{PPSKEW, Y→A}$				23.5	ns
2.5 V ± 0.2 V ≤ V_{CCA} ≤ V_{CCY}, V_{CCY} = 3.3 V ± 0.3 V						
A→Y Translation		R_S = R_T = 50 Ω, C_L = 50 pF, see Figure 37				
Propagation Delay	$t_{P, A→Y}$			7	10	ns
Rise Time	$t_{R, A→Y}$			2.5	4	ns
Fall Time	$t_{F, A→Y}$			2	5	ns
Maximum Data Rate	$D_{MAX, A→Y}$		60			Mbps
Channel-to-Channel Skew	$t_{SKEW, A→Y}$			1.5	2	ns
Part-to-Part Skew	$t_{PPSKEW, A→Y}$				4	ns
Y→A Translation		R_S = R_T = 50 Ω, C_L = 15 pF, see Figure 38				
Propagation Delay	$t_{P, Y→A}$			5	8	ns
Rise Time	$t_{R, Y→A}$			1	4	ns
Fall Time	$t_{F, Y→A}$			3	5	ns
Maximum Data Rate	$D_{MAX, Y→A}$		60			Mbps
Channel-to-Channel Skew	$t_{SKEW, Y→A}$			2	3	ns
Part-to-Part Skew	$t_{PPSKEW, Y→A}$				3	ns
POWER REQUIREMENTS						
Power Supply Voltages	V_{CCA}	V_{CCA} ≤ V_{CCY}	1.15		5.5	V
	V_{CCY}		1.65		5.5	V
Quiescent Power Supply Current	I_{CCA}	V_A = 0 V/V_{CCA}, V_Y = 0 V/V_{CCY}, V_{CCA} = V_{CCY} = 5.5 V, EN = 1		0.17	5	µA
	I_{CCY}	V_A = 0 V/V_{CCA}, V_Y = 0 V/V_{CCY}, V_{CCA} = V_{CCY} = 5.5 V, EN = 1		0.27	5	µA
Three-State Mode Power Supply Current	$I_{Hi-Z, A}$	V_{CCA} = V_{CCY} = 5.5 V, EN = 0		0.1	5	µA
	$I_{Hi-Z, Y}$	V_{CCA} = V_{CCY} = 5.5 V, EN = 0		0.1	5	µA

[1] T_A for typical specifications is 25°C.
[2] Guaranteed by design, not production tested.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{CCA} to GND	−0.3 V to +7 V
V_{CCY} to GND	V_{CCA} to +7 V
Digital Inputs (A)	−0.3 V to (V_{CCA} + 0.3 V)
Digital Inputs (Y)	−0.3 V to (V_{CCY} + 0.3 V)
EN to GND	−0.3 V to +7 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (4-Layer Board)	
14-Lead TSSOP	89.21°C/W
12-Ball WLCSP	120°C/W
20-Lead LFCSP	30.4°C/W
Lead Temperature, Soldering	As per JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

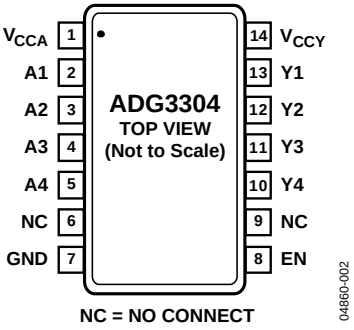


Figure 2. 14-Lead TSSOP Pin Configuration

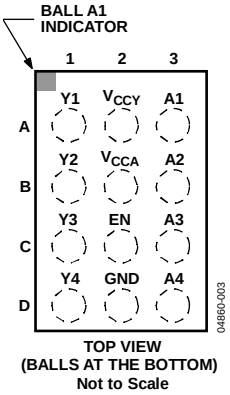


Figure 3. 12-Ball WLCSP Pin Configuration

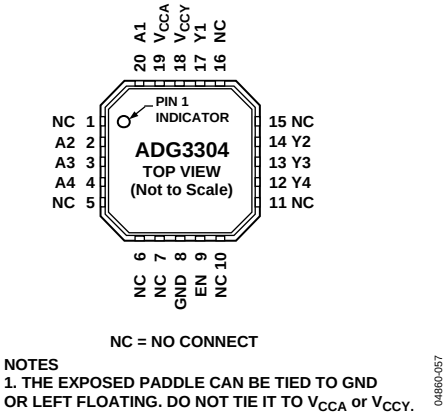


Figure 4. 20-Lead LFCSP_VQ Pin Configuration

Table 3. 14-Lead TSSOP and 20-lead LFCSP Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	V_{CCA}	Power Supply Voltage Input for the A1 to A4 I/O Pins (1.15 V ≤ V_{CCA} ≤ V_{CCY}).
2	20	A1	Input/Output A1. Referenced to V_{CCA}.
3	2	A2	Input/Output A2. Referenced to V_{CCA}.
4	3	A3	Input/Output A3. Referenced to V_{CCA}.
5	4	A4	Input/Output A4. Referenced to V_{CCA}.
6, 9	1, 5, 6, 7, 10, 11, 15, 16	NC	No Connect.
7	8	GND	Ground.
8	9	EN	Active High Enable Input.
10	12	Y4	Input/Output Y4. Referenced to V_{CCY}.
11	13	Y3	Input/Output Y3. Referenced to V_{CCY}.
12	14	Y2	Input/Output Y2. Referenced to V_{CCY}.
13	17	Y1	Input/Output Y1. Referenced to V_{CCY}.
14	18	V_{CCY}	Power Supply Voltage Input for the Y1 to Y4 I/O Pins (1.65 V ≤ V_{CCY} ≤ 5.5 V).

Table 4. 12-Ball WLCSP Pin Function Descriptions

Bump No.	Mnemonic	Description
A1	Y1	Input/Output Y1. Referenced to V_{CCY}.
B1	Y2	Input/Output Y2. Referenced to V_{CCY}.
C1	Y3	Input/Output Y3. Referenced to V_{CCY}.
D1	Y4	Input/Output Y4. Referenced to V_{CCY}.
A2	V_{CCY}	Power Supply Voltage Input for the Y1 to Y4 I/O Pins (1.65 V ≤ V_{CCY} ≤ 5.5 V).
B2	V_{CCA}	Power Supply Voltage Input for the A1 to A4 I/O Pins (1.15 V ≤ V_{CCA} ≤ V_{CCY}).
C2	EN	Active High Enable Input.
D2	GND	Ground.
A3	A1	Input/Output A1. Referenced to V_{CCA}.
B3	A2	Input/Output A2. Referenced to V_{CCA}.
C3	A3	Input/Output A3. Referenced to V_{CCA}.
D3	A4	Input/Output A4. Referenced to V_{CCA}.

TYPICAL PERFORMANCE CHARACTERISTICS

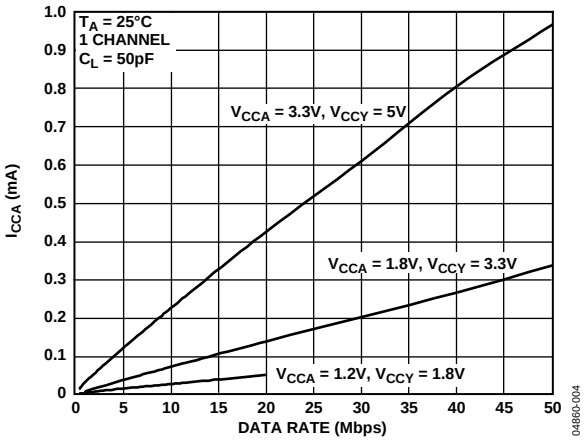


Figure 5. I_{CCA} vs. Data Rate (A→Y Level Translation)

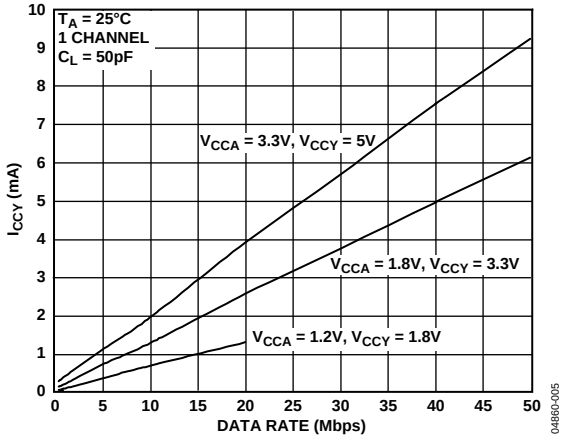


Figure 6. I_{CCY} vs. Data Rate (A→Y Level Translation)

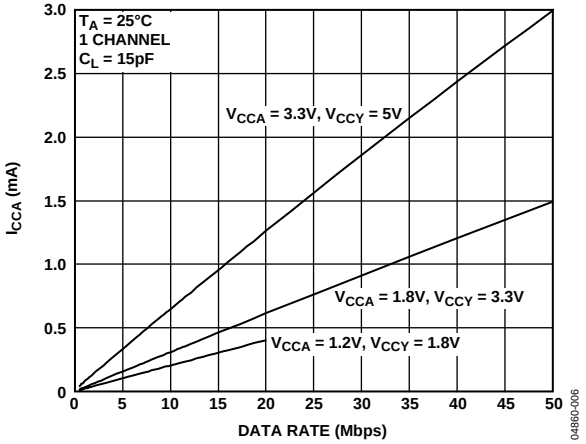


Figure 7. I_{CCA} vs. Data Rate (Y→A Level Translation)

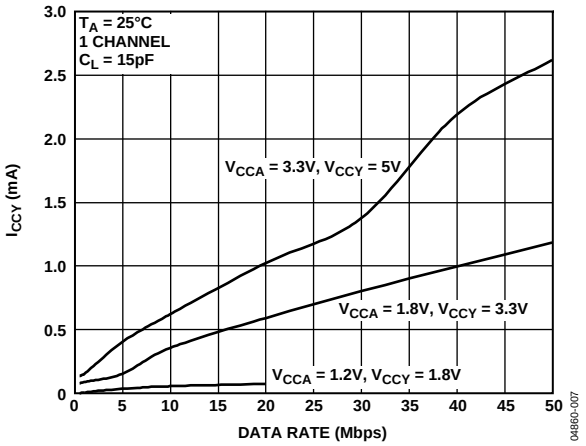


Figure 8. I_{CCY} vs. Data Rate (Y→A Level Translation)

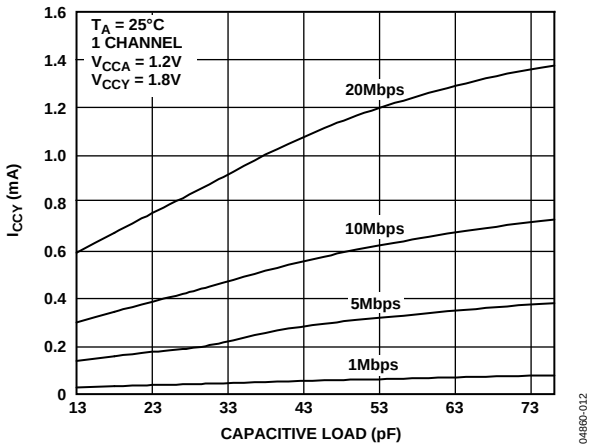


Figure 9. I_{CCY} vs. Capacitive Load at Pin Y for A→Y (1.2 V→1.8 V) Level Translation

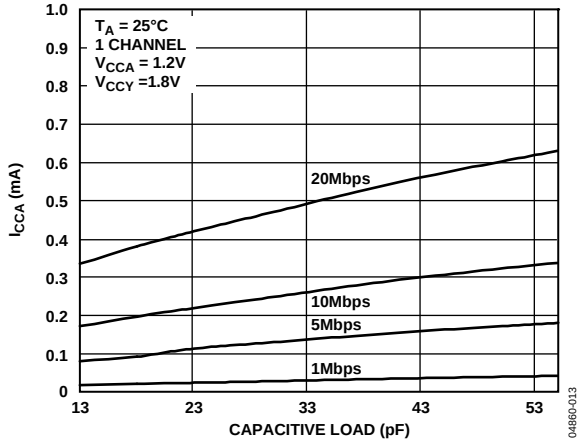


Figure 10. I_{CCA} vs. Capacitive Load at Pin A for Y→A (1.8 V→1.2 V) Level Translation

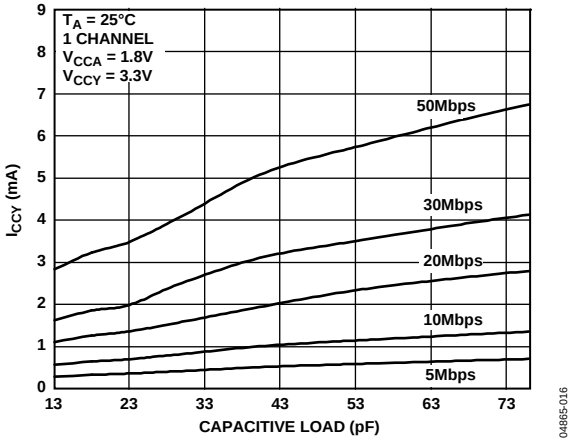


Figure 11. I_{CCY} vs. Capacitive Load at Pin Y for A→Y (1.8 V→3.3 V) Level Translation

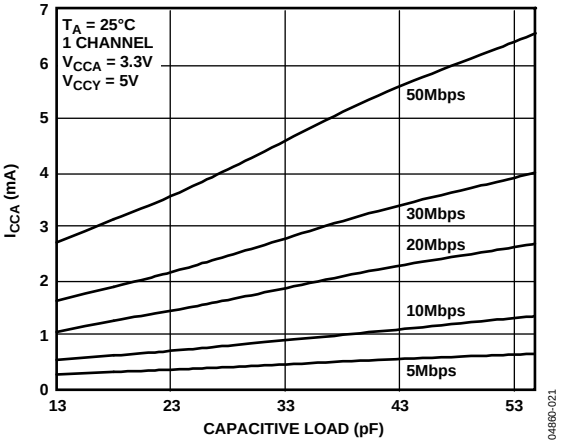


Figure 14. I_{CCA} vs. Capacitive Load at Pin A for Y→A (5 V→3.3 V) Level Translation

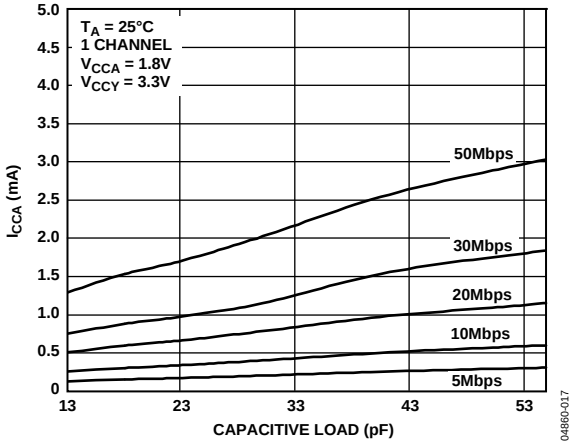


Figure 12. I_{CCA} vs. Capacitive Load at Pin A for Y→A (3.3 V→1.8 V) Level Translation

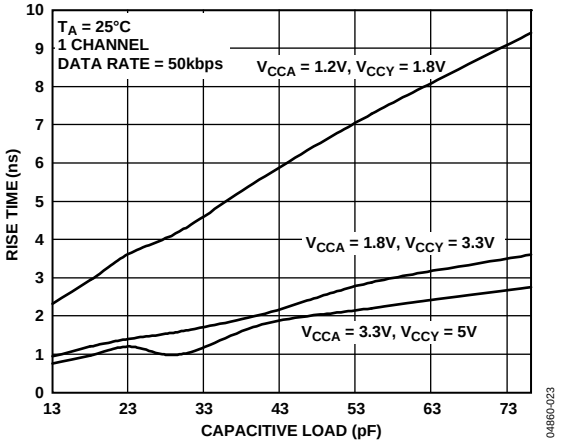


Figure 15. Rise Time vs. Capacitive Load at Pin Y (A→Y Level Translation)

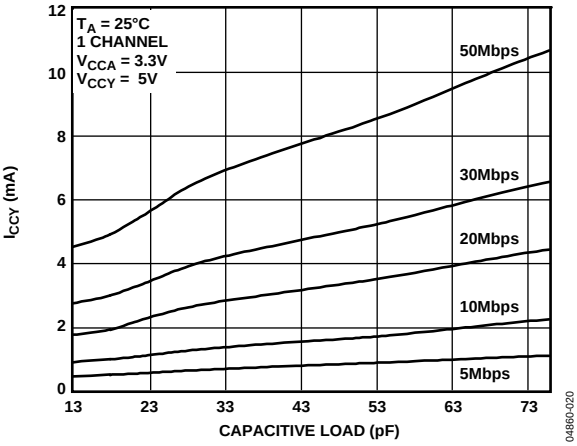


Figure 13. I_{CCY} vs. Capacitive Load at Pin Y for A→Y (3.3 V→5 V) Level Translation

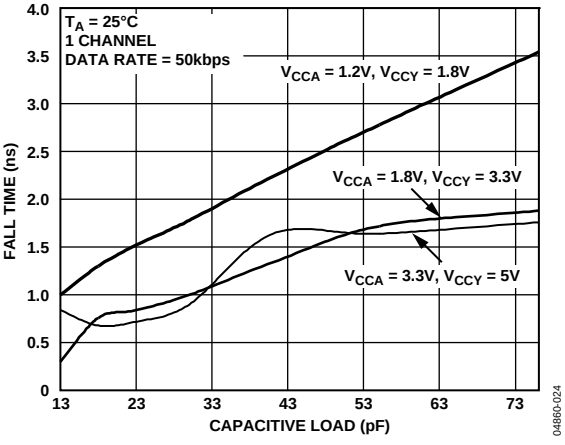


Figure 16. Fall Time vs. Capacitive Load at Pin Y (A→Y Level Translation)

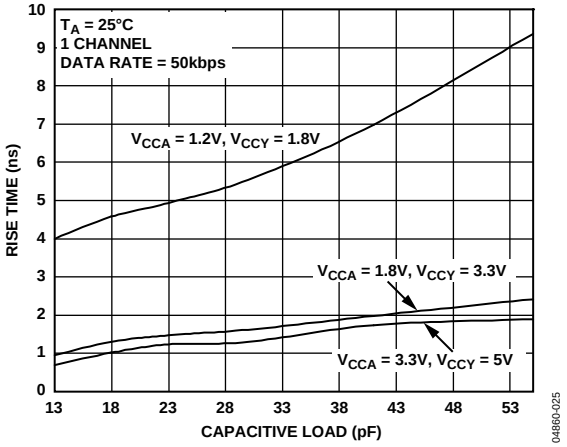


Figure 17. Rise Time vs. Capacitive Load at Pin A (Y→A Level Translation)

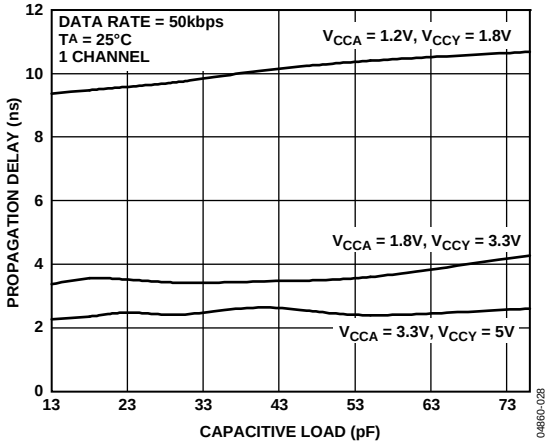


Figure 20. Propagation Delay (t_{PHL}) vs. Capacitive Load at Pin Y (A→Y Level Translation)

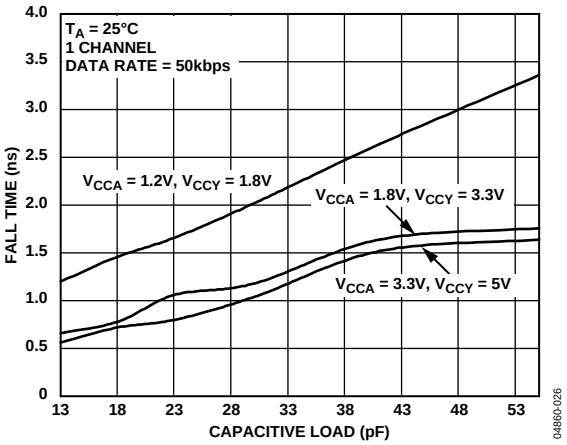


Figure 18. Fall Time vs. Capacitive Load at Pin A (Y→A Level Translation)

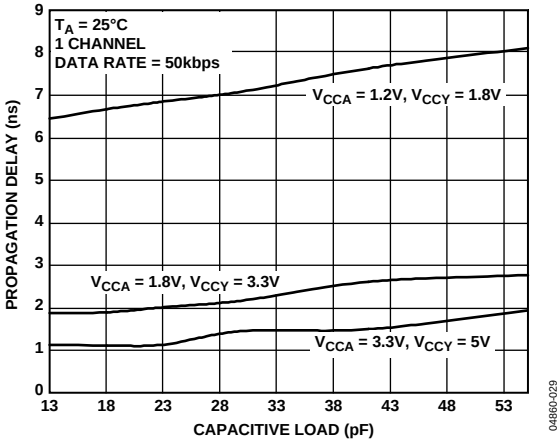


Figure 21. Propagation Delay (t_{PLH}) vs. Capacitive Load at Pin A (Y→A Level Translation)

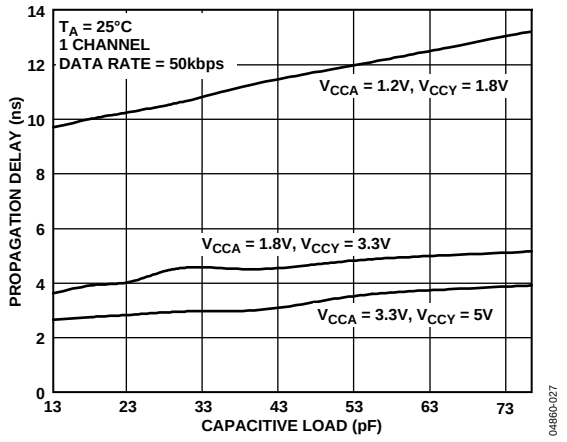


Figure 19. Propagation Delay (t_{PLH}) vs. Capacitive Load at Pin Y (A→Y Level Translation)

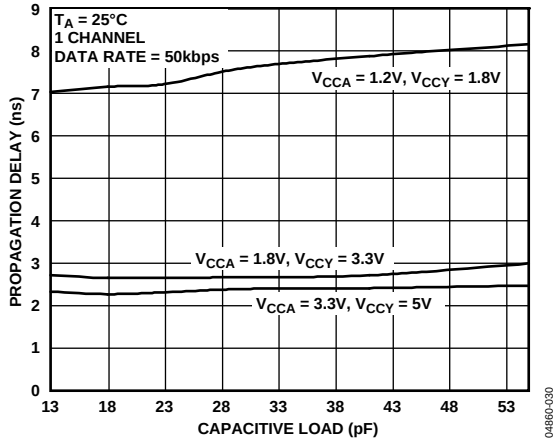


Figure 22. Propagation Delay (t_{PHL}) vs. Capacitive Load at Pin A (Y→A Level Translation)

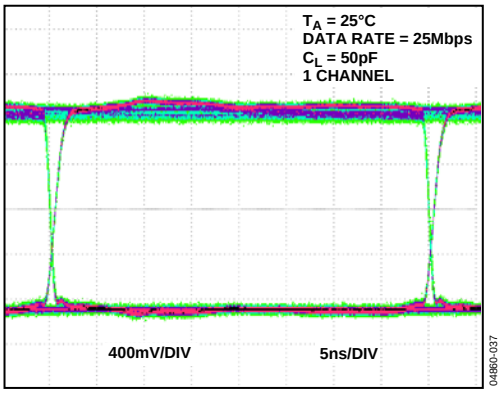


Figure 23. Eye Diagram at Y Output
(1.2 V to 1.8 V Level Translation, 25 Mbps)

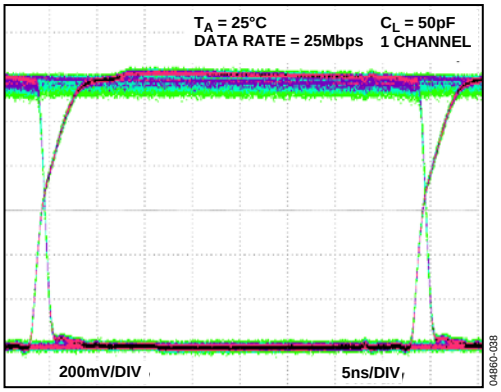


Figure 24. Eye Diagram at A Output
(1.8 V to 1.2 V Level Translation, 25 Mbps)

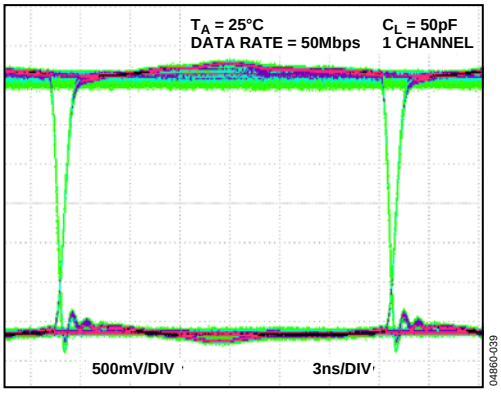


Figure 25. Eye Diagram at Y Output
(1.8 V to 3.3 V Level Translation, 50 Mbps)

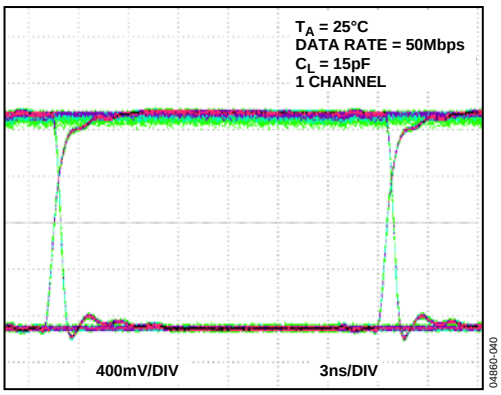


Figure 26. Eye Diagram at A Output
(3.3 V to 1.8 V Level Translation, 50 Mbps)

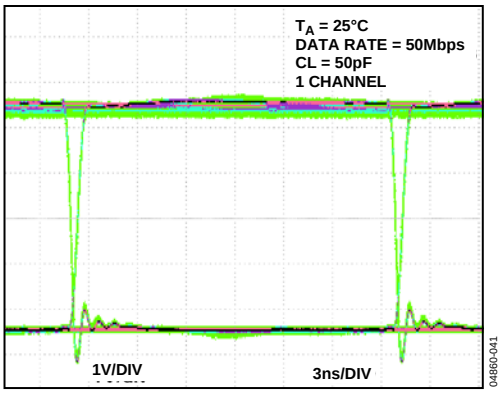


Figure 27. Eye Diagram at Y Output
(3.3 V to 5 V Level Translation, 50 Mbps)

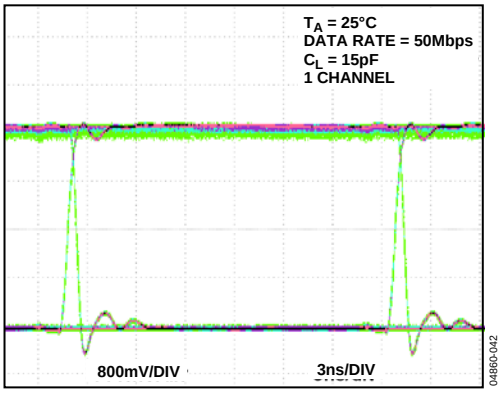


Figure 28. Eye Diagram at A Output
(5 V to 3.3 V Level Translation, 50 Mbps)

TEST CIRCUITS

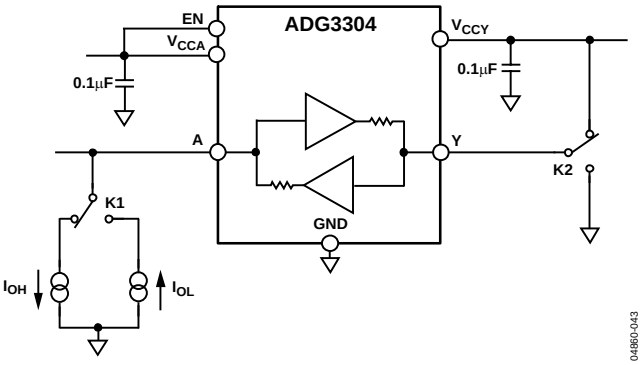


Figure 29. V_{OH}/V_{OL} Voltages at Pin A

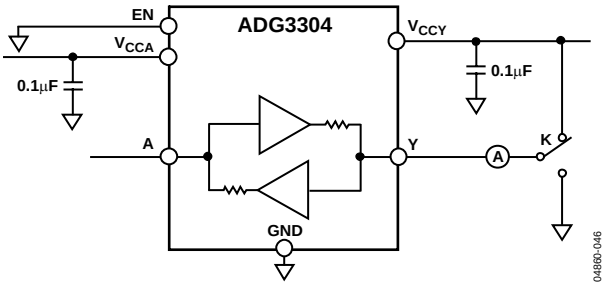


Figure 32. Three-State Leakage Current at Pin Y

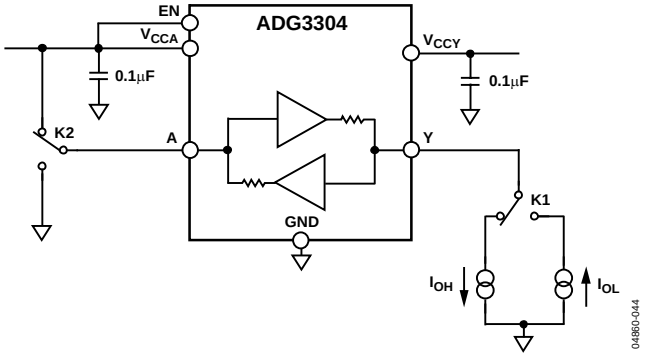


Figure 30. V_{OH}/V_{OL} Voltages at Pin Y

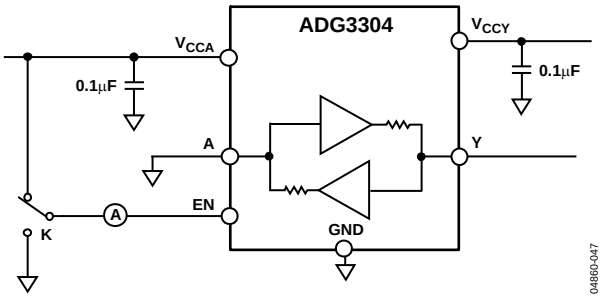


Figure 33. EN Pin Leakage Current

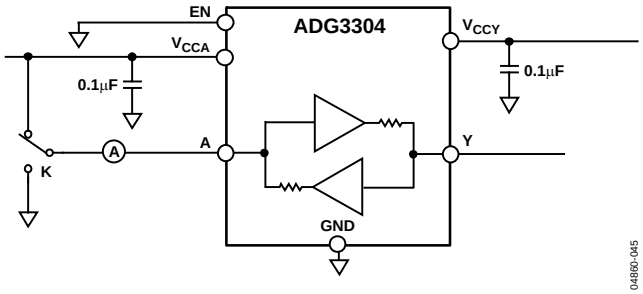


Figure 31. Three-State Leakage Current at Pin A

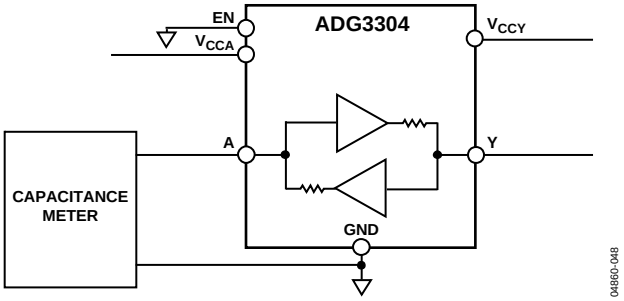


Figure 34. Capacitance at Pin A

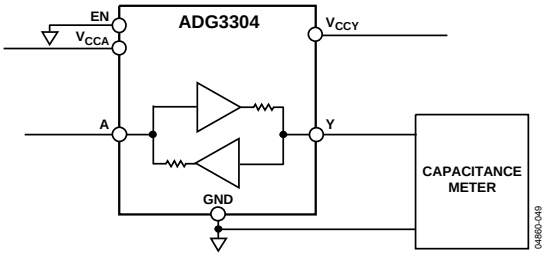
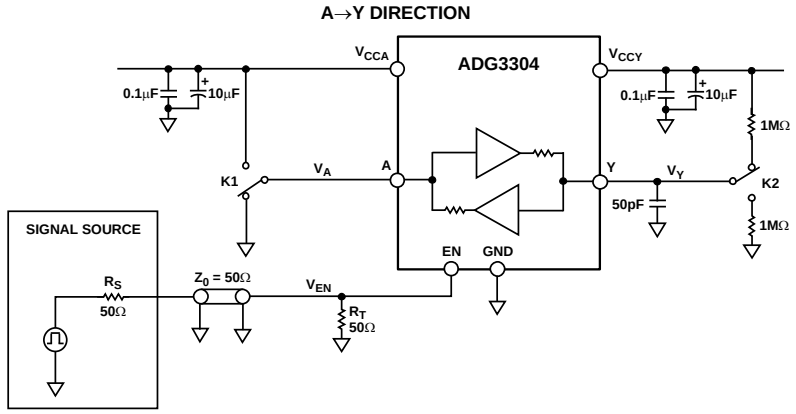
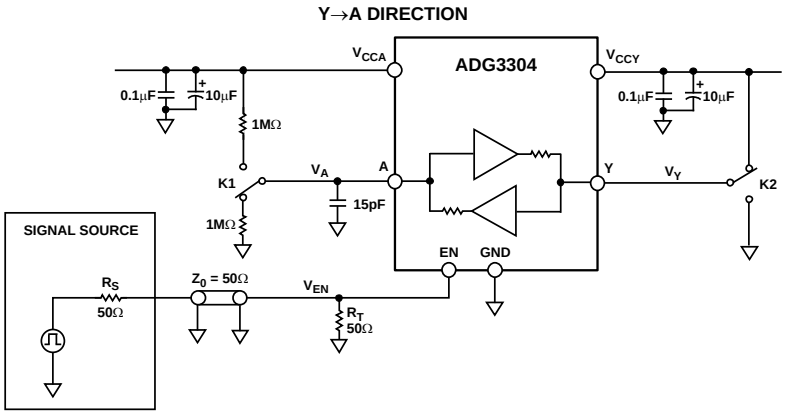
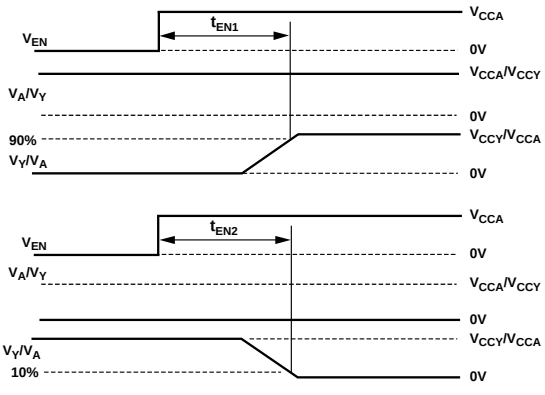


Figure 35. Capacitance at Pin Y







NOTES
1. t_{EN} IS WHICHEVER IS LARGER BETWEEN t_{EN1} AND t_{EN2} IN BOTH A→Y AND Y→A DIRECTIONS.

Figure 36. Enable Time

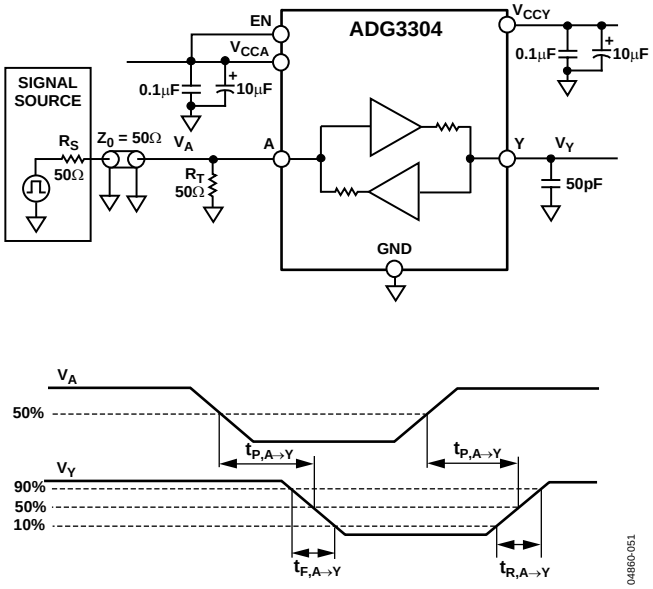


Figure 37. Switching Characteristics (A→Y Level Translation)

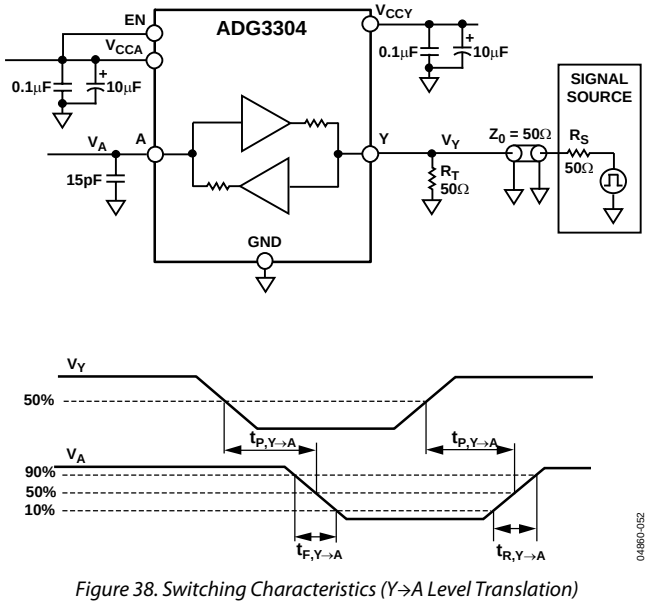


Figure 38. Switching Characteristics (Y→A Level Translation)

TERMINOLOGY

V_{IHA}
Logic input high voltage at Pin A1 to Pin A4.

V_{ILA}
Logic input low voltage at Pin A1 to Pin A4.

V_{OHA}
Logic output high voltage at Pin A1 to Pin A4.

V_{OLA}
Logic output low voltage at Pin A1 to Pin A4.

C_A
Capacitance measured at Pin A1 to Pin A4 (EN = 0).

$I_{LA, Hi-Z}$
Leakage current at Pin A1 to Pin A4 when EN = 0 (high impedance state at Pin A1 to Pin A4).

V_{IHY}
Logic input high voltage at Pin Y1 to Pin Y4.

V_{ILY}
Logic input low voltage at Pin Y1 to Pin Y4.

V_{OHY}
Logic output high voltage at Pin Y1 to Pin Y4.

V_{OLY}
Logic output low voltage at Pin Y1 to Pin Y4.

C_Y
Capacitance measured at Pin Y1 to Pin Y4 (EN = 0).

$I_{LY, Hi-Z}$
Leakage current at Pin Y1 to Pin Y4 when EN = 0 (high impedance state at Pin Y1 to Pin Y4).

V_{IHEN}
Logic input high voltage at the EN pin.

V_{ILEN}
Logic input low voltage at the EN pin.

C_{EN}
Capacitance measured at EN pin.

I_{LEN}
Enable (EN) pin leakage current.

t_{EN}
Three-state enable time for Pin A1 to Pin A4 and Pin Y1 to Pin Y4.

$t_{P, A\rightarrow Y}$
Propagation delay when translating logic levels in the A→Y direction.

$t_{R, A\rightarrow Y}$
Rise time when translating logic levels in the A→Y direction.

$T_{F, A\rightarrow Y}$
Fall time when translating logic levels in the A→Y direction.

$D_{MAX, A\rightarrow Y}$
Guaranteed data rate when translating logic levels in the A→Y direction under the driving and loading conditions specified in Table 1.

$T_{SKEW, A\rightarrow Y}$
Difference between propagation delays on any two channels when translating logic levels in the A→Y direction.

$t_{PPSKEW, A\rightarrow Y}$
Difference in propagation delay between any one channel and the same channel on a different part (under same driving/loading conditions) when translating in the A→Y direction.

$t_{P, Y\rightarrow A}$
Propagation delay when translating logic levels in the Y→A direction.

$t_{R, Y\rightarrow A}$
Rise time when translating logic levels in the Y→A direction.

$t_{F, Y\rightarrow A}$
Fall time when translating logic levels in the Y→A direction.

$D_{MAX, Y\rightarrow A}$
Guaranteed data rate when translating logic levels in the Y→A direction under the driving and loading conditions specified in Table 1.

$t_{SKEW, Y\rightarrow A}$
Difference between propagation delays on any two channels when translating logic levels in the Y→A direction.

$t_{PPSKEW, Y\rightarrow A}$
Difference in propagation delay between any one channel and the same channel on a different part (under the same driving/loading conditions) when translating in the Y→A direction.

V_{CCA}
V_{CCA} supply voltage.

V_{CCY}
V_{CCY} supply voltage.

I_{CCA}
V_{CCA} supply current.

I_{CCY}
V_{CCY} supply current.

$I_{Hi-Z, A}$
V_{CCA} supply current during three-state mode (EN = 0).

$I_{Hi-Z, Y}$
V_{CCY} supply current during three-state mode (EN = 0).

THEORY OF OPERATION

The ADG3304 level translator allows the level shifting necessary for data transfer in a system where multiple supply voltages are used. The device requires two supplies, V_{CCA} and V_{CCY} ($V_{CCA} \leq V_{CCY}$). These supplies set the logic levels on each side of the device. When driving the A pins, the device translates the V_{CCA}-compatible logic levels to V_{CCY}-compatible logic levels available at the Y pins. Similarly, because the device is capable of bidirectional translation, when driving the Y pins, the V_{CCY}-compatible logic levels are translated to V_{CCA}-compatible logic levels available at the A pins. When EN = 0, Pin A1 to Pin A4 and Pin Y1 to Pin Y4 are three-stated. When EN is driven high, the ADG3304 goes into normal operation mode and performs level translation.

LEVEL TRANSLATOR ARCHITECTURE

The ADG3304 consists of four bidirectional channels. Each channel can translate logic levels in either the A→Y or the Y→A direction. It uses a one-shot accelerator architecture, which ensures excellent switching characteristics. Figure 39 shows a simplified block diagram of a bidirectional channel.

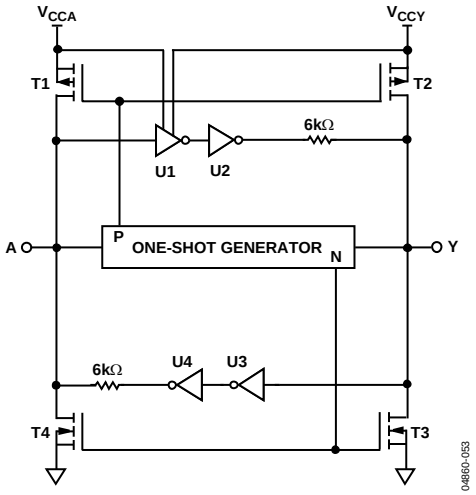


Figure 39. Simplified Block Diagram of an ADG3304 Channel

The logic level translation in the A→Y direction is performed using a level translator (U1) and an inverter (U2), while the translation in the Y→A direction is performed using Inverter U3 and Inverter U4. The one-shot generator detects a rising or falling edge present on either the A side or the Y side of the channel. It sends a short pulse that turns on the PMOS transistors (T1 to T2) for a rising edge, or the NMOS transistors (T3 to T4) for a falling edge. This charges/discharges the capacitive load faster, which results in faster rise and fall times.

The inputs of the unused channels (A or Y) should be tied to their corresponding V_{CC} rail (V_{CCA} or V_{CCY}) or to GND.

INPUT DRIVING REQUIREMENTS

To ensure correct operation of the ADG3304, the circuit that drives the input of the ADG3304 channels should have an output impedance of less than or equal to 150 Ω and a minimum peak current driving capability of 36 mA.

OUTPUT LOAD REQUIREMENTS

The ADG3304 level translator is designed to drive CMOS-compatible loads. If current-driving capability is required, it is recommended to use buffers between the ADG3304 outputs and the load.

ENABLE OPERATION

The ADG3304 provides three-state operation at the A and Y I/O pins by using the enable pin (EN), as shown in Table 5.

Table 5. Truth Table

EN	Y I/O Pins	A I/O Pins
0	Hi-Z[1]	Hi-Z[1]
1	Normal operation[2]	Normal operation[2]

[1] High impedance state.
[2] In normal operation, the ADG3304 performs level translation.

While EN = 0, the ADG3304 enters into three-state mode. In this mode, the current consumption from both the V_{CCA} and V_{CCY} supplies is reduced, allowing the user to save power, which is critical, especially on battery-operated systems. The EN input pin can be driven with either V_{CCA}-compatible or V_{CCY}-compatible logic levels.

POWER SUPPLIES

For proper operation of the ADG3304, the voltage applied to the V_{CCA} must be less than or equal to the voltage applied to V_{CCY}. To meet this condition, the recommended power-up sequence is V_{CCY} first and then V_{CCA}. The ADG3304 operates properly only after both supply voltages reach their nominal values. It is not recommended to use the part in a system where, during power-up, V_{CCA} can be greater than V_{CCY} due to a significant increase in the current taken from the V_{CCA} supply. For optimum performance, the V_{CCA} pin and V_{CCY} pin should be decoupled to GND as close as possible to the device.

DATA RATE

The maximum data rate at which the device is guaranteed to operate is a function of the V_{CCA} and V_{CCY} supply voltage combination and the load capacitance. It is given by the maximum frequency of a square wave that can be applied to the device, which meets the V_{OH} and V_{OL} levels at the output and does not exceed the maximum junction temperature (see the Absolute Maximum Ratings section). Table 6 shows the guaranteed data rates at which the ADG3304 can operate in both directions (A→Y or Y→A level translation) for various V_{CCA} and V_{CCY} supply combinations.

Table 6. Guaranteed Data Rate (Mbps)[1]

	V_{CCY}			
V_{CCA}	**1.8 V (1.65 V to 1.95 V)**	**2.5 V (2.3 V to 2.7 V)**	**3.3 V (3.0 V to 3.6 V)**	**5 V (4.5 V to 5.5 V)**
1.2 V (1.15 V to 1.3 V)	25	30	40	40
1.8 V (1.65 V to 1.95 V)	-	45	50	50
2.5 V (2.3 V to 2.7 V)	-	-	60	50
3.3 V (3.0 V to 3.6 V)	-	-	-	50
5 V (4.5 V to 5.5 V)	-	-	-	-

[1] The load capacitance used is 50 pF when translating in the A→Y direction and 15 pF when translating in the Y→A direction.

APPLICATIONS

The ADG3304 is designed for digital circuits that operate at different supply voltages; therefore, logic level translation is required. The lower voltage logic signals are connected to the A pins, and the higher voltage logic signals are connected to the Y pins. The ADG3304 can provide level translation in both directions from A→Y or Y→A on all four channels, eliminating the need for a level translator IC for each direction. The internal architecture allows the ADG3304 to perform bidirectional level translation without an additional signal to set the direction in which the translation is made. It also allows simultaneous data flow in both directions on the same part, for example, when two channels translate in A→Y direction while the other two translate in Y→A direction. This simplifies the design by eliminating the timing requirements for the direction signal and reducing the number of ICs used for level translation.

Figure 40 shows an application where two microprocessors operating at 1.8 V and 3.3 V, respectively, can transfer data simultaneously using two full-duplex serial links, TX1/RX1 and TX2/RX2.

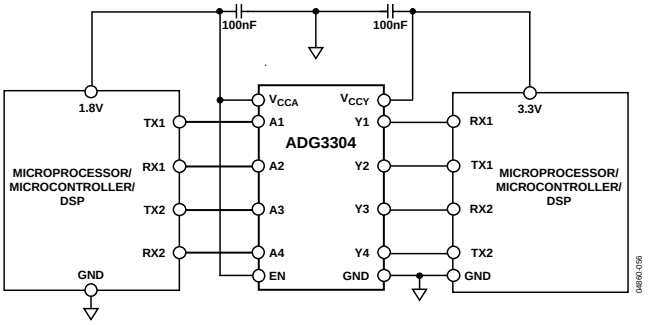


Figure 40. 1.8 V to 3.3 V Level Translation Circuit on Two Full-Duplex Serial Links

When the application requires level translation between a microprocessor and multiple peripheral devices, the ADG3304 I/O pins can be three-stated by setting EN = 0. This feature allows the ADG3304 to share the data buses with other devices without causing contention issues. Figure 41 shows an application where a 1.8 V microprocessor is connected to a 3.3 V peripheral device using the three-state feature.

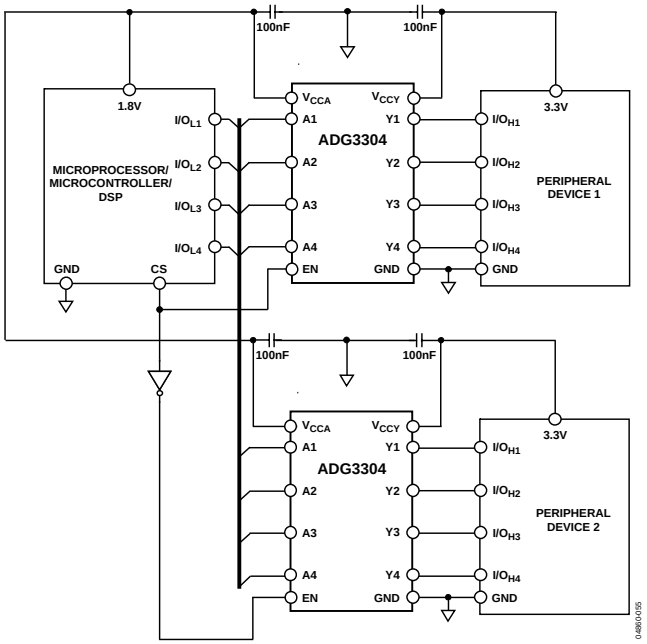


Figure 41. 1.8 V to 3.3 V Level Translation Circuit Using the Three-State Feature

LAYOUT GUIDELINES

As with any high speed digital IC, the printed circuit board layout is important for the overall performance of the circuit. Care should be taken to ensure proper power supply bypass and return paths for the high speed signals. Each V_{CC} pin (V_{CCA} and V_{CCY}) should be bypassed using low effective series resistance (ESR) and effective series inductance (ESI) capacitors placed as close as possible to the V_{CCA} pin and the V_{CCY} pin. The parasitic inductance of the high speed signal track may cause significant overshoot. This effect can be reduced by keeping the length of the tracks as short as possible. A solid copper plane for the return path (GND) is also recommended.

OUTLINE DIMENSIONS

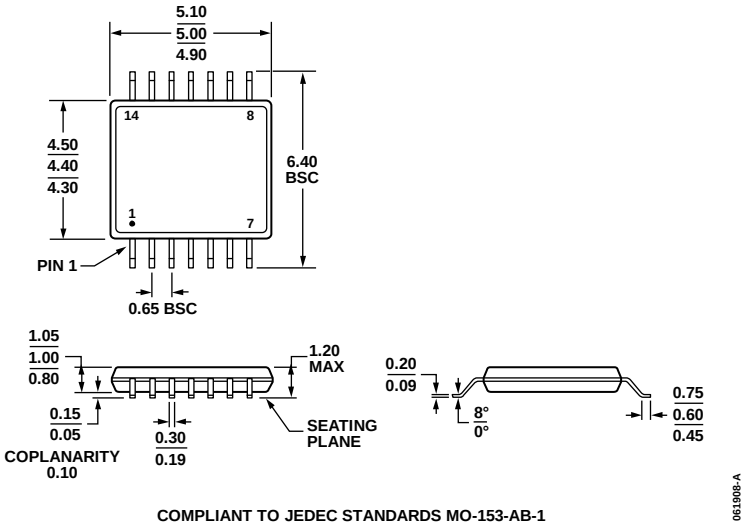


Figure 42. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

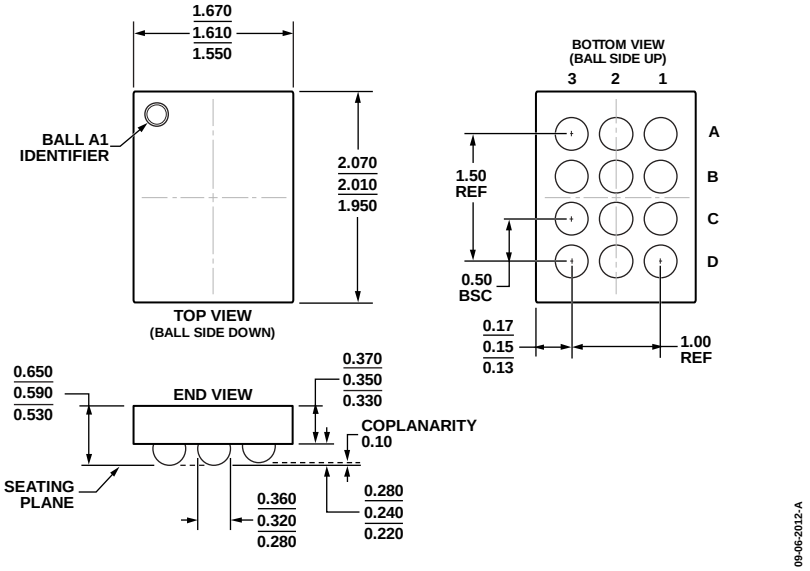


Figure 43. 12-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-12-1)
Dimensions shown in millimeters

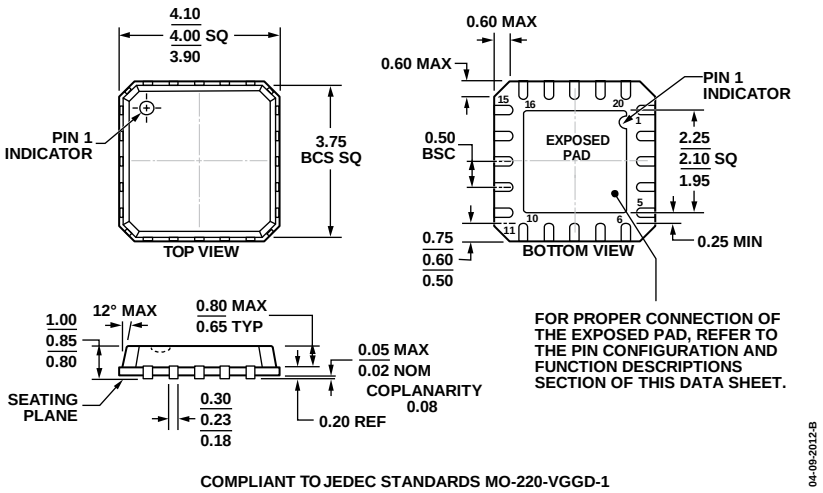


Figure 44. 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-20-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Branding[3]	Package Option
ADG3304BRUZ	−40°C to +85°C	14-Lead Thin Shrink Small Outline Package [TSSOP]		RU-14
ADG3304BRUZ-REEL	−40°C to +85°C	14-Lead Thin Shrink Small Outline Package [TSSOP]		RU-14
ADG3304BRUZ-REEL7	−40°C to +85°C	14-Lead Thin Shrink Small Outline Package [TSSOP]		RU-14
ADG3304BCPZ-REEL	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]		CP-20-1
ADG3304BCPZ-REEL7	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]		CP-20-1
ADG3304BCBZ-REEL	−40°C to +85°C	12-Ball Wafer Level Chip Scale Package [WLCSP]	SDC	CB-12-1
ADG3304BCBZ-REEL7	−40°C to +85°C	12-Ball Wafer Level Chip Scale Package [WLCSP]	SDC	CB-12-1
ADG3304WBRUZ-REEL	−40°C to +85°C	14-Lead Thin Shrink Small Outline Package [TSSOP]		RU-14

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] Branding on these packages is limited to three characters due to space constraints.

AUTOMOTIVE PRODUCTS

The ADG3304W model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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