



SP3243E

3 Driver/5 Receiver Intelligent +3.0V to +5.5V RS-232 Transceivers

FEATURES

- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- Interoperable with EIA/TIA-232 and adheres to EIA/TIA-562 down to a +2.7V power source
- AUTO ON-LINE® circuitry automatically wakes up from a 1µA shutdown
- Regulated Charge Pump Yields Stable RS-232 Outputs Regardless of V_{CC} Variations
- Enhanced ESD Specifications:
 - +15kV Human Body Model
 - +15kV IEC61000-4-2 Air Discharge
 - +8kV IEC61000-4-2 Contact Discharge
- 250 Kbps min. transmission rate (EB)
- 1000 Kbps min. transmission rate (EU)
- Ideal for High Speed RS-232 Applications



Now Available in Lead Free Packaging

DESCRIPTION

The SP3243E products are 3 driver/5 receiver RS-232 transceiver solutions intended for portable or hand-held applications such as notebook and palmtop computers. The SP3243E includes one complementary receiver that remains alert to monitor an external device's Ring Indicate signal while the device is shutdown. The SP3243E and EB devices feature slew-rate limited outputs for reduced crosstalk and EMI. The "U" and "H" series are optimized for high speed with data rates up to 1Mbps, easily meeting the demands of high speed RS-232 applications. The SP3243E series uses an internal high-efficiency, charge-pump power supply that requires only 0.1µF capacitors in 3.3V operation. This charge pump and Exar's driver architecture allow the SP3243E series to deliver compliant RS-232 performance from a single power supply ranging from +3.0V to +5.5V. The AUTO ON-LINE® feature allows the device to automatically "wake-up" during a shutdown state when an RS-232 cable is connected and a connected peripheral is turned on. Otherwise, the device automatically shuts itself down drawing less than 1µA.

SELECTION TABLE

| Device | Power Supplies | RS-232 Drivers | RS-232 Receivers | External Components | Auto On-Line Circuitry | TTL 3-State | # of Pins | Data Rate | ESD Rating |
|----------|----------------|----------------|------------------|---------------------|------------------------|-------------|-----------|-----------|------------|
| SP3243E | +3.0V to +5.5V | 3 | 5 | 4 Capacitors | Yes | Yes | 28 | 120 | 15kV |
| SP3243EB | +3.0V to +5.5V | 3 | 5 | 4 Capacitors | Yes | Yes | 28 | 250 | 15kV |
| SP3243EH | +3.0V to +5.5V | 3 | 5 | 4 Capacitors | Yes | Yes | 28 | 460 | 15kV |
| SP3243EU | +3.0V to +5.5V | 3 | 5 | 4 Capacitors | Yes | Yes | 28 | 1000 | 15kV |

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

| | |
|--|----------------|
| V _{CC} | -0.3V to +6.0V |
| V+ (NOTE 1)..... | -0.3V to +7.0V |
| V- (NOTE 1)..... | +0.3V to -7.0V |
| V+ + V- (NOTE 1)..... | +13V |
| I _{CC} (DC V _{CC} or GND current)..... | ±100mA |

Input Voltages

| | |
|---|--------------------------------|
| TxIN, <u>ONLINE</u> , <u>SHUTDOWN</u> , | -0.3V to V _{CC} +6.0V |
| RxIN..... | ±15V |

Output Voltages

| | |
|----------------------------|----------------------------------|
| TxOUT..... | ±13.2V |
| RxOUT, <u>STATUS</u> | -0.3V to (V _{CC} +0.3V) |

Short-Circuit Duration

| | |
|--------------------------|-----------------|
| TxOUT..... | Continuous |
| Storage Temperature..... | -65°C to +150°C |

NOTE 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

Power Dissipation per package

| | |
|--|--------|
| 28-pin SOIC (derate 12.7mW/°C above +70°C)..... | 1000mW |
| 28-pin SSOP (derate 11.2mW/°C above +70°C)..... | 900mW |
| 28-pin TSSOP (derate 13.2mW/°C above +70°C)..... | 1059mW |
| 32-pin QFN (derate 29.4mW/°C above +70°C)..... | 2352mW |

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.5V with T_{AMB} = T_{MIN} to T_{MAX}, C1 - C4 = 0.1µF. Typical values apply at V_{CC} = +3.3V or +5.0V and T_{AMB} = 25°C.

| PARAMETER | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|--|----------------------|----------------------|------|--------|--|
| DC CHARACTERISTICS | | | | | |
| Supply Current, AUTO ON-LINE® | | 1.0 | 10 | µA | All RxIN open, <u>ONLINE</u> = GND, <u>SHUTDOWN</u> = V _{CC} , V _{CC} = 3.3V T _{AMB} = 25°C, TxIN = GND or V _{CC} |
| Supply Current, Shutdown | | 1.0 | 10 | µA | <u>SHUTDOWN</u> = GND, V _{CC} = 3.3V, T _{AMB} = 25°C, TxIN = V _{CC} or GND |
| Supply Current AUTO ON-LINE® Disabled | | 0.3 | 1.0 | mA | <u>ONLINE</u> = <u>SHUTDOWN</u> = V _{CC} , no load, V _{CC} = 3.3V, T _{AMB} = +25°C, TxIN = GND or V _{CC} |
| LOGIC INPUTS AND RECEIVER OUTPUTS | | | | | |
| Input Logic Threshold LOW HIGH | | | 0.8 | V V | V _{CC} = =3.3V or =5.0V, TxIN <u>ONLINE</u> , <u>SHUTDOWN</u> |
| Input Leakage Current | | ±0.01 | ±1.0 | µA | TxIN, <u>ONLINE</u> , <u>SHUTDOWN</u> , T _{AMB} = +25°C, V _{IN} = 0V to V _{CC} |
| Output Leakage Current | | ±0.05 | ±10 | µA | Receivers disabled, V _{OUT} = 0V to V _{CC} |
| Output Voltage LOW | | | 0.4 | V | I _{OUT} = 1.6mA |
| Output Voltage HIGH | V _{CC} -0.6 | V _{CC} -0.1 | | V | I _{OUT} = -1.0mA |
| DRIVER OUTPUTS | | | | | |
| Output Voltage Swing | ±5.0 | ±5.4 | | V | All driver outputs loaded with 3KΩ to GND, T _{AMB} = +25°C |

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for $V_{CC} = +3.0V$ to $+5.5V$ with $T_{AMB} = T_{MIN}$ to T_{MAX} , $C1 - C4 = 0.1\mu F$. Typical values apply at $V_{CC} = +3.3V$ or $+5.0V$ and $T_{AMB} = 25^\circ C$.

| PARAMETER | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|----------------|--------------|------------|------------|--|
| DRIVER OUTPUTS (continued) | | | | | |
| Output Resistance | 300 | | | Ω | $V_{CC} = V+ = V- = 0V, V_{OUT} = \pm 2V$ |
| Output Short-Circuit Current | | ± 35 | ± 60 | mA | $V_{OUT} = 0V$ |
| Output Leakage Current | | | ± 25 | μA | $V_{CC} = 0V$ or $3.0V$ to $5.5V, V_{OUT} = \pm 12V$, Drivers disabled |
| RECEIVER INPUTS | | | | | |
| Input Voltage Range | -15 | | 15 | V | |
| Input Threshold LOW | 0.6 | 1.2 | | V | $V_{CC} = 3.3V$ |
| Input Threshold LOW | 0.8 | 1.5 | | V | $V_{CC} = 5.0V$ |
| Input Threshold HIGH | | 1.5 | 2.4 | V | $V_{CC} = 3.3V$ |
| Input Threshold HIGH | | 1.8 | 2.4 | V | $V_{CC} = 5.0V$ |
| Input Hysteresis | | 0.3 | | V | |
| Input Resistance | 3 | 5 | 7 | k Ω | |
| AUTO ON-LINE® CIRCUITRY CHARACTERISTICS ($\overline{ONLINE} = GND, \overline{SHUTDOWN} = VCC$) $25^\circ C$ | | | | | |
| STATUS Output Voltage LOW | | | 0.4 | V | $I_{OUT} = 1.6mA$ |
| STATUS Output Voltage HIGH | $V_{CC} - 0.6$ | | | V | $I_{OUT} = -1.0mA$ |
| Receiver Threshold to Drivers Enabled (t_{ONLINE}) | | 350 | | μs | Figure 14 |
| Receiver Positive or Negative Threshold to STATUS HIGH (t_{STSH}) | | 0.2 | | μs | Figure 14 |
| Receiver Positive or Negative Threshold to STATUS LOW (t_{STSL}) | | 30 | | μs | Figure 14 |
| TIMING CHARACTERISTICS | | | | | |
| Maximum Data Rate (U) | 1000 | | | Kbps | $R_L = 3K\Omega, C_L = 250pF$, one driver active |
| (H) | 460 | | | | $R_L = 3K\Omega, C_L = 1000pF$, one driver active |
| (B) | 250 | | | | $R_L = 3K\Omega, C_L = 1000pF$, one driver active |
| (-) | 120 | | | | $R_L = 3K\Omega, C_L = 1000pF$, one driver active |
| Receiver Propagation Delay t_{PHL} t_{PLH} | | 0.15 0.15 | | μs | Receiver input to Receiver output, $C_L = 150pF$ |
| Receiver Output Enable Time | | 200 | | ns | Normal operation |
| Receiver Output Disable Time | | 200 | | ns | Normal operation |
| Driver Skew (E, EB) (EH, EU) | | 100 50 | 500 100 | ns | $ t_{PHL} - t_{PLH} $ |
| Receiver Skew | | 50 | | ns | $ t_{PHL} - t_{PLH} $ |
| Transition-Region Slew Rate (EH, EU) (E, EB) | 6 | 90 | 30 | V/ μs | $V_{CC} = 3.3V, R_L = 3k\Omega, T_{AMB} = 25^\circ C$, measurements taken from $-3.0V$ to $+3.0V$ or $+3.0V$ to $-3.0V$ |

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for $V_{CC} = +3.3V$, 1000kbps data rate, all drivers loaded with 3k Ω , 0.1 μF charge pump capacitors, and $T_{AMB} = +25^{\circ}C$.



Figure 1. Transmitter Skew VS. Load Capacitance

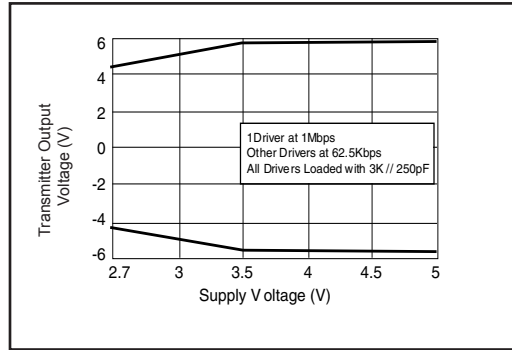


Figure 2. Transmitter Output Voltage VS. Supply Voltage for the SP3243EU



Figure 3. Transmitter Output Voltage VS. Load Capacitance for the SP3243EU

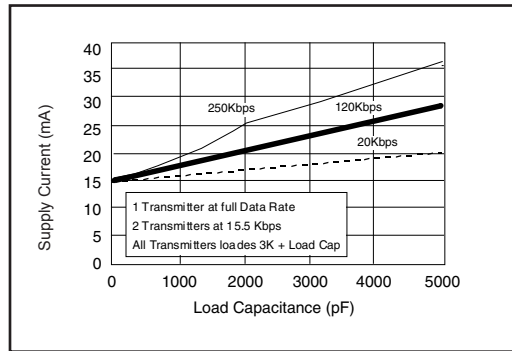


Figure 4. Supply Current VS. Load Capacitance for the SP3243EU



Figure 5. Supply Current VS. Supply Voltage for the SP3243EU

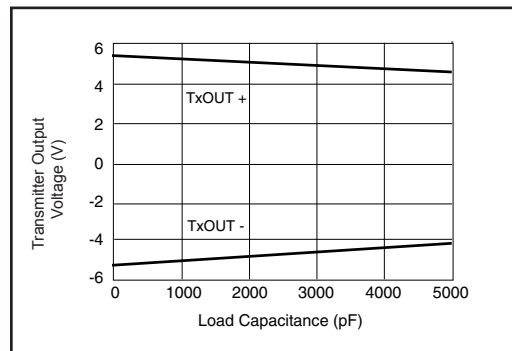


Figure 6. Transmitter Output Voltage VS. Load Capacitance for the SP3243EB

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for $V_{CC} = +3.3V$, 1000kbps data rate, all drivers loaded with $3k\Omega$, $0.1\mu F$ charge pump capacitors, and $T_{AMB} = +25^{\circ}C$.



Figure 7. Slew Rate VS. Load Capacitance

| NAME | FUNCTION | PIN NUMBER | |
|----------------------|--|------------|----------------|
| | | SP3243E | SP3243EUCR QFN |
| C1+ | Positive terminal of the voltage doubler charge-pump capacitor | 28 | 28 |
| V+ | Regulated +5.5V output generated by the charge pump | 27 | 26 |
| C1- | Negative terminal of the voltage doubler charge-pump capacitor | 24 | 22 |
| C2+ | Positive terminal of the inverting charge-pump capacitor | 1 | 29 |
| C2- | Negative terminal of the inverting charge-pump capacitor | 2 | 31 |
| V- | Regulated -5.5V output generated by the charge pump | 3 | 32 |
| R ₁ IN | RS-232 receiver input. | 4 | 2 |
| R ₂ IN | RS-232 receiver input | 5 | 3 |
| R ₃ IN | RS-232 receiver input | 6 | 4 |
| R ₄ IN | RS-232 receiver input | 7 | 5 |
| R ₅ IN | RS-232 receiver input | 8 | 6 |
| R ₁ OUT | TTL/CMOS receiver output | 19 | 17 |
| R ₂ OUT | TTL/CMOS receiver output | 18 | 16 |
| $\overline{R_2}$ OUT | Non-inverting receiver-2 output, active in shutdown | 20 | 18 |
| R ₃ OUT | TTL/CMOS receiver output | 17 | 15 |
| R ₄ OUT | TTL/CMOS receiver output | 16 | 14 |
| R ₅ OUT | TTL/CMOS receiver output | 15 | 13 |
| STATUS | TTL/CMOS Output indicating online and shutdown status | 21 | 19 |
| T ₁ IN | TTL/CMOS driver input | 14 | 12 |
| T ₂ IN | TTL/CMOS driver input | 13 | 11 |
| T ₃ IN | TTL/CMOS driver input | 12 | 10 |
| ONLINE | Apply logic HIGH to override AUTO ON-LINE® circuitry keeping drivers active (SHUTDOWN must also be logic HIGH, refer to Table 2) | 23 | 21 |
| T1 _{OUT} | RS-232 driver output | 9 | 7 |
| T2 _{OUT} | RS-232 driver output | 10 | 8 |
| T3 _{OUT} | RS-232 driver output | 11 | 9 |
| GND | Ground | 25 | 23 |
| V _{CC} | +3.0V to +5.5V supply voltage | 26 | 25 |
| SHUTDOWN | Apply logic LOW to SHUTDOWN driver and charge pump. This overrides all AUTO ON-LINE® circuitry and ONLINE (Refer to table 2) | 22 | 20 |
| NC | No Connection | - | 1,24,27,30 |

Table 1. Device Pin Description



Figure 8. SP3243E Typical Operating Circuit



Figure 9. SP3243E QFN Pinout Configuration

DESCRIPTION

The SP3243E transceivers meet the EIA/TIA-232 and ITU-TV.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The SP3243E devices feature Exar's proprietary and patented (U.S.-- 5,306,954) on-board charge pump circuitry that generates $\pm 5.5V$ RS-232 voltage levels from a single +3.0V to +5.5V power supply. The SP3243EU devices can operate at a data rate of 1000kbps fully loaded.

The SP3243E is a 3-driver/5-receiver device, ideal for portable or hand-held applications. The SP3243E includes one complementary always-active receiver that can monitor an external device (such as a modem) in shutdown. This aids in protecting the UART or serial controller IC by preventing forward biasing of the protection diodes where V_{CC} may be disconnected.

The SP3243E series is an ideal choice for power sensitive designs. The SP3243E devices feature AUTO ON-LINE[®] circuitry which reduces the power supply drain to a $1\mu A$ supply current.



Figure 10. Interface Circuitry Controlled by Microprocessor Supervisory Circuit

In many portable or hand-held applications, an RS-232 cable can be disconnected or a connected peripheral can be turned off. Under these conditions, the internal charge pump and the drivers will be shut down. Otherwise, the system automatically comes online. This feature allows design engineers to address power saving concerns without major design changes.

THEORY OF OPERATION

The SP3243E series is made up of four basic circuit blocks:

1. Drivers
2. Receivers
3. the Exar proprietary charge pump, and
4. AUTO ON-LINE[®] circuitry.

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to 5.0V EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is $\pm 5.4V$ with no load and $\pm 5V$ minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. These drivers comply with the EIA-TIA-232-F and all previous RS-232 versions. Unused drivers inputs should be connected to GND or V_{CC} .

The drivers have a minimum data rate of 250kbps (EB) or 1000kbps (EU) fully loaded.

Figure 11 shows a loopback test circuit used to test the RS-232 Drivers. Figure 12 shows the test results where one driver was active at 1Mbps and all three drivers loaded with an RS-232 receiver in parallel with a 250pF capacitor. Figure 13 shows the test results of the loopback circuit with all drivers active at 250kbps with typical RS-232 loads in parallel with 1000pF capacitors. A superior RS-232 data transmission rate of 1Mbps makes the SP3243EU an ideal match for high speed LAN and personal computer peripheral applications.

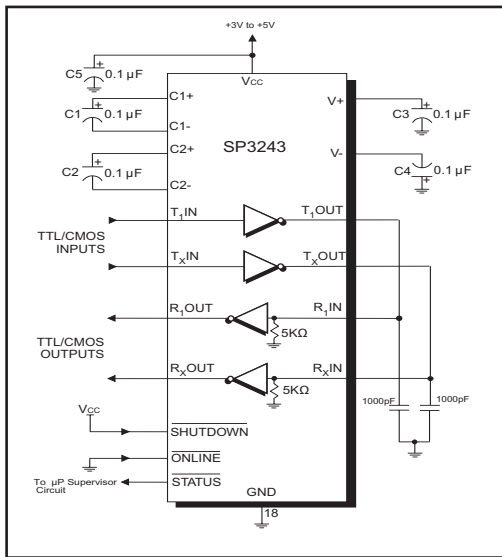


Figure 11. Loopback Test Circuit for RS-232 Driver Data Transmission Rates

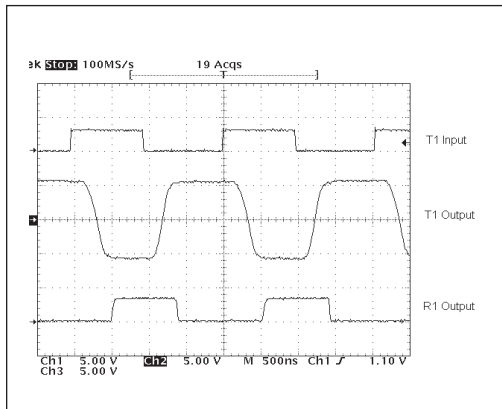


Figure 12. Loopback Test results at 1Mbps

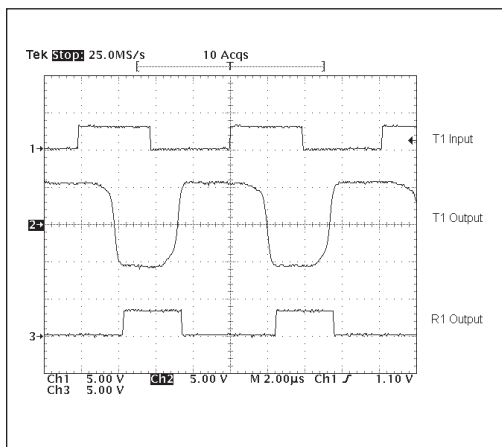


Figure 13. Loopback Test results at 250Kbps

Device: SP3243E

| SHUTDOWN | TxOUT | RxOUT | R2OUT |
|----------|--------|--------|--------|
| 0 | High-Z | High-Z | Active |
| 1 | Active | Active | Active |

Table 2. SHUTDOWN Truth Tables

Note: In AUTO ON-LINE[®] Mode where ONLINE = GND and SHUTDOWN = V_{CC}, the device will shut down if there is no activity present at the Receiver inputs.

Receivers

The receivers convert $\pm 5.0V$ EIA/TIA-232 levels to TTL or CMOS logic output levels. Receivers are High-Z when the AUTO ON-LINE[®] circuitry is enabled or when in shutdown. The truth table logic of the SP3243 driver and receiver outputs can be found in Table 2.

The SP3243E includes an additional non-inverting receiver with an output R₂OUT. R₂OUT is an extra output that remains active and monitors activity while the other receiver outputs are forced into high impedance. This allows a Ring Indicator (RI) signal from a peripheral to be monitored without forward biasing the TTL/CMOS inputs of the other devices connected to the receiver outputs.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5KΩ pull-down resistor to ground will commit the output of the receiver to a HIGH state.

Charge Pump

The charge pump is a Exar-patented design (U.S. 5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages 5.5V regardless of the input voltage (V_{CC}) over the +3.0V to +5.5V range. This is important to maintain compliant RS-232 levels regardless of power supply fluctuations.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC} . C_1^+ is then switched to GND and the charge in C_1^- is transferred to C_2^- . Since C_2^+ is connected to V_{CC} , the voltage potential across capacitor C_2 is now 2 times V_{CC} .

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_3 . This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C_3 , the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces $-V_{CC}$ in the negative terminal of C_1 , which is applied to the negative side of capacitor C_2 . Since C_2^+ is at V_{CC} , the voltage potential across C_2 is 2 times V_{CC} .

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_4 , the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_4 , the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V^+ and V^- are separately generated from V_{CC} , in a no-load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design. The clock rate for the charge pump typically operates at greater than 250kHz. The external capacitors can be as low as 0.1 μ F with a 16V breakdown voltage rating.

| Minimum recommended charge pump capacitor value | |
|---|--|
| Input Voltage Vcc | Charge pump capacitor value for SP32XX |
| 3.0V to 3.6V | C1 - C4 = 0.1 μ F |
| 4.5V to 5.5V | C1 = 0.047 μ F, C2 - C4 = 0.33 μ F |
| 3.0V to 5.5V | C1 - C4 = 0.22 μ F |

The Exar-patented charge pumps are designed to operate reliably with a range of low cost capacitors. Either polarized or non polarized capacitors may be used. If polarized capacitors are used they should be oriented as shown in the Typical Operating Circuit. The V+ capacitor may be connected to either ground or Vcc (polarity reversed.)

The charge pump operates with 0.1 μ F capacitors for 3.3V operation. For other supply voltages, see the table for required capacitor values. Do not use values smaller than those listed. Increasing the capacitor values (e.g., by doubling in value)

reduces ripple on the transmitter outputs and may slightly reduce power consumption. C2, C3, and C4 can be increased without changing C1's value.

For best charge pump efficiency locate the charge pump and bypass capacitors as close as possible to the IC. Surface mount capacitors are best for this purpose. Using capacitors with lower equivalent series resistance (ESR) and self-inductance, along with minimizing parasitic PCB trace inductance will optimize charge pump operation. Designers are also advised to consider that capacitor values may shift over time and operating temperature.

AUTO ONLINE CIRCUITRY

The SP3243E devices have a patent pending AUTO ON-LINE[®] circuitry on board that saves power in applications such as laptop computers, palmtop (PDA) computers and other portable systems.

The SP3243E devices incorporate an AUTO ON-LINE[®] circuit that automatically enables itself when the external transmitters are enabled and the cable is connected. Conversely, the AUTO ON-LINE[®] circuit also disables most of the internal circuitry when the device is not being used and goes into a standby mode where the device typically draws 1 μ A. This function is externally controlled by the $\overline{\text{ONLINE}}$ pin. When this pin is tied to a logic LOW, the AUTO ON-LINE[®] function is active. Once active, the device is enabled until there is no activity on the receiver inputs. The receiver input typically sees at least ± 3 V, which are generated from the transmitters at the other end of the cable with a ± 5 V minimum.

When the external transmitters are disabled or the cable is disconnected, the receiver inputs will be pulled down by their internal 5k Ω resistors to ground. When this occurs over a period of time, the internal transmitters will be disabled and the device goes into a shutdown or standby mode. When $\overline{\text{ONLINE}}$ is HIGH, the AUTO ON-LINE[®] mode is disabled.

The AUTO ON-LINE[®] circuit has two stages:

- 1) Inactive Detection
- 2) Accumulated Delay



Figure 14. AUTO ON-LINE® Timing Waveforms

The first stage, shown in Figure 21, detects an inactive input. A logic HIGH is asserted on R_x INACT if the cable is disconnected or the external transmitters are disabled. Otherwise, R_x INACT will be at a logic LOW. This circuit is duplicated for each of the other receivers.

The second stage of the AUTO ON-LINE® circuitry, shown in Figure 22, processes all the receiver's R_x INACT signals with an accumulated delay that disables the device to a 1µA supply current.

The $\overline{\text{STATUS}}$ pin goes to a logic LOW when the cable is disconnected, the external transmitters are disabled, or the $\overline{\text{SHUTDOWN}}$ pin is invoked. The typical accumulated delay is around 20µs.

When the SP3243E drivers or internal charge pump are disabled, the supply current is reduced to 1µA. This can commonly occur in hand-held or portable applications where the RS-232 cable is disconnected or the RS-232 drivers of the connected peripheral are turned off.

The AUTO ON-LINE® mode can be disabled by the $\overline{\text{SHUTDOWN}}$ pin. If this pin is a logic LOW, the AUTO ON-LINE® function will not operate regardless of the logic state of the $\overline{\text{ONLINE}}$ pin. Table 3 summarizes the logic of the AUTO ON-LINE® operating modes. The truth table logic of the SP3243E driver and receiver outputs can be found in Table 2.

The $\overline{\text{STATUS}}$ pin outputs a logic LOW signal if the device is shutdown. This pin goes to a logic HIGH when the external transmitters are enabled and the cable is connected.

When the SP3243E devices are shut down, the charge pumps are turned off. V+ charge pump output decays to V_{CC}, the V- output decays to GND. The decay time will depend on the size of capacitors used for the charge pump. Once in shutdown, the time required to exit the shut down state and have valid V+ and V- levels is typically 200µs.

For easy programming, the $\overline{\text{STATUS}}$ can be used to indicate DSR or a Ring Indicator signal. Tying $\overline{\text{ONLINE}}$ and $\overline{\text{SHUTDOWN}}$ together will bypass the AUTO ON-LINE® circuitry so this connection acts like a shutdown input pin.



Figure 15. Charge Pump — Phase 1



Figure 16. Charge Pump — Phase 2



Figure 17. Charge Pump — Phase 3



Figure 18. Charge Pump — Phase 4



Figure 19. SP3243E Driver Output Voltages vs. Load Current per Transmitter

The SP3243E driver outputs are able to maintain voltage under loading of up to 2.5mA per driver, ensuring sufficient output for mouse-driving applications.



Figure 20. Circuit for the connectivity of the SP3243E with a DB-9 connector

| RS-232 SIGNAL AT RECEIVER INPUT | $\overline{\text{SHUTDOWN}}$ INPUT | $\overline{\text{ONLINE}}$ INPUT | $\overline{\text{STATUS}}$ OUTPUT | TRANSCEIVER STATUS |
|---------------------------------|------------------------------------|----------------------------------|-----------------------------------|-----------------------------------|
| YES | HIGH | LOW | HIGH | Normal Operation (Auto-Online) |
| NO | HIGH | HIGH | LOW | Normal Operation |
| NO | HIGH | LOW | LOW | Shutdown (Auto-Online) |
| YES | LOW | HIGH / LOW | HIGH | Shutdown |
| NO | LOW | HIGH / LOW | LOW | Shutdown |

Table 3. AUTO ON-LINE[®] Logic



Figure 21. Stage I of AUTO ON-LINE[®] Circuitry



Figure 22. Stage II of AUTO ON-LINE[®] Circuitry

ESD TOLERANCE

The SP3243E series incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least $\pm 15\text{kV}$ without damage nor latch-up.

There are different methods of ESD testing applied:

- a) MIL-STD-883, Method 3015.7
- b) IEC61000-4-2 Air-Discharge
- c) IEC61000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semi-conductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 23. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-61000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC61000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives

most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC61000-4-2 is shown on Figure 24. There are two methods within IEC61000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.



Figure 23. ESD Test Circuit for Human Body Model



Figure 24. ESD Test Circuit for IEC61000-4-2

The circuit models in Figures 23 and 24 represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S , the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ an 100pF, respectively. For IEC-61000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330Ω an 150pF, respectively.

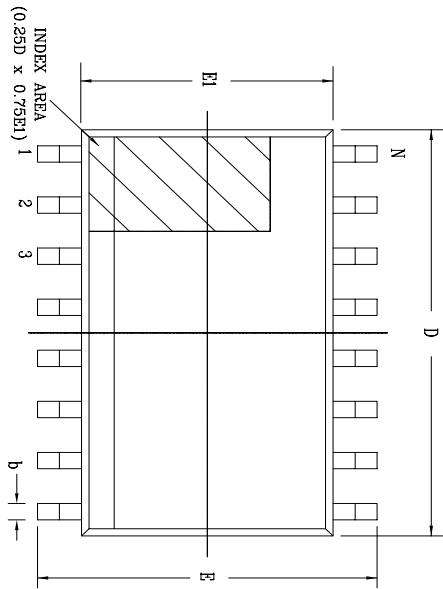
The higher C_S value and lower R_S value in the IEC61000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the



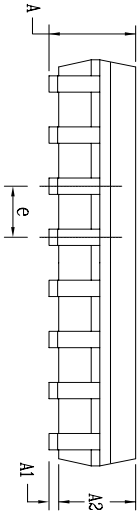
Figure 25. ESD Test Waveform for IEC61000-4-2

| DEVICE PIN TESTED | HUMAN BODY MODEL | IEC61000-4-2 | | |
|-------------------|------------------|---------------|----------------|-------|
| | | Air Discharge | Direct Contact | Level |
| Driver Outputs | ±15kV | ±15kV | ±8kV | 4 |
| Receiver Inputs | ±15kV | ±15kV | ±8kV | 4 |

Table 4. Transceiver ESD Tolerance Levels



Top View



Front View



Side View

| SYMBOLS | JEDEC MS-013 | | | Variation AE | | |
|---------|------------------------------------|-----|------|--|-----|-------|
| | DIMENSIONS IN MM (Control Unit) | | | DIMENSIONS IN INCH (Reference Unit) | | |
| A | 2.35 | — | 2.65 | 0.093 | — | 0.104 |
| A1 | 0.10 | — | 0.30 | 0.004 | — | 0.012 |
| A2 | 2.05 | — | 2.55 | 0.081 | — | 0.100 |
| b | 0.31 | — | 0.51 | 0.012 | — | 0.020 |
| c | 0.20 | — | 0.33 | 0.008 | — | 0.013 |
| E | 10.30 | BSC | — | 0.406 | BSC | — |
| E1 | 7.50 | BSC | — | 0.295 | BSC | — |
| e | 1.27 | BSC | — | 0.050 | BSC | — |
| h | 0.25 | — | 0.75 | 0.010 | — | 0.030 |
| L | 0.40 | — | 1.27 | 0.016 | — | 0.050 |
| L1 | 1.40 | REF | — | 0.055 | REF | — |
| L2 | 0.25 | BSC | — | 0.010 | BSC | — |
| R | 0.07 | — | — | 0.003 | — | — |
| R1 | 0.07 | — | — | 0.003 | — | — |
| θ | 0° | — | 8° | 0° | — | 8° |
| θ1 | 5° | — | 15° | 5° | — | 15° |
| θ2 | 0° | — | — | 0° | — | — |
| D | 17.90 | BSC | — | 0.705 | BSC | — |
| N | 28 | — | — | 28 | — | — |

| REVISION HISTORY | | | |
|------------------|--------------------------------------|----------|-------|
| REV. | DISCRIPTION | DATE | APP'D |
| A | DRAWING ORIGINATOR | 04/24/06 | JL |
| B | CHANGE DRAWING LOGO AND COMPANY NAME | 11/28/07 | JL |

| | | | |
|---------------------|--------------|------------------------------|---------------|
| | | EXAR CORPORATION | |
| | | 28 PIN SOICW PACKAGE OUTLINE | |
| Packaging Approval: | By: JL | Date: 11/28/07 | Revision: B |
| Drawing No.: | 28-PIN SOICW | | Sheet: 1 OF 1 |



| SYMBOLS | 32LD 5x5 QFN JEDEC MO-220 Variation VHHD | | | DIMENSIONS IN MM (Conversion Unit) | | | DIMENSIONS IN INCH (Reference Unit) | | |
|---------|--|------|------|------------------------------------|-------|-------|-------------------------------------|-----|-----|
| | MIN | NOM | MAX | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.80 | 0.90 | 1.00 | 0.032 | 0.036 | 0.039 | | | |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 | | | |
| A3 | 0.20 REF | | | 0.008 REF | | | | | |
| b | 0.18 | 0.25 | 0.30 | 0.007 | 0.010 | 0.012 | | | |
| D | 5.00 BSC | | | 0.197 BSC | | | | | |
| D2 | 3.00 | 3.10 | 3.20 | 0.118 | 0.122 | 0.126 | | | |
| E | 5.00 BSC | | | 0.197 BSC | | | | | |
| E2 | 3.00 | 3.10 | 3.20 | 0.118 | 0.122 | 0.126 | | | |
| e | 0.50 BSC | | | 0.020 BSC | | | | | |
| L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 | | | |
| K | 0.20 | — | — | 0.008 | — | — | | | |
| 0 | 0° | — | 14° | 0° | — | 14° | | | |
| N | 32 | | | 32 | | | | | |
| ND | 8 | | | 8 | | | | | |
| NE | 8 | | | 8 | | | | | |

| REVISION HISTORY | | | |
|------------------|--------------------------------------|----------|-------|
| REV. | DESCRIPTION | DATE | APP'D |
| A | DRAWING ORIGINATOR | 11/27/06 | JL |
| B | ISOART DRAWING FORMAT | 07/20/08 | JL |
| C | CHANGE DRAWING LOGO AND COMPANY NAME | 11/28/07 | JL |
| D | CHANGE DIMENSION D2 AND E2 | 04/29/09 | PC |

| | | | |
|---------------------|----------------|---|---------------|
| | | EXAR CORPORATION Precision Connectivity | |
| | | 32 PIN 5x5 QFN PACKAGE OUTLINE | |
| Packaging Approval: | | Drawing No: 32-PIN 5x5 QFN | |
| Bp: PC | Date: 04/29/09 | Revision: D | Sheet: 1 OF 1 |



| REVISION HISTORY | | | |
|------------------|--------------------------------------|----------|-------|
| REV. | DISCUSSION | DATE | APP'D |
| A | DRAWING ORIGINATION | 04/24/06 | JL |
| B | CHANGE DRAWING LOGO AND COMPANY NAME | 11/28/07 | JL |

| 28 Pin SSOP JEDEC MO-150 Variation AH | | | | | | |
|---------------------------------------|------------------------------------|--|-----------|-------|-------|-------|
| SYMBOLS | DIMENSIONS IN MM (Control Unit) | DIMENSIONS IN INCH (Reference Unit) | | | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | — | — | 2.00 | — | — | 0.079 |
| A1 | 0.05 | — | — | 0.002 | — | — |
| A2 | 1.65 | 1.75 | 1.85 | 0.065 | 0.069 | 0.073 |
| b | 0.22 | — | 0.38 | 0.009 | — | 0.015 |
| c | 0.09 | — | 0.25 | 0.004 | — | 0.010 |
| E | 7.40 | 7.80 | 8.20 | 0.291 | 0.307 | 0.323 |
| E1 | 5.00 | 5.30 | 5.60 | 0.197 | 0.209 | 0.220 |
| e | 0.65 BSC | | 0.026 BSC | | | |
| L | 0.55 | 0.75 | 0.95 | 0.022 | 0.030 | 0.037 |
| L1 | 1.25 REF | | 0.049 REF | | | |
| L2 | 0.25 BSC | | 0.010 BSC | | | |
| R1 | 0.09 | — | — | 0.004 | — | — |
| θ | 0° | 4° | 8° | 0° | 4° | 8° |
| D | 9.90 | 10.20 | 10.50 | 0.390 | 0.402 | 0.413 |
| N | 28 | | 28 | | | |

| | | | |
|---|----------------|-----------------------------|---------------|
|  | | EXAR CORPORATION | |
| Packaging Approval: | | Drawing No.: | |
| By: JL | Date: 11/28/07 | 28-PIN SSOP PACKAGE OUTLINE | 28-PIN SSOP |
| | | Revision: B | Sheet: 1 OF 1 |



| REVISION HISTORY | | | |
|------------------|--------------------------------------|----------|-------|
| REV. | DESCRIPTION | DATE | APP'D |
| A | DRAWING ORIGINATOR | 04/19/06 | JL |
| B | CHANGE DRAWING LOGO AND COMPANY NAME | 11/28/07 | JL |

| 28 Pin TSSOP JEDEC MO-153 Variation AE | | DIMENSIONS IN MM (Control Unit) | | | | DIMENSIONS IN INCH (Reference Unit) | | | |
|--|----------|---------------------------------|---------|-----------|-------|-------------------------------------|--|--|--|
| SYMBOLS | MIN | NOM | MAX | MIN | NOM | MAX | | | |
| A | — | — | 1.20 | — | — | 0.047 | | | |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 | | | |
| A2 | 0.80 | 1.00 | 1.05 | 0.031 | 0.039 | 0.041 | | | |
| b | 0.19 | — | 0.30 | 0.007 | — | 0.012 | | | |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 | | | |
| E | 6.40 BSC | | | 0.252 BSC | | | | | |
| E1 | 4.30 | 4.40 | 4.50 | 0.169 | 0.173 | 0.177 | | | |
| e | 0.65 BSC | | | 0.026 BSC | | | | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 | | | |
| L1 | 1.00 REF | | | 0.039 REF | | | | | |
| L2 | 0.25 BSC | | | 0.010 BSC | | | | | |
| R | 0.09 | — | — | 0.035 | — | — | | | |
| R1 | 0.09 | — | — | 0.035 | — | — | | | |
| theta | 12° REF | | 12° REF | | — | | | | |
| theta1 | 0° | — | 8° | 0° | — | 8° | | | |
| D | 9.60 | 9.70 | 9.80 | 0.378 | 0.382 | 0.386 | | | |
| N | 28 | | | 28 | | | | | |

| | | | | |
|--------|----------------|--|-------------|------------------------------|
| | | EXAR CORPORATION Packaging Approval: | | |
| | | | | 28 PIN TSSOP PACKAGE OUTLINE |
| By: JL | Date: 11/28/07 | Drawing No: 28-PIN TSSOP | Revision: B | Sheet: 1 OF 1 |

SP3243 E U EY-L/TR



ORDERING INFORMATION

| Part Number | Data Rate (kbps) | Temp. Range | Package |
|--------------|------------------|--------------|--------------|
| SP3243ECA-L | 120 | 0C to +70C | 28 Pin SSOP |
| SP3243ECT-L | 120 | 0C to +70C | 28 Pin WSOIC |
| SP3243ECY-L | 120 | 0C to +70C | 28 Pin TSSOP |
| SP3243EEA-L | 120 | -40C to +85C | 28 Pin SSOP |
| SP3243EET-L | 120 | -40C to +85C | 28 Pin WSOIC |
| SP3243EEY-L | 120 | -40C to +85C | 28 Pin TSSOP |
| SP3243EBCA-L | 250 | 0C to +70C | 28 Pin SSOP |
| SP3243EBCY-L | 250 | 0C to +70C | 28 Pin TSSOP |
| SP3243EBEA-L | 250 | -40C to +85C | 28 Pin SSOP |
| SP3243EBEY-L | 250 | -40C to +85C | 28 Pin TSSOP |
| SP3243EHCA-L | 460 | 0C to +70C | 28 Pin SSOP |
| SP3243EHCT-L | 460 | 0C to +70C | 28 Pin WSOIC |
| SP3243EHEA-L | 460 | -40C to +85C | 28 Pin SSOP |
| SP3243EHET-L | 460 | -40C to +85C | 28 Pin WSOIC |
| SP3243EUCA-L | 1000 | 0C to +70C | 28 Pin SSOP |
| SP3243EUCT-L | 1000 | 0C to +70C | 28 Pin WSOIC |
| SP3243EUCY-L | 1000 | 0C to +70C | 28 Pin TSSOP |
| SP3243EUER-L | 1000 | 0C to +70C | 32 Pin QFN |
| SP3243EUEA-L | 1000 | -40C to +85C | 28 Pin SSOP |
| SP3243EUET-L | 1000 | -40C to +85C | 28 Pin WSOIC |
| SP3243EUEY-L | 1000 | -40C to +85C | 28 Pin TSSOP |
| SP3243EUER-L | 1000 | -40C to +85C | 32 Pin QFN |

For Tape and Reel option add "/TR", Example: SP3243ECA-L/TR.

REVISION HISTORY

| DATE | REVISION | DESCRIPTION |
|----------|----------|--|
| 02/05/06 | -- | Legacy Sipex Datasheet |
| 07/23/09 | 1.0.0 | Convert to Exar Format, Update ordering information and change revision to 1.0.0. |
| 11/10/09 | 1.0.1 | Add missing (EH) model identification for Driver output Skew and Transition-Region Slew Rate specification and change revision to 1.0.1. |
| 06/06/11 | 1.0.2 | Remove obsolete devices per PDN 110510-01 and change ESD rating to IEC61000-4-2. |

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Datasheet June 2011

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- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
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Тел: +7 (812) 336 43 04 (многоканальный)

Email: org@lifeelectronics.ru