



STB32NM50N, STF32NM50N, STP32NM50N, STW32NM50N

N-channel 500 V, 0.1 Ω typ., 22 A MDmesh™ II Power MOSFET
in D²PAK, TO-220FP, TO-220, TO-247 packages

Datasheet — production data

Features

Order codes	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STB32NM50N	500 V	0.13 Ω	22 A	190 W
STF32NM50N				35 W
STP32NM50N				190 W
STW32NM50N				190 W

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

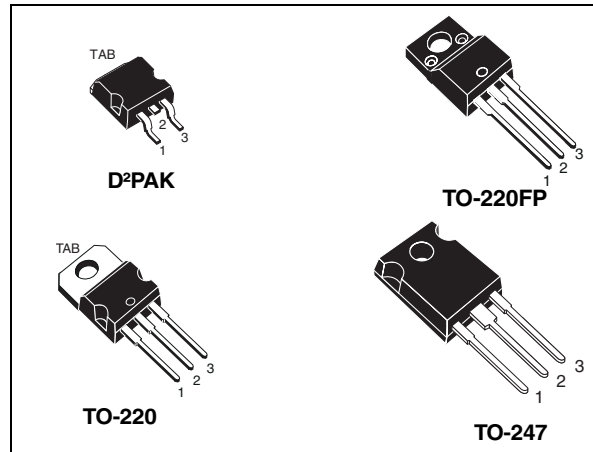


Figure 1. Internal schematic diagram

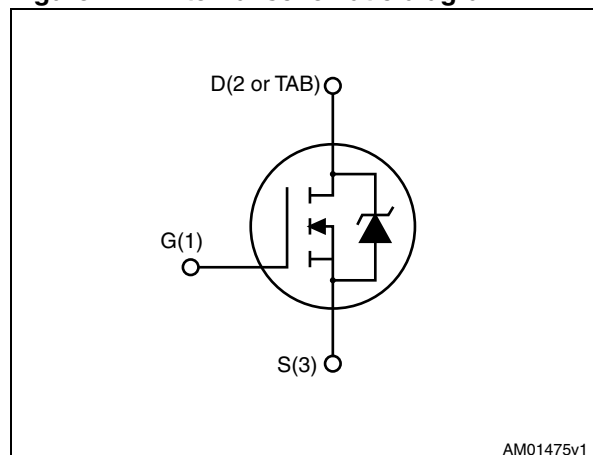


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB32NM50N	32NM50N	D ² PAK	Tape and reel
STF32NM50N		TO-220FP	Tube
STP32NM50N		TO-220	Tube
STW32NM50N		TO-247	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK, TO-220, TO-247	TO-220FP	
V _{DS}	Drain-source voltage	500		V
V _{GS}	Gate- source voltage	± 25		V
I _D	Drain current (continuous) at T _C = 25 °C	22	22 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	13.86	13.86 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	88	88	A
P _{TOT}	Total dissipation at T _C = 25 °C	190	35	W
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _J max)	7		A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	340		mJ
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)	2500		V
T _{stg}	Storage temperature	- 55 to 150		°C
T _J	Max. operating junction temperature	150		

- Limited by maximum junction temperature.
- Pulse width limited by safe operating area.
- I_{SD} ≤ 22 A, di/dt ≤ 400 A/μs, V_{DS} peak ≤ V_{(BR)DSS}, V_{DD} ≤ 80% V_{(BR)DSS}

Table 3. Thermal data

Symbol	Parameter	D ² PAK	TO-220FP	TO-220	TO-247	Unit
R _{thj-case}	Thermal resistance junction-case max	0.66	3.6	0.66		°C/W
R _{thj-amb}	Thermal resistance junction-ambient max		62.5	50		
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb max	30				

- When mounted on FR-4 board of 1 inch², 2 oz Cu.

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 1\text{ mA}$	500			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 500\text{ V}$ $V_{DS} = 500\text{ V}, T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 11\text{ A}$		0.1	0.13	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	1973	-	pF
C_{oss}	Output capacitance			179		pF
C_{rss}	Reverse transfer capacitance			9.7		pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0\text{ to }400\text{ V}$	-	325	-	pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}, I_D = 11\text{ A}$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 23), (see Figure 18)	-	21.5	-	ns
t_r	Rise time			9.5		ns
$t_{d(off)}$	Turn-off delay time			110		ns
t_f	Fall time			23.6		ns
Q_g	Total gate charge	$V_{DD} = 400\text{ V}, I_D = 22\text{ A},$ $V_{GS} = 10\text{ V},$ (see Figure 19)	-	62.5	-	nC
Q_{gs}	Gate-source charge			8.6		nC
Q_{gd}	Gate-drain charge			33		nC
R_g	Gate input resistance	f=1MHz Gate DC Bias=0 Test signal level=20 mV Open drain	-	3.8	-	Ω

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		22	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		88	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 22\text{ A}, V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 22\text{ A}, V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ (see Figure 20)	-	328		ns
Q_{rr}	Reverse recovery charge			5		nC
I_{RRM}	Reverse recovery current			30.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 22\text{ A}, V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 20)	-	392		ns
Q_{rr}	Reverse recovery charge			6.5		nC
I_{RRM}	Reverse recovery current			32.8		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK and TO-220

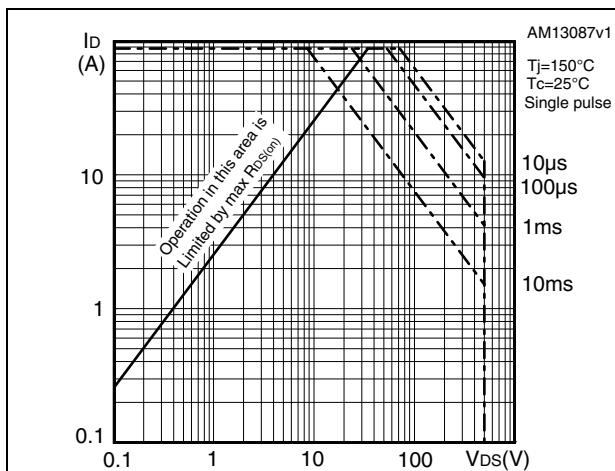


Figure 3. Thermal impedance for for D²PAK and TO-220

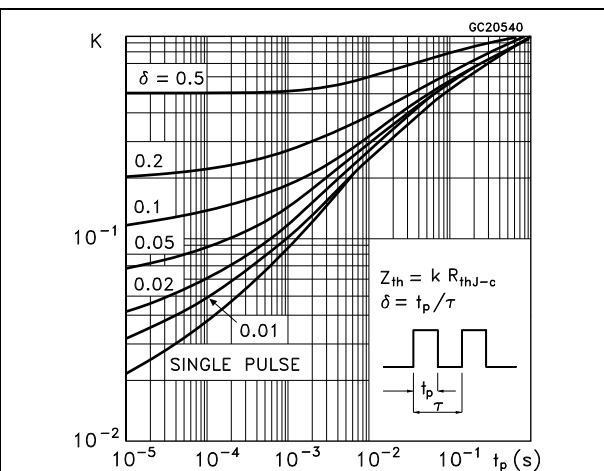


Figure 4. Safe operating area for TO-220FP

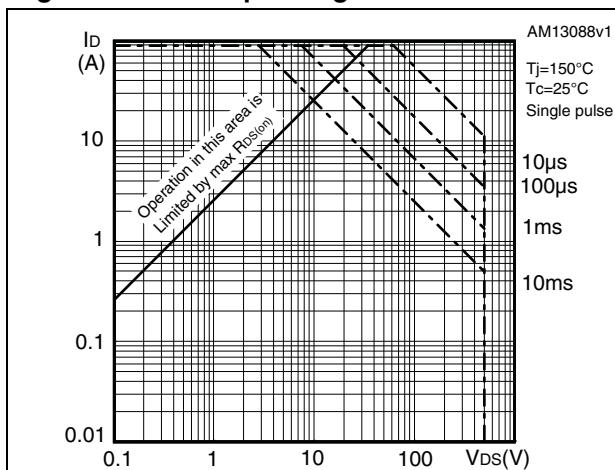


Figure 5. Thermal impedance for TO-220FP

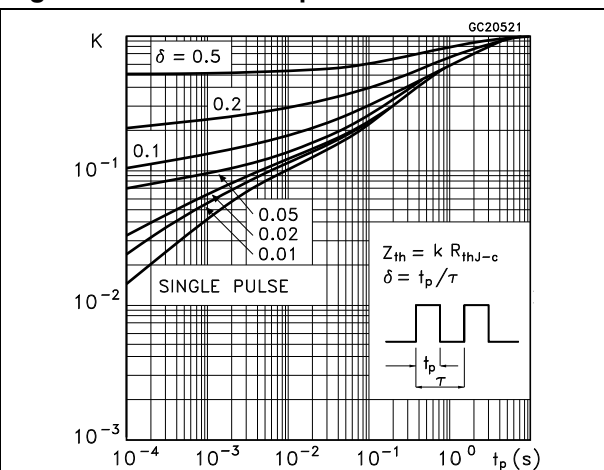


Figure 6. Safe operating area for TO-247

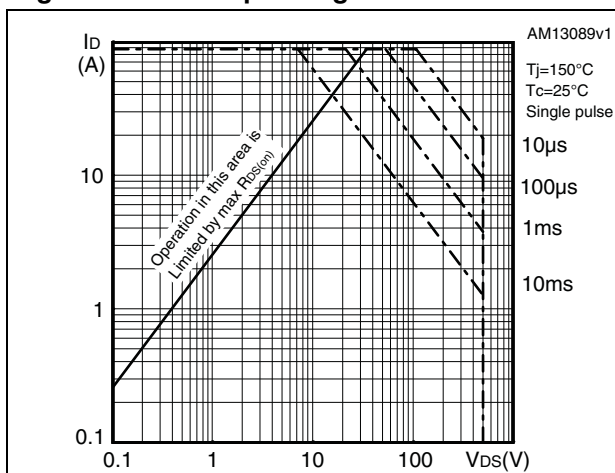


Figure 7. Thermal impedance for TO-247

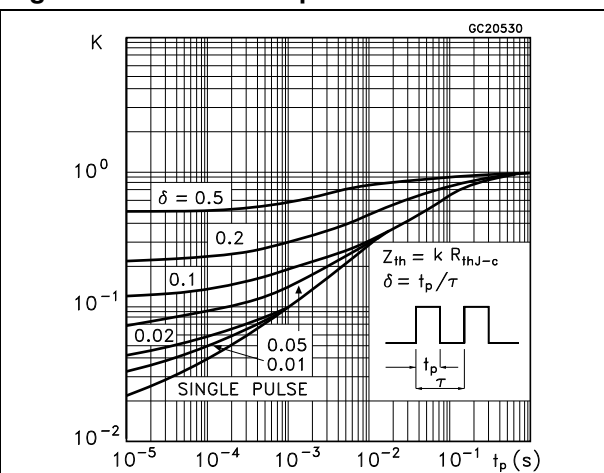


Figure 8. Output characteristics

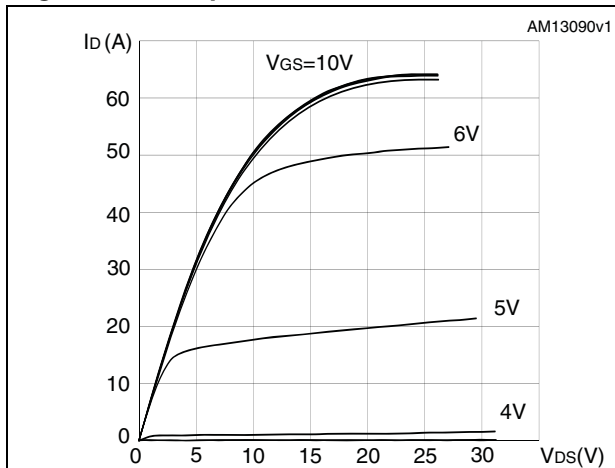


Figure 9. Transfer characteristics

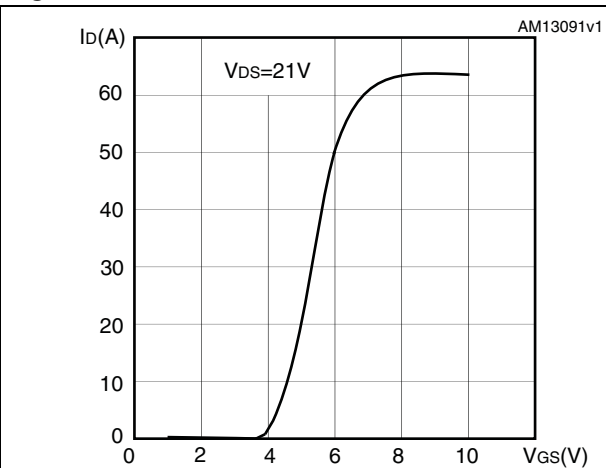


Figure 10. Gate charge vs gate-source voltage

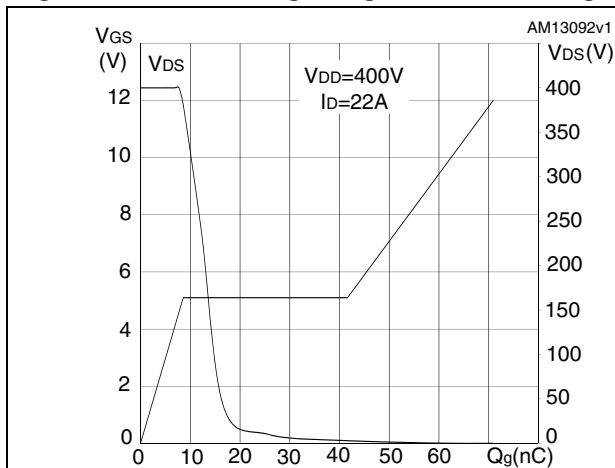


Figure 11. Static drain-source on-resistance

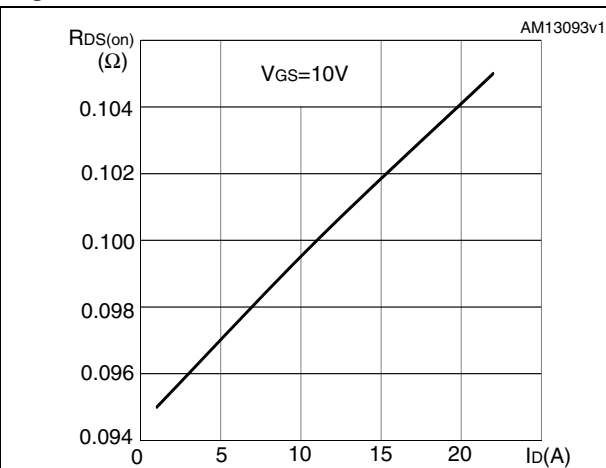


Figure 12. Capacitance variations

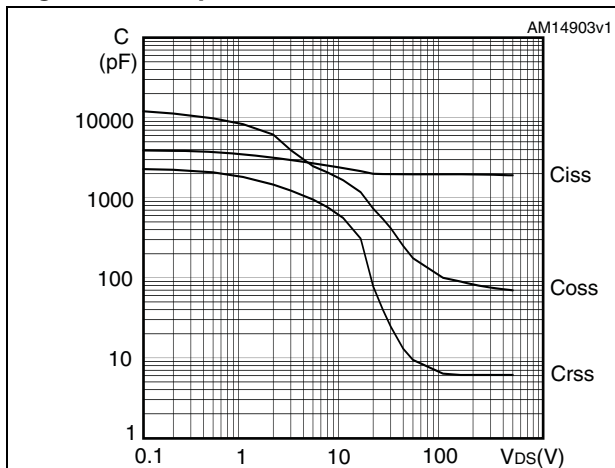


Figure 13. Output capacitance stored energy

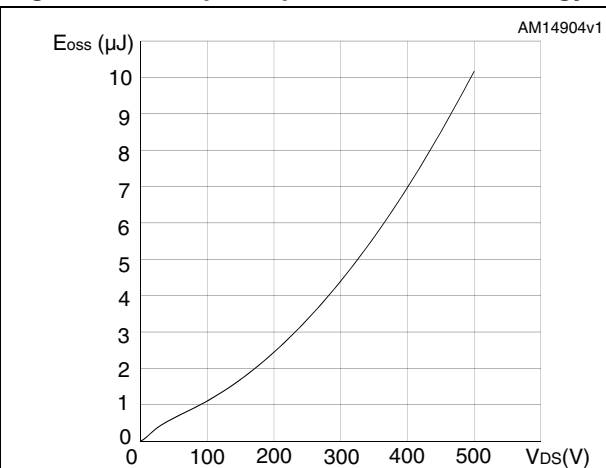


Figure 14. Normalized gate threshold voltage vs temperature

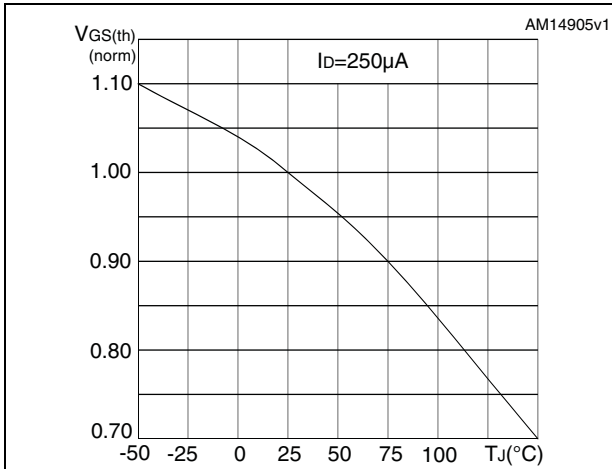


Figure 15. Normalized on-resistance vs temperature

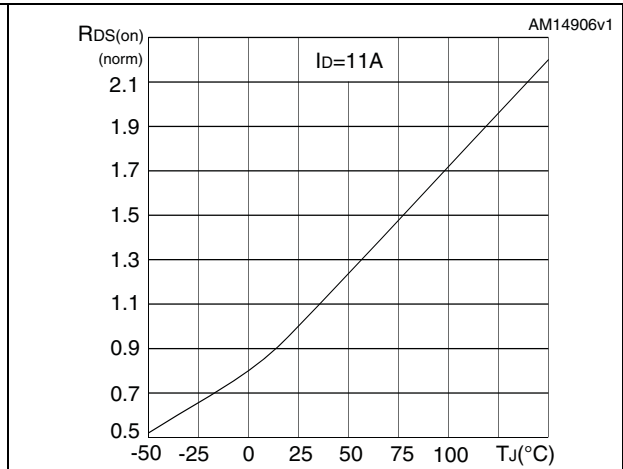


Figure 16. Normalized V_{DS} vs temperature

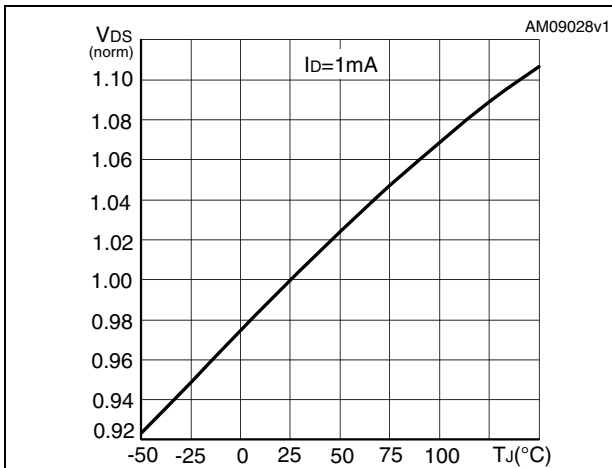
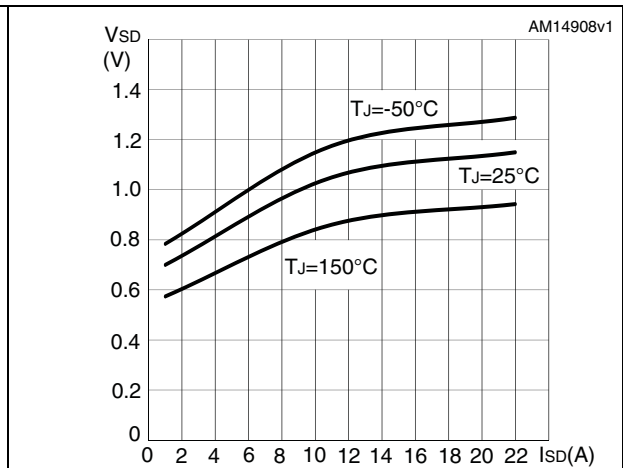


Figure 17. Source-drain diode forward characteristics



3 Test circuits

Figure 18. Switching times test circuit for resistive load

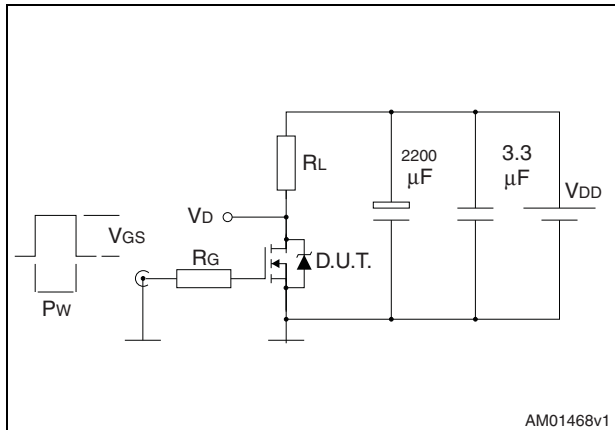


Figure 19. Gate charge test circuit

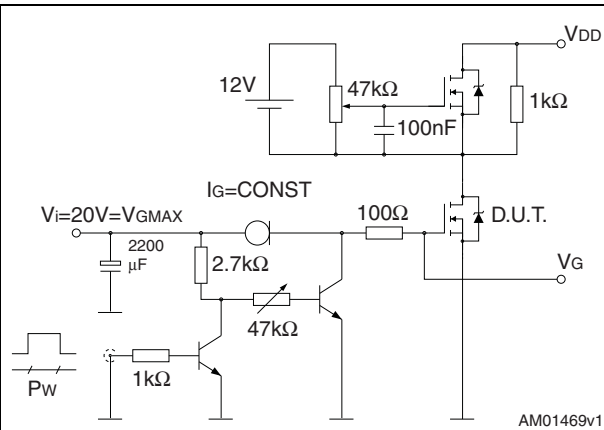


Figure 20. Test circuit for inductive load switching and diode recovery times

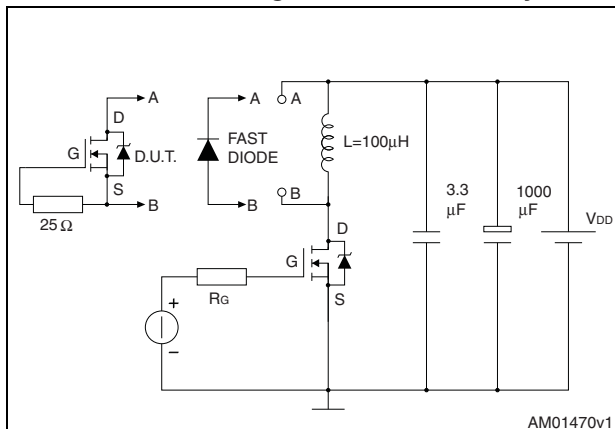


Figure 21. Unclamped inductive load test circuit

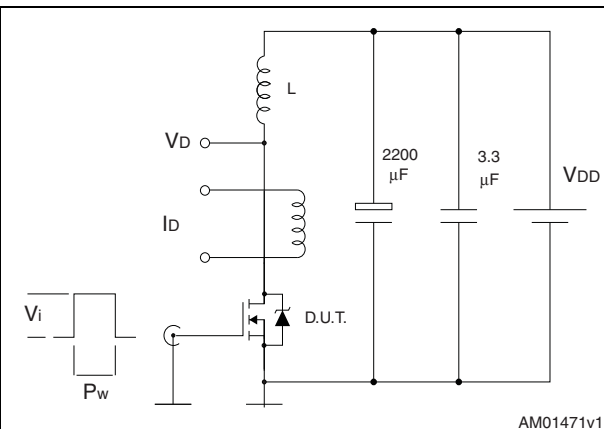


Figure 22. Unclamped inductive waveform

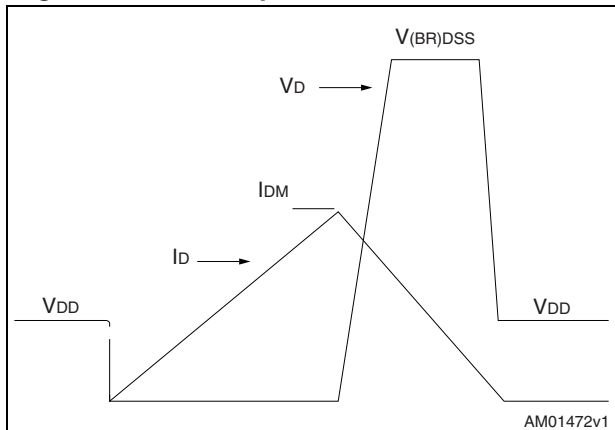
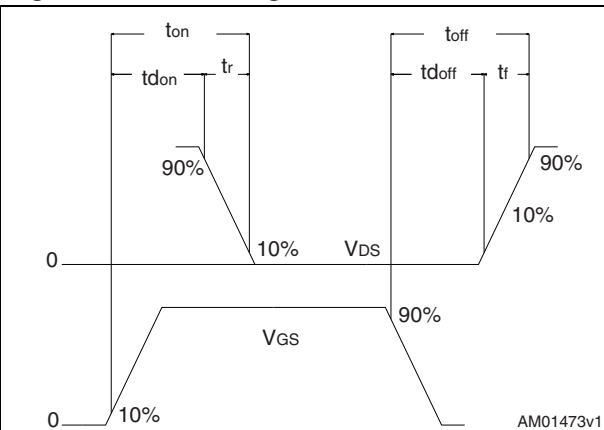


Figure 23. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 7. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 24. D²PAK (TO-263) drawing

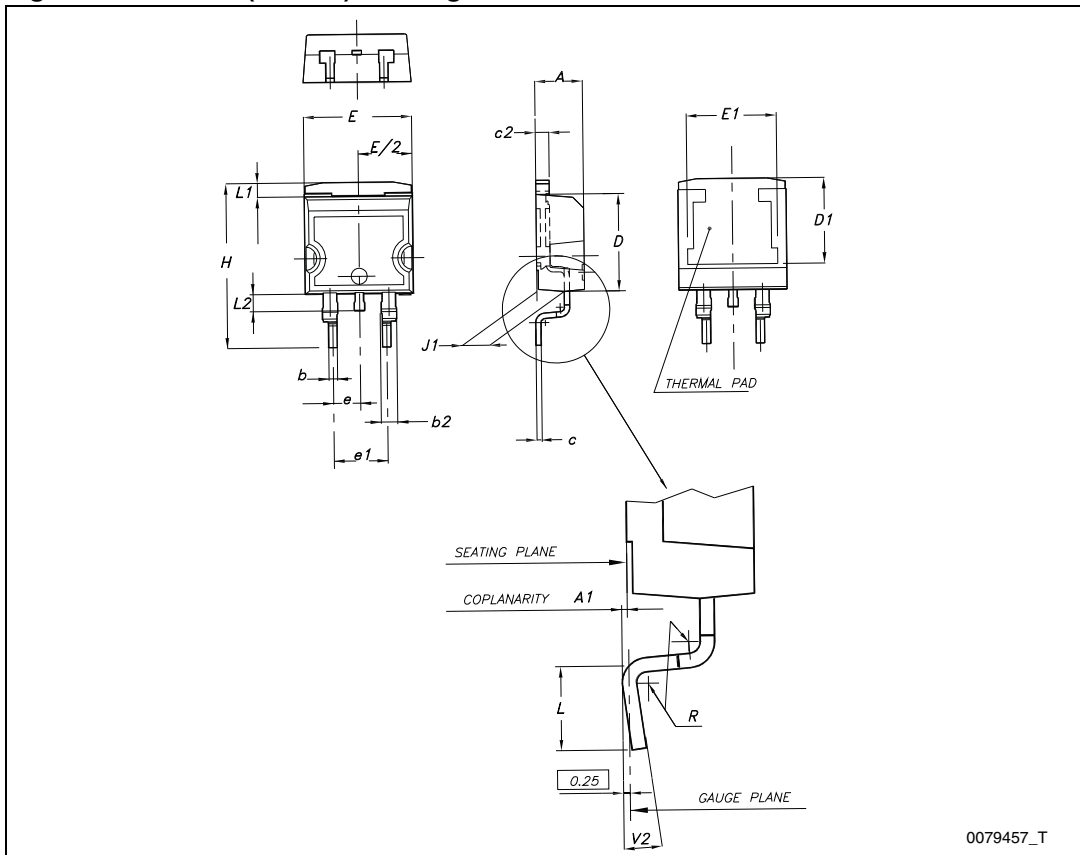
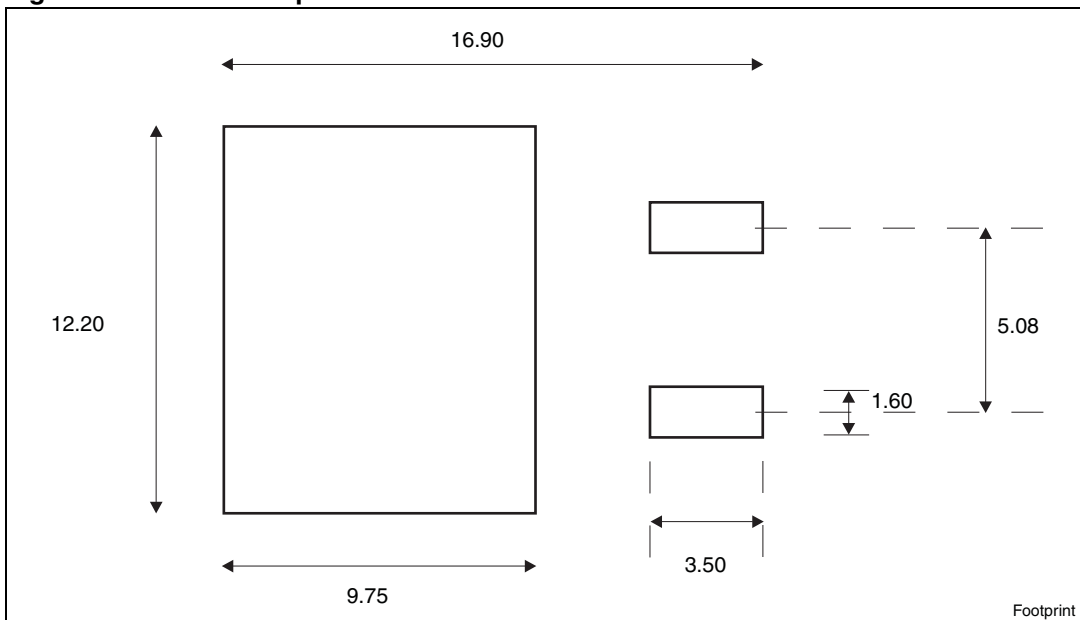


Figure 25. D²PAK footprint^(a)



a. All dimensions are in millimeters

Table 8. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 26. TO-220FP drawing

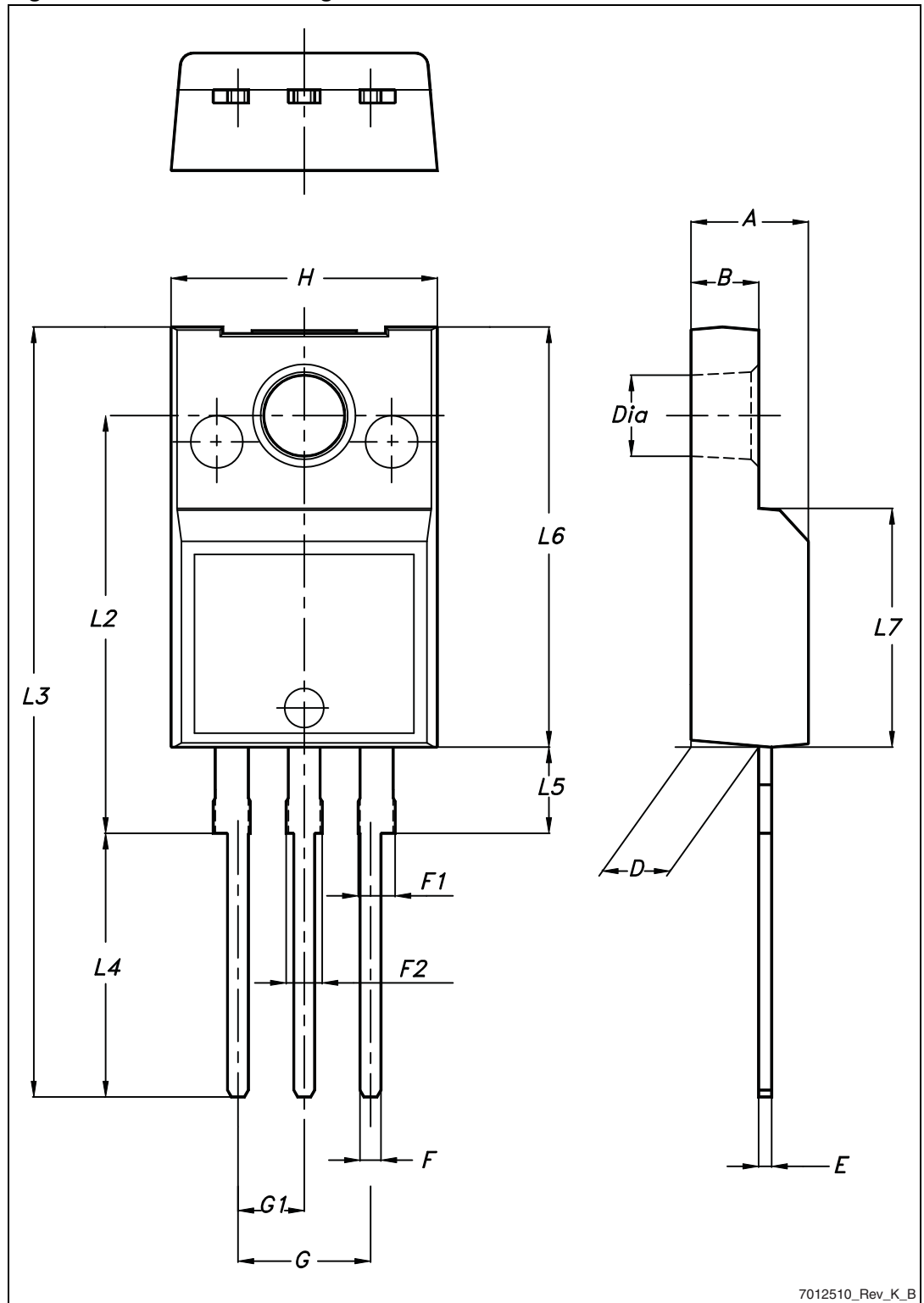


Table 9. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 27. TO-220 type A drawing

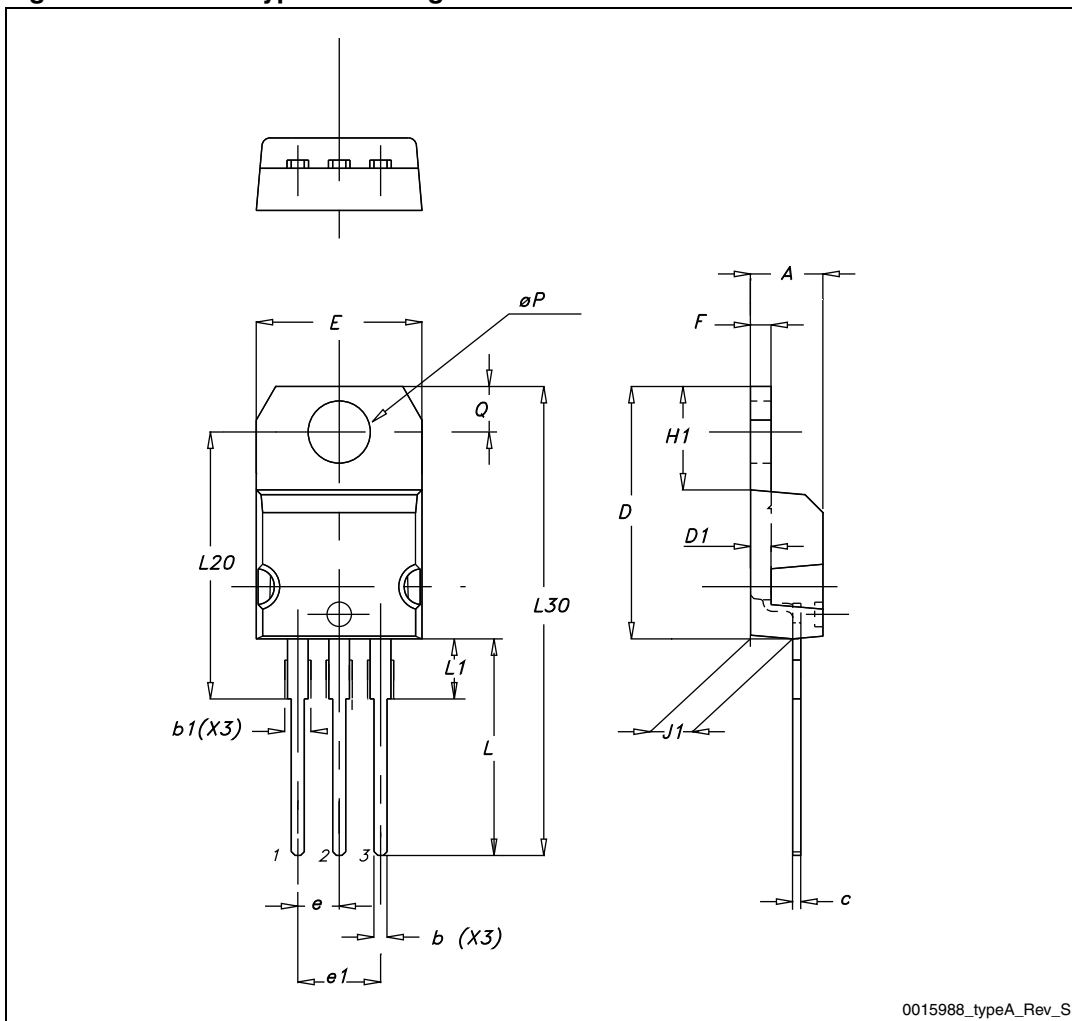
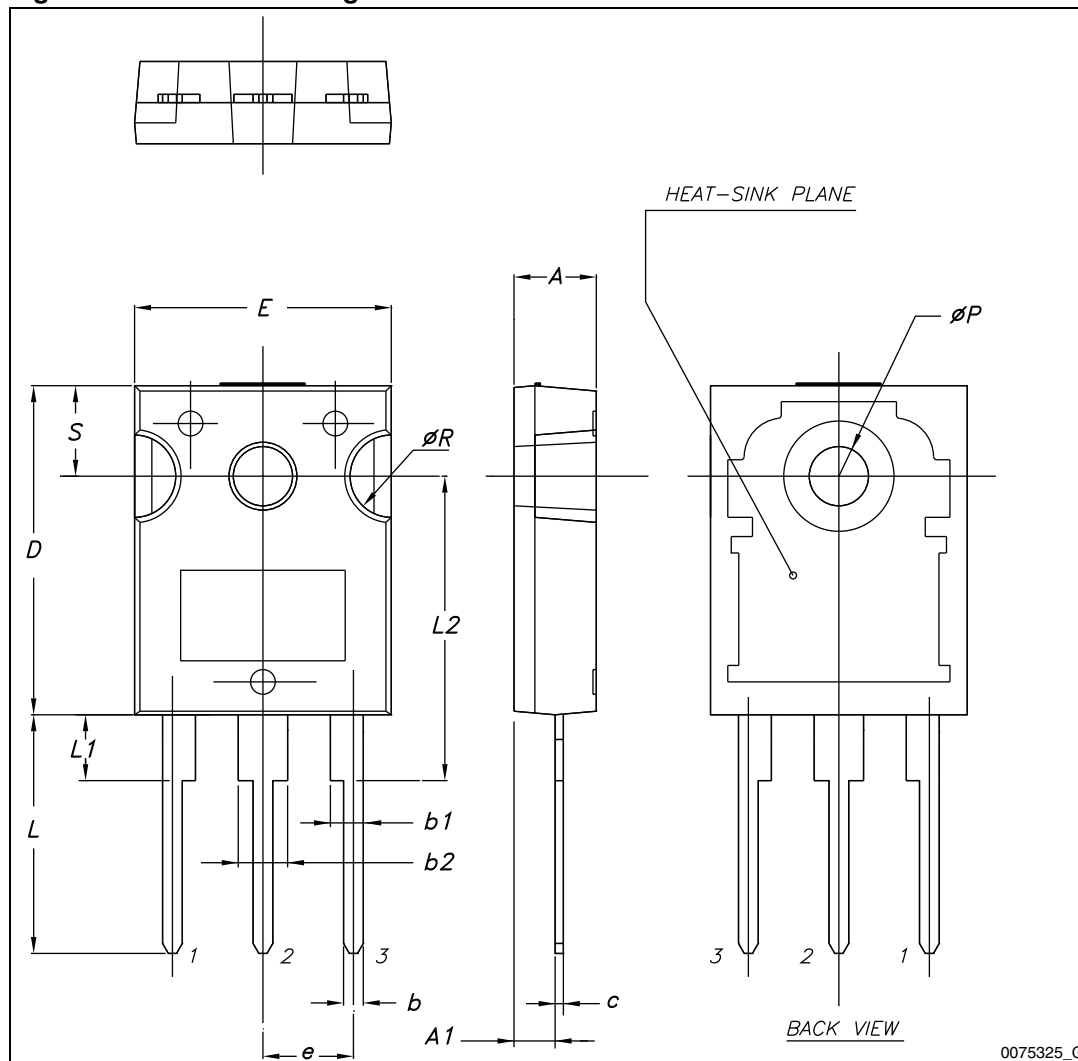


Table 10. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Figure 28. TO-247 drawing

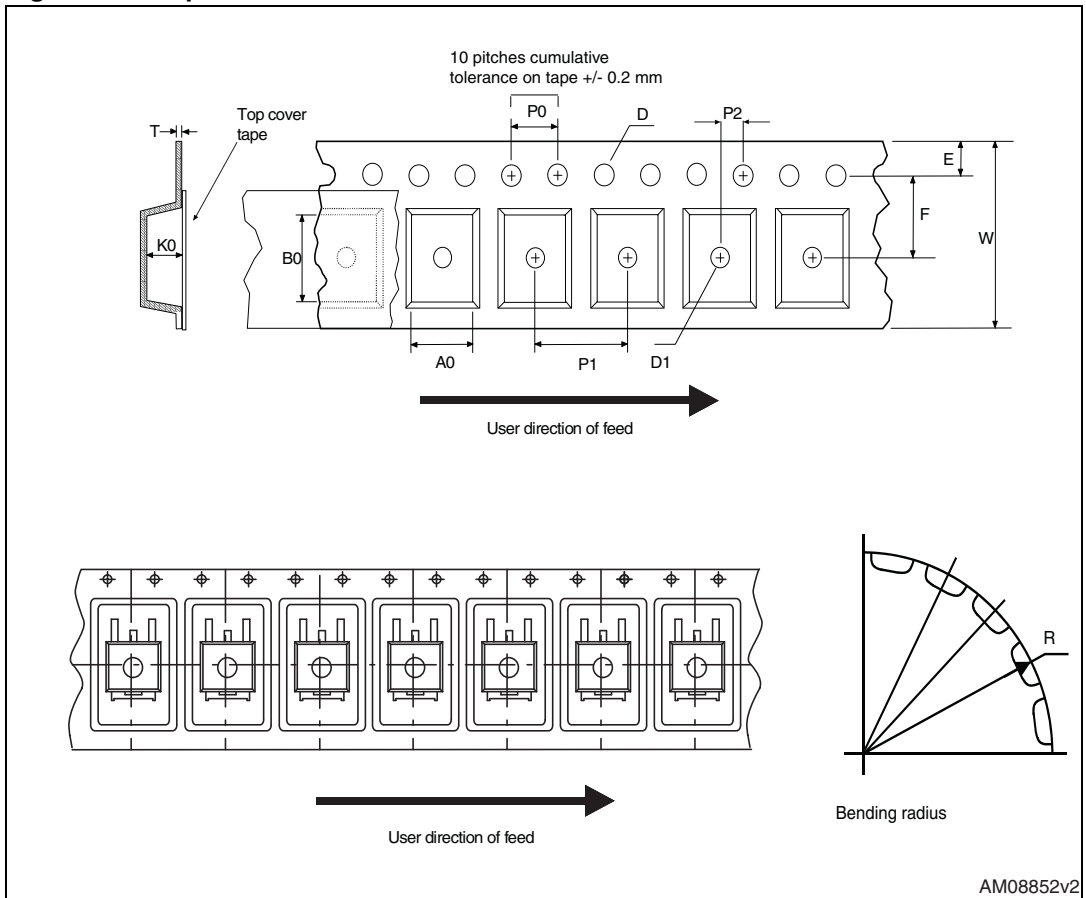


5 Packaging mechanical data

Table 11. D²PAK (TO-263) tape and reel mechanical data

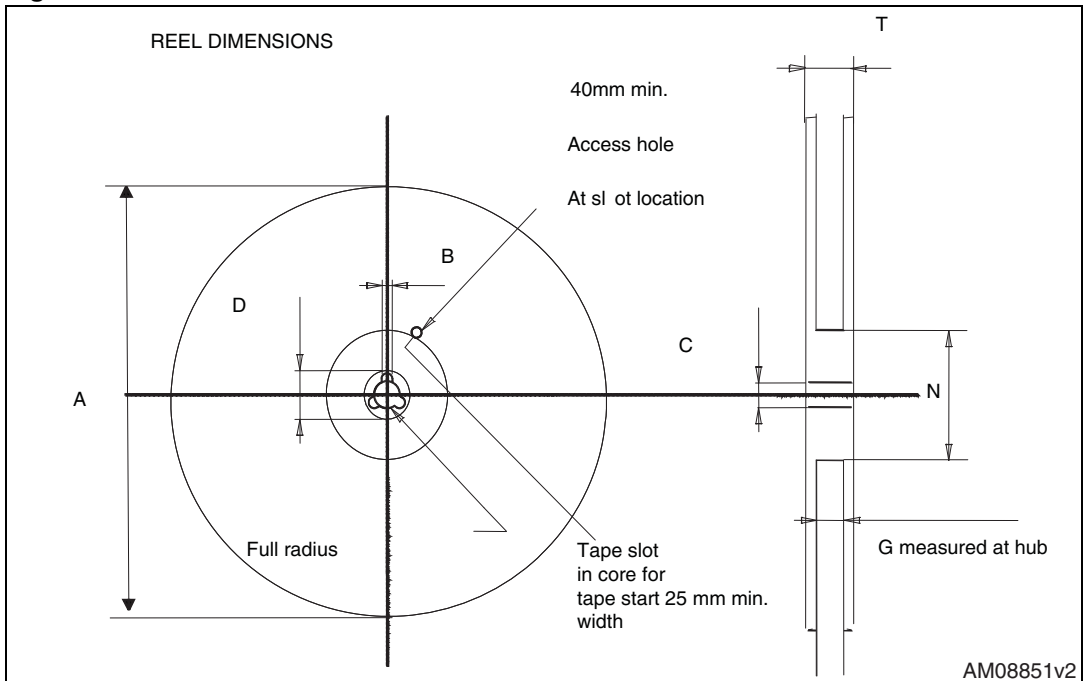
Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 29. Tape



AM08852v2

Figure 30. Reel



AM08851v2

6 Revision history

Table 12. Document revision history

Date	Revision	Changes
01-Aug-2012	1	Initial release.

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- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.

