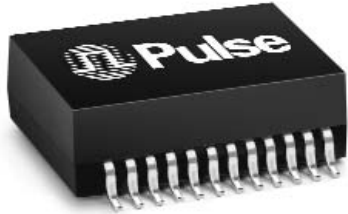




# 10/100BASE-T SINGLE PORT, SMT TRANSFORMER

For Fast Ethernet to Gigabit Ethernet  
Interchangeable Designs



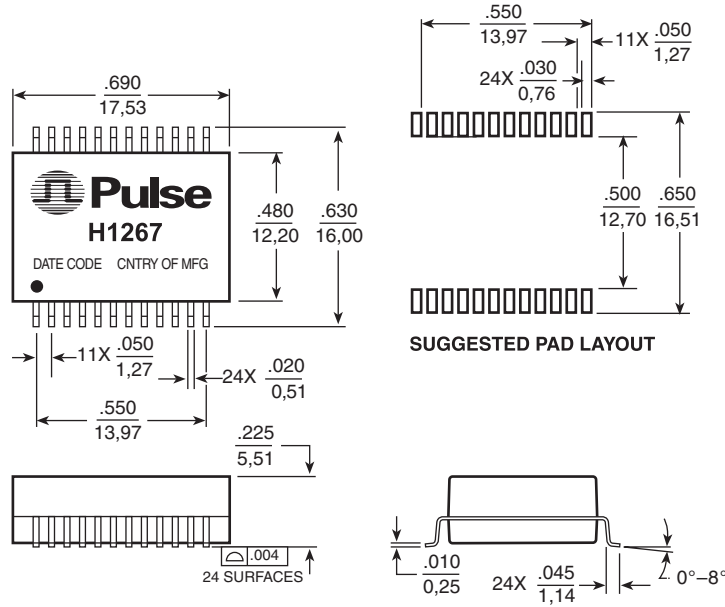
- 
 Meets IEEE802.3 and ANSI X3.263 standards, including 350  $\mu$ H OCL with 8 mA DC bias
- 
 Pin-compatible to Pulse Gigabit Ethernet part numbers H5004 and H5007

**Electrical Specifications @ 25°C — Operating Temperature 0°C to +70°C**

Part Number	Turns Ratio ( $\pm 5\%$ )		Insertion Loss (dB MAX) 100 kHz-100 MHz	Return Loss (dB MIN)			Crosstalk (dB MIN)			Differential to Common Mode Rejection (db MIN)			Hipot (Vrms MIN)
	Receive	Transmit		30 MHz	60 MHz	80 MHz	30 MHz	60 MHz	80 MHz	30 MHz	60 MHz	100 MHz	
H1267	1CT:1CT	1CT:1CT	-1.0	-16	-12	-12	-40	-40	-35	-42	-37	-33	1500

## Mechanical

### H1267



Dimensions:  $\frac{\text{Inches}}{\text{mm}}$

Unless otherwise specified all tolerances are  $\pm \frac{.010}{0.25}$ .

When ordering Tape & Reel packaging add the suffix "T" to the part number, such as "H1267T."

Weight ..... 2.7 grams  
Tape & Reel ..... 300/reel  
Tube ..... 25/tube

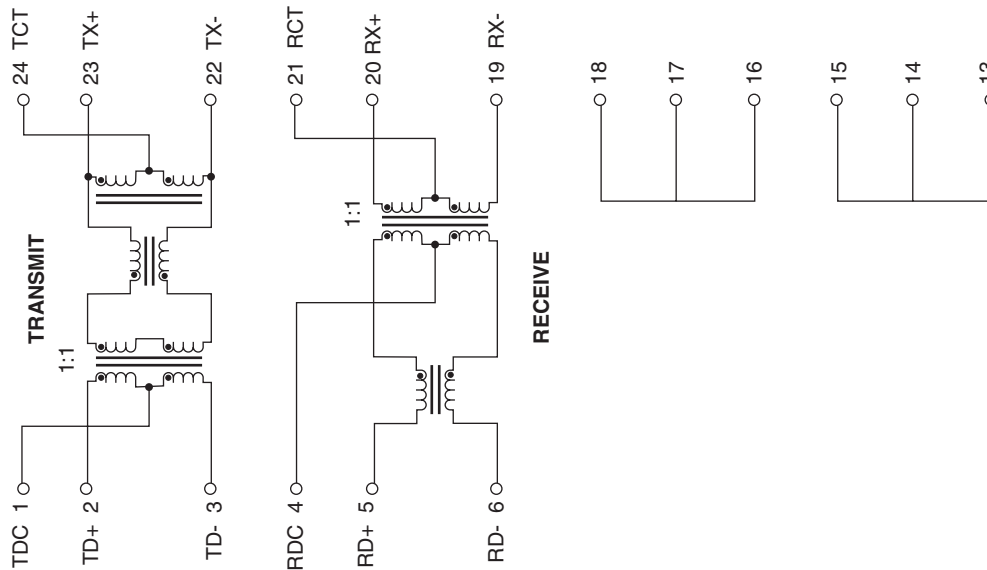
# 10/100BASE-T SINGLE PORT, SMT TRANSFORMER

For Fast Ethernet to Gigabit Ethernet Interchangeable Designs



## Schematic

H1267



## Application Notes

The Fast Ethernet to Gigabit Ethernet interchangeable design is a design concept that allows design engineers to design a network applications board that can support both Fast Ethernet (10/100Base-T) and Gigabit Ethernet (1000Base-T) applications by simply replacing several components without having to re-design the whole board.

Two components that play a part in this design are the Ethernet silicon and the transformer. Both the silicon and the transformer for both 10/100 and gigabit must have footprint compatibility. This footprint compatibility will mean a single board layout for the interface between the Ethernet silicon and the transformer of either 10/100 or gigabit applications.

Presently, if a network design engineer wants to design a 10/100 card, he would have to choose a 10/100 transformer. If the engineer wants to design a gigabit card, he would have to choose a gigabit transformer. This leads to two different designs (board layout) for two different applications.

The objective of interchangeable design is to allow the engineer to utilize the same design (and board layout) for 10/100 and for a gigabit design (and vice versa) with minimal change as possible to the design.

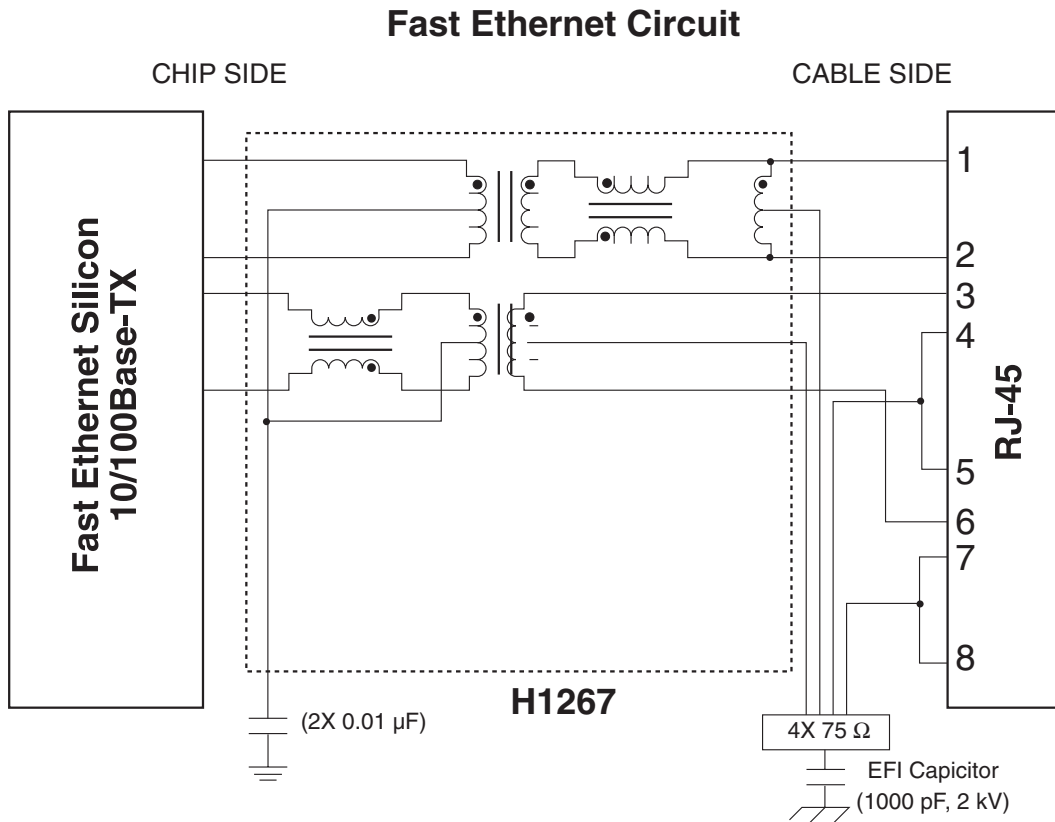
# 10/100BASE-T SINGLE PORT, SMT TRANSFORMER

For Fast Ethernet to Gigabit Ethernet  
Interchangeable Designs



## Application Circuit

**H1267**



The above circuit is a simple interface for a Fast Ethernet transformer connecting to both the Fast Ethernet silicon and the RJ-45 connector. In order to design a gigabit application, simply replace the Fast Ethernet Silicon, the Fast Ethernet transformer and the rest of the passive components with a gigabit ethernet silicon, a gigabit transformer and the rest of the passive components.

It is highly recommended that the cable side Center Taps of each transformer be terminated to 75 Ω resistors and that the four center taps be terminated to an EFI capacitor prior to ground termination.

# 10/100BASE-T SINGLE PORT, SMT TRANSFORMER

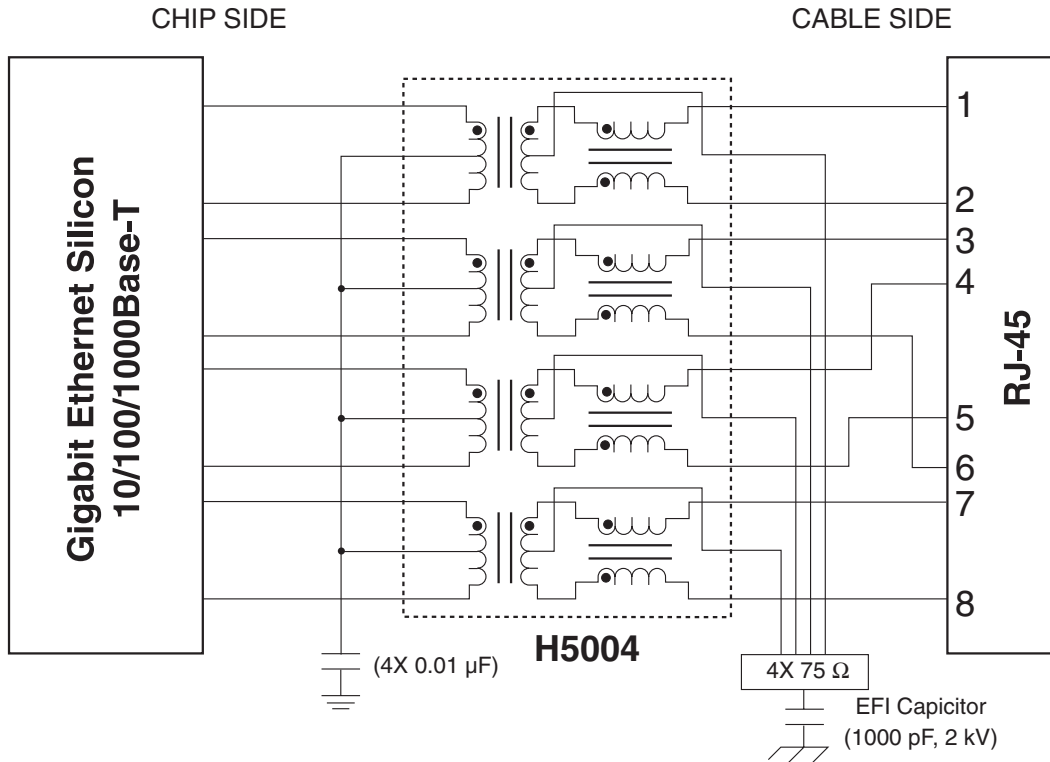
For Fast Ethernet to Gigabit Ethernet  
Interchangeable Designs



## Application Circuit

**H5004**

### Gigabit Circuit



The above circuit is a simple interface for a gigabit transformer connecting to both the Gigabit Ethernet silicon and the RJ-45 connector.

It is highly recommended that the cable side Center Taps of each transformer be terminated to 75  $\Omega$  resistors and that the four center taps be terminated to an EFI capacitor prior to ground termination.

# 10/100BASE-T SINGLE PORT, SMT TRANSFORMER

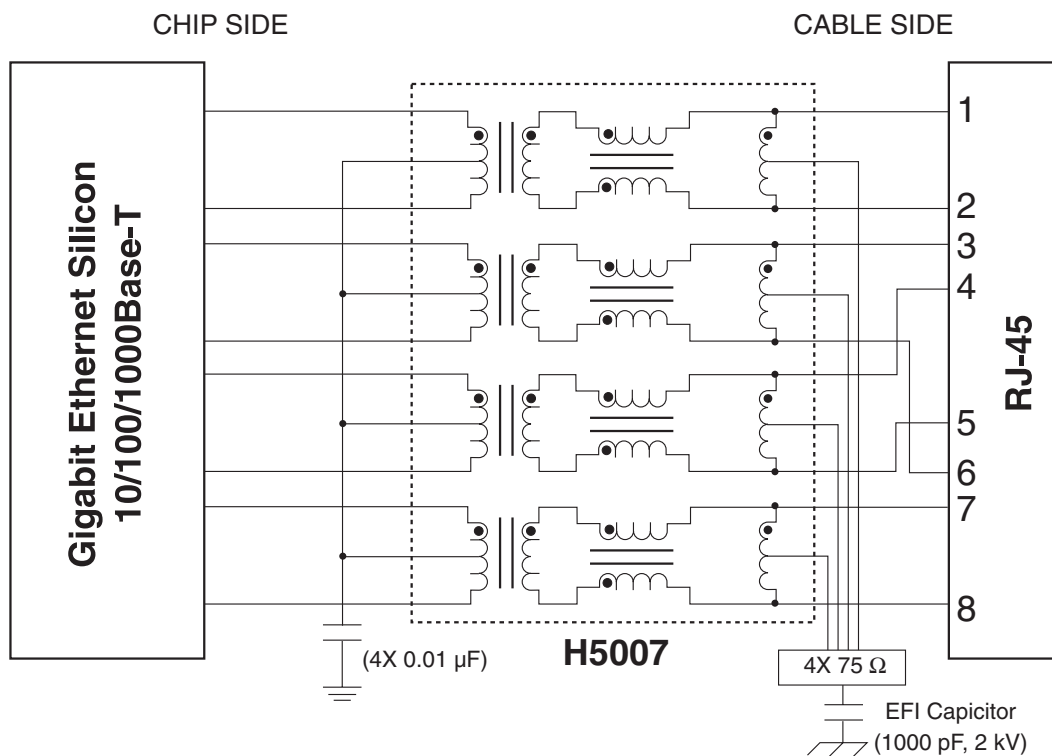
For Fast Ethernet to Gigabit Ethernet  
Interchangeable Designs



## Application Circuit

**H5007**

### Gigabit Circuit



The above circuit is a simple interface for a gigabit transformer connection to both the Gigabit Ethernet silicon and the RJ-45 connector.

It is highly recommended that the cable side Center Taps of each transformer be terminated to 75  $\Omega$  resistors and that the four center taps be terminated to an EFI capacitor prior to ground termination.

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