

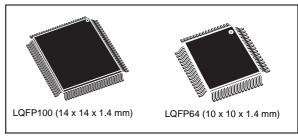
SPC560P34L1, SPC560P34L3 SPC560P40L1, SPC560P40L3

32-bit Power Architecture® based MCU with 320 KB Flash memory and 20 KB RAM for automotive chassis and safety applications

Datasheet - production data

Features

- Up to 64 MHz, single issue, 32-bit CPU core complex (e200z0h)
 - Compliant with Power Architecture[®] embedded category
 - Variable Length Encoding (VLE)
- Memory organization
 - Up to 256 KB on-chip code flash memory with ECC and erase/program controller
 - Additional 64 (4 x 16) KB on-chip data flash memory with ECC for EEPROM emulation
 - Up to 20 KB on-chip SRAM with ECC
- Fail-safe protection
 - Programmable watchdog timer
 - Non-maskable interrupt
 - Fault collection unit
- Nexus Class 1 interface
- Interrupts and events
 - 16-channel eDMA controller
 - 16 priority level controller
 - Up to 25 external interrupts
 - PIT implements four 32-bit timers
 - 120 interrupts are routed via INTC
- General purpose I/Os
 - Individually programmable as input, output or special function
 - 37 on LQFP64
 - 64 on LQFP100
- 1 general purpose eTimer unit
 - 6 timers each with up/down capabilities
 - 16-bit resolution, cascadable counters
 - Quadrature decode with rotation direction flag
 - Double buffer input capture and output compare



- Communications interfaces
 - 2 LINFlex channels (1x Master/Slave, 1x Master only)
 - Up to 3 DSPI channels with automatic chip select generation (up to 8/4/4 chip selects)
 - Up to 2 FlexCAN interface (2.0B Active) with 32 message buffers
 - 1 safety port based on FlexCAN with 32 message buffers and up to 8 Mbit/s at 64 MHz capability usable as second CAN when not used as safety port
- One 10-bit analog-to-digital converter (ADC)
 - Up to 16 input channels (16 on LQFP100 / 12 on LQFP64)
 - Conversion time < 1 µs including sampling time at full precision
 - Programmable Cross Triggering Unit (CTU)
 - 4 analog watchdogs with interrupt capability
- On-chip CAN/UART bootstrap loader with Boot Assist Module (BAM)
- 1 FlexPWM unit: 8 complementary or independent outputs with ADC synchronization signals

Table 1. Device summary

Package	Code flash memory		
1 ackage	192 KB	256 KB	
LQFP100	SPC560P34L3	SPC560P40L3	
LQFP64	SPC560P34L1 SPC560P40L1		

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1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC560P34/40 series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This 32-bit system-on-chip (SoC) automotive microcontroller family is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address chassis applications—specifically, electrical hydraulic power steering (EHPS) and electric power steering (EPS)—as well as airbag applications.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology.

The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

1.3 Device comparison

Table 2 provides a summary of different members of the SPC560P34/SPC560P40 family and their features—relative to full-featured version—to enable a comparison among the family members and an understanding of the range of functionality offered within this family.

Table 2. SPC560P34/SPC560P40 device comparison

Feature	SPC560P34 Full-featured	SPC560P40 Full-featured
Code flash memory (with ECC)	192 KB	256 KB
Data flash memory / EE option (with ECC)	64	КВ
SRAM (with ECC)	12 KB	20 KB
Processor core	32-bit e	200z0h
Instruction set	VLE (variable le	ength encoding)
CPU performance	0–64	MHz
FMPLL (frequency-modulated phase-locked loop) module	1	
INTC (interrupt controller) channels	12	20
PIT (periodic interrupt timer)	1 (with four 3	32-bit timers)

Table 2. SPC560P34/SPC560P40 device comparison (continued)

	Feature	SPC560P34 Full-featured	SPC560P40 Full-featured	
eDMA (enhance	ed direct memory access) channels	1	6	
FlexCAN (cont	roller area network)	1 ⁽¹⁾	2 ^{(1),(2)}	
Safety port		No	Yes (via second FlexCAN module)	
FCU (fault colle	ection unit)	Ye	es	
CTU (cross trig	gering unit)	Yes	Yes	
eTimer		1 (16-bit, 6	channels)	
FlexPWM (puls	se-width modulation) channels	8 (capture capabity not supported)	8 (capture capability not supported)	
Analog-to-digita	al converter (ADC)	1 (10-bit, 1	6 channels)	
LINFlex		2 (1 × Master/Slave, 1 × Master only)	2 (1 × Master/Slave, 1 × Master only)	
DSPI (deserial serial peripheral interface)		2	3	
CRC (cyclic red	dundancy check) unit	Yes		
Junction tempe	erature sensor	No		
JTAG controlle	r	Yes		
Nexus port con	ntroller (NPC)	Yes (Nexus Class 1)		
	Digital power supply ⁽³⁾	3.3 V or 5 V single supply with external transistor		
Supply	Analog power supply	3.3 V or 5 V		
Зирріу	Internal RC oscillator	16 MHz		
	External crystal oscillator	4–40 MHz		
Packages			P100	
Temperature Standard ambient temperature		−40 to 125 °C		

^{1.} Each FlexCAN module has 32 message buffers.

SPC560P34/SPC560P40 is available in two configurations having different features: Full-featured and airbag. *Table 3* shows the main differences between the two versions of the SPC560P40 MCU.

^{2.} One FlexCAN module can act as a safety port with a bit rate as high as 8 Mbit/s at 64 MHz.

^{3.} The different supply voltages vary according to the part number ordered.

Table 3. SPC560P40 device configuration differences

Feature	Configuration		
reature	Airbag	Full-featured	
SRAM (with ECC)	16 KB	20 KB	
FlexCAN (controller area network)	1	2	
Safety port	No	Yes (via second FlexCAN module)	
FlexPWM (pulse-width modulation) channels	No	8 (capture capability not supported)	
CTU (cross triggering unit)	No	Yes	

1.4 Block diagram

Figure 1 shows a top-level block diagram of the SPC560P34/SPC560P40 MCU. *Table 2* summarizes the functions of the blocks.

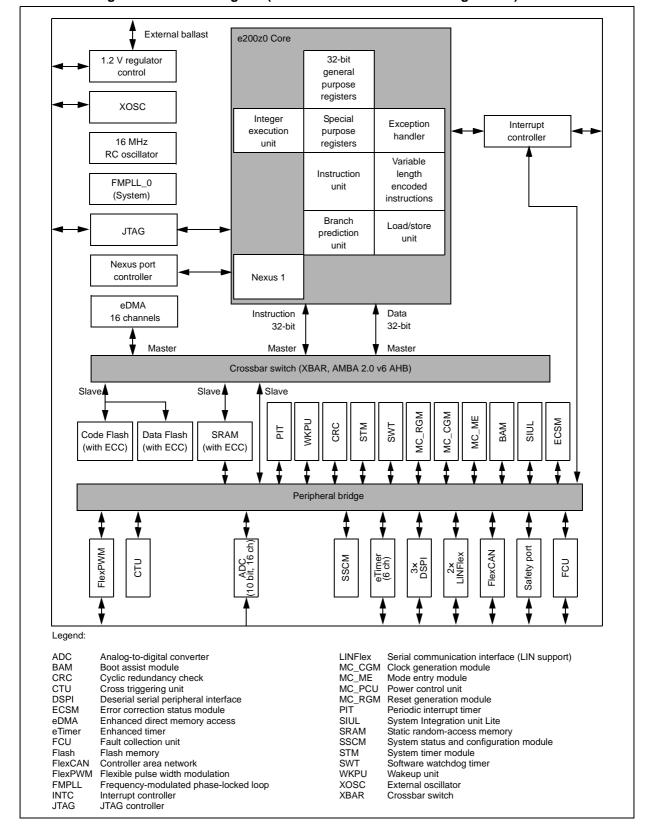


Figure 1. Block diagram (SPC560P40 full-featured configuration)

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Table 4. SPC560P34/SPC560P40 series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 10-bit analog-to-digital converter
Boot assist module (BAM)	Block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Controller area network (FlexCAN)	Supports the standard CAN communications protocol
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports; supports a 32-bit address bus width and a 32-bit data bus width
Cyclic redundancy check (CRC)	CRC checksum generator
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "n" programmable channels
Enhanced timer (eTimer)	Provides enhanced programmable up/down modulo counting
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
External oscillator (XOSC)	Provides an output clock used as input reference for FMPLL_0 or as reference clock for specific modules depending on system needs
Fault collection unit (FCU)	Provides functional safety to the device
Flash memory	Provides non-volatile storage for program code, constants and variables
Frequency-modulated phase- locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Peripheral bridge (PBRIDGE)	Is the interface between the system bus and on-chip peripherals
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU

Table 4. SPC560P34/SPC560P40 series block summary (continued)

Block	Function
Pulse width modulator (FlexPWM)	Contains four PWM submodules, each of which capable of controlling a single half-bridge power stage and two fault input channels
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR ⁽¹⁾ and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	Supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events

^{1.} AUTOSAR: AUTomotive Open System ARchitecture (see www.autosar.org)

1.5 Feature details

1.5.1 High performance e200z0 core processor

The e200z0 Power Architecture core provides the following features:

- High performance e200z0 core processor for managing peripherals and interrupts
- Single issue 4-stage pipeline in-order execution 32-bit Power Architecture CPU
- Harvard architecture
- Variable length encoding (VLE), allowing mixed 16- and 32-bit instructions
 - Results in smaller code size footprint
 - Minimizes impact on performance
- Branch processing acceleration using lookahead instruction buffer
- Load/store unit
 - 1-cycle load latency
 - Misaligned access support
 - No load-to-use pipeline bubbles
- Thirty-two 32-bit general purpose registers (GPRs)
- Separate instruction bus and load/store bus Harvard architecture
- Hardware vectored interrupt support
- Reservation instructions for implementing read-modify-write constructs
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency
- Extensive system development support through Nexus debug port
- Non-maskable interrupt support

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between three master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for two concurrent transactions to occur from any master port to any slave port; but one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port will be stalled until the higher priority master completes its transactions. Requesting masters will be treated with equal priority and will be granted access a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- 3 master ports:
 - e200z0 core complex instruction port
 - e200z0 core complex Load/Store Data port
 - eDMA
- 3 slave ports:
 - Flash memory (Code and Data)
 - SRAM
 - Peripheral bridge
- 32-bit internal address, 32-bit internal data paths
- Fixed Priority Arbitration based on Port Master
- Temporary dynamic priority elevation of masters

1.5.3 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels.

The eDMA module provides the following features:

- 16 channels support independent 8-, 16- or 32-bit single value or block transfers
- Supports variable-sized queues and circular queues
- Source and destination address registers are independently configured to either postincrement or to remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, DSPIs, ADC, FlexPWM, eTimer and CTU
- Programmable DMA channel multiplexer allows assignment of any DMA source to any available DMA channel with as many as 30 request sources
- eDMA abort operation through software

1.5.4 Flash memory

The SPC560P34/SPC560P40 provides 320 KB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash memory module is interfaced to the system bus by a dedicated flash memory controller. It supports a 32-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit wide prefetch buffers. Prefetch buffer hits allow no-wait responses. Normal flash memory array accesses are registered and are forwarded to the system bus on the following cycle, incurring two wait-states.

The flash memory module provides the following features:

- As much as 320 KB flash memory
 - 6 blocks (32 KB + 2x16 KB + 32 KB + 32 KB + 128 KB) code flash memory
 - 4 blocks (16 KB + 16 KB + 16 KB + 16 KB) data flash memory
 - Full Read-While-Write (RWW) capability between code flash memory and data flash memory
- Four 128-bit wide prefetch buffers to provide single cycle in-line accesses (prefetch buffers can be configured to prefetch code or data or both)
- Typical flash memory access time: no wait-state for buffer hits, 2 wait-states for page buffer miss at 64 MHz
- Hardware managed flash memory writes handled by 32-bit RISC Krypton engine
- Hardware and software configurable read and write access protections on a per-master basis
- Configurable access timing allowing use in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (up to 31 additional cycles) allowing use for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page sizes
 - Code flash memory: 128 bits (4 words)
 - Data flash memory: 32 bits (1 word)
- ECC with single-bit correction, double-bit detection for data integrity
 - Code flash memory: 64-bit ECC
 - Data flash memory: 32-bit ECC
- Embedded hardware program and erase algorithm
- Erase suspend and program abort
- Censorship protection scheme to prevent flash memory content visibility
- Hardware support for EEPROM emulation

1.5.5 Static random access memory (SRAM)

The SPC560P34/SPC560P40 SRAM module provides up to 20 KB of general-purpose memory.

The SRAM module provides the following features:

- Supports read/write accesses mapped to the SRAM from any master
- Up to 20 KB general purpose SRAM
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- Typical SRAM access time: no wait-state for reads and 32-bit writes; 1 wait-state for 8and 16-bit writes if back-to-back with a read to same memory block

1.5.6 Interrupt controller (INTC)

The interrupt controller (INTC) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC handles 128 selectable-priority interrupt sources.

For high-priority interrupt requests, the time from the assertion of the interrupt request by the peripheral to the execution of the interrupt service routine (ISR) by the processor has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR has to be executed. It also provides a wide number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol (PCP) for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the same resource can not preempt each other.

The INTC provides the following features:

- Unique 9-bit vector for each separate interrupt source
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority: modifying the priority can be used to implement the priority ceiling protocol for accessing shared resources.
- 1 external high priority interrupt (NMI) directly accessing the main core and I/O processor (IOP) critical interrupt mechanism

1.5.7 System status and configuration module (SSCM)

The system status and configuration module (SSCM) provides central device functionality.

The SSCM includes these features:

- System configuration and status
 - Memory sizes/status
 - Device mode and security status
 - Determine boot vector
 - Search code flash for bootable sector
 - DMA status
- Debug status port enable and selection
- Bus and peripheral abort enable/disable

1.5.8 System clocks and clock generation

The following list summarizes the system clock and clock generation on the SPC560P34/SPC560P40:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider (÷1, ÷2, ÷4, ÷8)
- FlexPWM module and eTimer module running at the same frequency as the e200z0h core
- Internal 16 MHz RC oscillator for rapid start-up and safe mode: supports frequency trimming by user application

1.5.9 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4–40 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable.

The FMPLL has the following major features:

- Input clock frequency: 4–40 MHz
- Maximum output frequency: 64 MHz
- Voltage controlled oscillator (VCO)—frequency 256–512 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the FMPLL to relock
- Frequency-modulated PLL
 - Modulation enabled/disabled through software
 - Triangle wave modulation
- Programmable modulation depth (±0.25% to ±4% deviation from center frequency): programmable modulation frequency dependent on reference frequency
- Self-clocked mode (SCM) operation

1.5.10 Main oscillator

The main oscillator provides these features:

- Input frequency range: 4–40 MHz
- Crystal input mode or oscillator input mode
- PLL reference

1.5.11 Internal RC oscillator

This device has an RC ladder phase-shift oscillator. The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared by the stable bandgap reference voltage.

The RC oscillator provides these features:

- Nominal frequency 16 MHz
- ±5% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the PLL
- RC oscillator is used as the default system clock during startup

1.5.12 Periodic interrupt timer (PIT)

The PIT module implements these features:

- 4 general-purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- Each channel usable as trigger for a DMA request

1.5.13 System timer module (STM)

The STM implements these features:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.5.14 Software watchdog timer (SWT)

The SWT has the following features:

- 32-bit time-out register to set the time-out period
- Programmable selection of window mode or regular servicing
- Programmable selection of reset or interrupt on an initial time-out
- Master access protection
- Hard and soft configuration lock bits
- Reset configuration inputs allow timer to be enabled out of reset

1.5.15 Fault collection unit (FCU)

The FCU provides an independent fault reporting mechanism even if the CPU is malfunctioning.

The FCU module has the following features:

- FCU status register reporting the device status
- Continuous monitoring of critical fault signals
- User selection of critical signals from different fault sources inside the device
- Critical fault events trigger 2 external pins (user selected signal protocol) that can be used externally to reset the device and/or other circuitry (for example, a safety relay)
- Faults are latched into a register

1.5.16 System integration unit – Lite (SIUL)

The SPC560P34/SPC560P40 SIUL controls MCU pad configuration, external interrupt, general purpose I/O (GPIO), and internal peripheral multiplexing.

The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIUL provides the following features:

- Centralized general purpose input output (GPIO) control of up to 49 input/output pins and 16 analog input-only pads (package dependent)
- All GPIO pins can be independently configured to support pull-up, pull-down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins, except ADC channels, can be alternatively configured as both general purpose input or output pins
- ADC channels support alternative configuration as general purpose inputs
- Direct readback of the pin value is supported on all pins through the SIUL
- Configurable digital input filter that can be applied to some general purpose input pins for noise elimination
- Up to 4 internal functions can be multiplexed onto 1 pin

1.5.17 Boot and censorship

Different booting modes are available in the SPC560P34/SPC560P40: booting from internal flash memory and booting via a serial link.

The default booting scheme uses the internal flash memory (an internal pull-down resistor is used to select this mode). Optionally, the user can boot via FlexCAN or LINFlex (using the boot assist module software).

A censorship scheme is provided to protect the content of the flash memory and offer increased security for the entire device.

A password mechanism is designed to grant the legitimate user access to the non-volatile memory.

Boot assist module (BAM)

The BAM is a block of read-only memory that is programmed once and is identical for all SPC560Pxx devices that are based on the e200z0h core. The BAM program is executed every time the device is powered on if the alternate boot mode has been selected by the user.

The BAM provides the following features:

- Serial bootloading via FlexCAN or LINFlex
- Ability to accept a password via the used serial communication channel to grant the legitimate user access to the non-volatile memory

1.5.18 Error correction status module (ECSM)

The ECSM provides a myriad of miscellaneous control functions regarding program-visible information about the platform configuration and revision levels, a reset status register, a software watchdog timer, wakeup control for exiting sleep modes, and information on

platform memory errors reported by error-correcting codes and/or generic access error information for certain processor cores.

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

- Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
- For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the SPC560P34/SPC560P40.

The sources of the ECC errors are:

- Flash memory
- SRAM

1.5.19 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Write buffering for peripherals
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.20 Controller area network (FlexCAN)

The SPC560P34/SPC560P40 MCU contains one controller area network (FlexCAN) module. This module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module contains 32 message buffers.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, version 2.0B
 - Standard data and remote frames
 - Extended data and remote frames
 - Up to 8-bytes data length
 - Programmable bit rate up to 1 Mbit/s
- 32 message buffers of up to 8-bytes data length
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
 - Supports configuration of multiple mailboxes to form message queues of scalable depth
 - Arbitration scheme according to message ID or message buffer number
 - Internal arbitration to guarantee no inner or outer priority inversion
 - Transmit abort procedure and notification
- Receive features
 - Individual programmable filters for each mailbox
 - 8 mailboxes configurable as a 6-entry receive FIFO
 - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
 - System clock
 - Direct oscillator clock to avoid PLL jitter

1.5.21 Safety port (FlexCAN)

The SPC560P34/SPC560P40 MCU has a second CAN controller synthesized to run at high bit rates to be used as a safety port. The CAN module of the safety port provides the following features:

- Identical to the FlexCAN module
- Bit rate up to 8 Mbit/s at 64 MHz CPU clock using direct connection between CAN modules (no physical transceiver required)
- 32 message buffers of up to 8-bytes data length
- Can be used as a second independent CAN module

1.5.22 Serial communication interface module (LINFlex)

The LINFlex (local interconnect network flexible) on the SPC560P34/SPC560P40 features the following:

- Supports LIN Master mode (both instances), LIN Slave mode (only one instance) and UART mode
- LIN state machine compliant to LIN1.3, 2.0 and 2.1 specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
 - Autonomous LIN frame handling
 - Message buffer to store Identifier and up to 8 data bytes
 - Supports message length of up to 64 bytes
 - Detection and flagging of LIN errors (sync field, delimiter, ID parity, bit framing, checksum, and time-out)
 - Classic or extended checksum calculation
 - Configurable Break duration of up to 36-bit times
 - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
 - Diagnostic features: Loop back; Self Test; LIN bus stuck dominant detection
 - Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features:
 - Autonomous LIN header handling
 - Autonomous LIN response handling
 - Optional discarding of irrelevant LIN responses using ID filter
- UART mode:
 - Full-duplex operation
 - Standard non return-to-zero (NRZ) mark/space format
 - Data buffers with 4-byte receive, 4-byte transmit
 - Configurable word length (8-bit or 9-bit words)
 - Error detection and flagging
 - Parity, Noise and Framing errors
 - Interrupt-driven operation with four interrupt sources
 - Separate transmitter and receiver CPU interrupt sources
 - 16-bit programmable baud-rate modulus counter and 16-bit fractional
 - 2 receiver wake-up methods

1.5.23 Deserial serial peripheral interface (DSPI)

The deserial serial peripheral interface (DSPI) module provides a synchronous serial interface for communication between the SPC560P34/SPC560P40 MCU and external devices.

The DSPI modules provide these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- Up to 8 chip select lines available:
 - 8 on DSPI_0
 - 4 each on DSPI_1 and DSPI_2
- 8 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for deglitching
- FIFOs for buffering up to 4 transfers on the transmit and receive side
- Queueing operation possible through use of the I/O processor or eDMA
- General purpose I/O functionality on pins when not used for SPI

1.5.24 Pulse width modulator (FlexPWM)

The pulse width modulator module (PWM) contains four PWM submodules each of which is set up to control a single half-bridge power stage. There are also three fault channels.

This PWM is capable of controlling most motor types: AC induction motors (ACIM), permanent magnet AC motors (PMAC), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

The FlexPWM block implements the following features:

- 16-bit resolution for center, edge-aligned, and asymmetrical PWMs
- Clock frequency same as that used for e200z0h core
- PWM outputs can operate as complementary pairs or independent channels
- Can accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
 - Integral reload rates from 1 to 16
 - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Write protection for critical registers
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software-control for each PWM output
- All outputs can be programmed to change simultaneously via a "Force Out" event
- PWMX pin can optionally output a third PWM signal from each submodule
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual-edge capture functionality
- eDMA support with automatic reload
- 2 fault inputs
- Capture capability for PWMA, PWMB, and PWMX channels not supported

1.5.25 eTimer

The SPC560P34/SPC560P40 includes one eTimer module which provides six 16-bit general purpose up/down timer/counter units with the following features:

- Clock frequency same as that used for the e200z0h core
- Individual channel capability
 - Input capture trigger
 - Output compare
 - Double buffer (to capture rising edge and falling edge)
 - Separate prescaler for each counter
 - Selectable clock source
 - 0–100% pulse measurement
 - Rotation direction flag (quad decoder mode)
- Maximum count rate
 - External event counting: max. count rate = peripheral clock/2
 - Internal clock counting: max. count rate = peripheral clock
- Counters are:
 - Cascadable
 - Preloadable
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Pins available as GPIO when timer functionality not in use

1.5.26 Analog-to-digital converter (ADC) module

The ADC module provides the following features:

Analog part:

- 1 on-chip analog-to-digital converter
 - 10-bit AD resolution
 - 1 sample and hold unit
 - Conversion time, including sampling time, less than 1 μ s (at full precision)
 - Typical sampling time is 150 ns minimum (at full precision)
 - DNL/INL ±1 LSB
 - TUE < 1.5 LSB
 - Single-ended input signal up to 3.3 V/5.0 V
 - 3.3 V/5.0 V input reference voltage
 - ADC and its reference can be supplied with a voltage independent from V_{DDIO}
 - ADC supply can be equal or higher than V_{DDIO}
 - ADC supply and ADC reference are not independent from each other (both internally bonded to same pad)
 - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles

Digital part:

- 16 input channels
- 4 analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location
- 2 modes of operation: Motor Control mode or Regular mode
- Regular mode features
 - Register based interface with the CPU: control register, status register and 1 result register per channel
 - ADC state machine managing 3 request flows: regular command, hardware injected command and software injected command
 - Selectable priority between software and hardware injected commands
 - DMA compatible interface
- CTU-controlled mode features
 - Triggered mode only
 - 4 independent result queues (1x16 entries, 2x8 entries, 1x4 entries)
 - Result alignment circuitry (left justified and right justified)
 - 32-bit read mode allows to have channel ID on one of the 16-bit part
 - DMA compatible interfaces

1.5.27 Cross triggering unit (CTU)

The cross triggering unit allows automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

It implements the following features:

- Double buffered trigger generation unit with up to 8 independent triggers generated from external triggers
- Trigger generation unit configurable in sequential mode or in triggered mode
- Each trigger can be appropriately delayed to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with up to 24 ADC commands
- Each trigger capable of generating consecutive commands
- ADC conversion command allows to control ADC channel, single or synchronous sampling, independent result queue selection

1.5.28 Nexus Development Interface (NDI)

The NDI (Nexus Development Interface) block is compliant with Nexus Class 1 of the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI block is an integration of several individual Nexus blocks that are selected to provide the development support interface for this device. The NDI block interfaces to the host processor and internal busses to provide development support as per the IEEE-ISTO 5001-2003 Nexus Class 1 standard.



The development support provided includes access to the MCU's internal memory map and access to the processor's internal registers.

The NDI provides the following features:

- Configured via the IEEE 1149.1
- All Nexus port pins operate at V_{DDIO} (no dedicated power supply)
- Nexus Class 1 supports Static debug

1.5.29 Cyclic redundancy check (CRC)

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC module features:

- Support for CRC-16-CCITT (x25 protocol):
 - $x^{16} + x^{12} + x^5 + 1$
- Support for CRC-32 (Ethernet protocol):

$$-x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$$

 Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

1.5.30 IEEE 1149.1 JTAG controller

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

The JTAG controller provides the following features:

- IEEE test access port (TAP) interface 4 pins (TDI, TMS, TCK, TDO)
- Selectable modes of operation include JTAGC/debug or normal system operation.
- 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
 - BYPASS
 - IDCODE
 - EXTEST
 - SAMPLE
 - SAMPLE/PRELOAD
- 5-bit instruction register that supports the additional following public instructions:
 - ACCESS AUX TAP NPC
 - ACCESS_AUX_TAP_ONCE
- 3 test data registers:
 - Bypass register
 - Boundary scan register (size parameterized to support a variety of boundary scan chain lengths)
 - Device identification register
- TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry

1.5.31 On-chip voltage regulator (VREG)

The on-chip voltage regulator module provides the following features:

- Uses external NPN (negative-positive-negative) transistor
- Regulates external 3.3 V/5.0 V down to 1.2 V for the core logic
- Low voltage detection on the internal 1.2 V and I/O voltage 3.3 V

2 Package pinouts and signal descriptions

2.1 Package pinouts

The LQFP pinouts are shown in the following figures. For pin signal descriptions, please refer to *Table 7*.

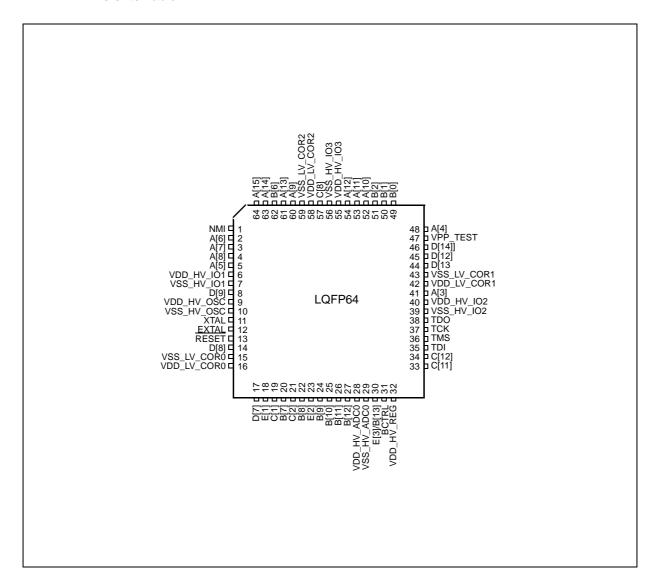


Figure 2. 64-pin LQFP pinout – Full featured configuration (top view)

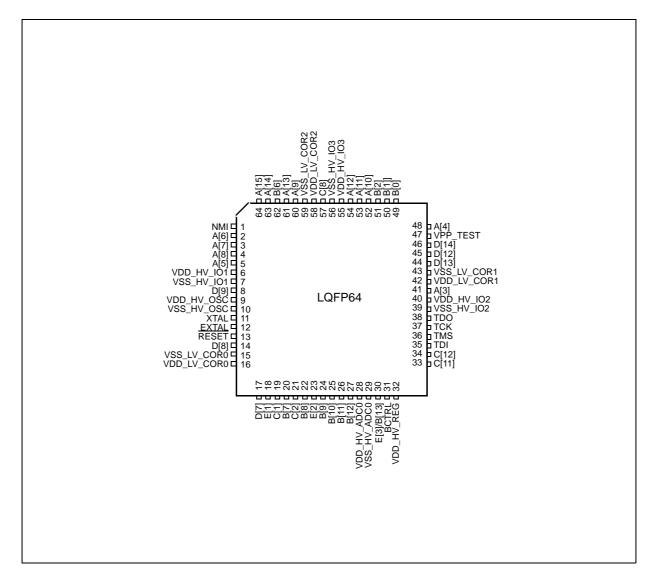


Figure 3. 64-pin LQFP pinout – Airbag configuration (top view)

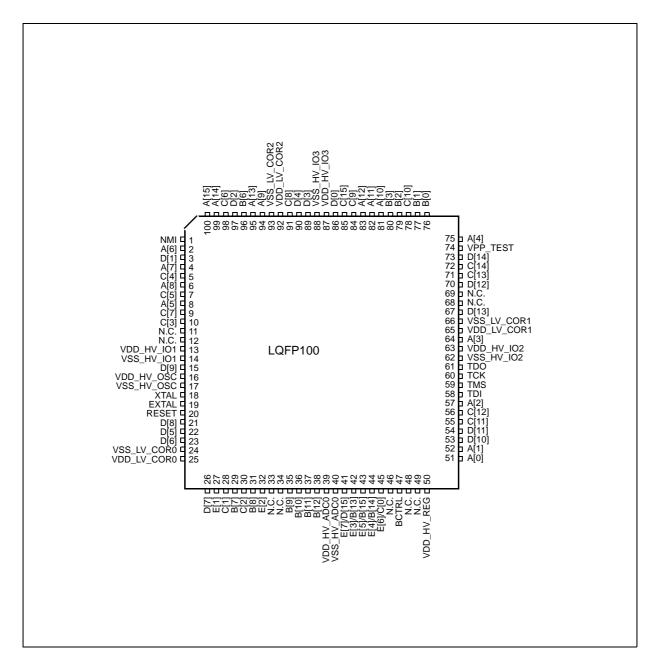


Figure 4. 100-pin LQFP pinout – Full featured configuration (top view)

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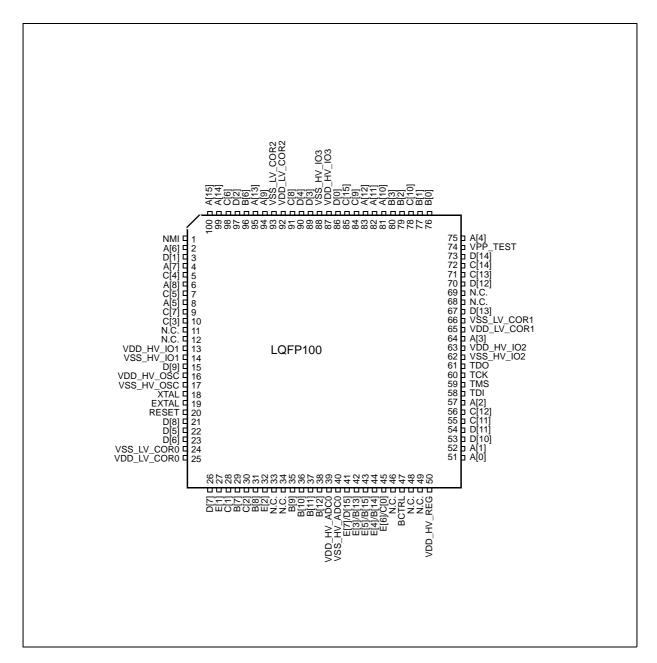


Figure 5. 100-pin LQFP pinout – Airbag configuration (top view)

2.2 Pin description

The following sections provide signal descriptions and related information about the functionality and configuration of the SPC560P34/SPC560P40 devices.

2.2.1 Power supply and reference voltage pins

Table 5 lists the power supply and reference voltage for the SPC560P34/SPC560P40 devices.

Table 5. Supply pins

Supply			in	
Symbol	Description	64-pin	100-pin	
VREG	VREG control and power supply pins. Pins available on 64-pin and 100-pin packa			
BCTRL	Voltage regulator external NPN ballast base control pin	31	47	
V _{DD_HV_REG} (3.3 V or 5.0 V)	Voltage regulator supply voltage	32	50	
ADC_0	reference and supply voltage. Pins available on 64-pin and 100-pin packa	ages		
V _{DD_HV_ADC0} ⁽¹⁾	ADC_0 supply and high reference voltage	28	39	
V _{SS_HV_ADC0}	ADC_0 ground and low reference voltage	29	40	
Powe	r supply pins (3.3 V or 5.0 V). Pins available on 64-pin and 100-pin packa	ges		
V _{DD_HV_IO1}	Input/output supply voltage	6	13	
V _{SS_HV_IO1}	Input/output ground	7	14	
V _{DD_HV_IO2}	Input/output supply voltage and data Flash memory supply voltage	40	63	
V _{SS_HV_IO2}	Input/output ground and Flash memory HV ground	39	62	
V _{DD_HV_IO3}	Input/output supply voltage and code Flash memory supply voltage	55	87	
V _{SS_HV_IO3}	Input/output ground and code Flash memory HV ground	56	88	
V _{DD_HV_OSC}	Crystal oscillator amplifier supply voltage	9	16	
V _{SS_HV_OSC}	Crystal oscillator amplifier ground	10	17	
Р	ower supply pins (1.2 V). Pins available on 64-pin and 100-pin packages			
V _{DD_LV_COR0}	1.2 V supply pins for core logic and PLL. Decoupling capacitor must be connected between these pins and the nearest $V_{\rm SS_LV_COR}$ pin.	16	25	
V _{SS_LV_COR0}	1.2 V supply pins for core logic and PLL. Decoupling capacitor must be connected between these pins and the nearest V _{DD_LV_COR} pin.	15	24	
V _{DD_LV_COR1}	1.2 V supply pins for core logic and data Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{\rm SS_LV_COR}$ pin.	42	65	
V _{SS_LV_COR1}	1.2 V supply pins for core logic and data Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR}$ pin.	43	66	

Table 5. Supply pins (continued)

	Pin			
Symbol	Symbol Description			
V _{DD_LV_COR2}	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected between these pins and the nearest V _{SS_LV_COR} pin.	58	92	
V _{SS_LV_COR2}	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected betwee.n these pins and the nearest $V_{DD_LV_COR}$ pin.	59	93	

Analog supply/ground and high/low reference lines are internally physically separate, but are shorted via a double-bonding connection on V_{DD_HV_ADCx}/V_{SS_HV_ADCx} pins.

2.2.2 System pins

Table 6 and *Table 7* contain information on pin functions for the SPC560P34/SPC560P40 devices. The pins listed in *Table 6* are single-function pins. The pins shown in *Table 7* are multi-function pins, programmable via their respective pad configuration register (PCR) values.

Table 6. System pins

Symbol	Description	Direction	Pad sp	peed ⁽¹⁾	Pin				
Symbol	Description	Direction	SRC = 0	SRC = 1	64-pin	100-pin			
NMI	Non-maskable Interrupt	Input only	Slow	_	1	1			
XTAL	Analog output of the oscillator amplifier circuit—needs to be grounded if oscillator is used in bypass mode	_	_	-	11	18			
EXTAL	Analog input of the oscillator amplifier circuit, when the oscillator is not in bypass mode Analog input for the clock generator when the oscillator is in bypass mode	_	_	_	12	19			
TDI	JTAG test data input	Input only	Slow	_	35	58			
TMS	JTAG state machine control	Input only	Slow	_	36	59			
TCK	JTAG clock	Input only	Slow	_	37	60			
TDO	JTAG test data output	Output only	Slow	Fast	38	61			
Reset pin									
RESET	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	_	13	20			
Test pin									
VPP_TEST	TEST Pin for testing purpose only. To be tied to ground in normal operating mode.		_	_	47	74			

^{1.} SRC values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.

2.2.3 Pin multiplexing

Table 7 defines the pin list and muxing for the SPC560P34/SPC560P40 devices.

Each row of *Table 7* shows all the possible ways of configuring each pin, via alternate functions. The default function assigned to each pin after reset is the ALT0 function.

SPC560P34/SPC560P40 devices provide three main I/O pad types, depending on the associated functions:

- Slow pads are the most common, providing a compromise between transition time and low electromagnetic emission.
- Medium pads provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads provide maximum speed. They are used for improved NEXUS debugging capability.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance. For more information, see "Pad AC Specifications" in the device datasheet.

Table 7. Pin muxing

Port pin	PCR register	Alternate function ^{(1),(2)}	Functions	Peripheral ⁽³⁾ I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin			
						SRC = 0	SRC = 1	64-pin	100-pin	
	Port A (16-bit)									
		ALT0	GPIO[0]	SIUL	I/O					
		ALT1	ETC[0]	eTimer_0	I/O					
A[0]	PCR[0]	ALT2	SCK	DSPI_2	I/O	Slow	Medium		51	
		ALT3	F[0]	FCU_0	0					
		_	EIRQ[0]	SIUL	I					
		ALT0	GPIO[1]	SIUL	I/O		Medium			
		ALT1	ETC[1]	eTimer_0	I/O	Slow				
A[1]	PCR[1]	ALT2	SOUT	DSPI_2	0				52	
		ALT3	F[1]	FCU_0	0					
		_	EIRQ[1]	SIUL	I					
	PCR[2]	ALT0	GPIO[2]	SIUL	I/O	Slow	Medium	_	57	
		ALT1	ETC[2]	eTimer_0	I/O					
		ALT2		_	_					
A[2]		ALT3	A[3]	FlexPWM_0	0					
		_	SIN	DSPI_2	I					
		_	ABS[0]	MC_RGM	I					
		_	EIRQ[2]	SIUL	I					
	PCR[3]	ALT0	GPIO[3]	SIUL	I/O	Slow N	Slow Medium	41	64	
A[3]		ALT1	ETC[3]	eTimer_0	I/O					
		ALT2	CS0	DSPI_2	I/O					
		ALT3	B[3]	FlexPWM_0	0		Slow	wealulli	41	04
		_	ABS[1]	MC_RGM	I					
		_	EIRQ[3]	SIUL	I					

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Table 7. Pin muxing (continued)

Port	PCR register	Alternate function ^{(1),(2)}	Functions	Peripheral ⁽³⁾	I/O direc- tion ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin	
pin						SRC = 0	SRC = 1	64-pin	100-pin
A[4]		ALT0	GPIO[4]	SIUL	I/O				
	PCR[4]	ALT1	_	_	_				
		ALT2	CS1	DSPI_2	0	Slow	Medium	48	75
		ALT3	ETC[4]	eTimer_0	I/O				
		_	FAB	MC_RGM	I				
		_	EIRQ[4]	SIUL	I				
		ALT0	GPIO[5]	SIUL	I/O				
		ALT1	CS0	DSPI_1	I/O				8
A[5]	PCR[5]	ALT2		_	_	Slow	Medium	5	
		ALT3	CS7	DSPI_0	0				
		_	EIRQ[5]	SIUL	I				
		ALT0	GPIO[6]	SIUL	I/O		Medium		
		ALT1	SCK	DSPI_1	I/O	Slow			
A[6]	PCR[6]	ALT2	_	_	_			2	2
		ALT3	_	_	_				
		_	EIRQ[6]	SIUL	I				
		ALT0	GPIO[7]	SIUL	I/O	Slow	Medium		
	PCR[7]	ALT1	SOUT	DSPI_1	0				
A[7]		ALT2	_	_	_			3	4
		ALT3	_	_	_				
		_	EIRQ[7]	SIUL	I				
	PCR[8]	ALT0	GPIO[8]	SIUL	I/O	Slow	Medium	4	6
		ALT1	_	_	_				
4.501		ALT2	_	_	_				
A[8]		ALT3		_	_				
		_	SIN	DSPI_1	I				
		_	EIRQ[8]	SIUL	I				
	PCR[9]	ALT0	GPIO[9]	SIUL	I/O		ow Medium		
		ALT1	CS1	DSPI_2	0	Slow			94
A[9]		ALT2		_	_			60	
		ALT3	B[3]	FlexPWM_0	0				
		_	FAULT[0]	FlexPWM_0	1				
	PCR[10]	ALT0	GPIO[10]	SIUL	I/O				
		ALT1	CS0	DSPI_2	I/O				
A[10]		ALT2	B[0]	FlexPWM_0	0	Slow	Medium	52	81
		ALT3	X[2]	FlexPWM_0	0				
		_	EIRQ[9]	SIUL	I				

Table 7. Pin muxing (continued)

Port	PCR	Alternate	Functions	Peripheral ⁽³⁾	1/0	Pad sp	peed ⁽⁵⁾	F	Pin
pin	register	function ^{(1),(2)}	Functions	Peripheral	direc- tion ⁽⁴⁾	SRC = 0	SRC = 1	64-pin	100-pin
A[11]	PCR[11]	ALT0 ALT1 ALT2 ALT3 —	GPIO[11] SCK A[0] A[2] EIRQ[10]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O I/O O O –	Slow	Medium	53	82
A[12]	PCR[12]	ALT0 ALT1 ALT2 ALT3 —	GPIO[12] SOUT A[2] B[2] EIRQ[11]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O O O O	Slow Medium		54	83
A[13]	PCR[13]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[13] — B[2] — SIN FAULT[0] EIRQ[12]	SIUL FlexPWM_0 DSPI_2 FlexPWM_0 SIUL	I/O — O Slow Medi		Medium	61	95
A[14]	PCR[14]	ALT0 ALT1 ALT2 ALT3 —	GPIO[14]	SIUL Safety Port_0 SIUL	I/O O — — I	Slow	Slow Medium		99
A[15]	PCR[15]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[15] — — — RXD EIRQ[14]	SIUL — — — Safety Port_0 SIUL	I/O — — — — I	Slow	Medium	64	100
				Port B (16-bit)					
B[0]	PCR[16]	ALT0 ALT1 ALT2 ALT3 —	GPIO[16] TXD — DEBUG[0] EIRQ[15]	SIUL FlexCAN_0 — SSCM SIUL	I/O O — — I	Slow	Medium	49	76
B[1]	PCR[17]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[17] — DEBUG[1] RXD EIRQ[16]	SIUL SSCM FlexCAN_0 SIUL	I/O — — — I	Slow	Medium	50	77

Table 7. Pin muxing (continued)

Port	PCR	Alternate	-	D: 1 1(3)	1/0	Pad sp	peed ⁽⁵⁾	P	in				
pin	register	function ^{(1),(2)}	Functions	Peripheral ⁽³⁾	direc- tion ⁽⁴⁾	SRC = 0	SRC = 1	64-pin	100-pin				
		ALT0	GPIO[18]	SIUL	I/O								
		ALT1	TXD	LIN_0	0								
B[2]	PCR[18]	ALT2	_	_	_	Slow	Medium	51	79				
		ALT3	DEBUG[2]	SSCM	_								
			EIRQ[17]	SIUL	I								
		ALT0	GPIO[19]	SIUL	I/O								
		ALT1		_	_								
B[3]	PCR[19]	ALT2	_	_	_	Slow	Medium	_	80				
		ALT3	DEBUG[3]	SSCM	_								
		_	RXD	LIN_0	I								
		ALT0	GPIO[22]	SIUL	I/O								
		ALT1	CLKOUT	Control	0								
B[6]	PCR[22]	ALT2	CS2	DSPI_2	0	Slow	Medium	62	96				
		ALT3	_	_	_								
		_	EIRQ[18]	SIUL	I								
		ALT0	GPIO[23]	SIUL									
		ALT1	_	_									
רבו	DODIOOI	ALT2	_	_	lanut ank			20	20				
B[7]	PCR[23]	PCR[23]	FOR[23]	ALT3	_	_	Input only	_	_	20	29		
									_	AN[0]	ADC_0		
		_	RXD	LIN_0									
		ALT0	GPIO[24]	SIUL									
		ALT1	_	_									
D101	DCD[04]	ALT2	_	_	Innut only			22	24				
B[8]	PCR[24]	ALT3	_	_	Input only	_	_	22	31				
		_	AN[1]	ADC_0									
		_	ETC[5]	eTimer_0									
		ALT0	GPIO[25]	SIUL									
		ALT1	_	_									
B[9]	PCR[25]	ALT2	_	_	Input only	_	_	24	35				
	3[9] PCR[20]	ALT3	_	_									
		_	AN[11]	ADC_0									
		ALT0	GPIO[26]	SIUL									
		ALT1		_									
B[10]	PCR[26]	ALT2	_	_	Input only	ly		25	36				
	- -	ALT3	_	_		y							
		_	AN[12]	ADC_0									

Table 7. Pin muxing (continued)

Port	PCR	Alternate		D (3)	1/0	Pad s	peed ⁽⁵⁾	P	Pin
pin	register	function ^{(1),(2)}	Functions	Peripheral ⁽³⁾	direc- tion ⁽⁴⁾	SRC = 0	SRC = 1	64-pin	100-pin
		ALT0	GPIO[27]	SIUL					
		ALT1	_	_					
B[11]	PCR[27]	ALT2	_	_	Input only	_	_	26	37
		ALT3	_	_					
		_	AN[13]	ADC_0					
		ALT0	GPIO[28]	SIUL					
		ALT1	_	_					
B[12]	PCR[28]	ALT2	_	_	Input only	_	_	27	38
		ALT3	_	_					
		_	AN[14]	ADC_0					
		ALT0	GPIO[29]	SIUL					
		ALT1	_	_					
		ALT2	_	_					
B[13]	PCR[29]	ALT3	_	_	Input only	_	_	30	42
		_	AN[6]	ADC_0					
		_	emu. AN[0]	emu. ADC_1 ⁽⁶⁾					
		_	RXD	LIN_1					
		ALT0	GPIO[30]	SIUL					
		ALT1	_	_					
		ALT2	_	_	Input only				
B[14]	PCR[30]	ALT3	_	_					44
D[14]	FUN[30]	_	AN[7]	ADC_0		_			44
		_	emu. AN[1]	emu. ADC_1 ⁽⁶⁾					
		_	ETC[4]	eTimer_0					
		_	EIRQ[19]	SIUL					
		ALT0	GPIO[31]	SIUL					
		ALT1	_	_					
		ALT2	_	_					
B[15]	PCR[31]	ALT3	_	_	Input only	_	_	_	43
		_	AN[8]	ADC_0					
		_	emu. AN[2]	emu. ADC_1 ⁽⁶⁾					
		_	EIRQ[20]	SIUL					
				Port C (16-bit)					
		ALT0	GPIO[32]	SIUL					
		ALT1	_	_					
CIOI	DCD[33]	ALT2	_	_	Input only				15
C[0]	PCR[32]	ALT3	_	_	Input only	nly — — —	_	45	
		_	AN[9]	ADC_0					
		_	emu. AN[3]	emu. ADC_1 ⁽⁶⁾					

Table 7. Pin muxing (continued)

Port	PCR	Alternate	-	D : 1 (3)	I/O	Pad sp	peed ⁽⁵⁾	F	Pin	
pin	register	function ^{(1),(2)}	Functions	Peripheral ⁽³⁾	direc- tion ⁽⁴⁾	SRC = 0	SRC = 1	64-pin	100-pin	
		ALT0	GPIO[33]	SIUL						
		ALT1	_	_						
C[1]	PCR[33]	ALT2	_	_	Input only	_	_	19	28	
		ALT3	_	_						
		—	AN[2]	ADC_0						
		ALT0	GPIO[34]	SIUL						
		ALT1	_	_						
C[2]	PCR[34]	ALT2	_	_	Input only	_	_	21	30	
		ALT3	_	_						
		_	AN[3]	ADC_0						
		ALT0	GPIO[35]	SIUL	I/O					
		ALT1	CS1	DSPI_0	0					
C[3]	PCR[35]	ALT2		_	_	Slow	Medium		10	
		ALT3	TXD	LIN_1	0					
		_	EIRQ[21]	SIUL	I					
		ALT0	GPIO[36]	SIUL	I/O					
		ALT1	CS0	DSPI_0	I/O					
C[4]	PCR[36]	ALT2	X[1]	FlexPWM_0	0	Slow	Medium		5	
		ALT3	DEBUG[4]	SSCM	_					
		_	EIRQ[22]	SIUL	I					
		ALT0	GPIO[37]	SIUL	I/O					
		ALT1	SCK	DSPI_0	I/O					
C[5]	PCR[37]	ALT2	_	_	_	Slow	Slow Medium	_	7	
		ALT3	DEBUG[5]	SSCM	_					
		_	EIRQ[23]	SIUL	I					
		ALT0	GPIO[38]	SIUL	I/O					
		ALT1	SOUT	DSPI_0	0					
C[6]	PCR[38]	ALT2	B[1]	FlexPWM_0	0	Slow	Medium	_	98	
		ALT3	DEBUG[6]	SSCM	_					
		_	EIRQ[24]	SIUL	I					
		ALT0	GPIO[39]	SIUL	I/O					
		ALT1	_	_	_					
C[7]	PCR[39]	ALT2	A[1]	FlexPWM_0	0	Slow	Medium	_	9	
		ALT3	DEBUG[7]	SSCM	_					
		_	SIN	DSPI_0	I					
		ALT0	GPIO[40]	SIUL	I/O					
0101	DOD: 403	ALT1	CS1	DSPI_1	0		Close Madicina		0.4	
C[8]	PCR[40]	ALT2	_	_	_		57	91		
		ALT3	CS6	DSPI_0	0					

Table 7. Pin muxing (continued)

Port	PCR	Alternate		(3)	I/O	Pad sp	peed ⁽⁵⁾	F	Pin
pin	register	function ^{(1),(2)}	Functions	Peripheral ⁽³⁾	direc- tion ⁽⁴⁾	SRC = 0	SRC = 1	64-pin	100-pin
		ALT0	GPIO[41]	SIUL	I/O				
C[9]	PCR[41]	ALT1	CS3	DSPI_2	0	Slow	Medium		84
C[9]	FUN[41]	ALT2	_	_	_	Siow	Mediaiii	_	04
		ALT3	X[3]	FlexPWM_0	0				
		ALT0	GPIO[42]	SIUL	I/O				
		ALT1	CS2	DSPI_2	0				
C[10]	PCR[42]	ALT2	_	_	_	Slow	Medium	_	78
		ALT3	A[3]	FlexPWM_0	0				
		_	FAULT[1]	FlexPWM_0	1				
		ALT0	GPIO[43]	SIUL	I/O				
C[11]	DCD[42]	ALT1	ETC[4]	eTimer_0	I/O	Slow	Medium	33	55
C[11]	PCR[43]	ALT2	CS2	DSPI_2	0	Slow	wealum	33	55
		ALT3	_	_	_				
		ALT0	GPIO[44]	SIUL	I/O				
C[4.0]	DCD[44]	ALT1	ETC[5]	eTimer_0	I/O	Class	Medium	24	F.C.
C[12]	PCR[44]	ALT2	CS3	DSPI_2	0	Slow	wealum	34	56
		ALT3	_	_	_				
		ALT0	GPIO[45]	SIUL	I/O				
		ALT1	_	_	_				
C[12]	PCR[45]	ALT2	_	_	_	Slow	Medium		71
C[13]	PCK[45]	ALT3	_	_	_	Slow	Medium	_	7.1
		_	EXT_IN	CTU_0	I				
		_	EXT_SYNC	FlexPWM_0	I				
		ALT0	GPIO[46]	SIUL	I/O				
C[14]	PCR[46]	ALT1	_	_	_	Slow	Medium	_	72
راحا	1 011[40]	ALT2	EXT_TGR	CTU_0	0	Olow	Wicalam		12
		ALT3	_	_	_				
		ALT0	GPIO[47]	SIUL	I/O				
		ALT1	_	_	_				
C[15]	PCR[47]	ALT2	_	_	_	Slow	Medium		85
C[13]	r Cit[47]	ALT3	A[1]	FlexPWM_0	0	SIOW	Mediaiii		03
		_	EXT_IN	CTU_0	I				
		_	EXT_SYNC	FlexPWM_0	I				
				Port D (16-bit)					
		ALT0	GPIO[48]	SIUL	I/O				
Dioi	DCD[40]	ALT1	_	_	_	Class	Madium		06
D[0]	PCR[48]	ALT2	_	_	_	Slow	ow Medium	_	86
		ALT3	B[1]	FlexPWM_0	0				

Table 7. Pin muxing (continued)

Port	PCR	Alternate	Formations	Danimb and (3)	I/O	Pad s	peed ⁽⁵⁾	F	Pin	
pin	register	function ^{(1),(2)}	Functions	Peripheral ⁽³⁾	direc- tion ⁽⁴⁾	SRC = 0	SRC = 1	64-pin	100-pin	
		ALT0 ALT1	GPIO[49]	SIUL	I/O					
D[1]	PCR[49]	ALT2	_	_	_	Slow	Medium	_	3	
		ALT3	EXT_TRG	CTU_0	0					
		ALT0	GPIO[50]	SIUL	I/O					
D[2]	PCR[50]	ALT1	_	_	_	Slow	Medium		97	
رکار	r Civ[30]	ALT2	_	_	_	Siow	Mediaiii		31	
		ALT3	X[3]	FlexPWM_0	0					
		ALT0	GPIO[51]	SIUL	I/O					
D[3]	PCR[51]	ALT1	_	_	_	Slow	Medium	_	89	
اکاری	i Ortion	ALT2	_	_	_	Olow	Wodiam			
		ALT3	A[3]	FlexPWM_0	0					
		ALT0	GPIO[52]	SIUL	I/O					
D[4]	PCR[52]	ALT1	_	_	_	Slow	Medium	_	90	
ر. ا	. 0. (02)	ALT2	_	_	_	Cion	Wodiam			
		ALT3	B[3]	FlexPWM_0	0					
		ALT0	GPIO[53]	SIUL	I/O					
DIEI	PCR[53]	ALT1	CS3	DSPI_0	0	Clave	Medium		20	
D[5]		ALT2	F[0]	FCU_0	0	Slow	iviedium	_	22	
		ALT3	_	_	_					
		ALT0	GPIO[54]	SIUL	I/O					
			ALT1	CS2	DSPI_0	0				
D[6]	PCR[54]	ALT2	_	_	_	Slow	Medium	_	23	
		ALT3	_	_	_					
		_	FAULT[1]	FlexPWM_0	I					
		ALT0	GPIO[55]	SIUL	I/O					
D[7]	PCR[55]	ALT1	CS3	DSPI_1	0	Slow	Medium	17	26	
D[/]	i Ort[55]	ALT2	F[1]	FCU_0	0	Olow	Mediaiii	17	20	
		ALT3	CS4	DSPI_0	0					
		ALT0	GPIO[56]	SIUL	I/O					
D[8]	PCR[56]	ALT1	CS2	DSPI_1	0	Slow	Medium	14	21	
D[0]	FUN[30]	ALT2	_	_	_	SIOW	Medium	14	21	
		ALT3	CS5	DSPI_0	0					
		ALT0	GPIO[57]	SIUL	I/O					
Dioi	DCDIEZI	ALT1	X[0]	FlexPWM_0	0	Class	Modium	0	4.5	
D[9]	PCR[57]	ALT2	TXD	LIN_1	0	Slow	Medium	8	15	
		ALT3	_	_	_					
		ALT0	GPIO[58]	SIUL	I/O					
D[40]	DCDIE01	ALT1	A[0]	FlexPWM_0	0			F2		
D[10]	PCR[58]	ALT2	_	_	_		_	53		
		ALT3	_	_	_					

Table 7. Pin muxing (continued)

Port	PCR	Alternate	-	5 (3)	I/O	Pad sp	peed ⁽⁵⁾	Pin	
pin	register	function ^{(1),(2)}	Functions	Peripheral ⁽³⁾	direc- tion ⁽⁴⁾	SRC = 0	SRC = 1	64-pin	100-pin
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] B[0] — —	SIUL FlexPWM_0 — —	I/O O —	Slow	Medium	_	54
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3 —	GPIO[60] X[1] — — RXD	SIUL FlexPWM_0 — — LIN_1	I/O O — — I	Slow	Medium	45	70
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3	GPIO[61] A[1] — —	SIUL FlexPWM_0 —	I/O O — —	Slow	Medium	44	67
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3	GPIO[62] B[1] — —	SIUL FlexPWM_0 —	I/O O — —	Slow Medium		46	73
D[15]	PCR[63]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[63] — — — AN[10] emu. AN[4]	SIUL — — ADC_0 emu. ADC_1 ⁽⁶⁾	Input only	_	ı	ı	41
				Port E (16-bit)					
E[1]	PCR[65]	ALT0 ALT1 ALT2 ALT3 —	GPIO[65] — — — — AN[4]	SIUL — — — ADC_0	Input only	_	-	18	27
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3 —	GPIO[66] — — — — AN[5]	SIUL ADC_0	Input only	_	_	23	32
E[3]	PCR[67]	ALT0 ALT1 ALT2 ALT3 —	GPIO[67] — — — — AN[6]	SIUL — — — ADC_0	Input only	_	_	30	42

Table 7. Pin muxing (continued)

Port	PCR	Alternate	Functions	Peripheral ⁽³⁾	I/O direc-	Pad sp	peed ⁽⁵⁾	F	Pin
pin	register	function ^{(1),(2)}	Functions	Peripheral	tion ⁽⁴⁾	SRC = 0	SRC = 1	64-pin	100-pin
		ALT0	GPIO[68]	SIUL					
		ALT1	_	_					
E[4]	PCR[68]	ALT2		_	Input only	_	_	_	44
		ALT3		_					
		_	AN[7]	ADC_0					
		ALT0	GPIO[69]	SIUL					
		ALT1	_	_					
E[5]	PCR[69]	ALT2	_	_	Input only	_	_	_	43
		ALT3	_	_					
		_	AN[8]	ADC_0					
		ALT0	GPIO[70]	SIUL					
		ALT1	_	_					
E[6]	PCR[70]	ALT2		_	Input only	_	_	_	45
		ALT3	_	_					
		_	AN[9]	ADC_0					
		ALT0	GPIO[71]	SIUL					
		ALT1	_	_					
E[7]	PCR[71]	ALT2	_	_	Input only	_	_	_	41
		ALT3	_	_					
		_	AN[10]	ADC_0					

- 1. ALT0 is the primary (default) function for each port after reset.
- 2. Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIU module. PCR.PA = 00 → ALT0; PCR.PA = 01 → ALT1; PCR.PA = 10 → ALT2; PCR.PA = 11 → ALT3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".
- 3. Module included on the MCU.
- 4. Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.
- 5. Programmable via the SRC (Slew Rate Control) bits in the respective Pad Configuration Register.
- ADC0.AN emulates ADC1.AN. This feature is used to provide software compatibility between SPC560P34/SPC560P40 and SPC560P50. Refer to ADC chapter of reference manual for more details.

3 Electrical characteristics

3.1 Introduction

This section contains device electrical characteristics as well as temperature and power considerations.

This microcontroller contains input protection against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down resistors, which are provided by the device for most general purpose pins.

The following tables provide the device characteristics and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol "CC" for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol "SR" for System Requirement is included in the Symbol column.

Caution:

All of the following parameter values can vary depending on the application and must be confirmed during silicon characterization or silicon reliability trial.

3.2 Parameter classification

The electrical parameters are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
Р	Those parameters are guaranteed during production testing on each individual device.
С	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
Т	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled "C" in the parameter tables where appropriate.

3.3 Absolute maximum ratings

Table 9. Absolute maximum ratings⁽¹⁾

0		Danier (au	0		Value	11!(
Symbol		Parameter	Conditions	Min	Max ⁽²⁾	Unit
V _{SS}	S R	Device ground	_	0	0	V
V _{DD_HV_IOx} ⁽³⁾	S R	3.3 V/5.0 V input/output supply voltage (supply). Code flash memory supply with VDD_HV_IO3 and data flash memory with VDD_HV_IO2	_	-0.3	6.0	V
V _{SS_HV_IOx}	S R	3.3 V/5.0 V input/output supply voltage (ground). Code flash memory ground with V _{SS_HV_IO3} and data flash memory with V _{SS_HV_IO2}	_	-0.1	0.1	>
	s	3.3 V/5.0 V crystal oscillator amplifier	_	-0.3	6.0	
V _{DD_HV_OSC}	R	supply voltage (supply)	Relative to V _{DD_HV_IOx}	-0.3	$V_{DD_HV_IOx} + 0.3$	V
V _{SS_HV_OSC}	S R	3.3 V/5.0 V crystal oscillator amplifier supply voltage (ground)	_	-0.1	0.1	V
V	S	3.3 V/5.0 V ADC_0 supply and high-	V _{DD_HV_REG} < 2.7 V	-0.3	V _{DD_HV_REG} + 0.3	V
V _{DD_HV_ADC0}	R	reference voltage	V _{DD_HV_REG} > 2.7 V	-0.3	6.0	V
V _{SS_HV_ADC0}	S R	3.3 V/5.0 V ADC_0 ground and low-reference voltage	_	-0.1	0.1	V
	s	3.3 V/5.0 V voltage-regulator supply	_	-0.3	6.0	
$V_{DD_HV_REG}$	R	voltage	Relative to V _{DD_HV_IOx}	-0.3	$V_{DD_HV_IOx} + 0.3$	V
TV_DD	S R	Slope characteristics on all V _{DD} during power up ⁽⁴⁾ with respect to ground (V _{SS})	_	3.0 ⁽⁵⁾	500 x 10 ³ (0.5 [V/μs])	V/s
V _{DD_LV_CORx}	C C	1.2 V supply pins for core logic (supply)	_	-0.1	1.5	V
V _{SS_LV_CORx}	S R	1.2 V supply pins for core logic (ground)	_	-0.1	0.1	V
	s	Voltage on any pin with respect to	_	-0.3	6.0	
V _{IN}	R	ground (V _{SS_HV_IOx})	Relative to V _{DD_HV_IOx}	-0.3	V _{DD_HV_IOx} + 0.3	V
I _{INJPAD}	S R	Input current on any pin during overload condition	_	-10	10	mA

Value **Symbol Conditions** Unit **Parameter** Max⁽²⁾ Min Absolute sum of all input currents 50 -50 mΑ I_{INJSUM} R during overload condition S Storage temperature -55 150 °C T_{STG} R S °C Junction temperature under bias -40 150 $T_{\rm J}$ R

Table 9. Absolute maximum ratings⁽¹⁾ (continued)

- Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings
 only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device
 reliability or cause permanent damage to the device.
- 2. Absolute maximum voltages are currently maximum burn-in voltages.
- 3. The difference between each couple of voltage supplies must be less than 300 mV, $|V_{DD\ HV\ IOV} V_{DD\ HV\ IOX}| < 300$ mV.
- 4. Guaranteed by device validation.
- 5. Minimum value of TV_{DD} must be guaranteed until $V_{DD_HV_REG}$ reaches 2.6 V (maximum value of V_{PORH})
- 6. Only when $V_{DD_HV_IOx} < 5.2 \text{ V}$

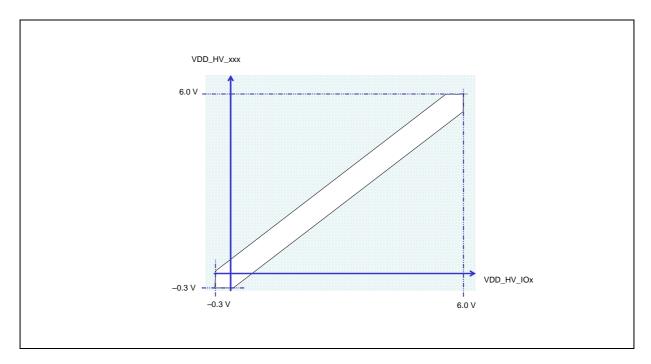


Figure 6 shows the constraints of the different power supplies.

Figure 6. Power supplies constraints ($-0.3 \text{ V} \le \text{V}_{DD \text{ HV IOx}} \le 6.0 \text{ V}$)

The SPC560P34/SPC560P40 supply architecture allows the ADC supply to be managed independently from the standard V_{DD_HV} supply. *Figure 7* shows the constraints of the ADC power supply.

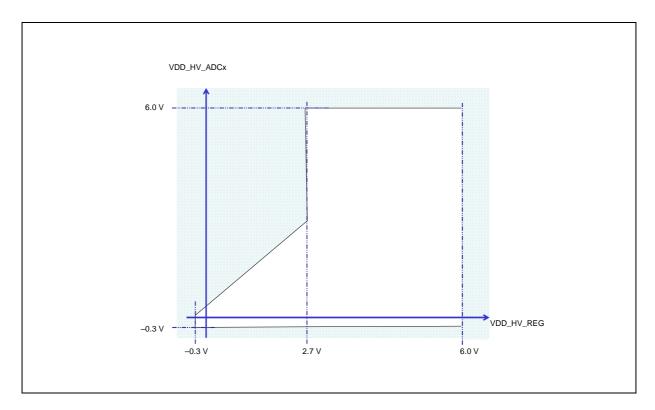


Figure 7. Independent ADC supply (–0.3 V \leq V_{DD_HV_REG} \leq 6.0 V)

3.4 Recommended operating conditions

Table 10. Recommended operating conditions (5.0 V)

0		B	O a malitia ma	Val	ue	11!
Symbol		Parameter	Conditions	Min	Max ⁽¹⁾	Unit
V _{SS}	SR	Device ground	_	0	0	V
V _{DD_HV_IOx} ⁽²⁾	SR	5.0 V input/output supply voltage	_	4.5	5.5	٧
V _{SS_HV_IOx}	SR	Input/output ground voltage	_	0	0	٧
		5.0 V crystal oscillator	_	4.5	5.5	
V _{DD_HV_OSC}	SR	amplifier supply voltage	Relative to V _{DD_HV_IOx}	V _{DD_HV_IOx} - 0.1	$V_{DD_HV_IOx} + 0.1$	V
V _{SS_HV_OSC}	SR	5.0 V crystal oscillator amplifier reference voltage	_	0	0	V
		5.0 V voltage regulator	_	4.5	5.5	
$V_{DD_HV_REG}$	SR	supply voltage	Relative to V _{DD_HV_IOx}	V _{DD_HV_IOx} - 0.1	V _{DD_HV_IOx} + 0.1	V

Table 10. Recommended operating conditions (5.0 V) (continued)

Comple of		Dovernotor	Canditions	Valu	ue	11:4
Symbol		Parameter	Conditions	Min	Max ⁽¹⁾	Unit
		5.0 V ADC_0 supply and	_	4.5	5.5	
V _{DD_HV_ADC0}	SR	high reference voltage	Relative to V _{DD_HV_REG}	V _{DD_HV_REG} - 0.1		V
V _{SS_HV_ADC0}	SR	ADC_0 ground and low reference voltage	_	0	0	V
V _{DD_LV_REGCOR} (3),(4)	СС	Internal supply voltage	_	_	_	V
V _{SS_LV_REGCOR} ⁽³⁾	SR	Internal reference voltage	_	0	0	V
V _{DD_LV_CORx} (3),(4)	СС	Internal supply voltage	_	_	_	V
V _{SS_LV_CORx} ⁽³⁾	SR	Internal reference voltage	_	0	0	V
T _A	SR	Ambient temperature	f _{CPU} = 60 MHz	-40	125	°C
'A	SIX	under bias	f _{CPU} = 64 MHz	-40	105	°C

Full functionality cannot be guaranteed when voltage drops below 4.5 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.

Table 11. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Val	lue	Unit
Symbol		raiailletei	Conditions	Min	Max ⁽¹⁾	Ollit
V _{SS}	SR	Device ground	_	0	0	V
V _{DD_HV_IOx} ⁽²⁾	SR	3.3 V input/output supply voltage	_	3.0	3.6	٧
V _{SS_HV_IOx}	SR	Input/output ground voltage	_	0	0	٧
	SR	3.3 V crystal oscillator	_	3.0	3.6	
V _{DD_HV_OSC}		amplifier supply voltage	Relative to V _{DD_HV_IOx}	V _{DD_HV_IOx} - 0.1	$V_{DD_HV_IOx} + 0.1$	>
V _{SS_HV_OSC}	SR	3.3 V crystal oscillator amplifier reference voltage	ı	0	0	>

^{2.} The difference between each couple of voltage supplies must be less than 100 mV, $V_{DD_HV_IOy} - V_{DD_HV_IOx} < 100$ mV.

^{3.} To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds (V_{SS_LV_xxx}) must be shorted to high voltage grounds (V_{SS_HV_xxx}) and the low voltage supply pins (V_{DD_LV_xxx}) must be connected to the external ballast emitter.

^{4.} The low voltage supplies (V_{DD_LV_xxx}) are not all independent.

- V_{DD_LV_COR1} and V_{DD_LV_COR2} are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash memory module. Similarly, V_{SS_LV_COR1} and V_{SS_LV_COR2} are internally shorted.

- V_{DD_LV_REGCOR} and V_{DD_LV_RECORx} are physically shorted internally, as are V_{SS_LV_REGCOR} and V_{SS_LV_CORx}.

Table 11. Recommended operating conditions (3.3 V) (continued)

Symbol		Bananatan	O a malitia ma	Va	lue	1116
		Parameter	Conditions	Min	Max ⁽¹⁾	Unit
		3.3 V voltage regulator	_	3.0	3.6	
$V_{DD_HV_REG}$	SR	supply voltage	Relative to V _{DD_HV_IOx}	V _{DD_HV_IOx} - 0.1	$V_{DD_HV_IOx} + 0.1$	V
		3.3.V.ADC O supply and	_	3.0	5.5	
V _{DD_HV_ADC0}	SR	3.3 V ADC_0 supply and high reference voltage	Relative to V _{DD_HV_REG}	V _{DD_HV_REG} – 0.1	5.5	V
V _{SS_HV_ADC0}	SR	ADC_0 ground and low reference voltage	_	0	0	V
V _{DD_LV_REGCOR} (3),(4)	СС	Internal supply voltage	_	_	_	V
V _{SS_LV_REGCOR} ⁽³⁾	SR	Internal reference voltage	_	0	0	V
$V_{DD_LV_CORx}^{(3),(4)}$	СС	Internal supply voltage	_	_	_	V
V _{SS_LV_CORx} ⁽³⁾	SR	Internal reference voltage		0	0	V
т.	Ambient temperature		f _{CPU} = 60 MHz	-40	125	°C
T _A	SIX	SR under bias	f _{CPU} = 64 MHz	-40	105	°C

^{1.} Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.

Figure 8 shows the constraints of the different power supplies.

^{2.} The difference between each couple of voltage supplies must be less than 100 mV, $V_{DD_HV_IOy} - V_{DD_HV_IOx} < 100$ mV.

^{3.} To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an onchip voltage regulator—but for the device to function properly the low voltage grounds (V_{SS_LV_xxx}) must be shorted to high voltage grounds (V_{SS_HV_xxx}) and the low voltage supply pins (V_{DD_LV_xxx}) must be connected to the external ballast emitter.

^{4.} The low voltage supplies (V_{DD_LV_xxx}) are not all independent.

- V_{DD_LV_COR1} and V_{DD_LV_COR2} are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash memory module. Similarly, V_{SS_LV_COR1} and V_{SS_LV_COR2} are internally shorted.

- V_{DD_LV_REGCOR} and V_{DD_LV_RECORx} are physically shorted internally, as are V_{SS_LV_REGCOR} and V_{SS_LV_CORx}.

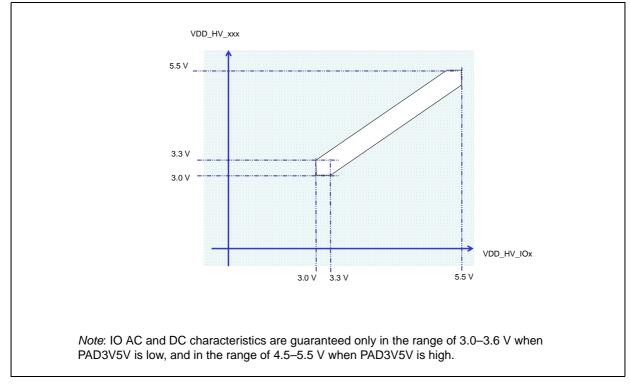


Figure 8. Power supplies constraints (3.0 V \leq V_{DD_HV_IOx} \leq 5.5 V)

The SPC560P34/SPC560P40 supply architecture allows the ADC supply to be managed independently from the standard V_{DD_HV} supply. *Figure 9* shows the constraints of the ADC power supply.

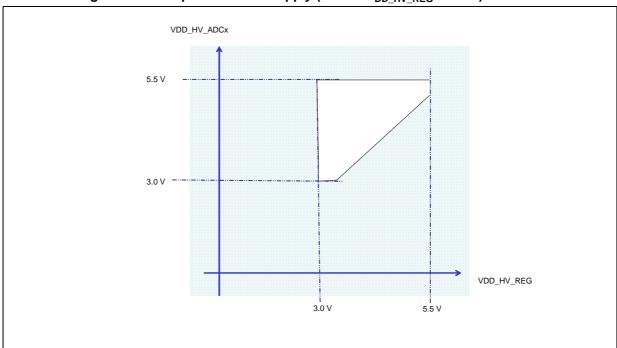


Figure 9. Independent ADC supply (3.0 V \leq V_{DD HV REG} \leq 5.5 V)

3.5 Thermal characteristics

3.5.1 Package thermal characteristics

Table 12. LQFP thermal characteristics

Symbol	Dozomotov	Conditions	Туріса	Unit	
	Parameter	Conditions	100-pin	64-pin	Unit
	Thermal resistance junction-to-ambient, natural	Single layer board—1s	63	57	°C/W
$R_{\theta JA}$	convection ⁽¹⁾	Four layer board—2s2p	51	41	°C/W
$R_{\theta JB}$	Thermal resistance junction-to-board ⁽²⁾	Four layer board—2s2p	33	22	°C/W
$R_{\theta JCtop}$	Thermal resistance junction-to-case (top) ⁽³⁾	Single layer board—1s	15	13	°C/W
Ψ_{JB}	Junction-to-board, natural convection ⁽⁴⁾	Operating conditions	33	22	°C/W
Ψ _{JC}	Junction-to-case, natural convection ⁽⁵⁾	Operating conditions	1	1	°C/W

- Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.
- Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. When Greek letters are not available, the symbols are typed as RthJB or Theta-JB.
- 3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
- Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
- Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

3.5.2 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from *Equation 1*:

Equation 1:
$$T_J = T_A + (R_{\theta JA} * P_D)$$

where:

T_A = ambient temperature for the package (°C)

R_{0.IA} = junction-to-ambient thermal resistance (°C/W)

 P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in *Equation 2* as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

 $R_{\theta,IA}$ = junction-to-ambient thermal resistance (°C/W)

R_{θJC} = junction-to-case thermal resistance (°C/W)

 $R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using *Equation 3*:

Equation 3: $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

 T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

 P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

- Semiconductor Equipment and Materials International 3081 Zanker Road
 San Jose, CA 95134U.S.A.
 (408) 943-6900
- MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at (800) 854-7179 or (303) 397-7956.
- JEDEC specifications are available on the WEB at http://www.jedec.org.
- C.E. Triplett and B. Joiner, An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module, Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
- G. Kromann, S. Shidore, and S. Addison, Thermal Modeling of a PBGA for Air-Cooled Applications, Electronic Packaging and Production, pp. 53–58, March 1998.
- B. Joiner and V. Adams, Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling, Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.6 Electromagnetic interference (EMI) characteristics

Table 13. EMI testing specifications

Symbol	Parameter	Conditions	Clocks	Frequency	Level (Typ)	Unit
			f _{OSC} = 8 MHz	150 kHz-150 MHz	11	dΒμ
		V _{DD} = 5.0 V; T _A = 25 °C	f _{CPU} = 64 MHz	150–1000 MHz	13	V
		,	No PLL frequency modulation	IEC level	М	_
		emissions $V_{DD} = 3.3 \text{ V; } T_{A} = 25 \text{ °C}$	f _{OSC} = 8 MHz	150 kHz-150 MHz	8	dΒμ
			f _{CPU} = 64 MHz ±4% PLL frequency modulation f _{OSC} = 8 MHz f _{CPU} = 64 MHz	150–1000 MHz 12		V
V	Radiated			IEC level	N	_
V _{EME}	emissions			150 kHz-150 MHz	9	dΒμ
				150–1000 MHz	12	V
			No PLL frequency modulation	IEC level	М	_
		Other device configuration, test conditions and EM testing	f _{OSC} = 8 MHz	150 kHz-150 MHz	7	dΒμ
		per standard IEC61967-2	f _{CPU} = 64 MHz	150–1000 MHz	12	V
			±4% PLL frequency modulation	IEC level	N	_

3.7 Electrostatic discharge (ESD) characteristics

Table 14. ESD ratings^{(1),(2)}

Symbol		Parameter	Conditions	Value	Unit
V _{ESD(HBM)}	S R	Electrostatic discharge (Human Body Model)	_	2000	V
V	S Electrostatic discharge (Ch	Electrostatic discharge (Charged Device Model)		750 (corners)	V
V _{ESD(CDM)}	R	Charged Device Model)	_	500 (other)	V

^{1.} All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

3.8 Power management electrical characteristics

3.8.1 Voltage regulator electrical characteristics

The internal voltage regulator requires an external NPN ballast, approved ballast list availbale in *Table 15*, to be connected as shown in *Figure 10*. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the $V_{DD_HV_REG}$, BCTRL and $V_{DD_LV_CORx}$ pins to less than L_{Reg} . (refer to *Table 16*).

^{2.} A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Note:

The voltage regulator output cannot be used to drive external circuits. Output pins are to be used only for decoupling capacitance.

 $V_{
m DD\ LV\ COR}$ must be generated using internal regulator and external NPN transistor. It is not possible to provide $V_{DD\ LV\ COR}$ through external regulator.

For the SPC560P34/SPC560P40 microcontroller, capacitor(s), with total values not below C_{DEC1} , should be placed between $V_{DD_LV_CORx}/V_{SS_LV_CORx}$ close to external ballast transistor emitter. 4 capacitors, with total values not below C_{DEC2} , should be placed close to microcontroller pins between each $V_{DD_LV_CORx}/V_{SS_LV_CORx}$ supply pairs and the $V_{DD_LV_REGCOR}/V_{SS_LV_REGCOR}$ pair . Additionally, capacitor(s) with total values not below C_{DEC3} , should be placed between the $V_{DD_HV_REG}/V_{SS_HV_REG}$ pins close to ballast collector. Capacitors values have to take into account capacitor accuracy, aging and variation versus temperature.

All reported information are valid for voltage and temperature ranges described in recommended operating condition, Table 10 and Table 11.

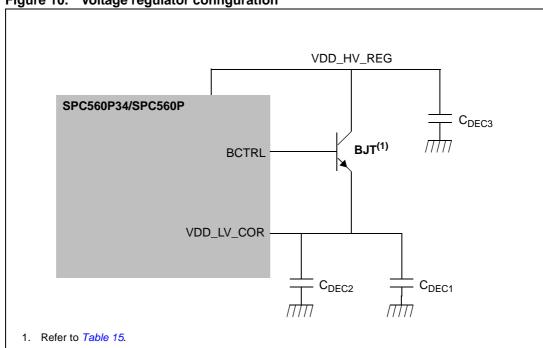


Figure 10. Voltage regulator configuration

Table 15. Approved NPN ballast components

- The state of the		
Part	Manufacturer	Approved derivatives ⁽¹⁾
	ON Semi	BCP68
BCP68	NXP	BCP68-25
	Infineon	BCP68-25
BCX68	Infineon	BCX68-10; BCX68-16; BCX-25
BC868	NXP	BC868

Table 15. Approved NPN ballast components

Part	Manufacturer	Approved derivatives ⁽¹⁾
BC817	Infineon	BC817-16; BC817-25; BC817SU
BCOTT	NXP	BC817-16; BC817-25
	ST	BCP56-16
BCP56	Infineon	BCP56-10; BCP56-16
BCF 30	ON Semi	BCP56-10
	NXP	BCP56-10; BCP56-16

^{1.} For automotive applications please check with the appropriate transistor vendor for automotive grade certification

Table 16. Voltage regulator electrical characteristics

Symbol		С	Parameter	Conditions		Value		Unit
		C	Farameter	Conditions	Min	Тур	Max	
V _{DD_LV_REGCOR}	C	Р	Output voltage under maximum load run supply current configuration	Post-trimming	1.15	_	1.32	V
C _{DEC1}	S R	_	External decoupling/stability ceramic capacitor	BJT from <i>Table 15</i> . Three capacitors (i.e. X7R or X8R capacitors) with nominal value of 10 µF	19.5	30	_	μF
				BJT BC817, one capacitance of 22 µF	14.3	22	_	μF
R _{REG}	S R	_	Resulting ESR of either one or all three C _{DEC1}	Absolute maximum value between 100 kHz and 10 MHz	_	_	45	mΩ
C _{DEC2}	S R	_	External decoupling/stability ceramic capacitor	Four capacitances (i.e. X7R or X8R capacitors) with nominal value of 440 nF	120 0	176 0	_	nF
C _{DEC3}	S R		External decoupling/stability ceramic capacitor on VDD_HV_REG	Three capacitors (i.e. X7R or X8R capacitors) with nominal value of 10 μ F; C_{DEC3} has to be equal or greater than C_{DEC1}	19.5	30	_	μF
L _{Reg}	S R	_	Resulting ESL of $V_{DD_HV_REG}$ BCTRL and $V_{DD_LV_CORx}$ pins	_	_	_	5	nΗ

3.8.2 Voltage monitor electrical characteristics

The device implements a power on reset module to ensure correct power-up initialization, as well as three low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- \bullet LVDHV5 monitors V_{DD} when application uses device in the 5.0 V \pm 10% range
- LVDLVCOR monitors low voltage digital power domain

Table 17. Low voltage monitor electrical characteristics

Cumbal	С	Baramatar	Conditions ⁽¹⁾	Value		Unit
Symbol		Parameter	Conditions	Min	Max	Jilit
V _{PORH}	Т	Power-on reset threshold	_	1.5	2.7	V
V _{PORUP}	Р	Supply for functional POR module	T _A = 25 °C	1.0	_	V
V _{REGLVDMOK_H}	Р	Regulator low voltage detector high threshold	_	_	2.95	V
V _{REGLVDMOK_L} P		Regulator low voltage detector low threshold	_	2.6	_	V
V _{FLLVDMOK_H}	Р	Flash low voltage detector high threshold	_	_	2.95	V
V _{FLLVDMOK_L}	Р	Flash low voltage detector low threshold	_	2.6	_	V
V _{IOLVDMOK_H}	Р	I/O low voltage detector high threshold	_	_	2.95	V
V _{IOLVDMOK_L}	Р	I/O low voltage detector low threshold	_	2.6	_	V
V _{IOLVDM5OK_H}	Р	I/O 5 V low voltage detector high threshold	_	_	4.4	V
V _{IOLVDM5OK_L} P		I/O 5 V low voltage detector low threshold	_	3.8	_	V
V _{MLVDDOK_H}	V _{MLVDDOK_H} P Digital supply low voltage detector high		_	_	1.145	V
V _{MLVDDOK_L}			_	1.08	—	V

^{1.} V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 °C to $T_{A~MAX}$, unless otherwise specified

3.9 Power up/down sequencing

To prevent an overstress event or a malfunction within and outside the device, the SPC560P34/SPC560P40 implements the following sequence to ensure each module is started only when all conditions for switching it ON are available:

- A POWER_ON module working on voltage regulator supply controls the correct startup of the regulator. This is a key module ensuring safe configuration for all voltage regulator functionality when supply is below 1.5 V. Associated POWER_ON (or POR) signal is active low.
- Several low voltage detectors, working on voltage regulator supply monitor the voltage
 of the critical modules (voltage regulator, I/Os, flash memory and low voltage domain).
 LVDs are gated low when POWER ON is active.
- A POWER_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, flash

memory and 16 MHz RC oscillator needed during power-up phase and reset phase. When POWER_OK is low the associated modules are set into a safe state.

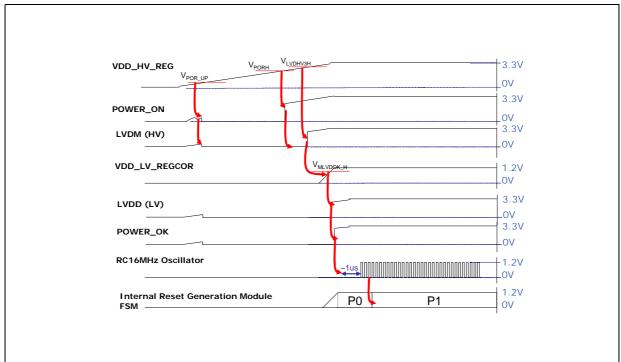
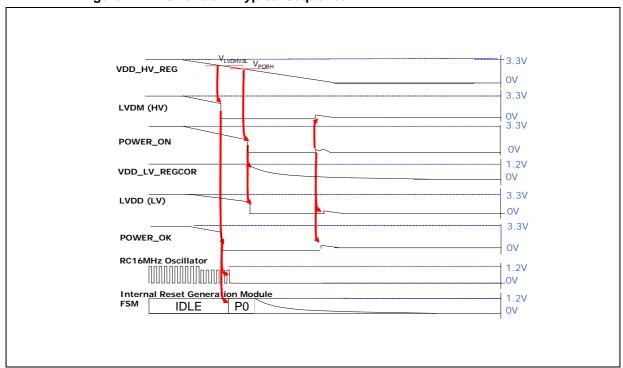


Figure 11. Power-up typical sequence





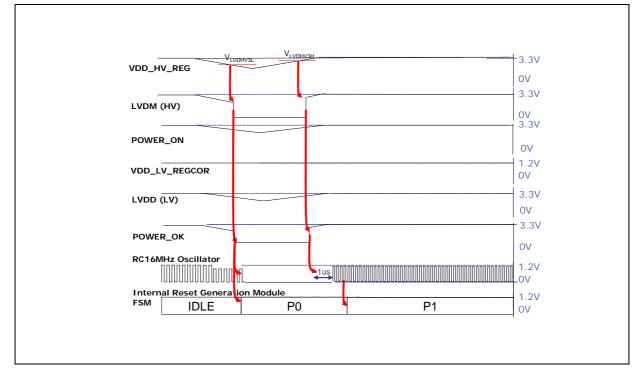


Figure 13. Brown-out typical sequence

3.10 DC electrical characteristics

3.10.1 NVUSRO register

Portions of the device configuration, such as high voltage supply and watchdog enable/disable after reset are controlled via bit values in the non-volatile user options (NVUSRO) register.

For a detailed description of the NVUSRO register, please refer to the device reference manual.

NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. *Table 18* shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 18. PAD3V5V field description

Value ⁽¹⁾	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. Default manufacturing value before flash initialization is '1' (3.3 V).

3.10.2 DC electrical characteristics (5 V)

Table 19 gives the DC electrical characteristics at 5 V ($4.5 \text{ V} < \text{V}_{DD_HV_IOx} < 5.5 \text{ V}$, NVUSRO[PAD3V5V] = 0).

Table 19. DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol	С	Poromotor	Conditions	Val	lue	Unit
Symbol		Parameter	Conditions	Min	Max	Unit
V	D	Low level input voltage	_	-0.4 ⁽¹⁾	_	V
V _{IL}	Р	Low level input voltage	_	_	0.35 V _{DD_HV_IOx}	V
	Р			0.65 V _{DD_HV_IOx}	_	V
V _{IH}	D	High level input voltage			$V_{DD_{-HV_{(1)}}}$ + 0.4	V
V _{HYS}	Т	Schmitt trigger hysteresis	_	0.1 V _{DD_HV_IOx}	_	V
V _{OL_S}	Р	Slow, low level output voltage	I _{OL} = 3 mA	_	0.1 V _{DD_HV_IOx}	V
V _{OH_S}	Р	Slow, high level output voltage	$I_{OH} = -3 \text{ mA}$	0.8 V _{DD_HV_IOx}	_	V
V _{OL_M}	Р	Medium, low level output voltage	$I_{OL} = 3 \text{ mA}$	1	0.1 V _{DD_HV_IOx}	V
V _{OH_M}	Р	Medium, high level output voltage	$I_{OH} = -3 \text{ mA}$	0.8 V _{DD_HV_IOx}	_	V
V _{OL_F}	Р	Fast, low level output voltage	I _{OL} = 14 mA	_	0.1 V _{DD_HV_IOx}	V
V _{OH_F}	Р	Fast, high level output voltage	$I_{OH} = -14 \text{ mA}$	0.8 V _{DD_HV_IOx}	_	V
1	Р	Equivalent pull-up current	$V_{IN} = V_{IL}$	-130	_	μA
I _{PU}	ı	Equivalent pull-up current	$V_{IN} = V_{IH}$		-10	μΛ
l	Р	Equivalent pull-down current	$V_{IN} = V_{IL}$	10	_	μA
I _{PD}		Equivalent pull-down current	$V_{IN} = V_{IH}$	1	130	μΛ
I _{IL}	Р	Input leakage current (all bidirectional ports)	$T_A = -40 \text{ to } 125 \text{ °C}$	-1	1	μА
I _{IL}	Р	Input leakage current (all ADC input-only ports)	$T_A = -40 \text{ to } 125 \text{ °C}$	-0.5	0.5	μA
C _{IN}	D	Input capacitance			10	pF

^{1. &}quot;SR" parameter values must not exceed the absolute maximum ratings shown in Table 9.

Table 20. Supply current (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol	С		Dorometer	Parameter Conditions		Value ⁽¹⁾		Unit	
Symbol	C		Farameter	Conditions		Тур	Max	Onic	
	Т		RUN—Maximum mode ⁽²⁾		40 MHz	44	55		
	Р		NON—Maximum mode.		64 MHz	52	65		
1	Т		RUN—Typical mode ⁽³⁾	V _{DD_LV_CORx} externally	40 MHz	38	46		
I _{DD_LV_CORx}	'		forced at 1.3 V	64 MHz	45	54			
	Р	.	HALT mode ⁽⁴⁾		_	1.5	10		
		rren	STOP mode ⁽⁵⁾		_	1	10		
	Т	upply current	Flash during read	V _{DD_HV_FL} at 5.0 V	_	8	10	mA	
I _{DD_FLASH}		Т	Т	Supp	Flash during erase operation on 1 flash module	V _{DD_HV_FL} at 5.0 V	_	15	19
I _{DD_ADC}	Т		ADC	$V_{DD_HV_ADC0}$ at 5.0 V f_{ADC} = 16 MHz	ADC_0	3	4		
I _{DD_OSC}	Т		Oscillator	V _{DD_HV_OSC} at 5.0 V	8 MHz	2.6	3.2		
I _{DD_HV_REG}	D		Internal regulator module current consumption	V _{DD_HV_REG} at 5.5 V			10		

^{1.} All values to be confirmed after characterization/data collection.

Maximum mode: FlexPWM, ADC, CTU, DSPI, LINFlex, FlexCAN, 15 output pins, PLL_0 enabled, 125 °C ambient. I/O supply current excluded.

^{3.} Typical mode configurations: DSPI, LINFlex, FlexCAN, 15 output pins, PLL_0, 105 °C ambient. I/O supply current excluded.

^{4.} Halt mode configurations: Code fetched from SRAM, code flash memory and data flash memory in low power mode, OSC/PLL_0 are OFF, core clock frozen, all peripherals disabled.

^{5.} STOP "P" mode Device Under Test (DUT) configuration: Code fetched from SRAM, code flash memory and data flash memory off, OSC/PLL_0 are OFF, core clock frozen, all peripherals disabled.

3.10.3 DC electrical characteristics (3.3 V)

Table 21 gives the DC electrical characteristics at 3.3 V (3.0 V < V_{DD_HV_IOX} < 3.6 V, NVUSRO[PAD3V5V] = 1); see *Figure 14*.

Table 21. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1) $^{(1)}$

Symbol	_	Parameter	Conditions	Va	alue	Unit
Symbol	С	Faranietei	Conditions	Min	Max	Ullit
V	D	Low level input voltage	_	$-0.4^{(2)}$	_	V
V _{IL}	Р	Low level input voltage	_	_	0.35 V _{DD_HV_IOx}	V
V _{IH}	Р	High level input voltage	_	0.65 V _{DD_HV_IOx}	_	V
VIH	D	Tilgit level lilput voltage	_	_	$V_{DD_HV_IOx} + 0.4^{(2)}$	V
V _{HYS}	Т	Schmitt trigger hysteresis	_	0.1 V _{DD_HV_IOx}	_	V
V_{OL_S}	Р	Slow, low level output voltage	$I_{OL} = 1.5 \text{ mA}$	_	0.5	V
V_{OH_S}	Р	Slow, high level output voltage	$I_{OH} = -1.5 \text{ mA}$	$V_{DD_HV_IOx} - 0.8$	_	V
V_{OL_M}	Р	Medium, low level output voltage	I _{OL} = 2 mA	_	0.5	V
V _{OH_M}	Р	Medium, high level output voltage	$I_{OH} = -2 \text{ mA}$	$V_{DD_HV_IOx} - 0.8$	_	V
V_{OL_F}	Р	Fast, low level output voltage	I _{OL} = 11 mA	_	0.5	V
V_{OH_F}	Р	Fast, high level output voltage	$I_{OH} = -11 \text{ mA}$	$V_{DD_HV_IOx} - 0.8$	_	V
l _{PU}	Р	Equivalent pull-up current	$V_{IN} = V_{IL}$	-130	_	μA
יפטי	•	Equivalent pair up current	$V_{IN} = V_{IH}$	_	-10	μπ
I _{PD}	Р	Equivalent pull-down current	$V_{IN} = V_{IL}$	10	_	μA
יפט	•	Equivalent pail down carrent	$V_{IN} = V_{IH}$	_	130	μπ
I _{IL}	Р	Input leakage current (all bidirectional ports)	$T_A = -40 \text{ to } 125 \text{ °C}$	_	1	
I _{IL}	Р	Input leakage current (all ADC input-only ports)	$T_A = -40 \text{ to } 125 \text{ °C}$	_	0.5	μA
C _{IN}	D	Input capacitance	_	_	10	pF

^{1.} These specifications are design targets and subject to change per device characterization.

^{2. &}quot;SR" parameter values must not exceed the absolute maximum ratings shown in Table 9.

Value⁽¹⁾ С **Conditions Symbol Parameter** Unit Max Typ 40 MHz 44 55 RUN—Maximum mode⁽²⁾ 64 MHz 52 65 40 MHz 38 46 $V_{DD_LV_CORx}$ externally forced at 1.3 V RUN—Typical mode⁽³⁾ I_{DD_LV_CORx} 64 MHz 45 54 current HALT mode⁽⁴⁾ 1.5 10 mΑ Supply STOP mode⁽⁵⁾ 1 10 V_{DD_HV_ADC0} at 3.3 V Т **ADC** ADC_0 3 4 I_{DD_ADC} $f_{ADC} = 16 \text{ MHz}$ Oscillator Т I_{DD_OSC} V_{DD_HV_OSC} at 3.3 V 8 MHz 2.6 3.2 Internal regulator module D V_{DD_HV_REG} at 5.5 V 10 I_{DD_HV_REG} current consumption

Table 22. Supply current (3.3 V, NVUSRO[PAD3V5V] = 1)

- 1. All values to be confirmed after characterization/data collection.
- Maximum mode: FlexPWM, ADC, CTU, DSPI, LINFlex, FlexCAN, 15 output pins, PLL_0 enabled, 125 °C ambient. I/O supply current excluded.
- Typical mode configurations: DSPI, LINFlex, FlexCAN, 15 output pins, PLL_0, 105 °C ambient. I/O supply current excluded.
- 4. Halt mode configurations: Code fetched from SRAM, code flash memory and data flash memory in low power mode, OSC/PLL_0 are OFF, core clock frozen, all peripherals disabled.
- 5. STOP "P" mode Device Under Test (DUT) configuration: Code fetched from SRAM, code flash memory and data flash memory off, OSC/PLL_0 are OFF, core clock frozen, all peripherals disabled.

3.10.4 Input DC electrical characteristics definition

Figure 14 shows the DC electrical characteristics behavior as function of time.

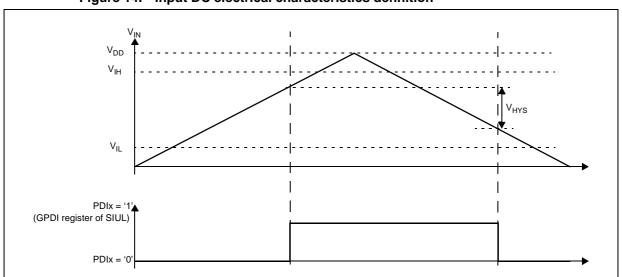


Figure 14. Input DC electrical characteristics definition

3.10.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in *Table 23*.

Table 23. I/O supply segment

Packago		Supply segment								
Package	1	2	3	4	5					
LQFP100	pin15-pin26	pin27-pin46	pin51-pin61	pin64-pin86	pin89–pin10					
LQFP64	pin8–pin17	pin18-pin30	pin33-pin38	pin41-pin54	pin57–pin5					

Table 24. I/O consumption

Symbol		С	Parameter	Conditions ⁽¹⁾		Value)	Unit				
Symbol			Farameter	Conditions			Тур	Max	Oilit				
I _{SWTSLW} ⁽²⁾	CC	D	Dynamic I/O current for SLOW	C _I = 25 pF	$V_{DD} = 5.0 \text{ V} \pm 10\%,$ PAD3V5V = 0	_	_	20	mA				
'SWTSLW` '	C		configuration	OL = 25 μΓ	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	_	_	16	IIIA				
I _{SWTMED} ⁽²⁾	00	D	Dynamic I/O current for MEDIUM	C ₁ = 25 pF	$V_{DD} = 5.0 \text{ V} \pm 10\%,$ PAD3V5V = 0	_		29	mA				
SWTMED	С		configuration	_ '	$V_{DD} = 3.3 \text{ V} \pm 10\%,$ PAD3V5V = 1	_	_	17	IIIA				
I _{SWTFST} ⁽²⁾	00	D	Dynamic I/O current	namic I/O current FAST $C_L = 25 \text{ pF}$ -nfiguration	$V_{DD} = 5.0 \text{ V} \pm 10\%,$ PAD3V5V = 0	_	_	110	mA				
'SWTFST`	С		configuration		$V_{DD} = 3.3 \text{ V} \pm 10\%,$ PAD3V5V = 1	_	_	50					
				C _L = 25 pF, 2 MHz		_	_	2.3					
								C _L = 25 pF, 4 MHz	$V_{DD} = 5.0 \text{ V} \pm 10\%,$ PAD3V5V = 0	_	_	3.2	
l	С	D	Root medium square I/O current for SLOW	C _L = 100 pF, 2 MHz		_	_	6.6	mA				
I _{RMSSLW}	С		configuration	C _L = 25 pF, 2 MHz	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	_	_	1.6					
				C _L = 25 pF, 4 MHz		_	_	2.3					
					C _L = 100 pF, 2 MHz		_	_	4.7				
				$C_L = 25 \text{ pF}, 13 \text{ MHz}$.,	_	_	6.6	mA				
			Root medium square	C _L = 25 pF, 40 MHz	$V_{DD} = 5.0 \text{ V} \pm 10\%,$ PAD3V5V = 0	_	_	13.4					
1 .	С	D	I/O current for	C _L = 100 pF, 13 MHz		_	_	18.3					
I _{RMSMED}	С			MEDIUM configuration	$C_L = 25 \text{ pF}, 13 \text{ MHz}$.,	_	_	5	mA			
			Comiguration	$C_L = 25 \text{ pF}, 40 \text{ MHz}$	$V_{DD} = 3.3 V \pm 10\%,$ PAD3V5V = 1	_	_	8.5					
				C _L = 100 pF, 13 MHz		_	_	11					

70

65

mΑ

Value Conditions⁽¹⁾ **Symbol** C **Parameter** Unit Min Тур Max $C_1 = 25 pF, 40 MHz$ 22 $V_{DD} = 5.0 \text{ V} \pm 10\%,$ $C_1 = 25 \text{ pF}, 64 \text{ MHz}$ 33 PAD3V5V = 0Root medium square $C_1 = 100 \text{ pF}, 40 \text{ MHz}$ 56 С I/O current for FAST mΑ I_{RMSFST} С $C_1 = 25 \text{ pF}, 40 \text{ MHz}$ 14 configuration $V_{DD} = 3.3 \text{ V} \pm 10\%,$ $C_1 = 25 \text{ pF}, 64 \text{ MHz}$ 20 PAD3V5V = 1 $C_1 = 100 pF, 40 MHz$ 35

 $V_{DD} = 5.0 \text{ V} \pm 10\%, \text{ PAD3V5V} = 0$

 $V_{DD} = 3.3 \text{ V} \pm 10\%, \text{ PAD3V5V} = 1$

Table 24. I/O consumption (continued)

SD

R

IAVGSEG

Sum of all the static

I/O current within a

supply segment

3.11 Main oscillator electrical characteristics

The SPC560P34/SPC560P40 provides an oscillator/resonator driver.

Table 25. Main oscillator output electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symb	۵l	С	Parameter	Conditions	Va	lue	Unit
Syllib	Oi	J	Farameter	Conditions	Min	Max	Oilit
fosc	SR	—	Oscillator frequency		4	40	MHz
g _m	_	Р	Transconductance		6.5	25	mA/V
Vosc	_	Т	Oscillation amplitude on XTAL pin		1	_	V
toscsu	_	Т	Start-up time ^{(1),(2)}		8	_	ms
		Т		4 MHz	5	30	
		Т		8 MHz	5	26	
	СС	Т	XTAL load capacitance ⁽³⁾	12 MHz	5	23	nf
CL		Т	TAL load capacitatice	16 MHz	5	19	pf
		Т		20 MHz	5	16	
		Т		40 MHz	5	8	

^{1.} The start-up time is dependent upon crystal characteristics, board leakage, etc. High ESR and excessive capacitive loads can cause long start-up time.

^{1.} V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified

^{2.} Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

^{2.} Value captured when amplitude reaches 90% of XTAL

^{3.} This value is determined by the crystal manufacturer and board design. For 4 MHz to 40 MHz crystals specified for this oscillator, load capacitors should not exceed these limits.

	in oscillator output electrical ch USRO[PAD3V5V] = 1)	aracteristics	(3.3 V,

Cumb	اء	С	Parameter (Conditions	Va	Unit		
Symb	OI		Parameter	Conditions	Min	Max	Oill	
fosc	SR	_	Oscillator frequency		4	40	MHz	
g _m	_	Р	Transconductance		4	20	mA/V	
Vosc	_	Т	Oscillation amplitude on XTAL pin		1	_	V	
toscsu	_	Т	Start-up time ^{(1),(2)}		8	_	ms	
		Т		4 MHz	5	30		
		Т		8 MHz	5	26		
	00	Т	XTAL load capacitance ⁽³⁾	12 MHz	5	23	n.f	
CL	CC	Т	TAL load capacitance	16 MHz	5	19	pf	
		Т		20 MHz	5	16		
		Т		40 MHz	5	8		

The start-up time is dependent upon crystal characteristics, board leakage, etc. High ESR and excessive capacitive loads can cause long start-up time.

Table 27. Input clock characteristics

Cum	hal	Doromotor		Unit		
Symi	DOI	Parameter	Min	Тур	Max	Unit
fosc	SR	Oscillator frequency	4	_	40	MHz
f _{CLK}	SR	Frequency in bypass	_	_	64	MHz
t _{rCLK}	SR	Rise/fall time in bypass	_	_	1	ns
t _{DC}	SR	Duty cycle	47.5	50	52.5	%

3.12 FMPLL electrical characteristics

Table 28. FMPLL electrical characteristics

Symbol	С	Parameter	Conditions ⁽¹⁾	Va	Unit	
			Conditions	Min	Max	Oilit
f _{ref_crystal} f _{ref_ext}	D	PLL reference frequency range ⁽²⁾	Crystal reference	4	40	MHz
f _{PLLIN}	D	Phase detector input frequency range (after pre-divider)	_	4	16	MHz
f _{FMPLLOUT}	D	Clock frequency range in normal mode	_	16	64	MHz

^{2.} Value captured when amplitude reaches 90% of XTAL

^{3.} This value is determined by the crystal manufacturer and board design. For 4 MHz to 40 MHz crystals specified for this oscillator, load capacitors should not exceed these limits.

Table 28. FMPLL electrical characteristics (continued)

Symbol	С	Po	ramatar	Conditions ⁽¹⁾	Va	lue	Unit
Symbol		Parameter		Conditions	Min	Max	Offic
f _{FREE}	Р	Free-running frequ	uency	Measured using clock division—typically /16	20	150	MHz
t _{CYC}	D	System clock perio	od	_	_	1 / f _{SYS}	ns
f _{LORL}	D	Loss of reference	frequency window ⁽³⁾	Lower limit	1.6	3.7	MHz
f _{LORH}	D	LOSS OF TETETICE	nequency window	Upper limit	24	56	IVIHZ
f _{SCM}	D	Self-clocked mode	e frequency ^{(4),(5)}	_	20	150	MHz
			Short-term jitter ⁽¹⁰⁾	f _{SYS} maximum	-4	4	% f _{CLKOUT}
C _{JITTER}	Т	CLKOUT period jitter ^{(6),(7),(8),(9)}	Long-term jitter (average over 2 ms interval)	f _{PLLIN} = 16 MHz (resonator), f _{PLLCLK} at 64 MHz, 4000 cycles	_	10	ns
t _{lpll}	D	PLL lock time ^{(11), (}	(12)	_	_	200	μs
t _{dc}	D	Duty cycle of refer	ence	_	40	60	%
f _{LCK}	D	Frequency LOCK	range	_	-6	6	% f _{SYS}
f _{UL}	D	Frequency un-LO	CK range	_	-18	18	% f _{SYS}
f _{CS}	D	Modulation depth		Center spread	±0.25	±4.0 (13)	% f _{SYS}
f _{DS}	D			Down spread	-0.5	-8.0	
f _{MOD}	D	Modulation freque	ncy ⁽¹⁴⁾	_	_	70	kHz

- 1. $V_{DD_LV_CORx} = 1.2 \text{ V} \pm 10\%$; $V_{SS} = 0 \text{ V}$; $T_A = -40 \text{ to } 125 \text{ °C}$, unless otherwise specified
- 2. Considering operation with PLL not bypassed.
- 3. "Loss of Reference Frequency" window is the reference frequency range outside of which the PLL is in self clocked mode.
- Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.
- f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
- 6. This value is determined by the crystal manufacturer and board design.
- 7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DD_LV_COR0} and V_{SS_LV_COR0} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
- 8. Proper PC board layout procedures must be followed to achieve specifications.
- 9. Values are obtained with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
- 10. Short term jitter is measured on the clock rising edge at cycle n and cycle n+4.
- 11. This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
- 12. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
- 13. This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).
- 14. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.13 16 MHz RC oscillator electrical characteristics

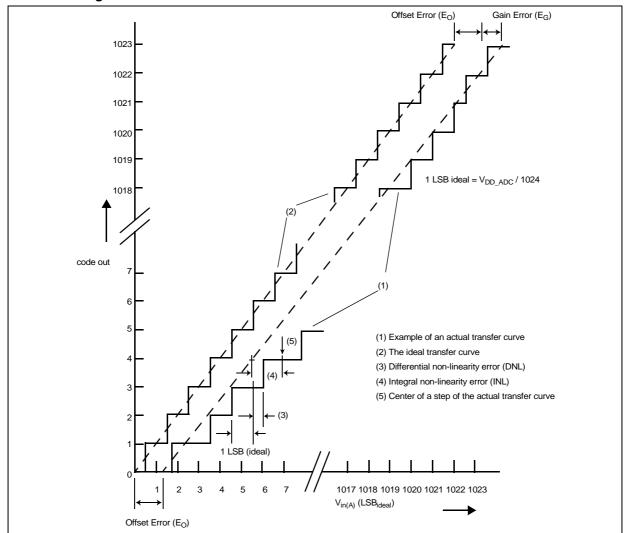
Table 29. 16 MHz RC oscillator electrical characteristics

Symbol	_	Parameter	Conditions		Unit		
		i arameter	Conditions	Min	Тур	Max	
f _{RC}	Р	RC oscillator frequency	T _A = 25 °C	_	16	—	MHz
$\Delta_{\sf RCMVAR}$	Р	Fast internal RC oscillator variation over temperature and supply with respect to f_{RC} at T_A = 25 °C in high-frequency configuration	_	-5	_	5	%

3.14 Analog-to-digital converter (ADC) electrical characteristics

The device provides a 10-bit Successive Approximation Register (SAR) analog-to-digital converter.

Figure 15. ADC characteristics and error definitions



3.14.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the source impedance value of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

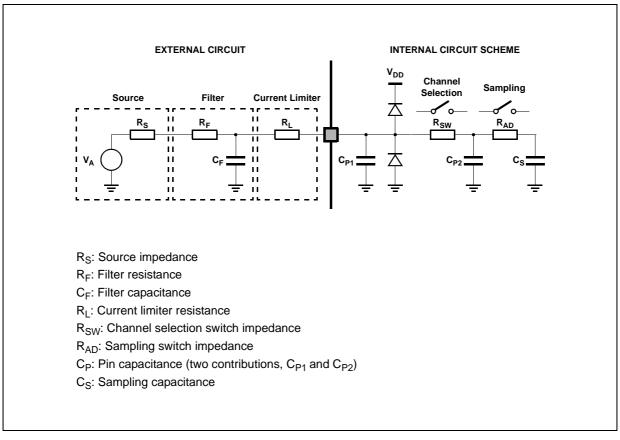
In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S and C_{P2} being substantially two switched capacitances, with a frequency equal to the ADC conversion rate, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with $C_S + C_{P2}$ equal to 3 pF, a resistance of 330 k Ω is obtained ($R_{EQ} = 1$ / (fc × ($C_S + C_{P2}$)), where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on $C_S + C_{P2}$) and the sum of $R_S + R_F$, the external circuit must be designed to respect the *Equation 4*:

Equation 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2}LSB$$

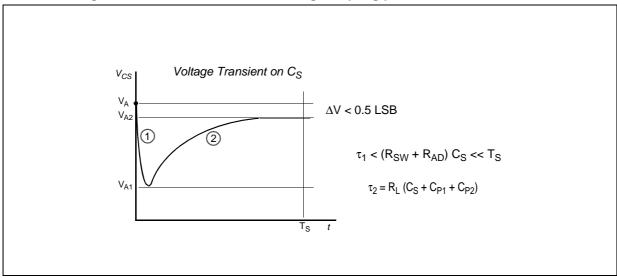
Equation 4 generates a constraint for external network design, in particular on resistive path.

Figure 16. Input equivalent circuit



A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F , C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in *Figure 16*): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch closed).

Figure 17. Transient behavior during sampling phase



In particular two different transient periods can be distinguished:

A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call C_P = C_{P1} + C_{P2}), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \cdot C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S , determining a new value of the voltage V_{A1} on the capacitance according to *Equation 7*:

Equation 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S , a constraints on R_1 sizing is obtained:

Equation 9

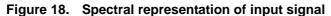
$$8.5 \bullet \tau_2 = 8.5 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

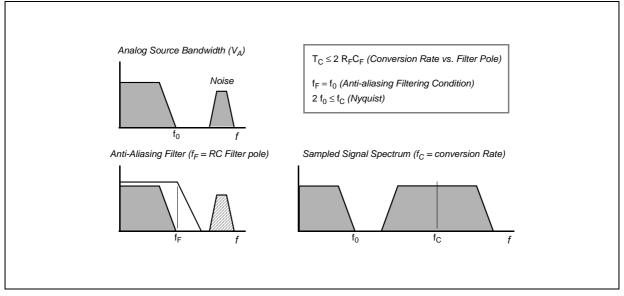
Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1} , C_{P2} and C_S , then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1} . Equation 10 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Equation 10

$${\rm V}_{\rm A2} \bullet ({\rm C}_{\rm S} + {\rm C}_{\rm P1} + {\rm C}_{\rm P2} + {\rm C}_{\rm F}) \\ = {\rm V}_{\rm A} \bullet {\rm C}_{\rm F} + {\rm V}_{\rm A1} \bullet ({\rm C}_{\rm P1} + {\rm C}_{\rm P2} + {\rm C}_{\rm S})$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A ; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S) . The filter is typically designed to act as anti-aliasing.





Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C) . Again the conversion period T_C is longer than the sampling time T_S , which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S , so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S ; from the two charge balance equations above, it is simple to derive *Equation 11* between the ideal and real sampled voltage on C_S :

Equation 11

$$\frac{v_A}{v_{A2}} = \frac{c_{P1} + c_{P2} + c_F}{c_{P1} + c_{P2} + c_F + c_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Equation 12

$$C_F > 2048 \cdot C_S$$

3.14.2 ADC conversion characteristics

Table 30. ADC conversion characteristics

0		_	Parameter.	O (1)		Value		1114
Symbo	OI	С	Parameter	Conditions ⁽¹⁾	Min	Тур	Max	Unit
f _{CK}	S R		ADC clock frequency (depends on ADC configuration) (The duty cycle depends on ADC clock ⁽²⁾ frequency)	_	3 ⁽³⁾	_	60	MHz
f _s	S R	_	Sampling frequency	_		_	1.53	MHz
t _s	_	D	Sampling time ⁽⁴⁾	f_{ADC} = 20 MHz, INPSAMP = 3 f_{ADC} = 9 MHz, INPSAMP = 255	125 —	_	 28.2	ns µs
t _c	_	Р	Conversion time ⁽⁵⁾	f _{ADC} = 20 MHz ⁽⁶⁾ , INPCMP = 1	0.65 0	_	_	μs
t _{ADC_P}	S R	_	ADC power-up delay (time needed for ADC to settle exiting from software power down; PWDN bit = 0)	_	_	_	1.5	μs
C _S ⁽⁷⁾	_	D	ADC input sampling capacitance	_	_	_	2.5	pF
C _{P1} ⁽⁷⁾	_	D	ADC input pin capacitance 1	_	_	_	3	pF
C _{P2} ⁽⁷⁾	ı	D	ADC input pin capacitance 2	_		_	1	pF
R _{SW} ⁽⁷⁾	_	D	Internal resistance of analog source	$V_{DD_HV_ADC0} = 5 \text{ V} \pm 10\%$ $V_{DD_HV_ADC0} = 3.3 \text{ V} \pm 10\%$	_	_	0.6	kΩ kΩ
R _{AD} ⁽⁷⁾	_	D	Internal resistance of analog source	_	_	_	2	kΩ
I _{INJ}	ı	Т	Input current injection	Current injection on one ADC input, different from the converted one. Remains within TUE specification	-5	_	5	mA
INL	$\circ \circ$	Р	Integral non-linearity	No overload	-1.5	_	1.5	LSB
DNL	\circ	Р	Differential non-linearity	No overload	-1.0	_	1.0	LSB
E _O	СС	Т	Offset error	_	l	±1	_	LSB
E _G	CC	Т	Gain error	_	_	±1	_	LSB
TUE	СС	Р	Total unadjusted error without current injection	_	-2.5	_	2.5	LSB
TUE	C Total unadjusted error with current		-3	_	3	LSB		

^{1.} V_{DD} = 3.3 V to 3.6 V / 4.5 V to 5.5 V, T_A = -40 °C to T_{A MAX}, unless otherwise specified and analog input voltage from V_{SS_HV_ADC0} to V_{DD_HV_ADC0}.

^{2.} AD_clk clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.

^{3.} When configured to allow 60 MHz ADC, the minimum ADC clock speed is 9 MHz, below which the precision is lost.

- 4. During the sampling time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_s. After the end of the sampling time t_s, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_s depend on programming.
- 5. This parameter includes the sampling time t_s.
- 6. 20 MHz ADC clock. Specific prescaler is programmed on MC_PLL_CLK to provide 20 MHz clock to the ADC.
- 7. See Figure 16.

3.15 Flash memory electrical characteristics

3.15.1 Program/Erase characteristics

Table 31. Program and erase specifications

				Val	ue		
Symbol	С	Parameter	Min	Typ ⁽¹⁾	Initial Max ⁽²⁾	Max ⁽³⁾	Unit
T _{wprogram}	Р	Word Program Time for data flash memory ⁽⁴⁾	_	30	70	500	μs
T _{dwprogram}	Р	Double Word Program Time for code flash memory ⁽⁴⁾	_	22	50	500	μs
	Р	Bank Program (256 KB) ⁽⁴⁾⁽⁵⁾	_	0.73	0.83	17.5	s
T _{BKPRG}	Р	Bank Program (64 KB) ⁽⁴⁾⁽⁵⁾	_	0.49	1.2	4.1	s
Т	Р	16 KB Block Pre-program and Erase Time for code flash memory	_	300	500	5000	ms
T _{16kpperase}		16 KB Block Pre-program and Erase Time for data flash memory	_	700	800	5000	1113
T _{32kpperase}	Р	32 KB Block Pre-program and Erase Time	_	400	600	5000	ms
T _{128kpperase}	Ρ	128 KB Block Pre-program and Erase Time	_	800	1300	7500	ms
t _{ESRT}	Р	Program and erase specifications ⁽⁶⁾	10	1	1	_	ms

Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

6. Time between erase suspend resume and next erase suspend request.

^{2.} Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

^{3.} The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

^{4.} Actual hardware programming times. This does not include software overhead.

^{5.} Typical Bank programming time assumes that all cells are programmed in a single pulse. In reality some cells will require more than one pulse, adding a small overhead to total bank programming time (see "Initial Max" column).

Table 32. Flash memory module life

Symbol	С	Parameter	Conditions	Val	ue	Unit
Symbol	C	Farameter	Conditions	Min	Тур	Ollit
P/E	С	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T _J)	_	100000	_	cycles
P/E	С	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T _J)	_	10000	100000	cycles
P/E	С	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T _J)	_	1000	100000	cycles
			Blocks with 0–1000 P/E cycles	20	_	years
Retention	C Minimum data retention at 85 °C average ambient temperature ⁽¹⁾	Blocks with 10000 P/E cycles	10	_	years	
		average ambient temperature(1)	Blocks with 100000 P/E cycles	5	_	years

Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

Table 33. Flash memory read access timing

Symbol	С	Parameter	Conditions ⁽¹⁾	Max value	Unit
f	_	Maximum working frequency for code flash memory at given	2 wait states	66	MHz
T _{max}		number of wait states in worst conditions	0 wait states	18	IVII IZ
f _{max}	С	Maximum working frequency for data flash memory at given number of wait states in worst conditions	8 wait states	66	MHz

^{1.} $V_{DD} = 3.3 \text{ V} \pm 10\% / 5.0 \text{ V} \pm 10\%$, $T_A = -40 \text{ to } 125 \,^{\circ}\text{C}$, unless otherwise specified

3.15.2 Flash memory power supply DC characteristics

Table 34 shows the power supply DC characteristics on external supply.

Table 34. Flash memory power supply DC electrical characteristics

Symbol		(Parameter	Conditions ⁽¹⁾		Unit			
		C	r arameter	Conditions	Min	Тур	Max	Oiiit	
I _{FLPW}	C C	D	Sum of the current consumption on V _{DD_HV_IOx} and V _{DD_LV_CORx} during low-power mode	Code flash memory	_	_	900	μA	
1	С	7	Sum of the current consumption on V _{DD_HV_IOx}	Code flash memory	_	_	150		
I _{FPWD} C	j D	; D	C D an	C D Sum of the current consumption on V _{DD_HV_IOx} and V _{DD_LV_CORx} during power-down mode	Data flash memory	_	_	150	μΑ

^{1.} V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

3.15.3 Start-up/Switch-off timings

Table 35. Start-up time/Switch-off time

Symbol		С	Parameter	Conditions ⁽¹⁾			Unit	
Symbol)	ralametei	Conditions	Min	Тур	Max	
T _{FLARSTEXIT}	СС	Т	Delay for Flash module to exit reset mode	Code flash memory	_	_	125	
	C	Т		Data flash memory	_	_	125	
T _{FLALPEXIT}	СС	D	Delay for Flash module to exit low-power mode	Code flash memory	_	_	0.5	110
T _{FLAPDEXIT}	CC	Т	Delay for Flash module to exit power-down mode	Code flash memory	_	_	30	μs
	C	Т	mode	Data flash memory	_	_	30	
T _{FLALPENTRY}	СС	D	Delay for Flash module to enter low-power mode	Code flash memory	_	_	0.5	

^{1.} V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 to 125 °C, unless otherwise specified.

3.16 AC specifications

3.16.1 Pad AC specifications

Table 36. Output pin transition times

Sum	hal	С	Parameter	Co	nditions ⁽¹⁾		Value)	Unit		
Sym	DOI	C	raiailletei		nations. /	Min	Тур	Max	Onit		
		D		C _L = 25 pF		_	_	50			
		Т		C _L = 50 pF	$V_{DD} = 5.0 \text{ V} \pm 10\%,$ PAD3V5V = 0	_	_	100			
	CC D		Output transition time output pin ⁽²⁾	C _L = 100 pF		_	_	125	ne		
t _{tr}	" D	D	SLOW configuration	C _L = 25 pF		_	_	40	ns		
		Т		C _L = 50 pF	$V_{DD} = 3.3 \text{ V} \pm 10\%,$ PAD3V5V = 1	_	_	50			
		D		C _L = 100 pF		_	_	75			
		D	-	C _L = 25 pF	$V_{DD} = 5.0 \text{ V} \pm 10\%,$	_	_	10			
		CC D	D		C _L = 50 pF	PAD3V5V = 0	_	_	20		
	t _{tr} CC D			D	D	Output transition time output pin ⁽²⁾	C _L = 100 pF	SIUL.PCRx.SRC = 1	_	_	40
^L tr			MEDIUM configuration	C _L = 25 pF	$V_{DD} = 3.3 \text{ V} \pm 10\%,$	_	_	12	ns		
			Т		C _L = 50 pF	PAD3V5V = 1	_	_	25		
		D		C _L = 100 pF	SIUL.PCRx.SRC = 1	_	_	40			

Value Conditions⁽¹⁾ Symbol **Parameter** Unit Min Тур Max $C_{L} = 25 pF$ 4 $V_{DD} = 5.0 \text{ V} \pm 10\%,$ PAD3V5V = 0 $C_L = 50 pF$ 6 SIUL.PCRx.SRC = 1 $C_1 = 100 pF$ 12 Output transition time output pin⁽²⁾ CC D ns t_{tr} FAST configuration $C_{L} = 25 \text{ pF}$ 4 $V_{DD} = 3.3 \text{ V} \pm 10\%,$ $C_{L} = 50 \text{ pF}$ PAD3V5V = 17 SIUL.PCRx.SRC = 1 $C_1 = 100 pF$ 12 $V_{DD} = 5.0 \text{ V} \pm 10\%, \text{ PAD3V5V} = 0$ Symmetric transition time, same drive t_{SYM} CC T ns strength between N and P transistor $V_{DD} = 3.3 \text{ V} \pm 10\%, \text{ PAD3V5V} = 1$ 5

Table 36. Output pin transition times (continued)

- 1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 °C to $T_{A~MAX}$, unless otherwise specified.
- 2. C_L includes device and package capacitances ($C_{PKG} < 5 pF$).
- 3. Transition timing of both positive and negative slopes will differ maximum 50%.

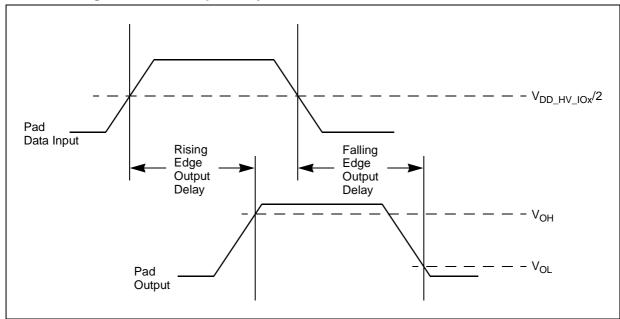


Figure 19. Pad output delay

3.17 AC timing characteristics

3.17.1 RESET pin characteristics

The SPC560P34/SPC560P40 implements a dedicated bidirectional RESET pin.

V_{RESET}
V_I
V_I
V_I
V_I
device reset forced by V_{RESET}
t_{POR}
device start-up phase

Figure 20. Start-up reset requirements



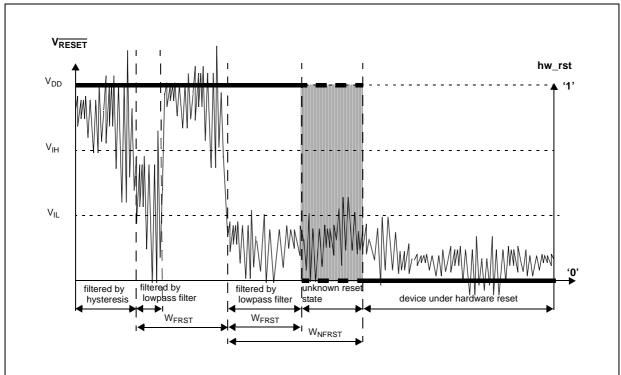


Table 37. RESET electrical characteristics

Cumba		_	Dovernotor	Conditions ⁽¹⁾		Value ⁽²	nlue ⁽²⁾	
Symbo)I	С	Parameter	Conditions	Min	Тур	Max	Unit
V _{IH}	S R	Р	Input high level CMOS (Schmitt Trigger)	_	0.65V _{DD}		V _{DD} + 0.4	V
V _{IL}	S R	Р	Input low level CMOS (Schmitt Trigger)	_	-0.4	l	0.35V _{DD}	V
V _{HYS}	$\circ \circ$	С	Input hysteresis CMOS (Schmitt Trigger)	_	0.1V _{DD}	1	1	٧
				Push Pull, $I_{OL} = 2$ mA, $V_{DD} = 5.0$ V \pm 10%, PAD3V5V $=$ 0 (recommended)	ı	l	0.1V _{DD}	
V _{OL}	C C	Р	Output low level	Push Pull, $I_{OL} = 1 \text{ mA}$, $V_{DD} = 5.0 \text{ V} \pm 10\%$, PAD3V5V = $1^{(3)}$			0.1V _{DD}	V
				Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	_	_	0.5	
				$C_L = 25 \text{ pF},$ $V_{DD} = 5.0 \text{ V} \pm 10\%, \text{ PAD3V5V} = 0$	_	_	10	
			$C_L = 50 \text{ pF},$ $V_{DD} = 5.0 \text{ V} \pm 10\%, \text{ PAD3V5V} = 0$		_	20		
	С	D	Output transition time output pin ⁽⁴⁾ MEDIUM	$C_L = 100 \text{ pF},$ $V_{DD} = 5.0 \text{ V} \pm 10\%, \text{ PAD3V5V} = 0$	l		40	ns
t _{tr}	С		configuration	$C_L = 25 \text{ pF},$ $V_{DD} = 3.3 \text{ V} \pm 10\%, \text{ PAD3V5V} = 1$	1	l	12	113
				$C_L = 50 \text{ pF},$ $V_{DD} = 3.3 \text{ V} \pm 10\%, \text{ PAD3V5V} = 1$	1	l	25	
				$C_L = 100 \text{ pF},$ $V_{DD} = 3.3 \text{ V} \pm 10\%, \text{ PAD3V5V} = 1$	1	l	40	
W _{FRST}	S R	Р	RESET input filtered pulse	_		-	40	ns
W _{NFRST}	S R	Р	RESET input not filtered pulse	_	500	1	ı	ns
t _{POR}	СС	D	Maximum delay before internal reset is released after all V _{DD_HV} reach nominal supply	Monotonic V _{DD_HV} supply ramp	_	_	1	ms
	_		Wash and o	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	_	150	
I _{WPU}	C	Р	Weak pull-up current absolute value	$V_{DD} = 5.0 \text{ V} \pm 10\%, \text{ PAD3V5V} = 0$	10	_	150	μΑ
				$V_{DD} = 5.0 \text{ V} \pm 10\%, \text{ PAD3V5V} = 1^{(5)}$	10	_	250	

^{1.} V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_{A} = -40 to 125 °C, unless otherwise specified

^{3.} This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of device reference manual).



^{2.} All values need to be confirmed during device validation.

- 4. C_L includes device and package capacitance (C_{PKG} < 5 pF).
- 5. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.17.2 IEEE 1149.1 interface timing

Table 38. JTAG pin AC electrical characteristics

No	Symbo		С	Parameter	Conditions	Va	lue	Unit
-	Syllibo	1	C	raiametei	Conditions	Min	Max	Ollic
1	t _{JCYC}	CC	D	TCK cycle time	_	100	_	ns
2	t _{JDC}	СС	D	TCK clock pulse width (measured at V _{DD_HV_IOx} /2)	_	40	60	ns
3	t _{TCKRISE} CC		D	TCK rise and fall times (40%–70%)	_	_	3	ns
4	t _{TMSS} , t _{TDIS} CC		D	TMS, TDI data setup time	_	5	_	ns
5	t _{TMSH} , CC		D	TMS, TDI data hold time	_	25	_	ns
6	t _{TDOV}	СС	D	TCK low to TDO data valid	_	_	40	ns
7	t _{TDOI}	СС	D	TCK low to TDO data invalid	_	0	_	ns
8	t _{TDOHZ}	CC	D	TCK low to TDO high impedance	_	40	_	ns
9	t _{BSDV}	СС	D	TCK falling edge to output valid	_	_	50	ns
10	t _{BSDVZ} CC		D	TCK falling edge to output valid out of high impedance	_	_	50	ns
11	t _{BSDHZ} CC		D	TCK falling edge to output high impedance	_	_	50	ns
12	t _{BSDST}	СС	D	Boundary scan input valid to TCK rising edge	_	50	—	ns
13	t _{BSDHT}	СС	D	TCK rising edge to boundary scan input invalid	_	50		ns

Figure 22. JTAG test clock input timing

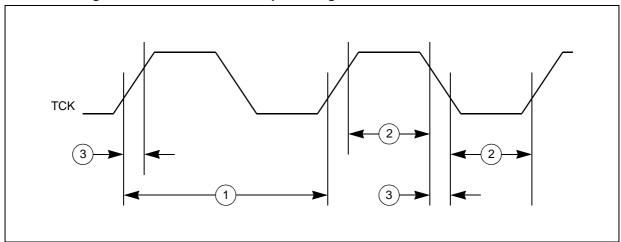


Figure 23. JTAG test access port timing

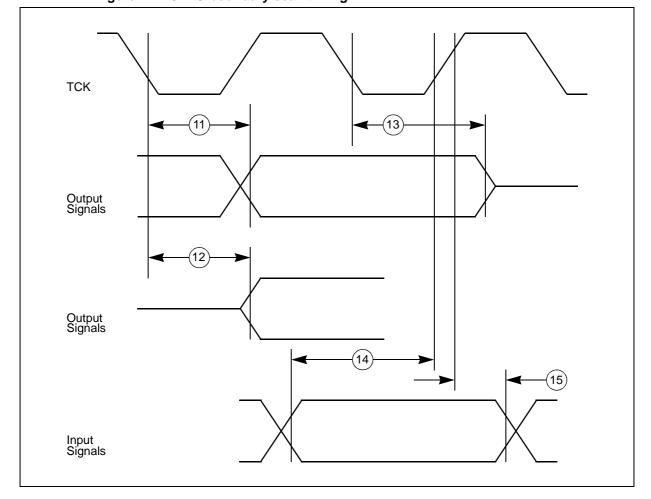


Figure 24. JTAG boundary scan timing

3.17.3 Nexus timing

Table 39. Nexus debug port timing⁽¹⁾

NI -	0			Barrandar		Value	Value									
No.	Symbo	Зушрог		Symbol		Symbol		Symbol		ool C		Parameter	Min	Тур	Max	Unit
1	t _{TCYC}	CC	D	TCK cycle time	4 ⁽²⁾	_	_	t _{CYC}								
2	t _{NTDIS}	CC	D	TDI data setup time	5	_	_	ns								
2	t _{NTMSS}	СС	D	TMS data setup time	5	_	_	ns								
3	t _{NTDIH}	СС	D	TDI data hold time	25	_	_	ns								
3	t _{NTMSH}	СС	D	TMS data hold time	25	_	_	ns								
4	t _{TDOV}	СС	D	TCK low to TDO data valid	10	_	20	ns								
5	t _{TDOI}	CC	D	TCK low to TDO data invalid	_	_	_	ns								

^{1.} All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.

^{2.} Lower frequency is required to be fully compliant to standard.

Figure 25. Nexus output timing

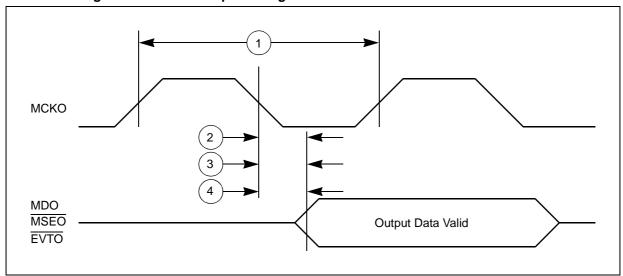
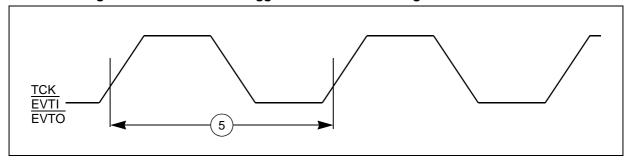


Figure 26. Nexus event trigger and test clock timing



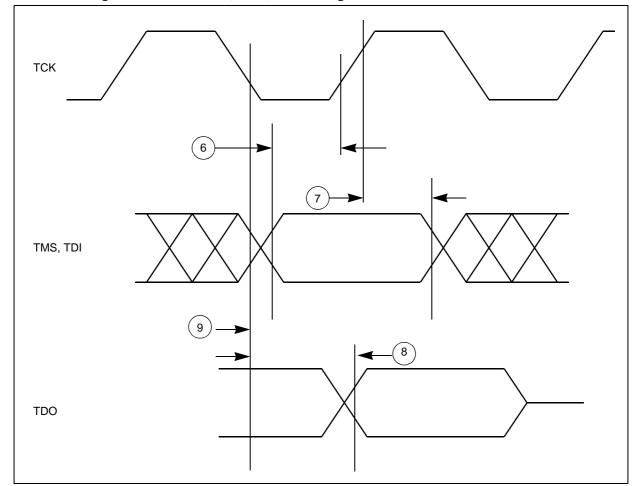


Figure 27. Nexus TDI, TMS, TDO timing

3.17.4 External interrupt timing (IRQ pin)

Table 40. External interrupt timing⁽¹⁾

No	No. Symbol		С	Parameter	Conditions	Valu	ıe	Unit
NO.			נ	Farameter	Conditions	Min	Max	Oilit
1	t _{IPWL}	СС	D	IRQ pulse width low	_	4	_	t _{CYC}
2	t _{IPWH}	СС	D	IRQ pulse width high	_	4	_	t _{CYC}
3	t _{ICYC}	СС	D	IRQ edge to edge time ⁽²⁾	_	4 + N (3)	_	t _{CYC}

- 1. IRQ timing specified at $f_{SYS} = 64$ MHz and $V_{DD_HV_IOx} = 3.0$ V to 5.5 V, $T_A = T_L$ to T_H , and $C_L = 200$ pF with SRC = 0b00
- 2. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.
- 3. N = ISR time to clear the flag

IRQ 1

Figure 28. External interrupt timing

3.17.5 DSPI timing

Table 41. DSPI timing⁽¹⁾

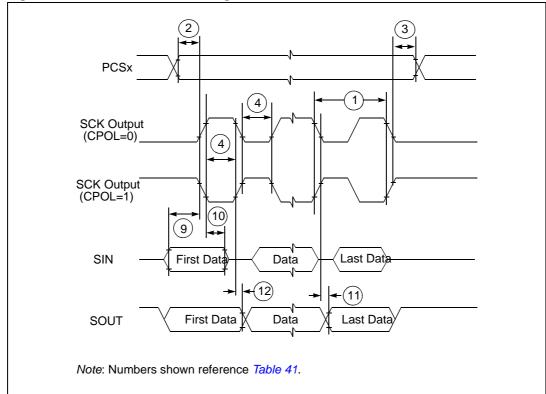
Iabit	; 41.	וטט	1 (111	ning` ′				
No.	Symi	h a l	С	Parameter	Conditions	Val	ue	Unit
NO.	Syllii	DOI	C	Farameter	Conditions	Min	Max	Unit
1	4	СС	D	DSPI cycle time	Master (MTFE = 0)	60	_	no
•	t _{SCK}	CC	D	DSFI Cycle time	Slave (MTFE = 0)	60	_	ns
2	t _{CSC}	СС	D	CS to SCK delay	_	16	_	ns
3	t _{ASC}	СС	D	After SCK delay	_	26	_	ns
4	t _{SDC}	СС	D	SCK duty cycle	_	0.4 * t _{SCK}	0.6 * t _{SCK}	ns
5	t _A	СС	D	Slave access time	SS active to SOUT valid	_	30	ns
6	t _{DIS}	СС	D	Slave SOUT disable time	SS inactive to SOUT high impedance or invalid	_	16	ns
7	t _{PCSC}	СС	D	PCSx to PCSS time	_	13	_	ns
8	t _{PASC}	СС	D	PCSS to PCSx time	_	13	_	ns
					Master (MTFE = 0)	35	_	
9		СС	D	Data actus tima for innuta	Slave	4	_	
9	t _{SUI}	CC	D	Data setup time for inputs	Master (MTFE = 1, CPHA = 0)	35	_	ns
					Master (MTFE = 1, CPHA = 1)	35	_	
					Master (MTFE = 0)	- 5	_	
10		00	_	Data hald time for inputs	Slave	4	_	
10	t _{HI}	CC	<u> </u>	Master (MTFE = 1, CPHA = 0)	11	_	ns	
				Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)		-5	_	

Table 41. DSPI timing⁽¹⁾ (continued)

No.	Cyml	hal	С	Parameter Conditions		Value		Unit
NO.	Symbol C		C	Farameter	Conditions	Min	Max	Ullit
					Master (MTFE = 0)	_	12	
				Data valid (after SCK edge)	Slave	_	36	
11	t _{SUO} C	СС	D		Master (MTFE = 1, CPHA = 0)	_	12	ns
					Master (MTFE = 1, CPHA = 1)	_	12	
					Master (MTFE = 0)	-2	_	
12	2 t _{HO} CC D Data hold time for outputs	Slave	6		ns			
12		HO CC D Data Hold	Data Hold time for outputs	Master (MTFE = 1, CPHA = 0)	6	_	113	
					Master (MTFE = 1, CPHA = 1)	-2	_	

^{1.} All timing are provided with 50 pF capacitance on output, 1 ns transition time on input signal





SCK Output (CPOL=0)

SCK Output (CPOL=1)

SIN

First Data

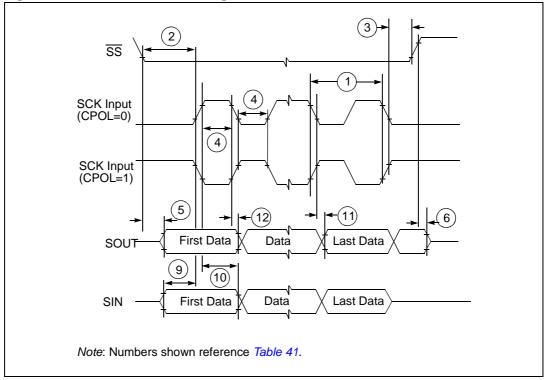
Data

Last Data

Note: Numbers shown reference Table 41.

Figure 30. DSPI classic SPI timing – Master, CPHA = 1





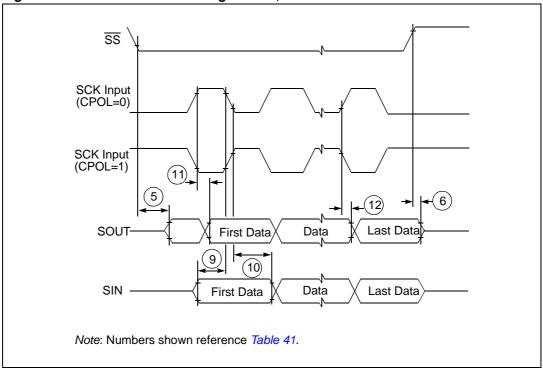
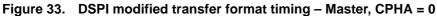
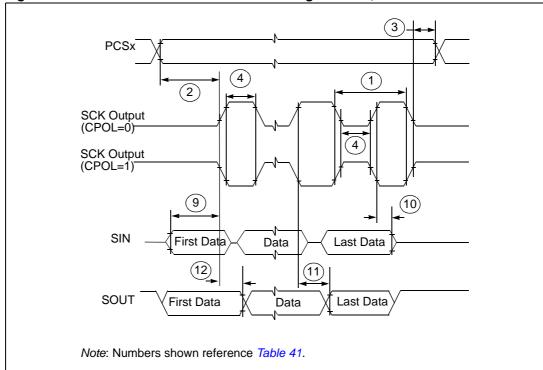


Figure 32. DSPI classic SPI timing – Slave, CPHA = 1





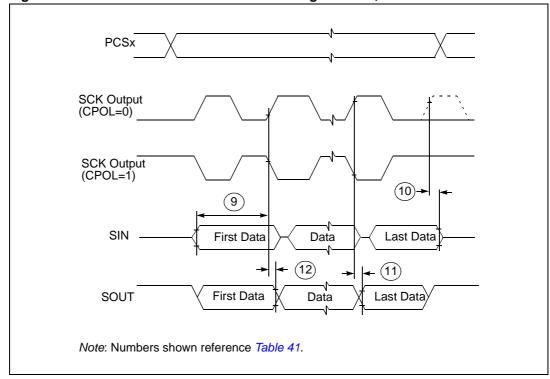
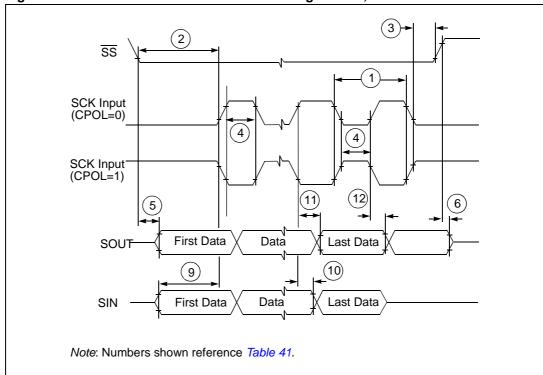


Figure 34. DSPI modified transfer format timing - Master, CPHA = 1





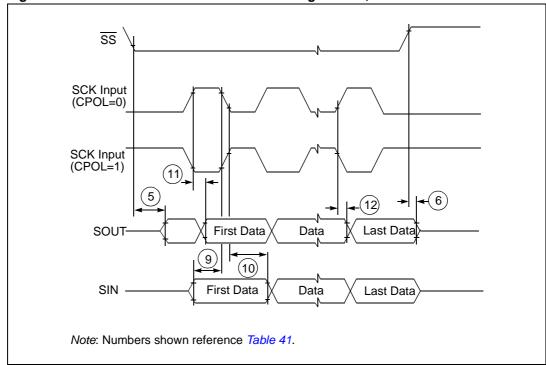
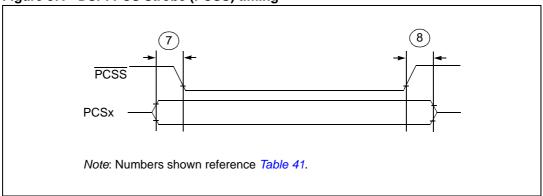


Figure 36. DSPI modified transfer format timing – Slave, CPHA = 1

Figure 37. DSPI PCS Strobe (PCSS) timing



4 Package characteristics

4.1 ECOPACK[®]

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

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4.2 Package mechanical data

4.2.1 LQFP100 mechanical outline drawing

Figure 38. LQFP100 package mechanical drawing

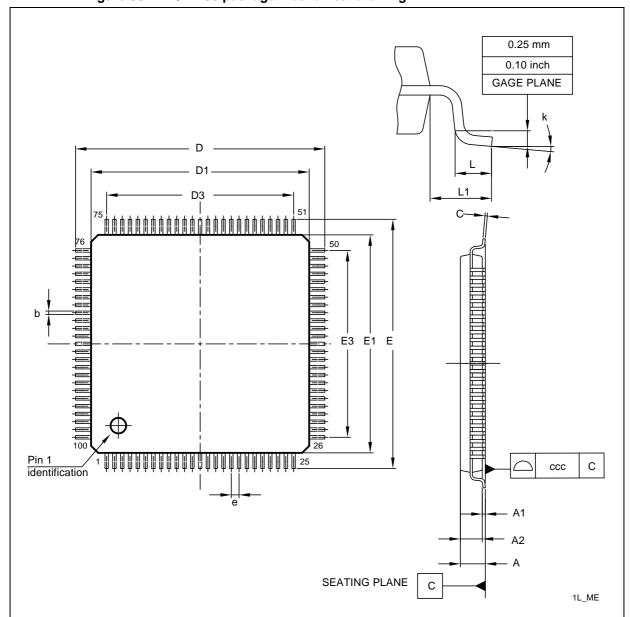


Table 42. LQFP100 package mechanical data

	Dimensions							
Symbol		mm		inches ⁽¹⁾				
	Min	Тур	Max	Min	Тур	Max		
Α	_	_	1.600	_	_	0.0630		
A1	0.050	_	0.150	0.0020	_	0.0059		
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571		
b	0.170	0.220	0.270	0.0067	0.0087	0.0106		
С	0.090	_	0.200	0.0035	_	0.0079		
D	15.800	16.000	16.200	0.6220	0.6299	0.6378		
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591		
D3	_	12.000	_	_	0.4724	_		
Е	15.800	16.000	16.200	0.6220	0.6299	0.6378		
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591		
E3	_	12.000	_	_	0.4724	_		
е	_	0.500	_	_	0.0197	_		
L	0.450	0.600	0.750	0.0177	0.0236	0.0295		
L1	_	1.000	_	_	0.0394	_		
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°		
ccc ⁽²⁾	0.08			0.0031				

^{1.} Values in inches are converted from millimeters (mm) and rounded to four decimal digits.

^{2.} Tolerance

4.2.2 LQFP64 mechanical outline drawing

Figure 39. LQFP64 package mechanical drawing

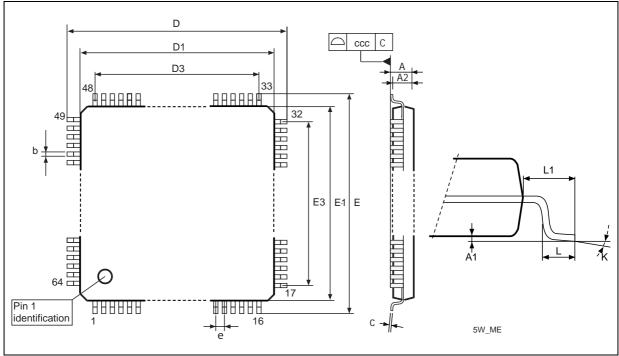


Table 43. LQFP64 package mechanical data

	Dimensions							
Symbol		mm		inches ⁽¹⁾				
	Min	Тур	Max	Min	Тур	Max		
А	_	_	1.6	_	_	0.063		
A1	0.05	_	0.15	0.002	_	0.0059		
A2	1.35	1.4	1.45	0.0531	0.0551	0.0571		
b	0.17	0.22	0.27	0.0067	0.0087	0.0106		
С	0.09	_	0.2	0.0035	_	0.0079		
D	11.8	12	12.2	0.4646	0.4724	0.4803		
D1	9.8	10	10.2	0.3858	0.3937	0.4016		
D3	_	7.5	_	_	0.2953	_		
Е	11.8	12	12.2	0.4646	0.4724	0.4803		
E1	9.8	10	10.2	0.3858	0.3937	0.4016		
E3	_	7.5	_	_	0.2953	_		
е	_	0.5	_	_	0.0197	_		
L	0.45	0.6	0.75	0.0177	0.0236	0.0295		
L1	_	1	_	_	0.0394	_		

Table 43. LQFP64 package mechanical data (continued)

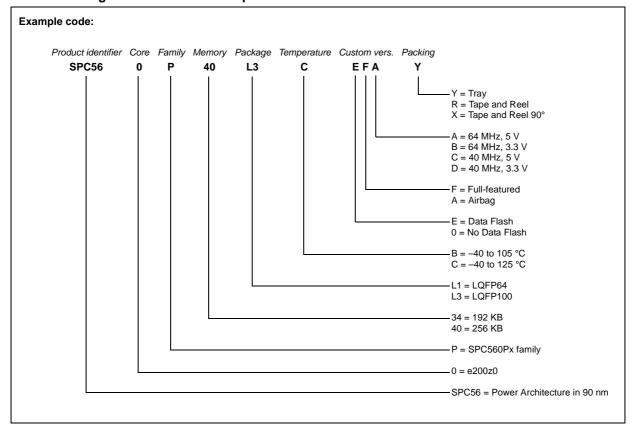
	Dimensions							
Symbol		mm		inches ⁽¹⁾				
	Min	Тур	Max	Min	Тур	Max		
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°		
ccc ⁽²⁾	0.08				0.0031			

^{1.} Values in inches are converted from millimeters (mm) and rounded to four decimal digits.

^{2.} Tolerance

5 Ordering information

Figure 40. Commercial product code structure



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Appendix A Abbreviations

Table 44 lists abbreviations used in this document.

Table 44. Abbreviations

Abbreviation	Meaning
CMOS	Complementary metal-oxide-semiconductor
СРНА	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
DUT	Device under test
ECC	Error code correction
EVTO	Event out
GPIO	General purpose input / output
MC	Modulus counter
МСКО	Message clock out
MCU	Microcontroller unit
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
NPN	Negative-positive-negative
NVUSRO	Non-volatile user options register
PTF	Post trimming frequency
PWM	Pulse width modulation
RISC	Reduced instruction set computer
SCK	Serial communications clock
SOUT	Serial data out
TBC	To be confirmed
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select

Revision history

Table 45. Document revision history

Date	Revision	Changes
01-Sep-2009	1	Initial release.
21-May-2010	2	Editorial updates Updated the following items in the "SPC560P34/SPC560P40 device comparison" table: - The heading - The "SRAM" row - The "FlexCAN" row - The "FlexCAN" row - The "FlexCAN" row - The "FlexPWM" row - The "SPI" row - The "SPI" row - The "SPSP" row - The "SPSP" row - The "SPSP" row Updated the "SPC560P34/SPC560P40 device configuration difference" table: - Editorial updates - Added the "CTU" row - Deleted the "temperature" row - Swapped the content of Airbag and Full Featured cells Added the "Wakeup unit" block in the SPC560P34/SPC560P40 block diagram Updated the "Absolute Maximum Ratings" table Updated the "Recommended operating conditions (5.0 V)" table Updated the "Recommended operating conditions (5.0 V)" table Updated the "Thermal characteristics for 100-pin LQFP" table: - Ψ _{JT} : changed the typical value Updated the "EMI testing specifications" table: replaced all values in "Level (Max)" column with TBD Updated the "Electrical characteristics" section: - Added the "Parameter classification" section - Added the "Parameter classification" section - Added the "NUSRO register" section - Added the "NUSRO register section - Added the "Independent ADC supply (-0.3 V ≤ V _{DD_HV_REG} ≤ 6.0 V)" figure - Added the "Power supplies constraints (3.0 V ≤ V _{DD_HV_REG} ≤ 5.5 V)" figure - Added the "Power supplies constraints (3.0 V ≤ V _{DD_HV_REG} ≤ 5.5 V)" figure - Added the "Power management electrical characteristics" section Updated the "Power ply/Down sequencing" section - Deleted the "NVUSRO register" section - Deleted the "NVUSRO register" section - Deleted the "NVUSRO register" section - Deleted all rows concerning RESET - Deleted all rows concerning RESET - Deleted Tlypp" row - Added the max value for C _{IN}

Table 45. Document revision history (continued)

Date	Revision	Changes
		Updated the "DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 0)" section:
24 May 2040	2	 Deleted all rows concerning RESET Deleted "I_{VPP}" row Added the max value for C_{IN}
21-May-2010	(continued)	Added the "I/O pad current specification" section
		Updated the Order codes table.
		Added "Appendix A"
		"Introduction" section:
		Changed title (was "Overview")
		 Updated contents
		"SPC560P34/SPC560P40 device comparison" table:
		Added sentence above table
		- Removed "FlexRay" row
		- "FlexCAN" row: removed link to footnote 2 for SPC560P34- Updated "Safety port" row for SPC560P34
		- Updated "DSPI" row for SPC560P34
		"SPC560P34/SPC560P40 block diagram": added the following blocks: MC_CGM,
		MC_ME, MC_PCU, MC_RGM, CRC, and SSCM
	3	Added "SPC560P34/SPC560P40 series block summary" table
		"Pin muxing" section: removed information on "Symmetric pads"
		"Electrical characteristics" section: — Updated "Caution" note
		- Demoted "NVUSRO register" section to subsection of "DC electrical characteristics"
		section - "NVUSRO register" section: deleted "NVUSRO[WATCHDOG_EN] field description" section
23-Dec-2010		Updated "EMI testing specifications" table
		"Low voltage monitor electrical characteristics" table: updated $V_{MLVDDOK_H}$ max value "DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)" table: removed V_{VOL_SYM} ,
		and V _{OH_SYM} rows "Supply current (5.0 V, NVUSRO[PAD3V5V] = 0)" table:
		- I _{DD_LV_CORE} , RUN—Maximum mode, 40/64 MHz: updated typ/max values
		- I _{DD_LV_CORE} , RUN—Airbag mode, 40/64 MHz: updated typ/max values
		- I _{DD_LV_CORE} , RUN—Maximum mode, "P" parameter classification: removed
		- I _{DD_FLASH} : removed rows
		- I _{DD_ADC} , Maximum mode: updated typ/max values
		- I _{DD_OSC} : updated max value
		Updated "DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)" table "Supply current (3.3 V, NVUSRO[PAD3V5V] = 1)" table:
		- I _{DD LV CORE} , RUN—Maximum mode, 40/64 MHz: updated typ/max values
		- I _{DD_LV_CORE} , RUN—Airbag mode, 40/64 MHz: updated typ/max values
		- I _{DD_FLASH} : removed rows
		- I _{DD_ADC} , Maximum mode: updated typ/max values
		- I _{DD_OSC} : updated max value
		Added "I/O consumption" table Removed "I/O weight" table

Table 45. Document revision history (continued)

Date	Revision	Changes
23-Dec-2010	3 (continued)	Updated "Main oscillator electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)" table Updated "Main oscillator electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)" table "Input clock characteristics" table: updated f _{CLK} max value "PLLMRFM electrical specifications (V _{DDPLL} = 1.08 V to 1.32 V, V _{SS} = V _{SSPLL} = 0 V, T _A = T _L to T _H)" table: - Updated supply voltage range for V _{DDPLL} in the table title - Updated supply voltage range for V _{DDPLL} in the table title - Updated f _{SCM} max value - Updated "16 MHz RC oscillator electrical characteristics" table Updated "ADC conversion characteristics" table: - T _{wprogram} : updated initial max and max values - T _{BKPRG} 64 KB: updated initial max and max values - added information about "erase time" for Data Flash "Flash module life" table: - P/E, 32 KB: added typ value - P/E, 128 KB: added typ value Replaced "Pad AC specifications (5.0 V, NVUSRO[PAD3V5V] = 0)" and "Pad AC specifications (3.3 V, INVUSRO[PAD3V5V] = 1)" tables with "Output pin transition times" table "JTAG pin AC electrical characteristics" table: - t _{TDOV} : updated max value - t _{TDOHZ} : added min value and removed max value "Nexus debug port timing" table: removed the rows "t _{MCYC} ", "t _{MDOV} ", "t _{MSEOV} ", and "t _{EVTOV} " Updated "External interrupt timing (IRQ pin)" table Updated "OsPI timing" table Updated "Ordering information" section

Table 45. Document revision history (continued)

Date	Revision	Changes
,		
13-May-2011	4	Editorial and formatting changes throughout Cover page features list: • changed core feature "64 MHz" to "Up to 64 MHz" • changed Data flash memory "64 (4 × 16) KB" to "Additional 64 (4 × 16) KB" • changed "1 FlexCAN interface" to "Up to 2 FlexCAN interface" Updated Device summary Section "Introduction": Reorganized contents SPC560P40 device configuration differences: Editorial changes to indicate that the table concerns only the SPC560P40 devices); removed "DSPI" row Block diagram (SPC560P40 full-featured configuration): reorganized blocks above and below peripheral bridge; made arrow going from peripheral bridge to crossbar switch bidirectional; removed SPC560P34 part number from title Added section "Features details" 64-pin and 100-pin LQFP pinout diagrams: replaced instances of HV_AD0 with HV_ADC0 System pins: updated "XTAL" and "EXTAL" rows Updated LQFP thermal characteristics Updated EMI testing specifications section "Voltage regulator electrical characteristics": removed BCP56 from named BJTs; replaced two configuration diagrams and two electrical characteristics tables with single diagram and single table Voltage regulator electrical characteristics: updated V _{DD_LV_REGCOR} row Low voltage monitor electrical characteristics: updated V _{DD_LV_REGCOR} row Low voltage monitor electrical characteristics: updated V _{MLVDDOK_H} max value—was 1.15 V; is 1.145 V Supply current (5.0 V, NVUSRO[PAD3V5V] = 0): changed symbol I _{DD_LV_CORx} RUN—Maximum mode at 64 MHz; added I _{DD_FLASH} characteristics; replaced instances of "Airbag" mode with "Typical mode" Supply current (3.3 V, NVUSRO[PAD3V5V] = 1): changed symbol I _{DD_LV_CORx} RUN—Maximum mode at 64 MHz; added I _{DD_FLASH} characteristics; replaced instances of "Airbag" mode with "Typical mode" DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1): corrected parameter description for V _{OL_F} —was "Fast, high level output voltage"; is "Fast, low level output voltage" Added Section 3.10.4, Input DC electrical characteristics replaced instances o

Table 45. Document revision history (continued)

Date	Revision	Changes
13-May-2011	4 (continued)	Commercial product code structure: Replaced "Conditioning" with "Packing" Table 44: added "DUT", "NPN", and "RISC"
22-Dec-2011	5	Updated <i>Table 1: Device summary</i> Updated <i>Section 1.5.28: Nexus Development Interface (NDI)</i> Section Table 2.: SPC560P34/SPC560P40 device comparison: changed Nexus L1+ with Nexus Class 1 Table 7: Pin muxing: removed E[0] row Table 9: Absolute maximum ratings: updated minumum and maximum values for TV _{DD} parameter Section 3.10: DC electrical characteristics: Removed oscillator margin. Removed Section NVUSRO[OSCILLATOR_MARGIN] field description and Table NVUSRO[OSCILLATOR_MARGIN] field description Updated Section 3.8.1: Voltage regulator electrical characteristics Updated Section Figure 10.: Voltage regulator configuration Table 16: Voltage regulator electrical characteristics: added L _{Reg} row, updated condition for C _{DEC1} , C _{DEC2} and C _{DEC3} Removed "Order codes" tables
20-Dec-2012	6	Table 9 (Absolute maximum ratings): updated TV _{DD} parameter, the minimum value to 3.0 V/s, added note on minimum value, and the maximum value to 0.5 V/µs Table 20 (Supply current (5.0 V, NVUSRO[PAD3V5V] = 0)): added I _{DD_HV_REG} row Table 22 (Supply current (3.3 V, NVUSRO[PAD3V5V] = 1)): added I _{DD_HV_REG} row Updated Section 3.14.1, Input impedance and ADC accuracy Table 30 (ADC conversion characteristics): renamed "R _{SW1} " in "R _{SW} " Table 31 (Program and erase specifications): added t _{ESRT} row
18-Sep-2013	7	Updated Disclaimer.

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Тел: +7 (812) 336 43 04 (многоканальный) Email: org@lifeelectronics.ru