



## LatticeSC™ PCI Express x1 Evaluation Board

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**User's Guide**

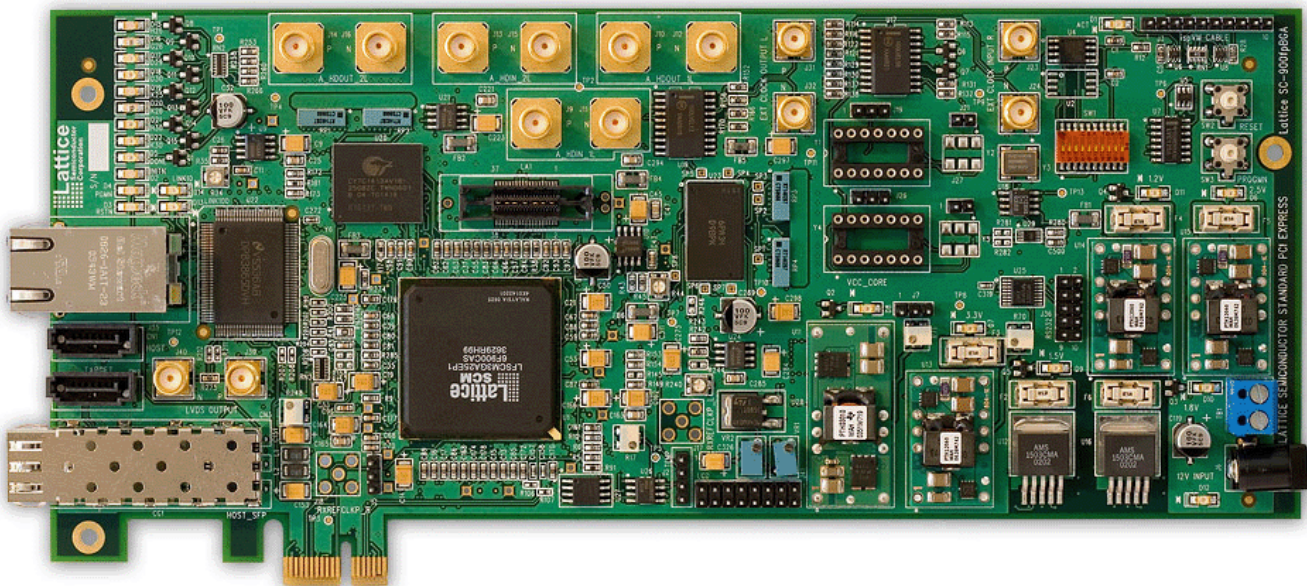
## Introduction

This user's guide describes the LatticeSC PCI Express x1 Evaluation Board featuring the LatticeSC LFSCM3GA25 device in a 900 fpBGA package. The stand-alone evaluation PCB provides a functional platform for development and rapid prototyping of applications that require high-speed SERDES interfaces to PCI Express protocols.

The evaluation board includes provisioning to connect high-speed SERDES channels via SMA connectors to test and measurement equipment. The board is manufactured using standard FR4 dielectric and through-hole vias. The nominal impedance is 50-ohm for single-ended traces and 100-ohm for differential traces.

The board has several debugging and analyzing features for complete evaluation of the LatticeSC device. This user's guide is intended to be referenced in conjunction with evaluation design tutorials to demonstrate the LatticeSC FPGA.

**Figure 1. LatticeSC PCI Express x1 Evaluation Board**



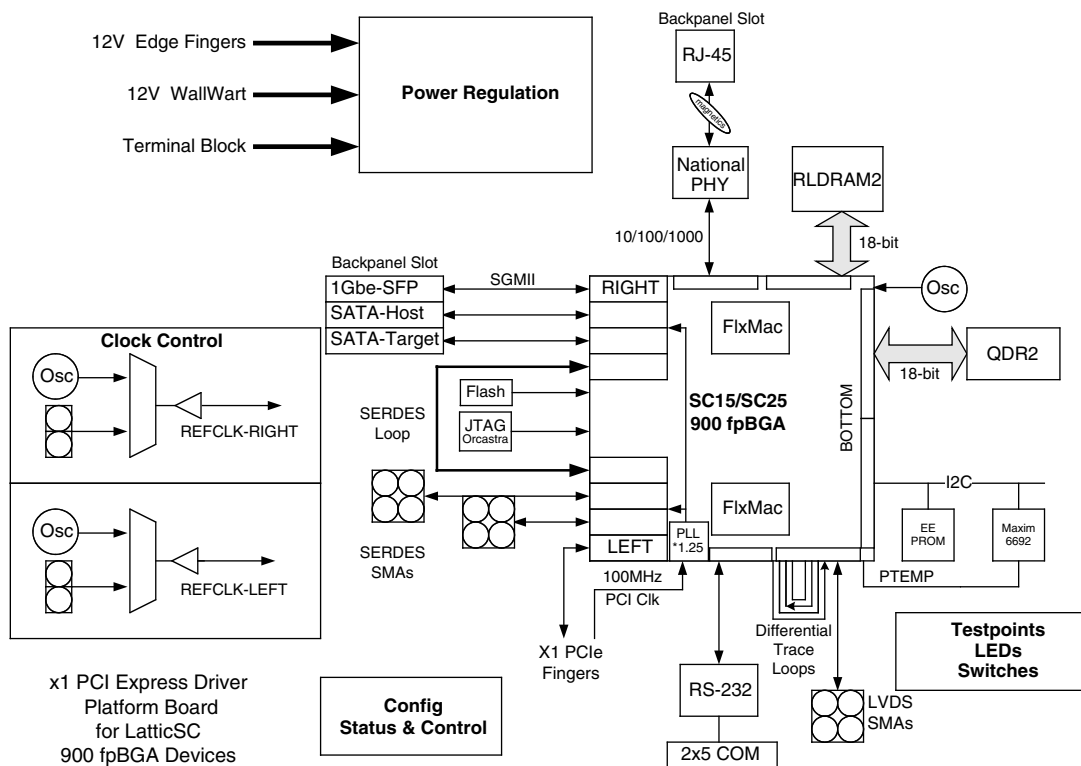
## Features

- Four SERDES high-speed channels interfaced to SMA test points and clock connections SERDES interface to x1 PCI Express edge fingers
- RJ-45 interface for Ethernet
- QDR2 and RLDRAMII memory devices
- SFP Transceiver cage and associated interface
- SATA-like connections to SERDES channels
- Power connections and power sources
- ispVM<sup>®</sup> programming support
- On-board and external reference clock sources
  - Interchangeable clock oscillators
  - On-board reference clock management
- ORCAstra Demonstration Software interface via standard ispVM JTAG connection

- RS-232 Communications Port
- Logic analyzer connection
- Liquid Crystal Display interface connection
- User-defined input and output points
- SMA connectors included for high-speed clock or data interfacing
- Performance monitoring via test headers, LEDs and switches

The contents of this user's guide include top-level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, diodes and switches and a complete set of schematics of the board. Figure 2 shows the functional partitioning of the board.

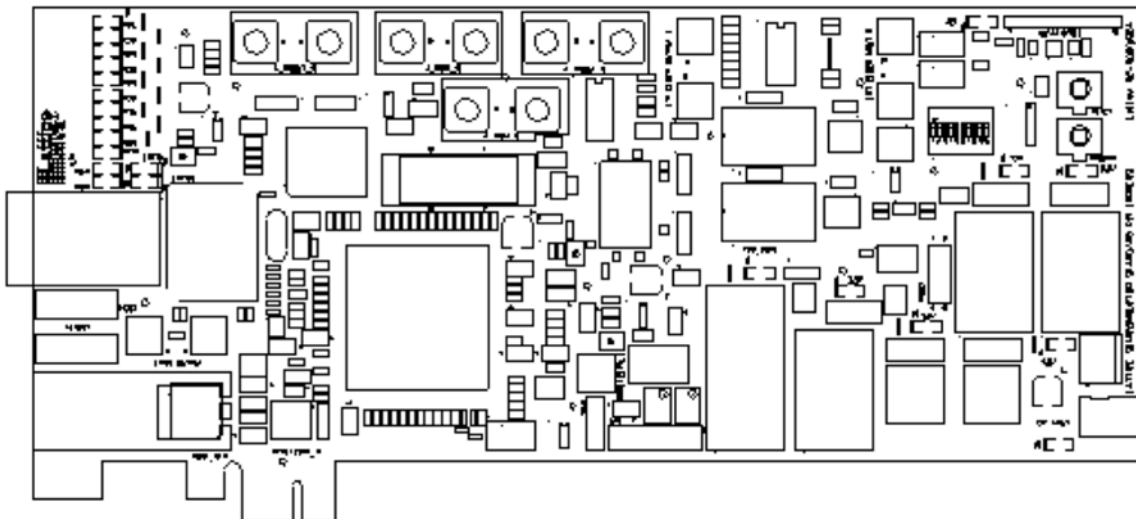
**Figure 2. LatticeSC PCI Express x1 Evaluation Board Block Diagram**



## Additional Resources

For additional information and resources related to this board, including updated documentation and software demos, please see the Lattice web site at: [www.latticesemi.com/boards](http://www.latticesemi.com/boards), and navigate to the appropriate page for this board.

Lattice makes its best effort to provide evaluation board designs to help users with evaluation and development. However it remains the user's responsibility to verify proper and reliable operation of Lattice products in their end application by consulting documentation provided by Lattice. Differences in component selection and/or PCB layout in the user's application may significantly affect circuit performance and reliability.

**Figure 3. LatticeSC PCI Express x1 Evaluation Board, Top View**

## LatticeSC Device

This board features a LatticeSC FPGA with a 1.2V core supply. It can accommodate all pin compatible LatticeSC devices in the 900-ball fpBGA (1mm pitch) package. A complete description of this device can be found in the LatticeSC Family Data Sheet on the Lattice web site at [www.latticesemi.com](http://www.latticesemi.com).

*Note: The connections referenced in this document refer to the LFSCM3GA25EP1-XXF900 device. Available I/Os and associated sysIO™ banks may differ for other densities within this device family.*

## Applying Power to the Board

The LatticeSC PCI Express x1 Evaluation Board is ready to power on. The board can be supplied with power from an AC wall-type transformer power supply shipped with the board or it can be supplied from a bench top supply via terminal screw connections. It also has provisions to be supplied from the PCI Express edge fingers from a host board.

To supply power from the factory-supplied wall transformer, simply connect the output connection of the power cord to J6 and plug the wall transformer into an AC wall outlet.

## Power Supplies

(see Appendix A, Figure 6)

The evaluation board incorporates an alternate scheme to provide power to the board. The board is equipped to accept a main supply via the TB1 connection. This connection is provided to use with a bench top supply adjusted to provide a nominal 12V DC.

All input power sources and on-board power supplies are fused with surface mounted fuses and have green LEDs to indicate power GOOD status of the intermediate supplies

**Table 1. Board Power Supply Fuses (see Appendix A, Figure 6)**

|    |                     |
|----|---------------------|
| F1 | 1.0V/1.2V Core Fuse |
| F2 | 1.5V Fuse           |
| F3 | 3.3V Fuse           |
| F4 | 1.2V Fuse           |
| F5 | 2.5V Fuse           |
| F6 | 1.8V Fuse           |

**Table 2. Board Power Supply Indicators (see Appendix A, Figure 6)**

|     |  |
|-----|--|
| D6  | 2.5V Source Good Indicator               |
| D7  | 3.3V Source Good Indicator               |
| D8  | 1.0V/1.2V VCC Core Source Good Indicator |
| D9  | 1.5V Source Good Indicator               |
| D10 | 1.8V Source Good Indicator               |
| D11 | 1.2V Source Good Indicator               |
| D12 | 12V Input Good Indicator                 |

**Table 3. Board Supply Disconnects (see Appendix A, Figure 7)**

|     |                                 |
|-----|---------------------------------|
| TB1 | Screw Terminal for 12V DC       |
|     | Pin 1 (Square PCB Pad) = 12V DC |
|     | Pin 2 = Ground                  |

## PCI Express Power Interface

Power can be sourced to the board via the PCB edge-finger (CN1). This interface allows the user to provide power from a PCI Express host board.

## VCC Core Selection

(see Appendix A, Figure 6)

The VCC core can be selected on the board to be either 1.0V or 1.2V using J7.

A jumper shunt placed between pin 1 and pin 2 will connect 1.0V. A jumper shunt between pin 2 and pin 3 will connect 1.2V.

## Programming/FPGA Configuration

(see Appendix A, Figure 5)

A programming header is provided on the evaluation board, providing access to the LatticeSC JTAG port.

**Important Note:** The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can result in damage to the LatticeSC FPGA device and render the board inoperable.

An ispDOWNLOAD® Cable is included with this board and also with each ispLEVER® design tool shipment. Cables may also be purchased separately from Lattice.

## ispVM Download Interface

J3 is an 10-pin JTAG connector used in conjunction with the ispVM USB download cable to program and control the device. Connections to the cable typically consist of Pin[1:2:3:6:7:8]. The other pins are considered optional and are not required to be connected for standard operation.

**Table 4. ispVM JTAG Connector (see Appendix A, Figure 5)**

| Pin 1  | VCC                   |
|--------|-----------------------|
| Pin 2  | TDO                   |
| Pin 3  | TDI                   |
| Pin 4  | PROGRAMN <sup>1</sup> |
| Pin 5  | NC                    |
| Pin 6  | TMS                   |
| Pin 7  | GND                   |
| Pin 8  | TCK                   |
| Pin 9  | DONE <sup>1</sup>     |
| Pin 10 | INITN <sup>1</sup>    |

1. Optional pins.

## Download Procedures

### Requirements

- PC with ispVM System v.16.0 (or later) programming management software, installed with appropriate drivers (USB driver for USB Cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD Cable). The latest ispVM System software can be downloaded from the Lattice web site at [www.latticesemi.com/ispvm](http://www.latticesemi.com/ispvm).

*Note: An option to install these drivers is included as part of the ispVM System setup.*

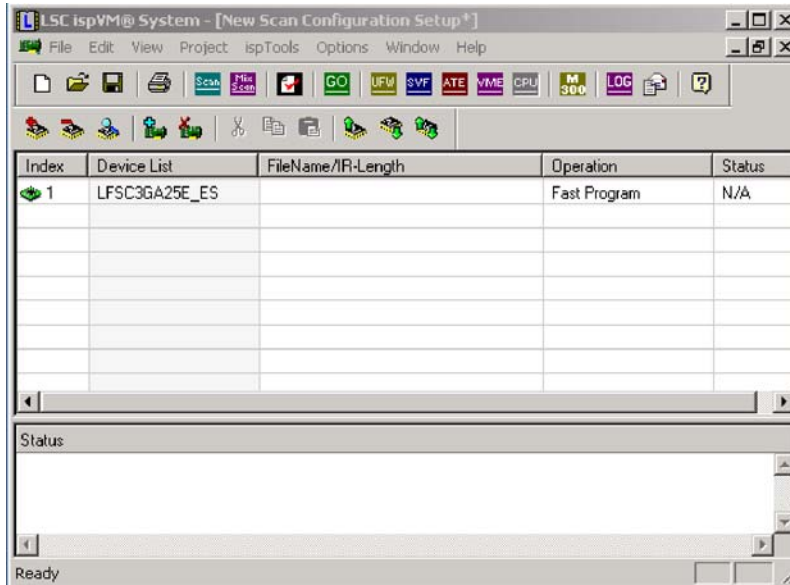
- ispDOWNLOAD Cable

### JTAG Download

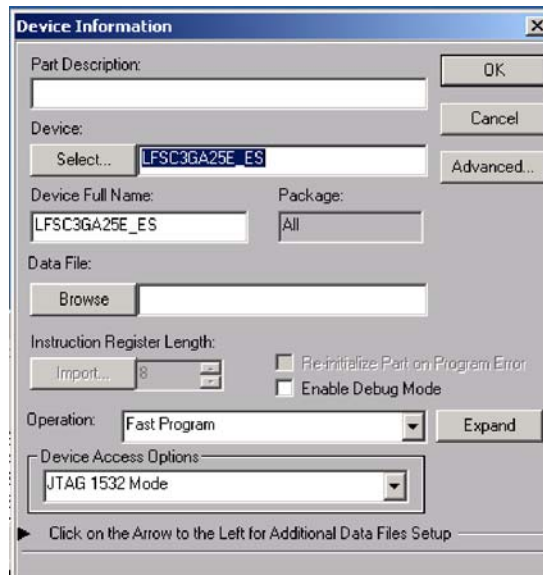
The LatticeSC device can be configured easily via its JTAG port. The device is SRAM-based; it must remain powered on to retain its configuration when programmed in this fashion.

1. Connect the ispDOWNLOAD cable to the appropriate header. J3 is used for the 1x10 cable. Connections to J3 use only pins[1-3][6-8].
2. Connect the LatticeSC PCI Express x1 evaluation board to the appropriate power sources and power up board.
3. Start the ispVM System software.

- Press the **SCAN** button located in the toolbar. The LatticeSC device is automatically detected.



- Double-click the device to open the device information dialog. In the device information dialog, click the **Browse** button located under **Data File**. Locate the desired bitstream file (.bit). Click **OK** to both dialog boxes.



- Click the green **GO** button. This will begin the download process into the device. Upon successful download, the device will be operational.

### Configuration Status Indicators

(see Appendix A, Figure 5)

These LEDs indicate the status of configuration to the FPGA.

- D2 (RED) illuminated: This indicates that the programming was aborted or reinitialized driving the INITN output low.

- D5 (GREEN) is illuminated: This indicates the successful completion of configuration by releasing the open collector DONE output pin.
- D1 (GREEN) will flash indicating TDI activity.
- D4 (RED) illuminated: This indicates that PROGRAMN is low.
- D3 (RED) illuminated: This indicates that GSRN is low.

## PROGRAMN and GSRN

(see Appendix A, Figure 5)

These push-button switches assert/de-assert the logic levels on the PROGRAMN (SW3) and GSRN (SW2). Depressing the button drives a logic level "0" to the device.

## Bank1 VCCIO

(see Appendix A, Figure 6)

VCCIO1 can be selected on the board to be either 3.3V or 2.5V using J5.

A jumper shunt placed between pin 1 and pin 2 will connect 2.5V. A jumper shunt between pin 2 and pin 3 will connect 3.3V.

## On-Board Flash Memory

(see Appendix A, Figure 5)

Two memory devices (U2 and U3) are on-board for non-volatile configuration memory storage. These two devices occupy the same Flash slot on the board. U2 can be populated with an 8M or smaller 8-pin SOIC device. U3 can be used in place of U2 with a 16-pin TSSOP 64M Flash device. This is the factory supplied Flash memory configuration. U4 is always supplied as an 8M Flash device. SW1 is used to control the selection of the Flash memory to be accessed.

Refer to Lattice technical note TN1100, *SPI Serial Flash Programming Using ispJTAG™ on LatticeSC FPGAs* for recommended procedures and software usage. To use both SPI Flash devices to program the LatticeSC device, the user must write to the Flash devices individually. This is accomplished by setting SW1 accordingly. Writing to Flash #1(U2 OR U3), close 3 and 5 switch positions (ON) and open all others. Writing to Flash #2(U4), close 2 and 4 switch positions (ON) and open all others. For reading from the Flash devices individually, use the same switch settings as described for writing. For reading from both Flash devices in cascading format, close switch positions (1, 3, 4, 5, 8).

## FPGA Clock Management

(see Appendix A, Figures 10 and 11)

The evaluation board includes various features for generating and managing on-board clocks. The clocks are generated from either input provided from SMAs (see Table 5) or from crystal oscillators (Y1 and Y4). Y1 and Y4 are socketed for interchangeability. Y2 and Y5 are 321.25MHz surface-mounted oscillators. The Y3 oscillator is fanned out around U1 for reference clocks with a fan-out buffer IC.

Y1 and Y4 can be a 4-pin DIP type oscillator like Connor-Winfield XO-400 series.

Clock oscillators are selected per quad. Y1 and Y2 can source a clock to the Right SERDES Quads. Y4 and Y5 can source a clock to the Left SERDES Quad. The user needs to select the appropriate oscillator by placing jumper shunts on J20 and/or J22 for the Left reference clock source or J25 and/or J28 for the Right reference clock source. The selection of these clock sources is dependent on the selection pins of the clock multiplexers. The mux select pins are driven from the FPGA and will need to be driven according to the needs of the user design. The following table defines the selection of the clock sources.



**Table 5. Clock Source Selection (see Appendix A, Figures 5 and 10)**

| BGA-A19 | BGA-A20 | Right Clock Source | Left Clock Source |
|---------|---------|--------------------|-------------------|
| L       | L       | SMA                | SMA               |
| H       | H       | Oscillator         | Oscillator        |

Pin is low when open/float. FPGA general purpose I/O must be driven to control the mux selection.

When using FPGA control, 3.3V VCCIO must be used in bank 1. Refer to Bank1 VCCIO section of this document.

**Table 6. Clock Input SMA (see Appendix A, Figure 10)**

| SMA | Signal                              |
|-----|-------------------------------------|
| J29 | SMA Reference + Input to Left Quad  |
| J30 | SMA Reference - Input to Left Quad  |
| J23 | SMA Reference + Input to Right Quad |
| J24 | SMA Reference - Input to Right Quad |

The clocks sources are fanned-out across the board to several destinations. These clocks are all differential and must be used accordingly. These include SERDES reference clocks, PLL, and primary clock inputs.

**Table 7. Clock Distribution (see Appendix A, Figure 11)**

| Clock Net      | BGA  | Clock Destination |
|----------------|------|-------------------|
| FPGA_REFCLKP_L | P8   | PCLKT7_2          |
| FPGA_REFCLKN_L | R8   | PCLKC7_2          |
| FPGA_REFCLKP_R | AD26 | LRC_PLLB_T        |
| FPGA_REFCLKN_R | AC25 | LRC_PLLB_C        |
| A_REFCLKP_L    | B1   | SERDES[360]       |
| A_REFCLKN_L    | C1   | SERDES[360]       |
| A_REFCLKP_R    | B30  | SERDES[3e0]       |
| A_REFCLKN_R    | C30  | SERDES[3e0]       |

The clocks are also driven to SMA connections for driving off-board.

**Table 8. Clock Output SMAs (see Appendix A, Figure 11)**

| Net Name   | SMA | SMA |
|------------|-----|-----|
| EXTCLOCK_L | J31 | J32 |
| EXTCLOCK_R | J33 | J34 |

## SERDES Reference Clock

The 50-ohm terminated SMA connectors are provided the supply reference clocks directly to the LatticeSC device from the clock management device. This device will drive clocks to both SERDES quads via 100-ohm LVDS signaling. On-board clock oscillators mentioned in the previous sections can be chosen to drive the same SERDES reference clocks. Also the board can be provisioned to source the clock from the PCI Express edge-fingers directly to FPGA input pins.

Both of these input clock sources are routed through clock management devices allowing for clock source selection from a SMA input connector. This is accomplished by using the MUX selector driven by the FPGA output.

## SERDES Channels

### SMA Connections

(see Appendix A, Figure 5)

DC coupled top-mounted SMA connectors connect to the two SERDES TX and RX channels. These pins are directly coupled to the designated SMA connector creating a path for both input and output differential data.

**Table 9. SERDES Connectors (see Appendix A, Figure 8)**

| SMA | Channel Name  | 900-Ball fpBGA | SMA | Channel Name   | 900-Ball fpBGA |
|-----|---------------|----------------|-----|----------------|----------------|
| J13 | A_HDINP1_LEFT | B6             | J10 | A_HDOUTP1_LEFT | A6             |
| J15 | A_HDINN1_LEFT | B5             | J12 | A_HDOUTN1_LEFT | A5             |
| J9  | A_HDINP2_LEFT | B7             | J14 | A_HDOUTP2_LEFT | A7             |
| J11 | A_HDINN2_LEFT | B8             | J16 | A_HDOUTN2_LEFT | A8             |

### SERDES SFP Transceiver Interface

(see Appendix A, Figure 8)

A small form-factor pluggable (SFP) transceiver cage is included for evaluation of SFP specific protocols. The PCB includes the appropriate power and high-speed circuitry needed for the SFP standard transceiver.

**Table 10. SFP Connections to SERDES Pins (see Appendix A, Figure 5)**

| SFP RX | Channel Name   | 900-Ball fpBGA | SFP TX | Channel Name    | 900-Ball fpBGA |
|--------|----------------|----------------|--------|-----------------|----------------|
| RD+    | A_HDINP0_RIGHT | B28            | TD+    | A_HDOUTP0_RIGHT | A28            |
| RD-    | A_HDINN0_RIGHT | B27            | TD-    | A_HDOUTN0_RIGHT | A27            |

**Table 11. SFP Control and Status Connections to FPGA**

| SFP Pin | 900-Ball fpBGA | SFP Pin  | 900-Ball fpBGA |
|---------|----------------|----------|----------------|
| TxFault | A15            | ModeDef0 | E15            |
| TxDis   | C13            | ModeDef1 | D15            |
| LOS     | G15            | ModeDef3 | C14            |
| RateSel | F15            |          |                |

### SERDES SATA Channels

(see Appendix A, Figure 8)

AC-coupled connections are included to attach SATA type cables to SERDES channels for board-to-board or loop-back purposes. The connectors are configured using the 7-pin SATA specifications.

**Table 12. SERDES to SATA Connections**

| CN1 Pin | SERDES Pin  | 900-Ball fpBGA |  | CN2 Pin | SERDES Pin  | 900-Ball fpBGA |
|---------|-------------|----------------|--|---------|-------------|----------------|
| 1       | —           | GND            |  | 1       | —           | GND            |
| 2       | A_HDOUTP1_R | A25            |  | 2       | A_HDINP2_R  | B24            |
| 3       | A_HDOUTN1_R | A26            |  | 3       | A_HDINN2_R  | B23            |
| 4       | —           | GND            |  | 4       | —           | GND            |
| 5       | A_HDINP1_R  | B25            |  | 5       | A_HDOUTP2_R | A24            |
| 6       | A_HDINN1_R  | B26            |  | 6       | A_HDOUTN2_R | A23            |
| 7       | —           | GND            |  | 7       | —           | GND            |

**SERDES PCI Express Channels**

(see Appendix A, Figure 8)

This board is equipped to communicate directly as an add-on card to a PCI Express host. It is designed with edge-fingers (CN1) to fit directly into an x1 host receptacle. Power can be supplied directly from the PCI Express host via the edge-finger connections.

**Table 13. SERDES to PCI Express Connections**

| PCI Express Pin | PCI Express Signal | SCM Device Pin        | 900-Ball fpBGA |
|-----------------|--------------------|-----------------------|----------------|
| B14             | PETp0              | A_HDINP0_L            | B3             |
| B15             | PETn0              | A_HDINN0_L            | B4             |
| A16             | PERp0              | A_HDOUTP0_L           | A3             |
| A17             | PERn0              | A_HDOUTN0_L           | A4             |
| A13             | Refclk+            | FPGA URC_A PLL Input+ | D28            |
| A14             | Refclk-            | FPGA URC_A PLL Input+ | E28            |

**FPGA Test Pins**

(see Appendix A, Figure 15)

General purpose FPGA pins are available for user applications. FPGA pins are connected to SW4 DIP switch. This switch is used for static settings to FPGA input pins. The pins must be set to LVCMOS18 buffer types and are externally pulled up when the switch is open and driven low when the switch is set to "ON" or closed.

General purpose outputs are connected to LEDs for observing output status of pins. The FPGA output buffers should be LVCMOS18 and will illuminate the LED when driving a "1" and the LED will be off when driving a "0" or when not used.

**Table 14. FPGA Test Pins (see Appendix A, Figure 15)**

| Switch | BGA | Netname | LED | 900-Ball fpBGA | NetName | LED Color |
|--------|-----|---------|-----|----------------|---------|-----------|
| SW4A   | G28 | Switch1 | D15 | H26            | LED1    | Red       |
| SW4B   | F28 | Switch2 | D16 | G26            | LED2    | Yellow    |
| SW4C   | L25 | Switch3 | D17 | D29            | LED3    | Green     |
| SW4D   | L26 | Switch4 | D18 | D30            | LED4    | Blue      |
| SW4E   | E29 | Switch5 | D19 | K25            | LED5    | Red       |
| SW4F   | E30 | Switch6 | D20 | K26            | LED6    | Yellow    |
| SW4G   | J28 | Switch7 | D21 | H30            | LED7    | Green     |
| SW4H   | H28 | Switch8 | D22 | K30            | LED8    | Blue      |

## Test SMA Connections

General-purpose FPGA pins are available via SMA test connections. These connections are designed to permit evaluations of several types of FPGA I/O buffers. The use of several termination schemes permits easy interfaces for the type of buffer.

**Table 15. Test SMA Connections for FPGA Pins (see Appendix A, Figure 16)**

| SMA Designation | Name       | SCM25 Signal | 900-Ball fpBGA | Termination Description | Termination Resistor(s) |
|-----------------|------------|--------------|----------------|-------------------------|-------------------------|
| J37             | LVDS_INP   | PR52A        | AB28           | None                    | —                       |
| J39             | LVDS_INN   | PR52B        | AC28           | None                    | —                       |
| J38             | LVDS_OUTP0 | PR35A        | M29            | 100-ohm Differential    | R275                    |
| J40             | LVDS_OUTN0 | PR35B        | N30            | 100-ohm Differential    | R275                    |

## High Speed Test Point

### DP2

(see Appendix A, Figure 15 and 16)

General-purpose FPGA pins are available via a differential test pad. These connections allow a high-impedance probe to measure the performance of a coupled-differential output buffer pair.

**Table 16. Differential I/O Test Point**

| Probe True | Probe Compliment | 100-ohm Differential Resistor |
|------------|------------------|-------------------------------|
| AF30       | AG30             | R274                          |

## Logic Analysis Connection

### LA1

(see Appendix A, Figure 15 and 16)

Agilent single-ended probes designed for connection to the supplies Tyco/AMP's 2-767004-2 MICTOR connector can be easily attached for signal bus analysis. Connections to general-purpose I/O pins are provided to the board ready 38-pin MICTOR connector.

**Table 17. Logic Analyzer Connections**

| MICTOR Pin | Signal  | 900-Ball fpBGA | MICTOR Pin | Signal  | 900-Ball fpBGA |
|------------|---------|----------------|------------|---------|----------------|
| 5          | LA_CLK1 | AJ1            | 6          | LA_CLK2 | AF4            |
| 7          | LA_0    | AG3            | 8          | LA_16   | AH13           |
| 9          | LA_1    | AH2            | 10         | LA_17   | AK8            |
| 11         | LA_2    | AD8            | 12         | LA_18   | AK9            |
| 13         | LA_3    | AF7            | 14         | LA_19   | AH14           |
| 15         | LA_4    | AJ7            | 16         | LA_20   | AG14           |
| 17         | LA_5    | AJ8            | 18         | LA_21   | AK10           |
| 19         | LA_6    | AH10           | 20         | LA_22   | AK11           |
| 21         | LA_7    | AH11           | 22         | LA_23   | AH15           |
| 23         | LA_8    | AF13           | 24         | LA_24   | AG15           |
| 25         | LA_9    | AE14           | 26         | LA_25   | AH12           |

**Table 17. Logic Analyzer Connections (Continued)**

| MICTOR Pin | Signal | 900-Ball fpBGA | MICTOR Pin | Signal | 900-Ball fpBGA |
|------------|--------|----------------|------------|--------|----------------|
| 27         | LA_10  | AK6            | 28         | LA_26  | AJ13           |
| 29         | LA_11  | AK7            | 30         | LA_27  | AD15           |
| 31         | LA_12  | AF14           | 32         | LA_28  | AE15           |
| 33         | LA_13  | AF15           | 34         | LA_29  | AK12           |
| 35         | LA_14  | AJ11           | 36         | LA_30  | AK13           |
| 37         | LA_15  | AG13           | 38         | LA_31  | AJ14           |

## RS-232 Interface

### J36

(see Appendix A, Figures 5 and 16)

A simple 2x5 Header provides a connection to create a RS-232 serial communications port. The connection includes the proper level shift needed to connect to a serial port of a PC. The RX and TX pins are connected to the FPGA.

**Table 18. RS-232 TX/RX**

| Signal    | 900-Ball fpBGA | Buffer Type |
|-----------|----------------|-------------|
| RS232-RXD | F13            | LVC MOS25   |
| RS232-TXD | F12            | LVC MOS25   |

## LCD Interface

### J41

(see Appendix A, Figures 5 and 16)

A 2x8 Header provides a connection to 16-character x 2 line LCD modules such as Varitronix VDM16265. A ribbon cable connection will allow attachment to the connector. The board includes two variable resistors for LCD adjustments. VR1 adjusts the backlight and VR2 provides contrast adjustment. A user design must be included in the FPGA to drive this feature.

## I<sup>2</sup>C Interface

(see Appendix A, Figures 5 and 16)

I<sup>2</sup>C interface is supplied between the FPGA and two ICs. This interface is used to access a Maxim temperature sensing device as well as a EEPROM. The temperature-sensing device is also connected back to the FPGA via the PTEMP pins to monitor device temperature.

**Table 19. I<sup>2</sup>C Interface**

| Signal | 900-Ball fpBGA | Buffer Type           |
|--------|----------------|-----------------------|
| SCL    | B11            | LVC MOS25 or LV TTL33 |
| SDA    | B12            | LVC MOS25 or LV TTL33 |

## Ethernet Interface

(see Appendix A, Figures 5 and 13)

Interconnection to Base 10/100/1000 Ethernet protocols is supported via a RJ-45 connection (J35). This connection is electrically interfaced to the FPGA through a tri-speed PHY device. Use of this interface requires a MAC

design to be included in the FPGA. The board includes two status LEDs to indicate Base 10 or Base 100 link. LED(D13) is a green LED which will light to indicate a Base100 link and LED(D14) indicates an established Base 10 link. LED indicators on the RJ-45 connector will indicate activity and Base 1000 link status. Table 20 defines the pinout between the FPGA and PHY device.

**Table 20. LatticeSC FPGA to Ethernet PHY Connections**

| Signal         | 900-Ball fpBGA |
|----------------|----------------|
| ETH_TX_D0      | D3             |
| ETH_TX_D1      | D2             |
| ETH_TX_D2      | J6             |
| ETH_TX_D3      | J5             |
| ETH_TX_D4      | E3             |
| ETH_TX_D5      | E2             |
| ETH_TX_D6      | K4             |
| ETH_TX_D7      | J4             |
| ETH_RX_D0      | F3             |
| ETH_RX_D1      | G3             |
| ETH_RX_D2      | K5             |
| ETH_RX_D3      | K6             |
| ETH_RX_D4      | F2             |
| ETH_RX_D5      | F1             |
| ETH_RX_D6      | E1             |
| ETH_RX_D7      | D1             |
| ETH_CRS        | K3             |
| ETH_COL        | L3             |
| ETH_RX_CLK     | L6             |
| ETH_RX_DV      | M6             |
| ETH_TX_EN      | J1             |
| ETH_TX_CLK     | K1             |
| ETH_GTX_CLK    | L1             |
| ETH_CLK_TO_MAC | M1             |

## QDR2 Memory Interface

(see Appendix A, Figures 12 and 15)

Interconnection to a Cypress CY7C1413AV18-2Mx18 QDR2 SRAM memory device is supplied on board. It includes the proper termination and interface requirements needed to operate at speed.

**Table 21. QDR2 Memory Interface Pinouts**

| NetName | FPGA Ball | NetName | FPGA Ball | NetName | FPGA Ball |
|---------|-----------|---------|-----------|---------|-----------|
| A_0     | T30       | Q_0     | AG29      | D_0     | AK16      |
| A_1     | W28       | Q_1     | AG28      | D_1     | AK17      |
| A_2     | U26       | Q_2     | AH30      | D_2     | AJ16      |
| A_3     | U28       | Q_3     | AJ30      | D_3     | AJ17      |
| A_4     | M30       | Q_4     | AH29      | D_4     | AE16      |
| A_5     | R29       | Q_5     | AJ29      | D_5     | AH16      |
| A_6     | P29       | Q_6     | AE25      | D_6     | AG16      |

**Table 21. QDR2 Memory Interface Pinouts (Continued)**

| NetName | FPGA Ball | NetName | FPGA Ball | NetName | FPGA Ball |
|---------|-----------|---------|-----------|---------|-----------|
| A_7     | P27       | Q_7     | AH28      | D_7     | AK18      |
| A_8     | N29       | Q_8     | AJ28      | D_8     | AK19      |
| A_9     | N28       | Q_9     | AE22      | D_9     | AH17      |
| A_10    | R25       | Q_10    | AK29      | D_10    | AH18      |
| A_11    | R28       | Q_11    | AK28      | D_11    | AG17      |
| A_12    | N27       | Q_12    | AH21      | D_12    | AJ18      |
| A_13    | L30       | Q_13    | AH23      | D_13    | AJ19      |
| A_14    | J30       | Q_14    | AH22      | D_14    | AK20      |
| A_15    | M26       | Q_15    | AG22      | D_15    | AK21      |
| A_16    | G29       | Q_16    | AG21      | D_16    | AF18      |
| A_17    | F29       | Q_17    | AF21      | D_17    | AG18      |
| R_N     | AA30      |         |           |         |           |
| W_N     | Y30       |         |           |         |           |
| CQ      | AK24      |         |           |         |           |
| K       | AJ20      |         |           |         |           |
| K_N     | AJ21      |         |           |         |           |

## RLDRAM-II Memory Interface

(see Appendix A, Figures 14 and 15)

Interconnection to a Micron MT49H16M18CFM-25 SDRAM memory device is supplied on board. It includes the proper termination and interface requirements needed to operate at speed.

**Table 22. LatticeSC FPGA to On-board SDRAM Connections**

| NetName | 900 Ball fpBGA | NetName | 900 Ball fpBGA | NetName | 900 Ball fpBGA | NetName | 900 Ball fpBGA |
|---------|----------------|---------|----------------|---------|----------------|---------|----------------|
| A_0     | AH4            | D_0     | V2             | Q_0     | V1             | BA_0    | AJ2            |
| A_1     | AG5            | D_1     | W2             | Q_1     | U5             | BA_1    | AK2            |
| A_2     | AF8            | D_2     | V5             | Q_2     | U4             | BA_2    | AD7            |
| A_3     | AG8            | D_3     | V4             | Q_3     | T4             | CS_N    | AH1            |
| A_4     | AH3            | D_4     | Y1             | Q_4     | T5             | DM      | AJ12           |
| A_5     | AJ3            | D_5     | AA1            | Q_5     | U1             | QK      | AC7            |
| A_6     | AF9            | D_6     | Y2             | Q_6     | T1             | QVLD    | N3             |
| A_7     | AE10           | D_7     | AA2            | Q_7     | V3             | DK      | AC4            |
| A_8     | AK3            | D_8     | Y3             | Q_8     | U3             | DK_N    | AD4            |
| A_9     | AJ4            | D_9     | W3             | Q_9     | T6             | CK      | AC3            |
| A_10    | AE11           | D_10    | AB1            | Q_10    | U2             | CK_N    | AD3            |
| A_11    | AF10           | D_11    | AC1            | Q_11    | T2             |         |                |
| A_12    | AH7            | D_12    | W5             | Q_12    | R4             |         |                |
| A_13    | AH8            | D_13    | Y5             | Q_13    | R1             |         |                |
| A_14    | AE12           | D_14    | Y6             | Q_14    | P1             |         |                |
| A_15    | AE13           | D_15    | AD2            | Q_15    | R2             |         |                |
| A_16    | AK4            | D_16    | AE2            | Q_16    | P4             |         |                |
| A_17    | AK5            | D_17    | AB5            | Q_17    | P3             |         |                |

| NetName | 900 Ball fpBGA | NetName | 900 Ball fpBGA | NetName | 900 Ball fpBGA | NetName | 900 Ball fpBGA |
|---------|----------------|---------|----------------|---------|----------------|---------|----------------|
| A_18    | AJ5            |         |                |         |                |         |                |
| A_19    | AJ6            |         |                |         |                |         |                |

## Ordering Information

| Description                               | Ordering Part Number | China RoHS Environment-Friendly Use Period (EFUP)                                   |
|---|----------------------|---|
| LatticeSC PCI Express x1 Evaluation Board | LFSC25E-P1-EV        |  |

## Technical Support Assistance

Hotline: 1-800-LATTICE (North America)  
+1-503-268-8001 (Outside North America)  
e-mail: [techsupport@latticesemi.com](mailto:techsupport@latticesemi.com)  
Internet: [www.latticesemi.com](http://www.latticesemi.com)

## Revision History

| Date          | Version | Change Summary   |
|---------------|---------|--|
| October 2006  | 01.0    | Initial release.   |
| December 2006 | 01.1    | Includes new SERDES schematic in Appendix A.   |
| March 2007    | 01.2    | Added Ordering Information section.  |
| April 2007    | 01.3    | Added important information for proper connection of ispDOWNLOAD (Programming) Cables. |
| November 2008 | 01.4    | Updated FPGA Clock Management text section.  |
|               |         | Updated Clock Source Selection table.  |
|               |         | Updated Clock Input SMA table.   |
|               |         | Updated 10/100/1000 PHY schematic.   |

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Appendix A. Schematic

Figure 4. Cover Page

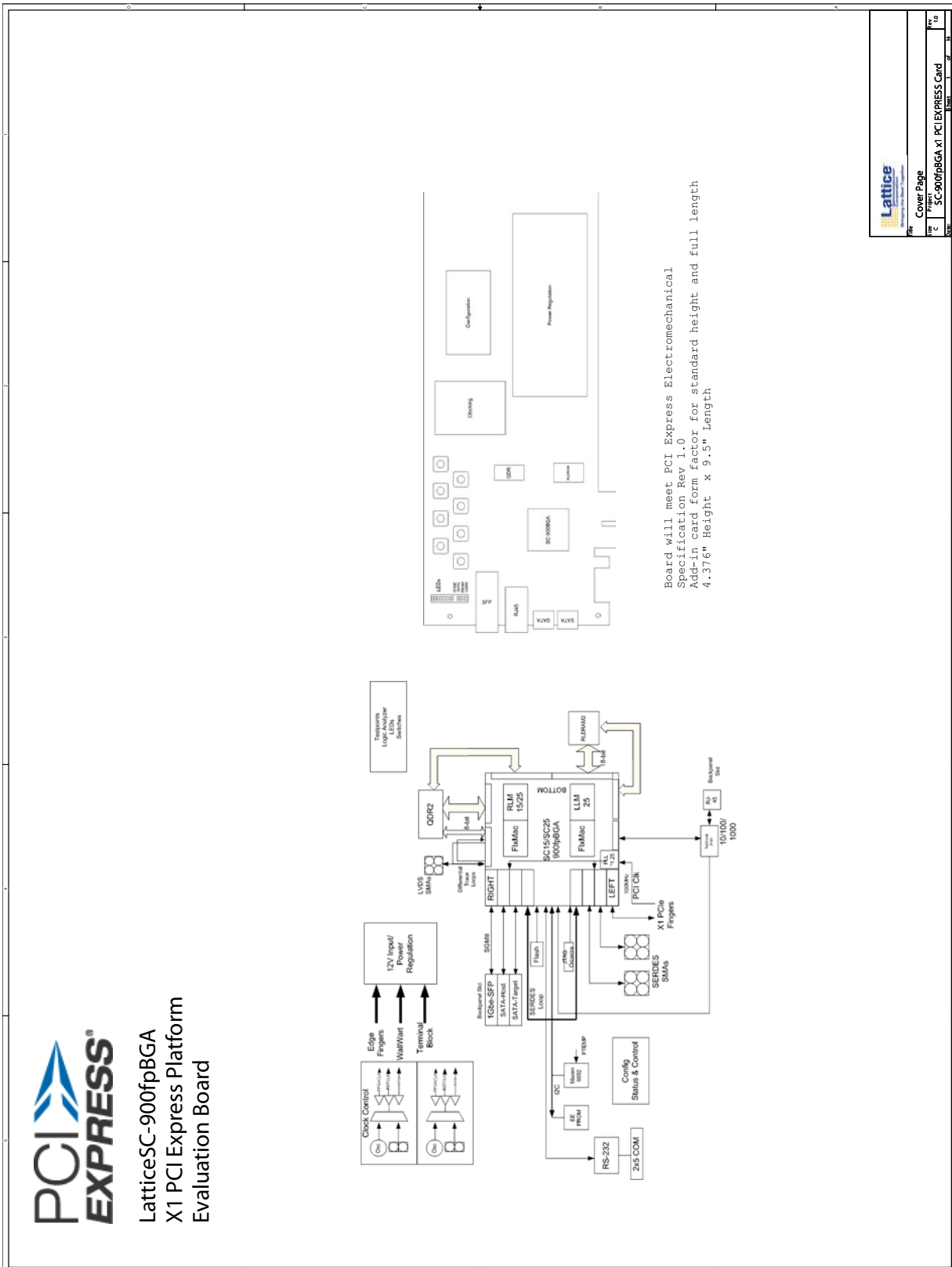


Figure 5. Configuration/Top Bank

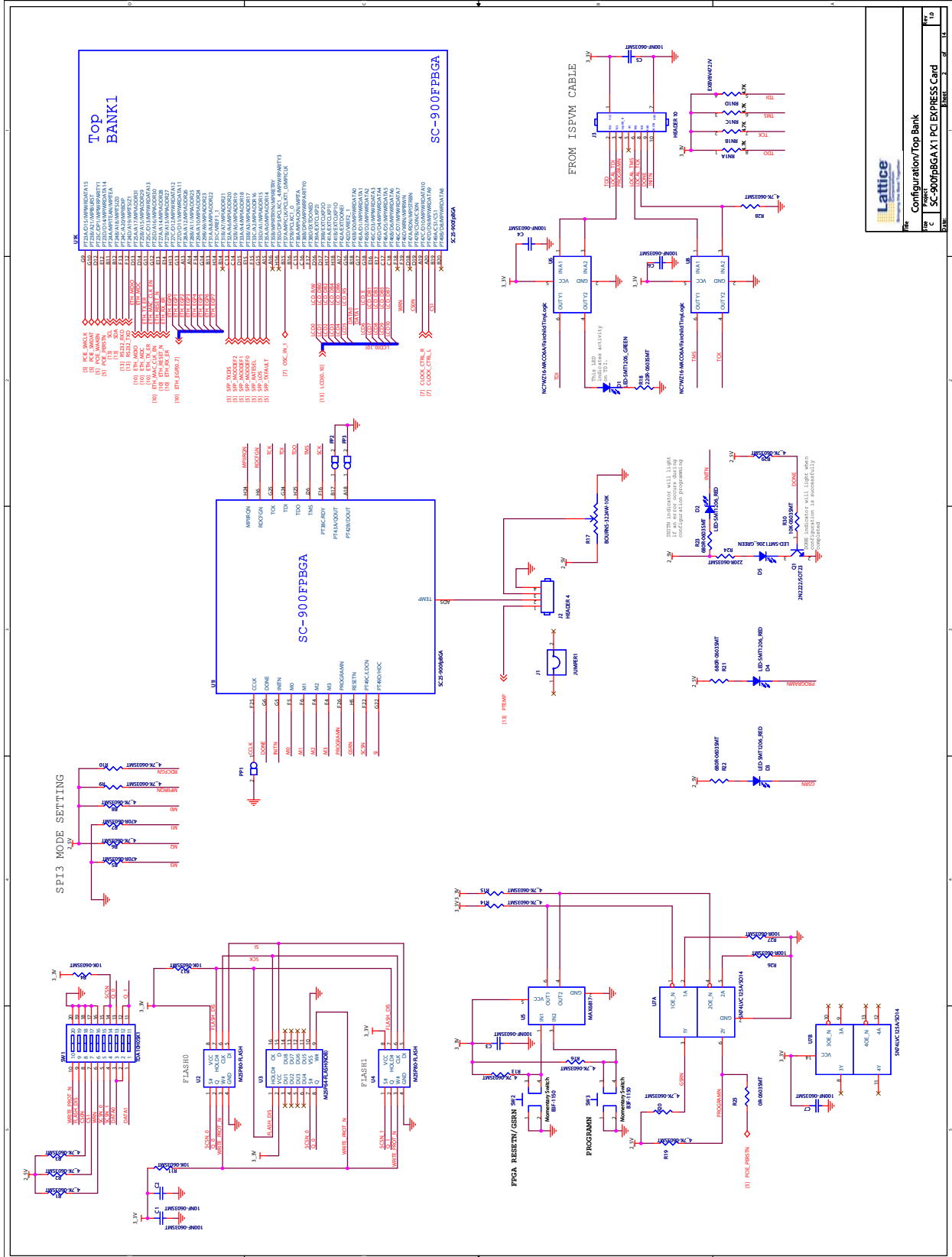


Figure 6. Power Supplies

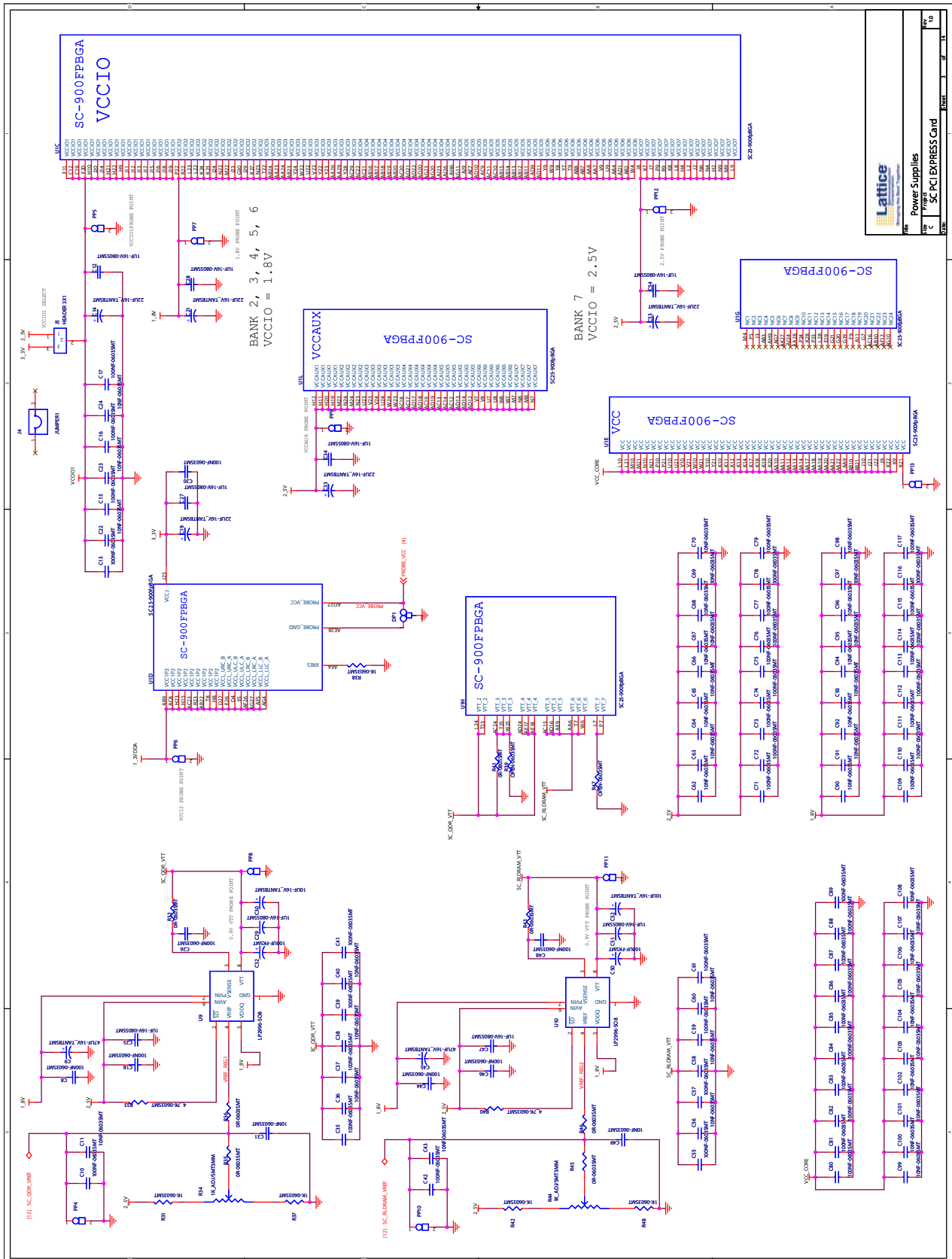


Figure 7. DC/DC Conversion

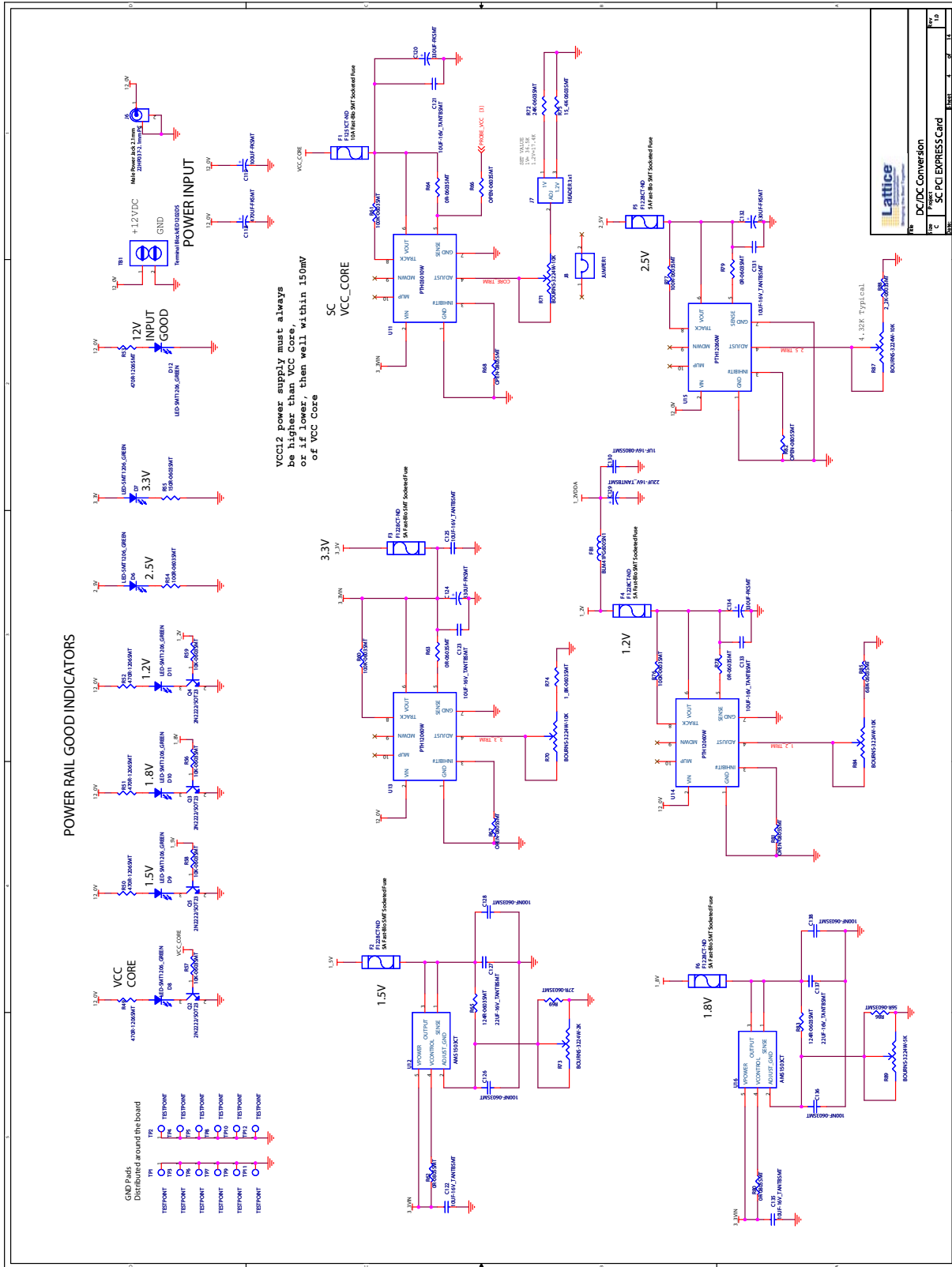
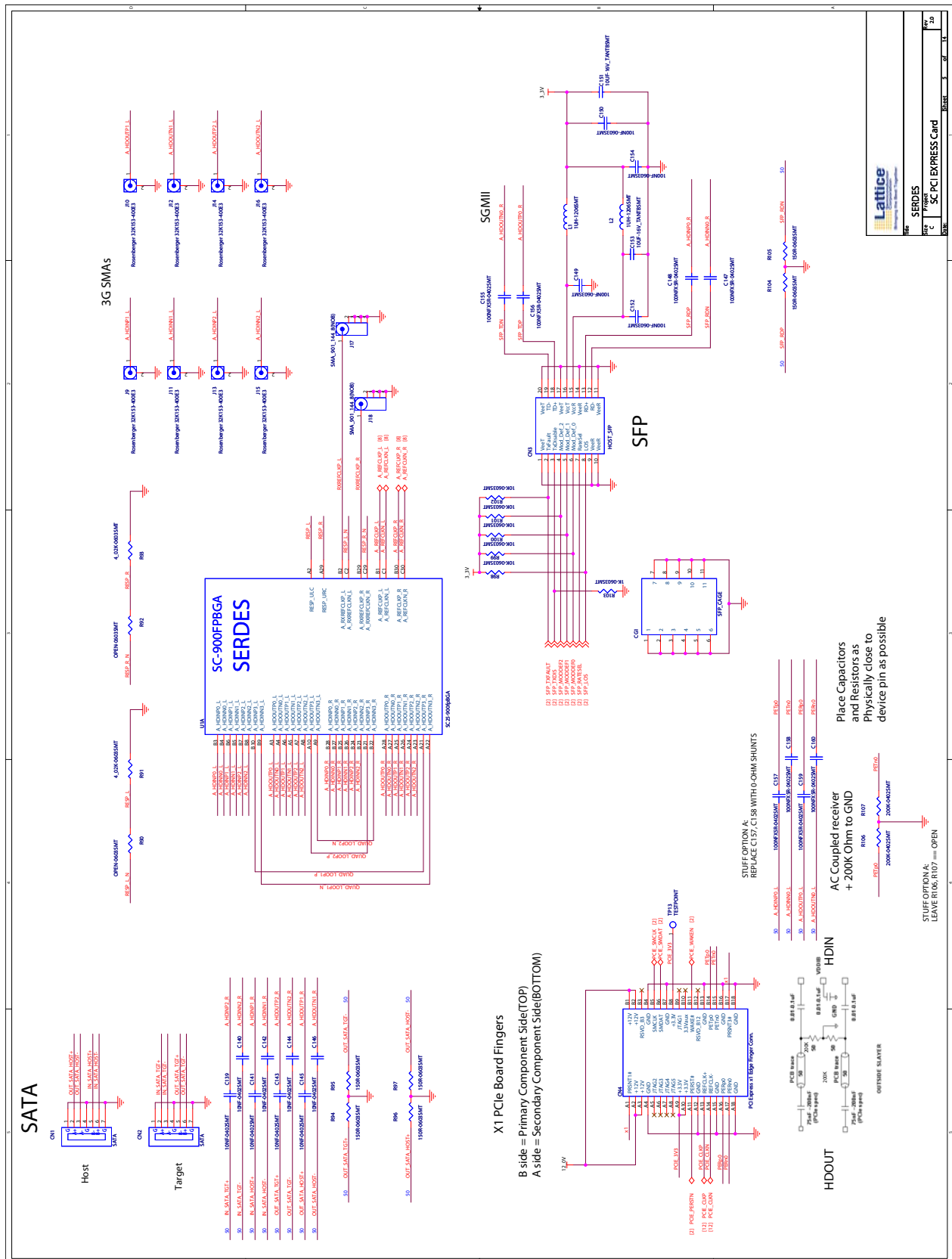


Figure 8. SERDES



|         |                     |      |            |
|---------|---------------------|------|------------|
| REV     | 0                   | DATE | 08/14/2012 |
| PROJECT | SERDES              |      |            |
| PROJECT | SC PCI EXPRESS CARD |      |            |
| REV     | 0                   | DATE | 08/14/2012 |



Figure 10. Clocks

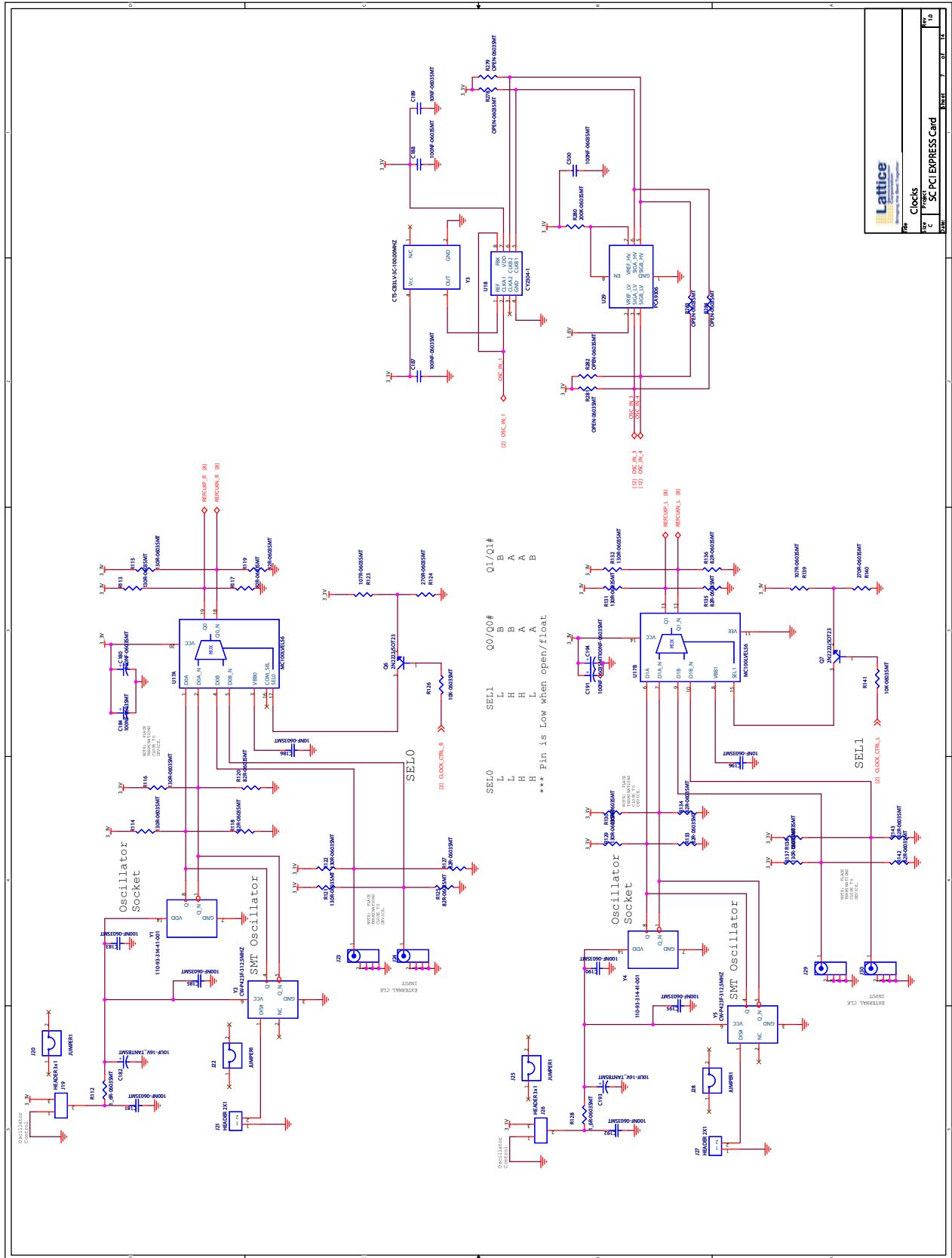
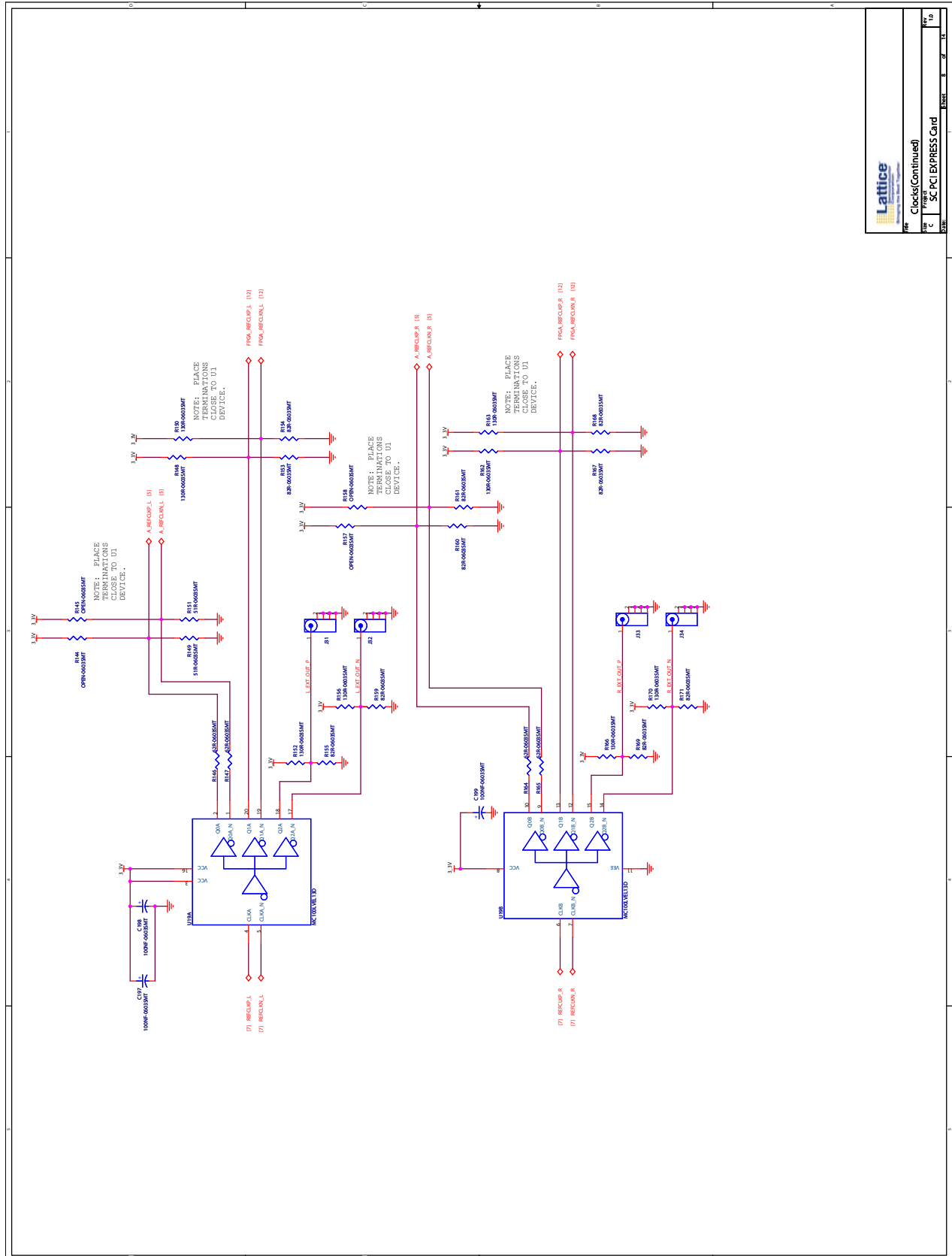



Figure 11. Clocks (Cont.)




  
 Lattice Semiconductor Corporation

Part: Clocks(Continued)
   
 Rev: 1.0
   
 Date: 08/20/10



Figure 12. QDR2 SRAM

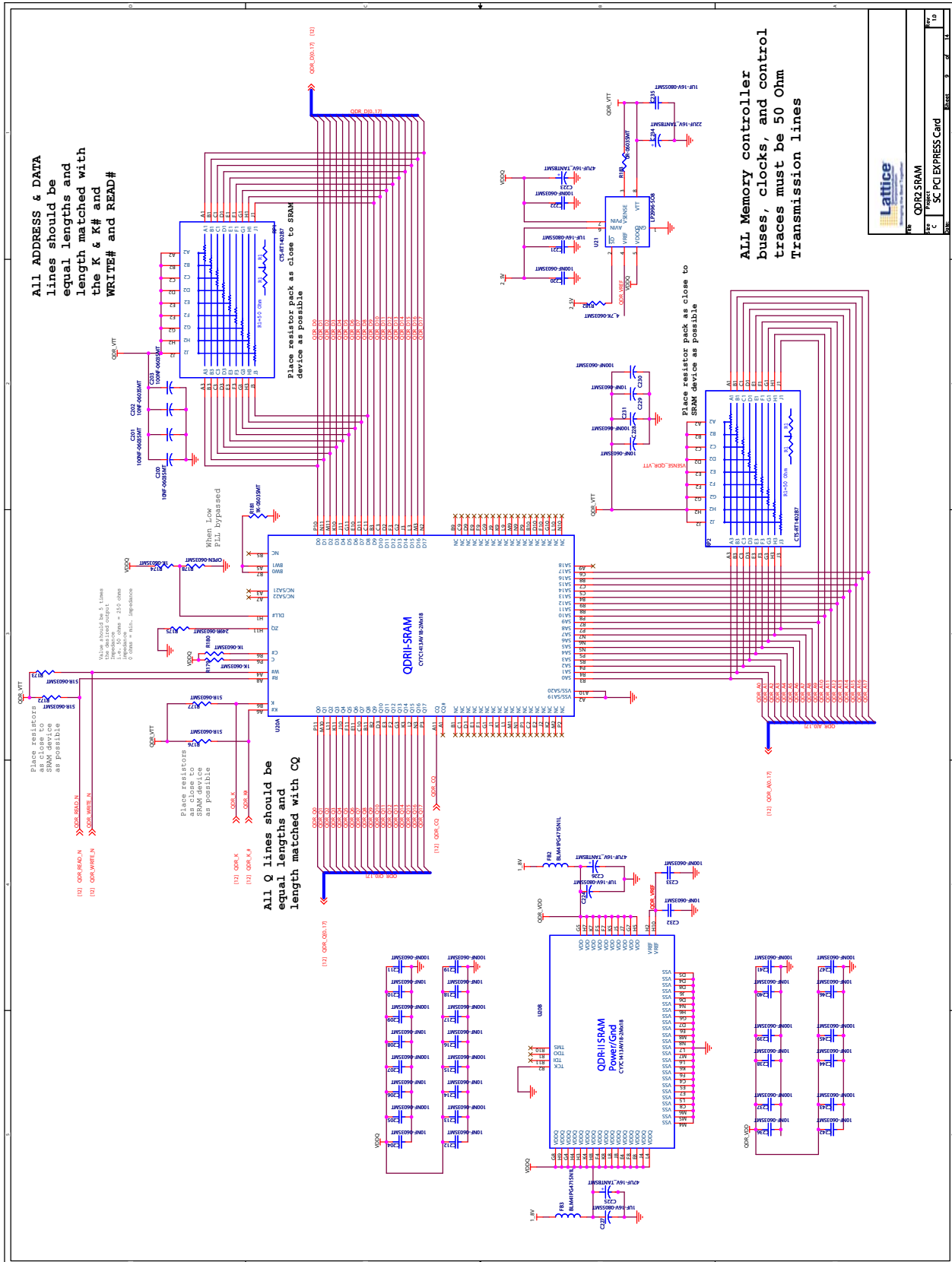
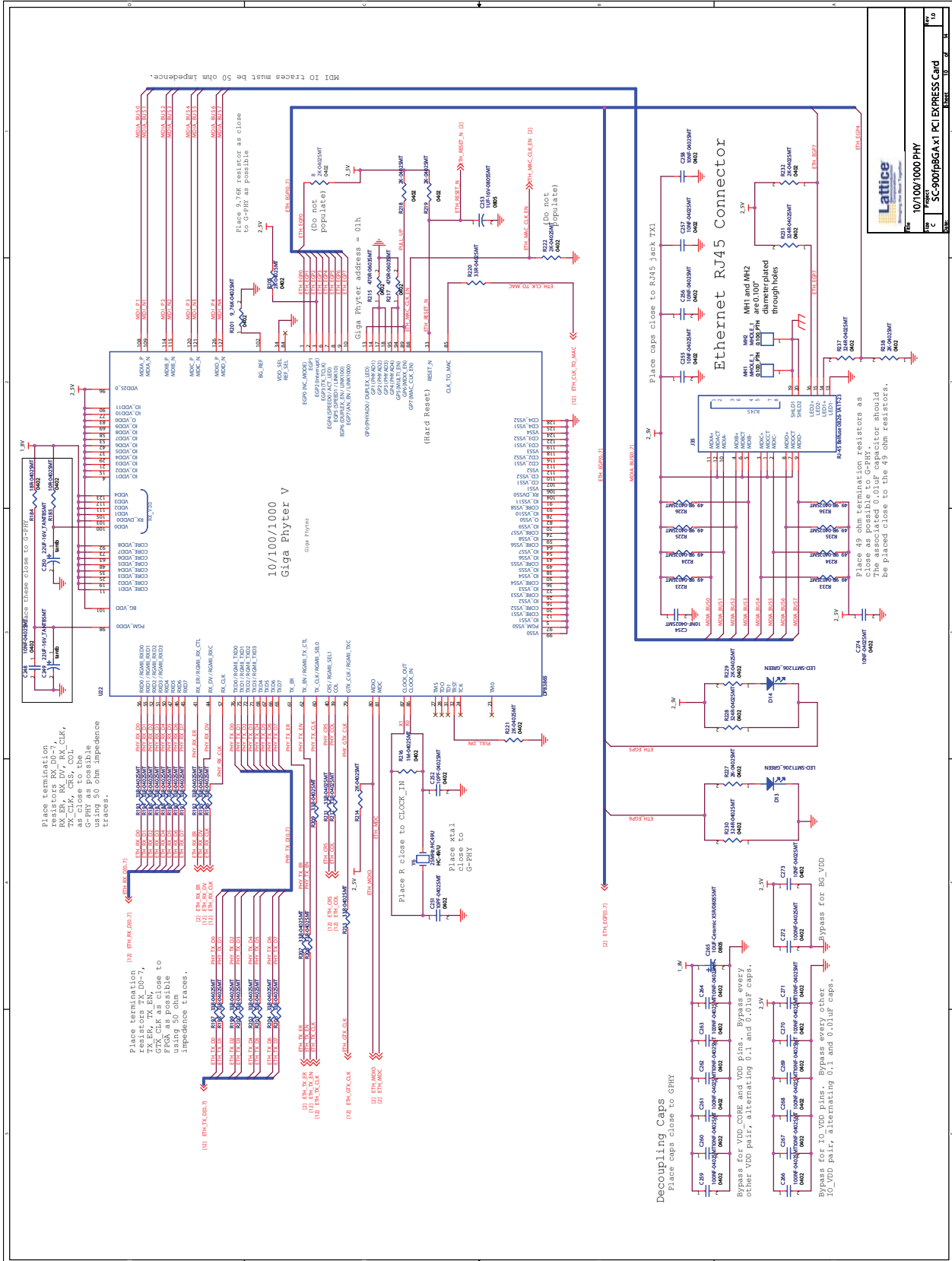
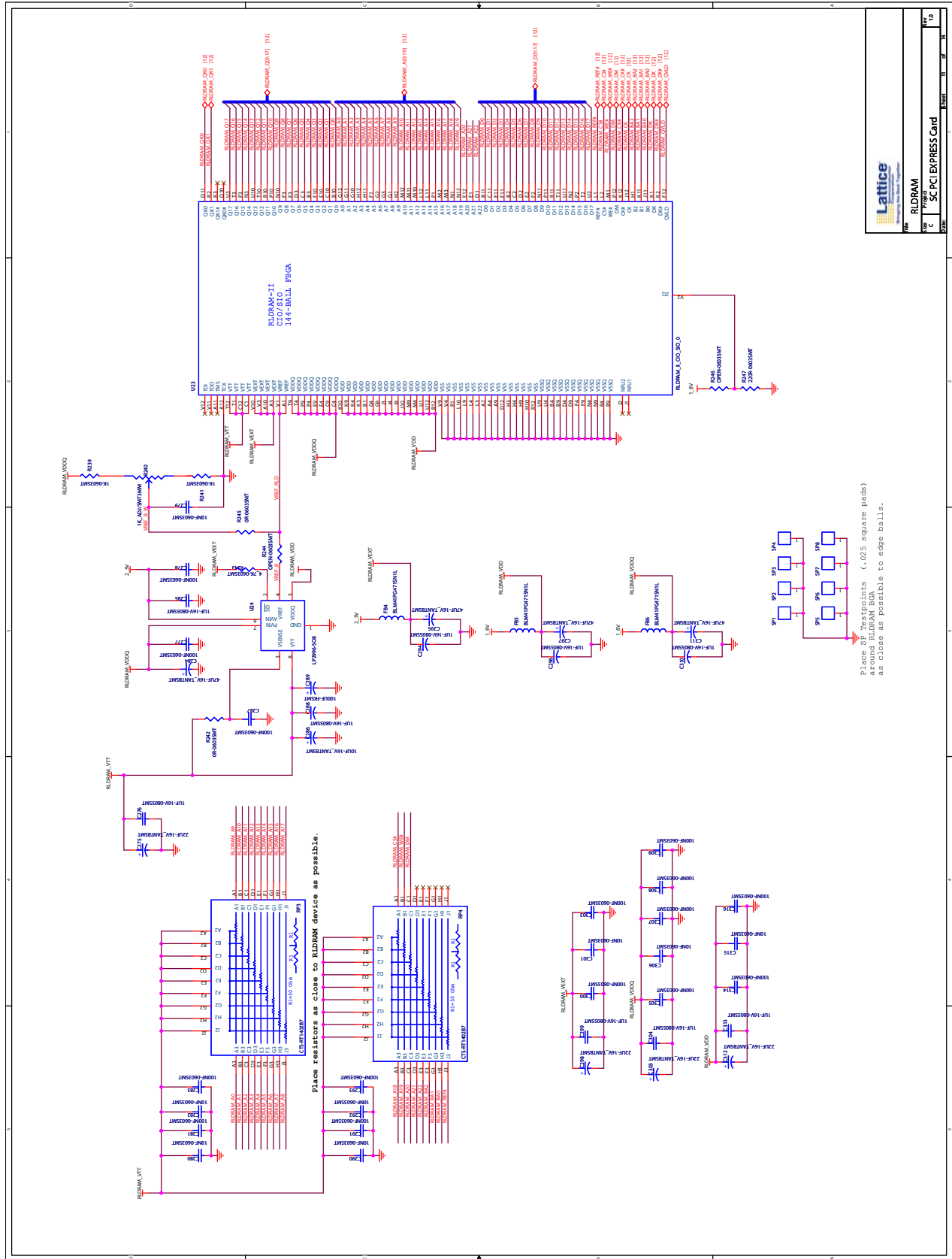


Figure 13. 10/100/1000 PHY



|         |                                 |
|---------|---------------------------------|
| Lattice |                                 |
| Part    | 10/100/1000 PHY                 |
| Product | SC-9001PBGA x1 PCI EXPRESS Card |
| Rev     | 1.0                             |

Figure 14. RLDRAM



|                  |        |
|------------------|--------|
| Lattice          |        |
| Part             | RLDRAM |
| Rev              | 1.0    |
| PCI EXPRESS CARD |        |
| Page             | 10     |

Figure 15. FPGA Banks

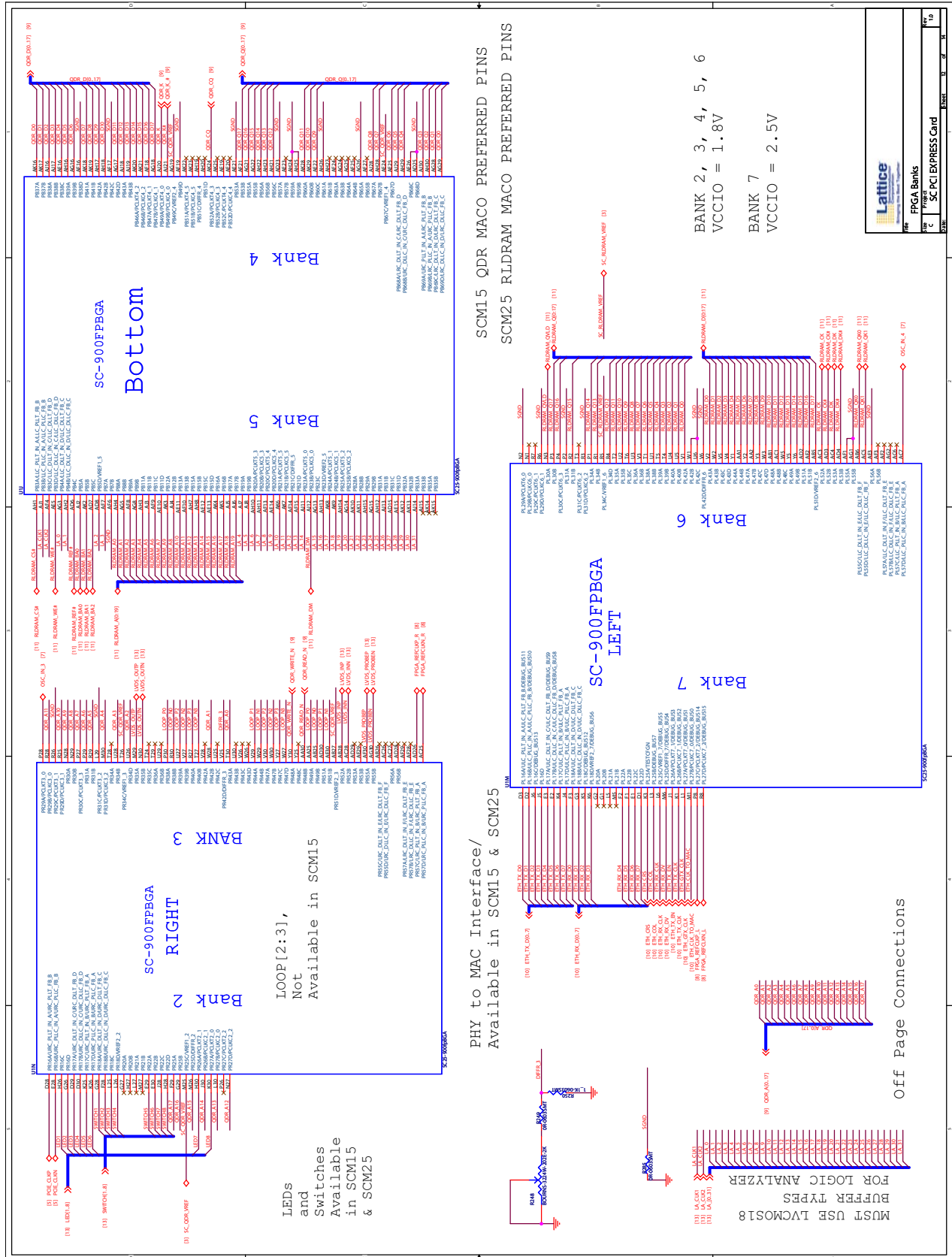
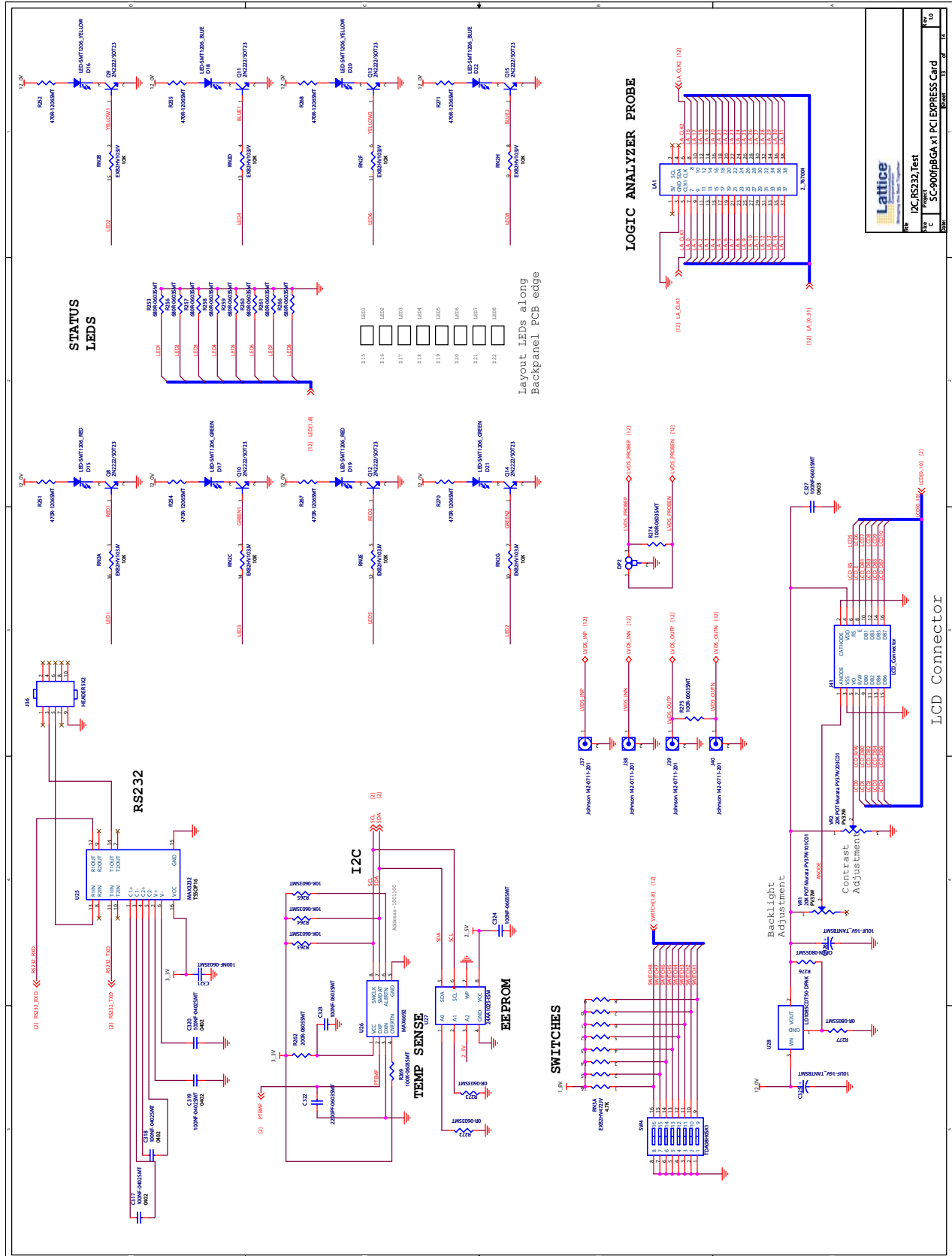


Figure 16. PC RS232 Test





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- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
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- Комплексную поставку.
- Работу по проектам и поставку образцов.
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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
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