

Serial-in / Parallel-out Driver Series

4-input Serial-in / Parallel-out Drivers

BU2152FS

Description

BU2152FS is a CMOS output driver. It incorporates a built-in shift register and a latch circuit to turn on a maximum of 24 output by a 4-wire interface, linked to a microcontroller.

A CMOS output can provides maximum 25mA current.

Features

- Possible to drive LED directly
- 24bit parallel output

Key Specifications

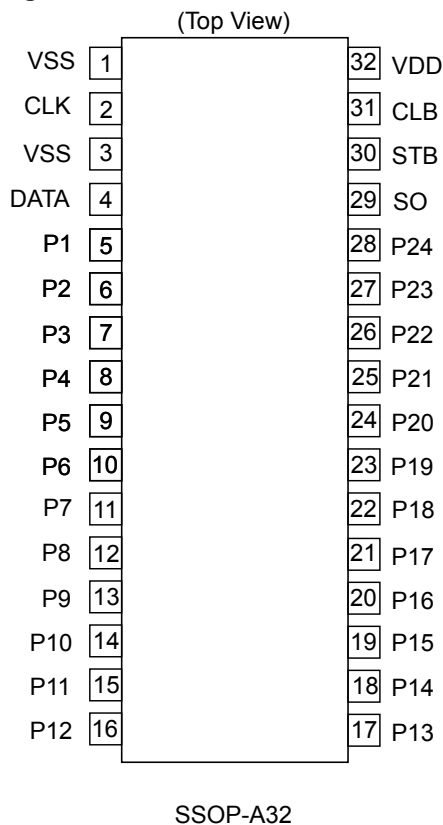
- Power supply voltage range: 2.7V to 5.5V
- Output voltage: 0V to V_{DD}
- Operating temperature range: -25°C to +85°C

Package

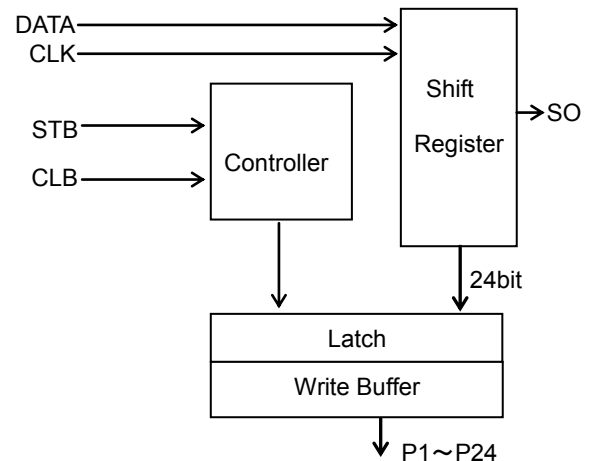
SSOP-A32

 W(Typ) x D(Typ) x H(Max)
 13.60mm x 7.80mm x 2.01mm

Pin Configurations



Block Diagrams



Pin Descriptions

Pin No.	Pin Name	I/O	Function
1	VSS	-	Ground
2	CLK	I	Serial Clock Input
3	VSS	-	Ground
4	DATA	I	Serial Data Input
5	P1	O	Parallel Data Output
6	P2		
7	P3		
8	P4		
9	P5		
10	P6		
11	P7		
12	P8		
13	P9		
14	P10		
15	P11		
16	P12		
17	P13		
18	P14		
19	P15		
20	P16		
21	P17		
22	P18		
23	P19		
24	P20		
25	P21		
26	P22		
27	P23		
28	P24		
29	SO	O	Serial Data Output
30	STB	I	Strobe Signal Input (active Low)
31	CLB	I	Clear Signal Input (active Low)
32	VDD	-	Power Supply

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Output Voltage	V_O	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Total output current	ΣI_o	55	mA
Operating Temperature Range	T_{opr}	-25 to +85	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Power Dissipation	P_D	0.76 ^(Note 1)	W

(Note 1) Derate by 7.6mW/°C when operating above $T_A=25^\circ\text{C}$ (when mounted in ROHM's standard board).

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions ($T_A=25^\circ\text{C}$, $V_{SS}=0\text{V}$)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Power Supply Voltage	V_{DD}	2.7	-	5.5	V	(Note 2)
Output Voltage	V_O	0	-	V_{DD}	V	-
Input rise time	t_r	-	-	1	μs	applied to CLK, DATA, STB, CLB pins ^(Note 3)
Input fall time	t_f	-	-	1	μs	

(Note 2) Set "L" to CLB pin during power up. Set "H" to CLB pin after power is stable.

When V_{DD} become equal to or less than 2.2V, set "L" to CLB pin to clear the latch circuit.

(Note 3) The input signal transition should be linear. Noise shouldn't be on these input pins as there is no hysteresis countermeasure on them.

The length of power and ground lines should be as short as possible and the bypass capacitor should be as close to the IC as possible so that the ground noise caused by the current in its operation don't cause any undesirable data errors.

The rise and fall times had better be smaller than the specified limits.

Electrical Characteristics (Unless otherwise specified $V_{DD}=5V, V_{SS}=0V, T_A=25^{\circ}C$)

Parameter	Symbol	Limits			Symbol	Limits
		Min	Typ	Min		
Input High-level Voltage	V_{IH}	2.0	-	-	V	-
Input Low-level Voltage	V_{IL}	-	-	0.6	V	-
Output Hi-level Voltage	V_{OH}	$V_{DD}-1.5$	-	-	V	$I_{OH}=-25mA$
		$V_{DD}-1.0$	-	-		$I_{OH}=-15mA$
		$V_{DD}-0.5$	-	-		$I_{OH}=-10mA$
Output Low-level Voltage	V_{OL}	-	-	1.5	V	$I_{OL}=+25mA$
		-	-	1.0		$I_{OL}=+15mA$
		-	-	0.8		$I_{OL}=+10mA$
Input High-level Leak Current	I_{IH}	-	-	1	μA	
Input Low-level Leak Current	I_{IL}	-	-	1	μA	
Quiescent Current	I_{DD}	-	-	5	μA	$V_{IL}=V_{SS}, V_{IH}=V_{DD},$ OUTPUT:OPEN

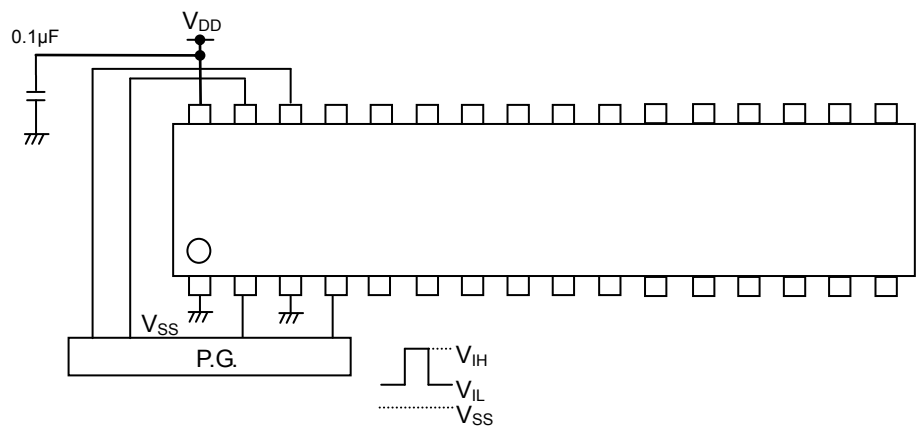


Figure 1. Input High/Low Voltage Measurement Circuit

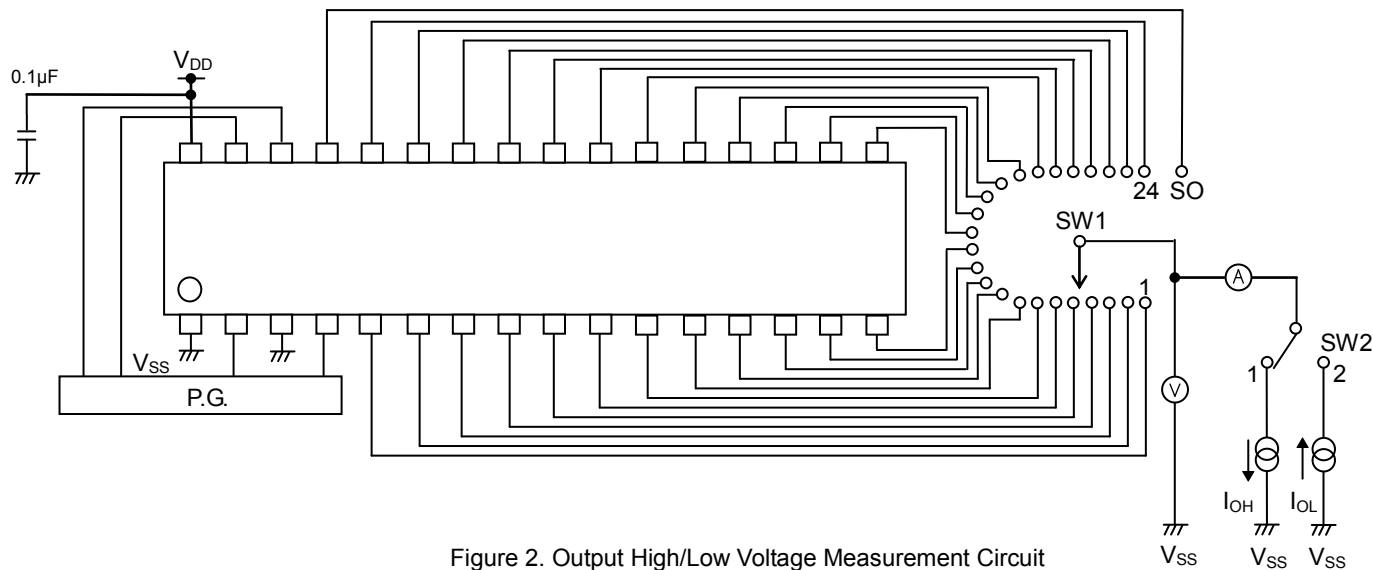


Figure 2. Output High/Low Voltage Measurement Circuit

Test condition

V_{OL} : Set all data "Low". SW2="2", SW1="1" to "24", SO.

V_{OH} : Set all data "High". SW2="1", SW1="1" to "24", SO.

Switching Characteristics (Unless otherwise specified $V_{DD}=5V$, $V_{SS}=0V$, $T_A=25^\circ C$)

Parameter	Symbol	Limit			Unit	Condition
		Min	Min	Min		
Maximum Clock Frequency	f_{MAX}	5	-	-	MHz	-
Setup Time 1	t_{SU1}	20	-	-	ns	DATA-CLK
Hold Time 1	t_{HD1}	20	-	-	ns	CLK-DATA
Setup Time 2	t_{SU2}	30	-	-	ns	STB-CLK
Hold Time 2	t_{HD2}	30	-	-	ns	CLK-STB
Setup Time 3	t_{SU3}	30	-	-	ns	CLB-CLK
Hold Time 3	t_{HD3}	30	-	-	ns	CLK-CLB
Setup Time 4	t_{SU4}	30	-	-	ns	STB-CLB
Hold Time 4	t_{HD4}	30	-	-	ns	CLB-STB
Output Delay Time 1	t_{PD1}	-	-	100	ns	CLK-P1 to P24, $C_L=50pF$
Output Delay Time 2	t_{PD2}	-	-	80	ns	STB-P1 to P24, $C_L=50pF$
Output Delay Time 3	t_{PD3}	-	-	80	ns	CLB-P1 to P24, $C_L=50pF$

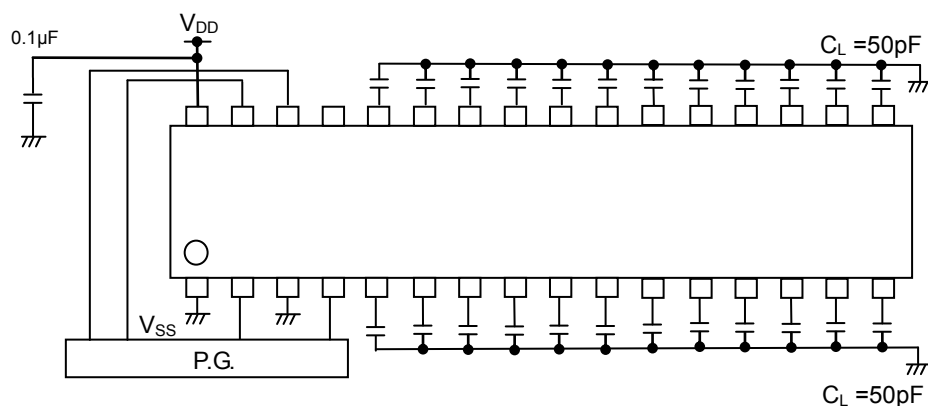
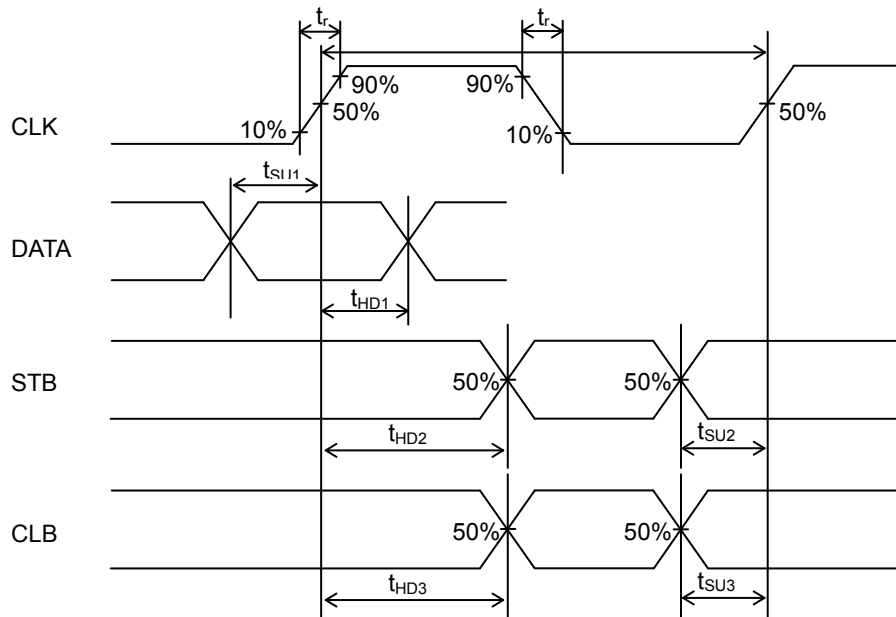
Switching Time Test Circuit

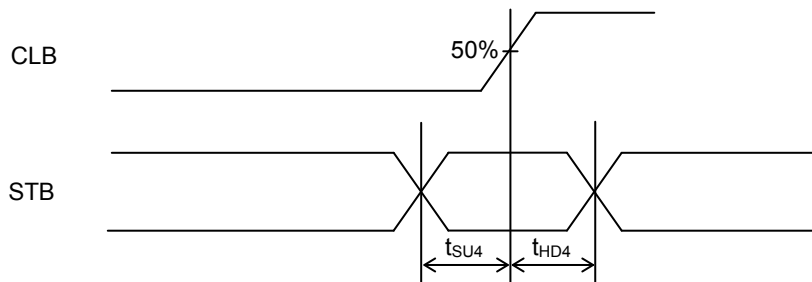
Figure 3. Switching Time Test Circuit

Switching Time Test Waveform

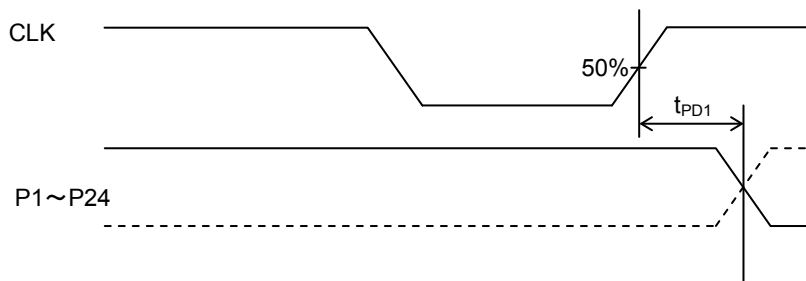
Set-up/Hold Time (DATA-CLK, STB-CLK, CLB-CLK)



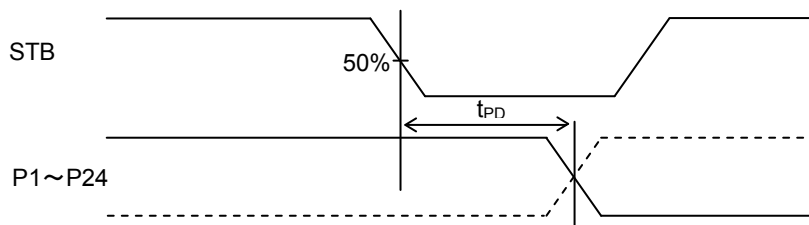
Set-up/Hold Time (STB-CLB)



Output Delay Time (CLK- P1 to P24)



Output Delay Time (STB- P1 to P24)



Output Delay Time (CLB- P1 to P24)

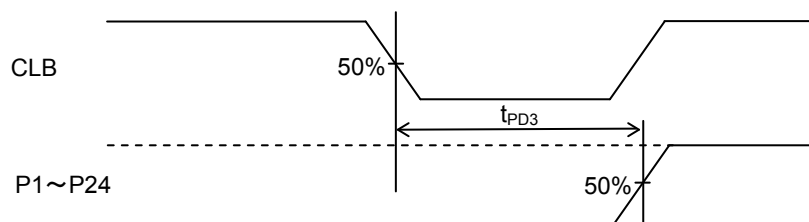


Figure 4. Switching Time Test Waveform

Timing Chart

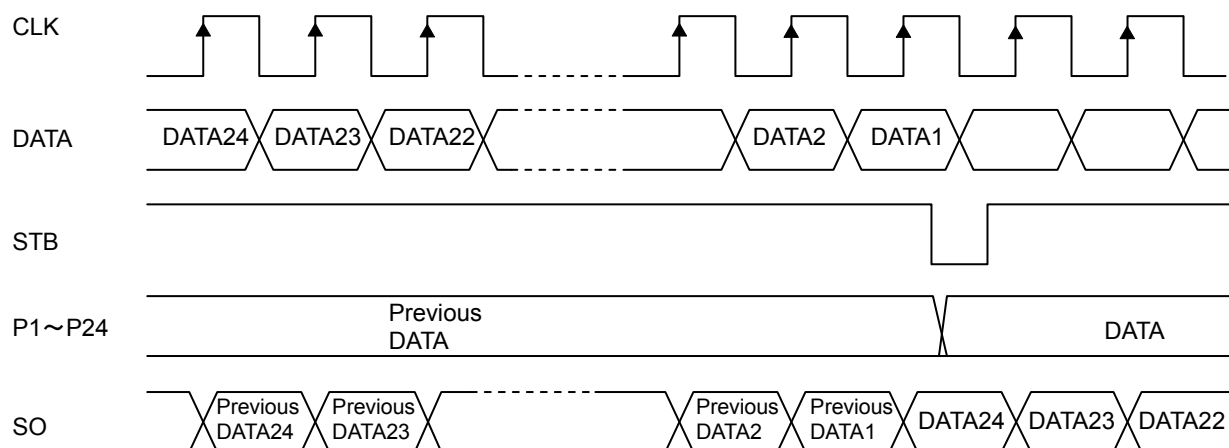


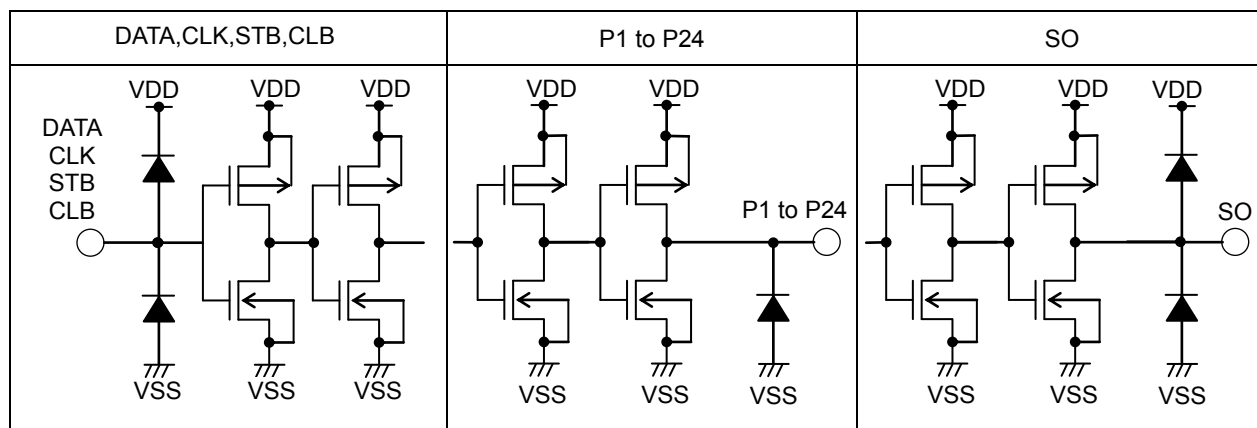
Figure 5. Timing Chart

1. After the power is turned on and the voltage is stabilized, STB should be activated, after clocking 24 data bits into the DATA terminal.
2. P1 to P24 parallel output data of the shift register is set after the 24th clock by the LCK.
3. Since the STB is a level trigger latch, data is retained in the "H" section and renewed in the "L" section of the STB.
4. The final stage data of the shift register is outputted to the SO by synchronizing with the rise time of the CLK.

[Truth Table]

Input			Function
CLK	STB	CLB	
×	×	L	All the data of the latch circuit are set to "H" (data of shift register does not change), all the parallel outputs are "H".
┐	H	H	Serial data of DATA pin are latched to the shift register. At this time, the data of the latch circuit does not change.
L	L	H	The data of the shift register are transferred to the latch circuit, and the data of the latch circuit are outputted from the parallel output pin.
H			
┐			The data of the shift register shifts 1bit, and the data of the latch circuit and parallel output also change.

I/O Equivalence Circuits



Power Dissipation

Power dissipation(total loss) indicates the power that can be consumed by IC at $T_A=25^{\circ}\text{C}$ (normal temperature). IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip(maximum junction temperature) and thermal resistance of package(heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability(hardness of heat release)is called thermal resistance, represented by the symbol θ_{JA} ($^{\circ}\text{C/W}$).The temperature of IC inside the package can be estimated by this thermal resistance. Figure 6 shows the model of thermal resistance of the package. Thermal resistance θ_{JA} , ambient temperature T_A , maximum junction temperature T_{Jmax} , and power dissipation P_D can be calculated by the equation below:

$$\theta_{JA} = (T_{Jmax} - T_A) / P_D \quad (^{\circ}\text{C/W})$$

Derating curve in Figure 7 indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θ_{JA} . Thermal resistance θ_{JA} depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition.

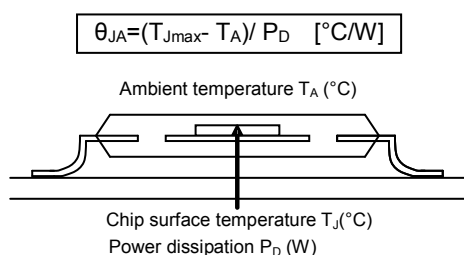


Figure 6. Thermal resistance

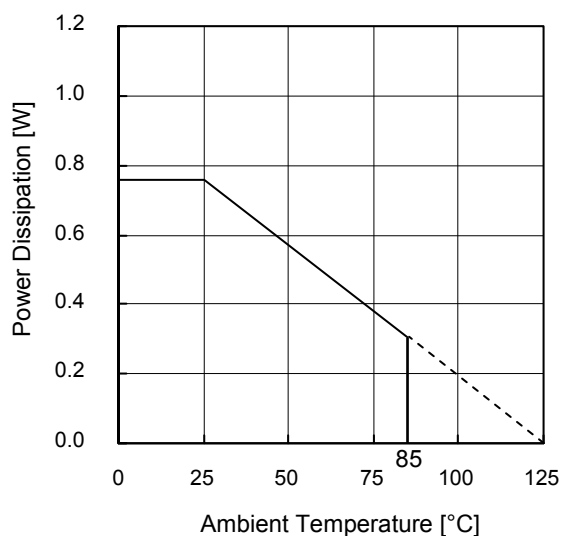


Figure 7. Derating curve of BU2152FS

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

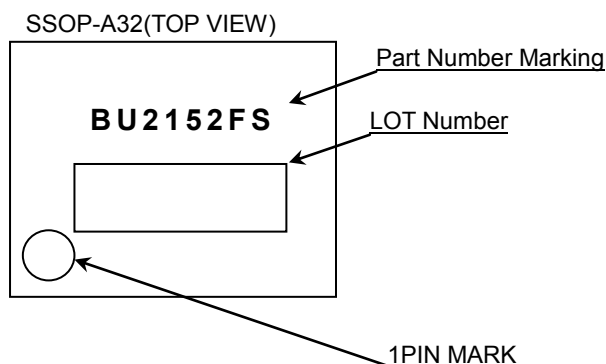
14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

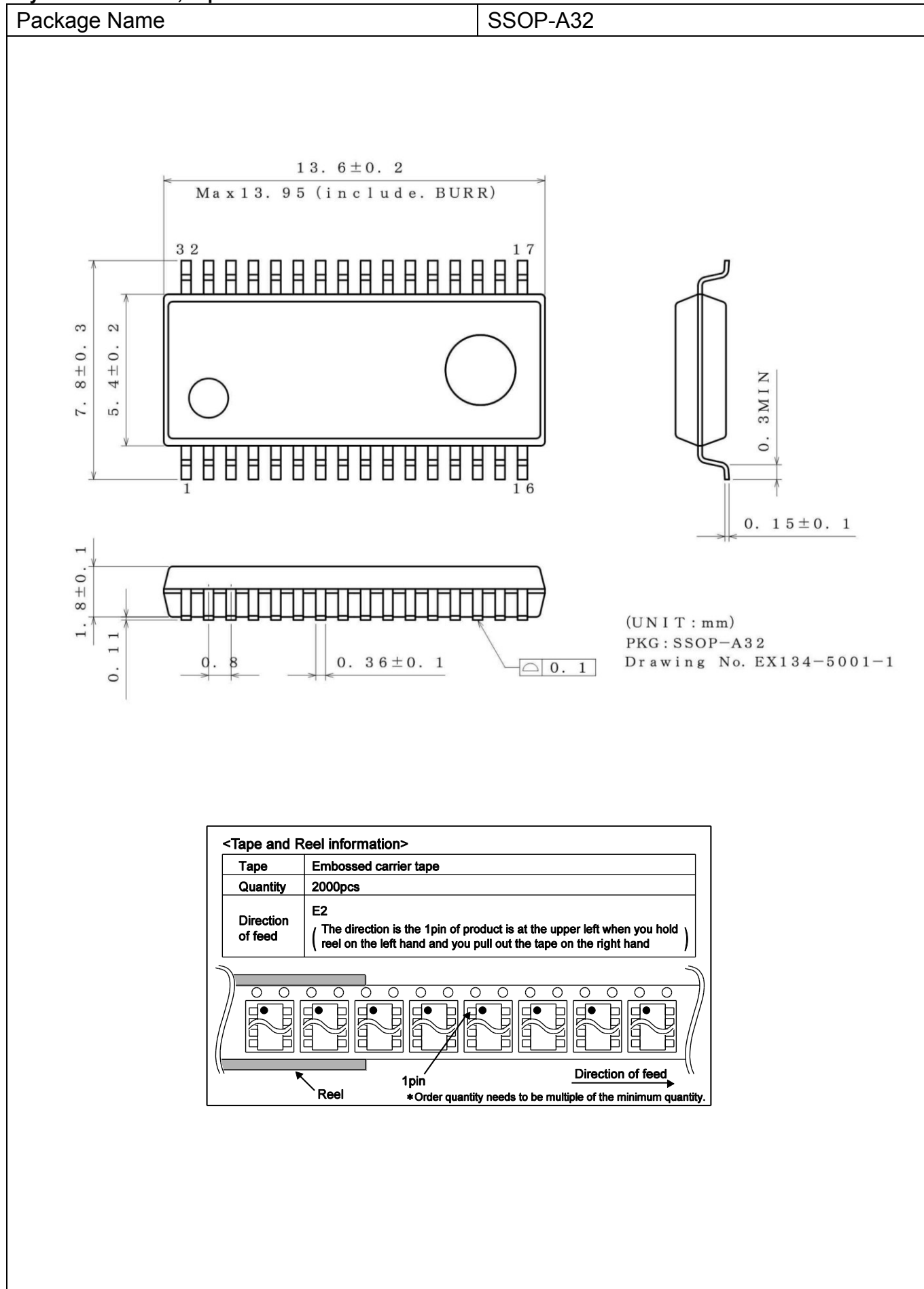
Ordering Information

B U 2 1 5 2 F S	-	E 2
Part Number	Package FS:SSOP-A32	Packaging and forming specification E2: Embossed tape and reel

Marking Diagrams



Physical Dimension, Tape and Reel Information



Revision History

Date	Revision	Changes
18.Apr.2014	001	New Release
24.Aug.2015	002	Add the total output current at absolute maximum ratings. Add the input rise time & the input fall time at recommended operating conditions. Renewal of the Note No. Correction of the power dissipation & the derating curve

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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