AX5051

Advanced Multi-channel Single Chip UHF Transceiver

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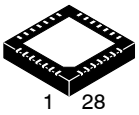


QFN28 5x5, 0.5P
CASE 485EF

ORDERING INFORMATION

Device	Type	Qty
AX5051−1−TA05	Tape & Reel	500
AX5051−1−TW30	Tape & Reel	3,000

OVERVIEW

The AX5051 is a true single chip low−power CMOS transceiver primarily for use in SRD bands. The on−chip transceiver consists of a fully integrated RF front−end with modulator, and demodulator. Base band data processing is implemented in an advanced and flexible communication controller that enables user−friendly communication via the SPI interface.

Features

- Advanced Multi−channel Single Chip UHF Transceiver
- Configurable for Usage in 400−470 MHz and 800−940 MHz SRD Bands
- Wide Variety of Shaped Modulations Supported in RX and TX (ASK, PSK, MSK, FSK)
- Data Rates from 1 to 350 kbps (FSK, MSK), 1 to 600 kbps (ASK), 10 to 600 kbps (PSK)
- Ultra Fast Settling RF Frequency Synthesizer for Low−power Consumption
- Variable Channel Filtering from 40 kHz to 600 kHz
- RF Carrier Frequency and FSK Deviation Programmable in 1 Hz Steps
- Fully Integrated Frequency Synthesizer with VCO Auto−ranging and Band−width Boost Modes for Fast Locking
- Few External Components
- On−chip Communication Controller and Flexible Digital Modem
- Channel Hopping up to 2000 hops/s
- Sensitivity down to −116 dBm at 1.2 kbps
- Up to +16 dBm Programmable Transmitter Power Amplifier
- Crystal Oscillator with Programmable Transconductance and Programmable Internal Tuning Capacitors for Low Cost Crystals
- Automatic Frequency Control (AFC)
- SPI Micro−controller Interface
- Fully Integrated Current/Voltage References
- QFN28 Package
- Low Power Receiver: 18 − 21 mA in High Sensitivity Mode and 16 − 18 mA in Low Power Mode
- Low Power Transmitter: 11 − 45 mA during Transmit
- Extended Supply Voltage Range 2.2 V − 3.6 V
- Internal Power−on−reset
- 32 Bit RX/TX Data FIFO
- Programmable Cyclic Redundancy Check (CRC−CCITT, CRC−16, CRC−32)
- Optional Spectral Shaping Using a Self Synchronizing Shift Register
- Brown−out Detection
- Integrated RX/TX Switching
- Differential Antenna Pins
- RoHS Compliant

Applications

- Telemetry
- Sensor Readout, Thermostats
- AMR
- Toys
- Wireless Audio
- Wireless Networks
- Wireless M−Bus
- Access Control
- Remote Keyless Entry
- Remote Controls
- Active RFID
- Compatible with FCC Part 15.247, FCC Part 15.249, EN 300 220 Wide Band, Wireless M−Bus S/T Mode 868 MHz, Konnex RF, ARIB T−67, 802.15.4

BLOCK DIAGRAM

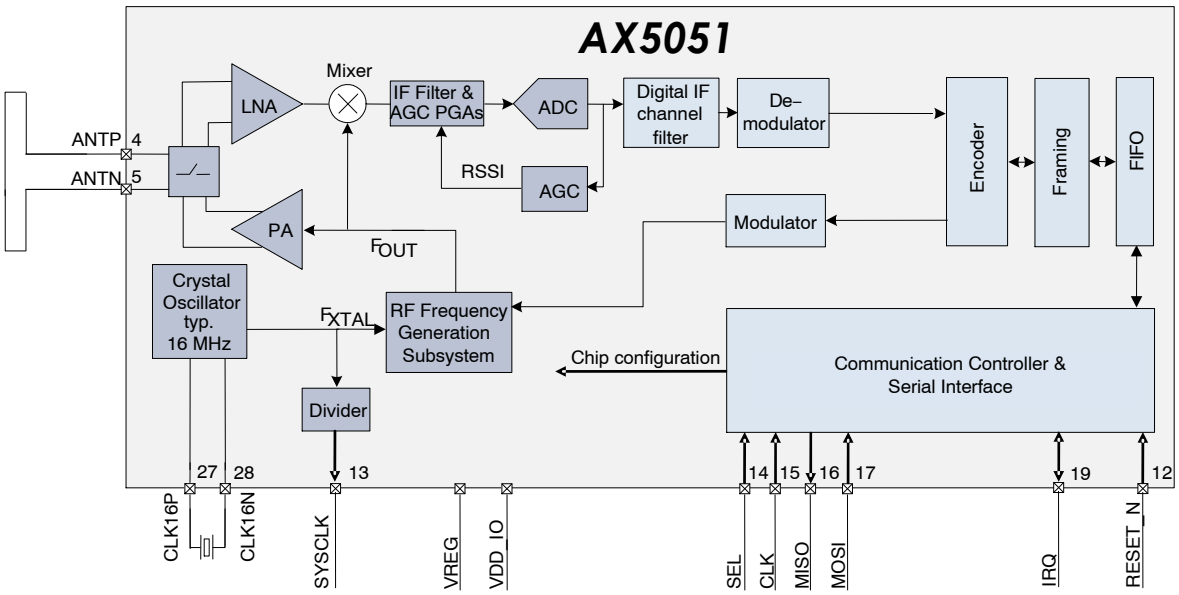


Figure 1. Functional Block Diagram of the AX5051

Table 1. PIN FUNCTION DESCRIPTIONS

Symbol	Pin(s)	Type	Description
NC	1	N	Not to be connected
VDD	2	P	Power supply, must be supplied with regulated voltage VREG
GND	3	P	Ground
ANTP	4	A	Antenna input/output
ANTN	5	A	Antenna input/output
GND	6	P	Ground
VDD	7	P	Power supply, must be supplied with regulated voltage VREG
NC	8	N	Not to be connected
TST1	9	I	Must be connected to GND
TST2	10	I	Must be connected to GND
GND	11	P	Ground
RESET_N	12	I	Optional reset input If this pin is not used it must be connected to VDD_IO
SYSCLK	13	I/O	Default functionality: Crystal oscillator (or divided) clock output Can be programmed to be used as a general purpose I/O pin
SEL	14	I	Serial peripheral interface select
CLK	15	I	Serial peripheral interface clock
MISO	16	O	Serial peripheral interface data output
MOSI	17	I	Serial peripheral interface data input
TST3	18	I	Must be connected to GND
IRQ	19	I/O	Default functionality: Transmit and receive interrupt Can be programmed to be used as a general purpose I/O pin
VDD_IO	20	P	Unregulated power supply
NC	21	N	Not to be connected
GND	22	P	Ground
NC	23	N	Not to be connected
VREG	24	P	Regulated output voltage VDD pins must be connected to this supply voltage A 1 μF low ESR capacitor to GND must be connected to this pin
NC	25	N	Not to be connected
NC	26	N	Not to be connected
CLK16P	27	A	Crystal oscillator input/output
CLK16N	28	A	Crystal oscillator input/output

A = analog signal
I = digital input signal
O = digital output signal
I/O = digital input/output signal
N = not to be connected
P = power or ground

All digital inputs are Schmitt trigger inputs; digital input and output levels are LVCMOS/LVTTL compatible and 5 V tolerant.

The center pad of the QFN28 package should be connected to GND.

Pinout Drawing

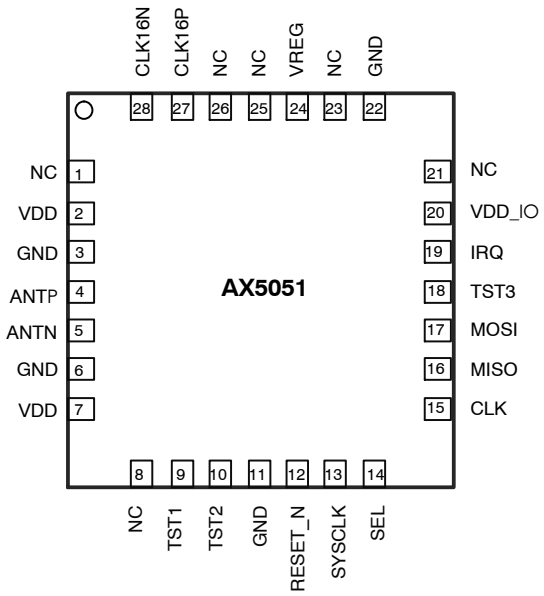


Figure 2. Pinout Drawing (Top View)

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Condition	Min	Max	Units
VDD_IO	Supply voltage		−0.5	5.5	V
IDD	Supply current			100	mA
P_{tot}	Total power consumption			800	mW
P_I	Absolute maximum input power at receiver input			15	dBm
I_{I1}	DC current into any pin except ANTP, ANTN		−10	10	mA
I_{I2}	DC current into pins ANTP, ANTN		−100	100	mA
I_O	Output current			40	mA
V_{ia}	Input voltage ANTP, ANTN pins		−0.5	5.5	V
	Input voltage digital pins		−0.5	5.5	V
V_{es}	Electrostatic handling	HBM	−2000	2000	V
T_{amb}	Operating temperature		−40	85	°C
T_{stg}	Storage temperature		−65	150	°C
T_j	Junction temperature			150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Table 3. SUPPLIES

Symbol	Description	Condition	Min	Typ	Max	Units
T_{AMB}	Operational ambient temperature		−40	27	85	°C
VDD_IO	I/O and voltage regulator supply voltage	RX operation or TX operation up to 4 dBm output power	2.2	3.0	3.6	V
		TX operation up to 16 dBm output power	2.4	3.0	3.6	V
VREG	Internally regulated supply voltage	Power−down mode PWRMODE=0x00		1.7		V
		All other power modes	2.1	2.5	2.8	V
$VREG_{droptyp}$	Regulator voltage drop	RX operation or TX operation up to 4 dBm output power			50	mV
$VREG_{dropmax}$	Regulator voltage drop at maximum internal current consumption	TX mode with 16 dBm output power			300	mV
I_{PDOWN}	Power−down current	PWRMODE = 0x00		0.5		μA
I_{RX-HS}	Current consumption RX High sensitivity mode: VCO_I = 001; REF_I = 011	Bit rate 10 kbit/s		19		mA
I_{RX-LP}	Current consumption RX Low power mode: VCO_I = 001; REF_I = 101	Bit rate 10 kbit/s		17		mA
I_{TX}	Current consumption TX VCO_I = 001; REF_I = 011; LOCURST = 1, (Note 1)	868 MHz, 15 dBm		45		mA
		433 MHz, 15 dBm		45		
TX_{varvdd}	Variation of output power over voltage	VDD > 2.5 V		± 0.5		dB
$TX_{vartemp}$	Variation of output power over temperature	VDD > 2.5 V		± 0.5		dB

1. The PA voltage is regulated to 2.5 V. Between 2.2 V and 2.55 V VDD_IO a drop of 1 dBm of output power is visible.

Note on Current Consumption in TX Mode

To achieve best output power the matching network has to be optimized for the desired output power and frequency. As a rule of thumb a good matching network produces about 50% efficiency with the AX5051 power amplifier although over 90% are theoretically possible. A typical matching network has between 1 dB and 2 dB loss (P_{loss}).

The current consumption can be calculated as

$$I_{TX}[mA] = \frac{1}{PA_{efficiency}} \times 10^{\left(\frac{P_{out}[dBm]+P_{loss}[dB]}{10}\right)} \div 2.5V + I_{offset}$$

I_{offset} is about 12 mA for the VCO at 400−470 MHz and 11 mA for 800−940 MHz. The following table shows calculated current consumptions versus output power for P_{loss} = 1 dB, $PA_{efficiency}$ = 0.5 and I_{offset} = 11 mA at 868 MHz.

Table 4.

Pout [dBm]	I [mA]
0	13.0
1	13.2
2	13.6
3	14.0
4	14.5
5	15.1
6	16.0
7	17.0
8	18.3
9	20.0
10	22.0
11	24.6
12	27.96
13	32.1
14	37.3
15	43.8

The AX5051 power amplifier runs from the regulated VDD supply and not directly from the battery. This has the advantage that the current and output power do not vary much over supply voltage and temperature from 2.55 V to 3.6 V supply voltage. Between 2.55 V and 2.2 V a drop of about 1 dB in output power occurs.

Table 5. LOGIC

Symbol	Description	Condition	Min	Typ	Max	Units
Digital Inputs						
V_{T+}	Schmitt trigger low to high threshold point			1.9		V
V_{T-}	Schmitt trigger high to low threshold point			1.2		V
V_{IL}	Input voltage, low				0.8	V
V_{IH}	Input voltage, high		2.0			V
I_L	Input leakage current		−10		10	μA
Digital Outputs						
I_{OH}	Output Current, high	V_{OH} = 2.4 V	4			mA
I_{OL}	Output Current, low	V_{OL} = 0.4 V	4			mA
I_{OZ}	Tri−state output leakage current		−10		10	μA

AC Characteristics

Table 6. CRYSTAL OSCILLATOR

Symbol	Description	Condition	Min	Typ	Max	Units
f_{XTAL}	Crystal frequency	Notes 1, 3	15.5	16	25	MHz
gm_{osc}	Transconductance oscillator	XTALOSCGM = 0000		1		mS
		XTALOSCGM = 0001		2		
		XTALOSCGM = 0010 default		3		
		XTALOSCGM = 0011		4		
		XTALOSCGM = 0100		5		
		XTALOSCGM = 0101		6		
		XTALOSCGM = 0110		6.5		
		XTALOSCGM = 0111		7		
		XTALOSCGM = 1000		7.5		
		XTALOSCGM = 1001		8		
		XTALOSCGM = 1010		8.5		
		XTALOSCGM = 1011		9		
		XTALOSCGM = 1100		9.5		
		XTALOSCGM = 1101		10		
		XTALOSCGM = 1110		10.5		
		XTALOSCGM = 1111		11		
C_{osc}	Programmable tuning capacitors at pins CLK16N and CLK16P	XTALCAP = 000000 default		2		pF
		XTALCAP = 111111		33		
$C_{osc-lsb}$	Programmable tuning capacitors, increment per LSB of XTALCAP			0.5		pF
f_{ext}	External clock input	Notes 2, 3	15.5	15	25	MHz
RIN_{osc}	Input DC impedance		10			kΩ

1. Tolerances and start−up times depend on the crystal used. Depending on the RF frequency and channel spacing the IC must be calibrated to the exact crystal frequency using the readings of the register TRKFREQ.
2. If an external clock is used, it should be input via an AC coupling at pin CLK16P with the oscillator powered up and XTALCAP = 000000
3. Lower frequencies than 15.5 MHz or higher frequencies than 25 MHz can be used. However, not all typical RF frequencies can then be generated.

Table 7. RF FREQUENCY GENERATION SUBSYSTEM (SYNTHESIZER)

Symbol	Description	Condition	Min	Typ	Max	Units
f_{REF}	Reference frequency	Note 1		16 24		MHz
f_{range_hi}	Frequency range	BANDSEL = 0	800		940	MHz
f_{range_low}		BANDSEL = 1	400		470	
f_{RESO}	Frequency resolution		1			Hz
BW_1	Synthesizer loop bandwidth VCO current: VCOI = 001	Loop filter configuration: FLT = 01 Charge pump current: PLLCPI = 010		100		kHz
BW_2		Loop filter configuration: FLT = 01 Charge pump current: PLLCPI = 001		50		
BW_3		Loop filter configuration: FLT = 11 Charge pump current: PLLCPI = 010		200		
BW_4		Loop filter configuration: FLT = 10 Charge pump current: PLLCPI = 010		500		
T_{set1}	Synthesizer settling time for 1 MHz step as typically required for RX/TX switching VCO current: VCO_I = 001	Loop filter configuration: FLT = 01 Charge pump current: PLLCPI = 010		15		μs
T_{set2}		Loop filter configuration: FLT = 01 Charge pump current: PLLCPI = 001		30		
T_{set3}		Loop filter configuration: FLT = 11 Charge pump current: PLLCPI = 010		7		
T_{set4}		Loop filter configuration: FLT = 10 Charge pump current: PLLCPI = 010		3		
T_{start1}	Synthesizer start−up time if crystal oscillator and reference are running VCO current: VCO_I = 001	Loop filter configuration: FLT = 01 Charge pump current: PLLCPI = 010		25		μs
T_{start2}		Loop filter configuration: FLT = 01 Charge pump current: PLLCPI = 001		50		
T_{start3}		Loop filter configuration: FLT = 11 Charge pump current: PLLCPI = 010		12		
T_{start4}		Loop filter configuration: FLT = 10 Charge pump current: PLLCPI = 010		5		
$PN868_1$	Synthesizer phase noise Loop filter configuration: FLT = 01 Charge pump current: PLLCPI = 010 VCO current: VCO_I = 001	868 MHz, 50 kHz from carrier		−85		dBc/Hz
		868 MHz, 100 kHz from carrier		−90		
		868 MHz, 300 kHz from carrier		−100		
		868 MHz, 2 MHz from carrier		−110		
$PN433_1$		433 MHz, 50 kHz from carrier		−90		
		433 MHz, 100 kHz from carrier		−95		
		433 MHz, 300 kHz from carrier		−105		
		433 MHz, 2 MHz from carrier		−115		
$PN868_2$	Synthesizer phase noise Loop filter configuration: FLT = 01 Charge pump current: PLLCPI = 001 VCO current: VCO_I = 001	868 MHz, 50 kHz from carrier		−80		dBc/Hz
		868 MHz, 100 kHz from carrier		−90		
		868 MHz, 300 kHz from carrier		−105		
		868 MHz, 2 MHz from carrier		−115		
$PN433_2$		433 MHz, 50 kHz from carrier		−90		
		433 MHz, 100 kHz from carrier		−95		
		433 MHz, 300 kHz from carrier		−110		
		433 MHz, 2 MHz from carrier		−122		

1. ASK, PSK and 0.1−200 kbps FSK with 16 MHz crystal, 200−350 kbps FSK with 24 MHz crystal.

Table 8. TRANSMITTER

Symbol	Description	Condition	Min	Typ	Max	Units
SBR	Signal bit rate	ASK	1		600	kbps
		PSK	10		600	
		FSK, (Note 2)	1		350	
		802.15.4 (DSSS) ASK and PSK	1		40	
		802.15.4 (DSSS) FSK	1		16	
PTX_{868}	Transmitter power @ 868 MHz	TXRNG = 0000 LOCURST = 1		15		dBm
PTX_{433}	Transmitter power @ 433 MHz	TXRNG = 1111 LOCURST = 1		16		dBm
$PTX_{868-harm2}$	Emission @ 2nd harmonic	(Note 1)		−50		dBc
$PTX_{868-harm3}$	Emission @ 3rd harmonic			−55		

1. Additional low−pass filtering was applied to the antenna interface, see section Application Information.
2. 1 − 200 kbps with 16 MHz crystal, 200 − 350 kbps with 24 MHz crystal

Table 9. RECEIVER

	Input Sensitivity in dBm TYP. at SMA Connector for BER = 10^{-3} (433 or 868 MHz)					
Datarate [kbps]	ASK	FSK h = 1	FSK h = 4	FSK h = 8	FSK h = 16	PSK
1.2				−115	−116	
2				−115	−115	
10	−103			−109		−110
100	−97	−103	−98			−104
200	−94	−100				−100
600	−90					−98

Table 10.

Symbol	Description	Condition	Min	Typ	Max	Units
SBR	Signal bit rate	ASK	1		600	kbps
		PSK	10		600	
		FSK	1		350	
		802.15.4 (DSSS) ASK and PSK	1		40	
		802.15.4 (DSSS) FSK	1		16	
IL	Maximum input level				−20	dBm
CP_{1dB}	Input referred compression point	2 tones separated by 100 kHz		−35		dBm
IIP3	Input referred IP3			−25		
RSSIR	RSSI control range			85		dB
$RSSIS_1$	RSSI step size	Before digital channel filter; calculated from register AGCCOUNTER		0.625		dB
$RSSIS_2$	RSSI step size	Behind digital channel filter; calculated from registers AGCCOUNTER, TRKAMPL		0.1		dB
SEL_{868}	Adjacent channel suppression	FSK 50 kbps, (Notes 1 & 2)		18		dB
	Alternate channel suppression			19		
	Adjacent channel suppression	FSK 100 kbps, (Notes 1 & 3)		16		dB
	Alternate channel suppression			30		
	Adjacent channel suppression	PSK 200 kbps, (Notes 1 & 4)		17		dB
	Alternate channel suppression			28		
BLK_{868}	Blocking at ± 1 MHz offset	FSK 100 kbps, (Note 5)		38		dB
	Blocking at − 2 MHz offset			40		
	Blocking at ± 10 MHz offset			60		
	Blocking at ± 100 MHz offset			82		
$IMRR_{868}$	Image rejection			30		

1. Interferer/Channel @ BER = 10^{-3}, channel level is +10 dB above the typical sensitivity, the interfering signal is a random data signal (except PSK200); both channel and interferer are modulated without shaping
2. FSK 50 kbps: 868 MHz, 200 kHz channel spacing, 25 kHz deviation, programming as recommended in Programming Manual
3. FSK 100 kbps: 868 MHz, 400 kHz channel spacing, 50 kHz deviation , programming as recommended in Programming Manual
4. PSK 200 kbps: 868 MHz, 400 kHz channel spacing, programming as recommended in Programming Manual, interfering signal is a constant wave
5. Channel/Blocker @ BER = 10^{-3}, channel level is +10 dB above the typical sensitivity, the blocker signal is a constant wave; channel signal is modulated without shaping, the image frequency lies 2 MHz above the wanted signal

Table 11. SPI TIMING

Symbol	Description	Condition	Min	Typ	Max	Units
Tss	SEL falling edge to CLK rising edge		10			ns
Tsh	CLK falling edge to SEL rising edge		10			ns
Tssd	SEL falling edge to MISO driving		0		10	ns
Tssz	SEL rising edge to MISO high−Z		0		10	ns
Ts	MOSI setup time		10			ns
Th	MOSI hold time		10			ns
Tco	CLK falling edge to MISO output				10	ns
Tck	CLK period	(Note 1)	50			ns
Tcl	CLK low duration		40			ns
Tch	CLK high duration		40			ns

1. For SPI access during power−down mode the period should be relaxed to 100 ns.

For a figure showing the SPI timing parameters see section Serial Peripheral Interface (SPI).

CIRCUIT DESCRIPTION

The AX5051 is a true single chip low−power CMOS transceiver primarily for use in SRD bands. The on−chip transceiver consists of a fully integrated RF front−end with modulator, and demodulator. Base band data processing is implemented in an advanced and flexible communication controller that enables user−friendly communication via the SPI interface.

AX5051 can be operated from 2.2 V to 3.6 V power supply over a temperature range from −40°C to 85°C, it consumes 11 − 45 mA for transmitting depending on the output power, 19 mA for receiving in high sensitivity mode and 18 mA for receiving in low power mode.

The AX5051 features make it an ideal interface for integration into various battery powered SRD solutions such as ticketing or as transceiver for telemetric applications e.g. in sensors. As primary application, the transceiver is intended for UHF radio equipment in accordance with the European Telecommunication Standard Institute (ETSI) specification EN 300 220−1 and the US Federal Communications Commission (FCC) standard CFR47, part 15. The use of AX5051 in accordance to FCC Par 15.247, allows for improved range in the 915 MHz band. Additionally AX5051 is compatible with the low frequency standards of 802.15.4 (ZigBee). It therefore incorporates a DSSS engine, which spreads data on the transmitter and despreads data for the receiver. Spreading and despreading is possible on all data rates and modulation schemes. The net transfer rate is reduced by a factor of 15 in this case. For 802.15.4 either 600 or 300 kbps modes have to be chosen.

The AX5051 sends and receives data via the SPI port in frames. This standard operation mode is called Frame Mode. Pre and post ambles as well as checksums can be generated automatically. Interrupts control the data flow between a controller and the AX5051.

The AX5051 behaves as a SPI slave interface. Configuration of the AX5051 is also done via the SPI interface.

AX5051 supports any data rate from 1 kbps to 350 kbps for FSK and MSK and from 1 kbps for 600 kbps for ASK and 10 kbps to 600 kbps PSK. To achieve optimum performance for specific data rates and modulation schemes several register settings to configure the AX5051 are necessary, they are outlined in the following, for details see the AX5051 Programming Manual.

The receiver supports multi−channel operation for all data rates and modulation schemes.

Voltage Regulator

The AX5051 uses an on−chip voltage regulator to create a stable supply voltage for the internal circuitry at pin VREG from the primary supply VDD_IO. All VDD pins of the device must be connected to VREG. The antenna pins ANTP and ANTN must be DC biased to VREG. The I/O level of the digital pins is VDD_IO.

The voltage regulator requires a 1 μF low ESR capacitor at pin VREG.

In power−down mode the voltage regulator typically outputs 1.7 V at VREG, if it is powered−up its output rises to typically 2.5 V. At device power−up the regulator is in power−down mode.

The voltage regulator must be powered−up before receive or transmit operations can be initiated. This is handled automatically when programming the device modes via the PWRMODE register.

Register VREG contains status bits that can be read to check if the regulated voltage is above 1.3 V or 2.3 V, sticky versions of the bits are provided that can be used to detect low power events (brown−out detection).

Crystal Oscillator

The on−chip crystal oscillator allows the use of an inexpensive quartz crystal as the RF generation subsystem's timing reference. Although a wider range of crystal frequencies can be handled by the crystal oscillator circuit, it is recommended to use 16 MHz as reference frequency for ASK and PSK modulations independent of the data rate. For FSK it is recommended to use a 16 MHz crystal for data rates below 200 kbps and 24 MHz for data rates above 200 kbps.

The oscillator circuit is enabled by programming the PWRMODE register. At power−up it is not enabled.

To adjust the circuit's characteristics to the quartz crystal being used without using additional external components, both the transconductance and the tuning capacitance of the crystal oscillator can be programmed.

The transconductance is programmed via register bits XTALOSCGM[3:0] in register XTALOSC.

The integrated programmable tuning capacitor bank makes it possible to connect the oscillator directly to pins CLK16N and CLK16P without the need for external capacitors. It is programmed using bits XTALCAP[5:0] in register XTALCAP.

To synchronize the receiver frequency to a carrier signal, the oscillator frequency could be tuned using the capacitor bank however, the recommended method to implement frequency synchronization is to make use of the high resolution RF frequency generation sub−system together with the Automatic Frequency Control, both are described further down.

Alternatively a single ended reference (TXCO, CXO) may be used. The CMOS levels should be applied to CLK16P via an AC coupling with the crystal oscillator enabled.

SYSCLK Output

The SYSCLK pin outputs the reference clock signal divided by a programmable integer. Divisions from 1 to 2048 are possible. For divider ratios > 1 the duty cycle is

50%. Bits SYSCLK[3:0] in the PINCFG1 register set the divider ratio. The SYSCLK output can be disabled.

Outputting a frequency that is identical to the IF frequency (default 1 MHz) on the SYSCLK pin is not recommended during receive operation, since it requires extensive decoupling on the PCB to avoid interference.

Power−on−reset (POR) and RESET_N Input

AX5051 has an integrated power−on−reset block. No external POR circuit or signal at the RESET_N pin is required, prior to POR the RESET_N pin is disabled.

After POR the AX5051 can be reset in two ways:

1. By SPI accesses: the bit RST in the PWRMODE register is toggled.
2. Via the RESET_N pin: A low pulse is applied at the RESET_N pin. With the rising edge of RESET_N the device goes into its operational state.

After POR or reset all registers are set to their default values.

If the RESET_N pin is not used it must be tied to VDD_IO.

RF Frequency Generation Subsystem

The RF frequency generation subsystem consists of a fully integrated synthesizer, which multiplies the reference frequency from the crystal oscillator to get the desired RF frequency. The advanced architecture of the synthesizer enables frequency resolutions of 1 Hz, as well as fast settling times of 5 – 50 μs depending on the settings (see section: AC Characteristics). Fast settling times mean fast start−up and fast RX/TX switching, which enables low−power system design.

For receive operation the RF frequency is fed to the mixer, for transmit operation to the power−amplifier.

The frequency must be programmed to the desired carrier frequency. The RF frequency shift by the IF frequency that is required for RX operation, is automatically set when the receiver is activated and does not need to be programmed by the user. The default IF frequency is 1 MHz. It can be programmed to other values. Changing the IF−frequency and thus the center frequency of the digital channel filter can be used to adapt the blocking performance of the device to specific system requirements.

The synthesizer loop bandwidth can be programmed. This serves three purposes:

1. Start−up time optimization, start−up is faster for higher synthesizer loop bandwidths.
2. TX spectrum optimization, phase−noise at 300 kHz to 1 MHz distance from the carrier improves with lower synthesizer loop bandwidths.
3. Adaptation of the bandwidth to the data−rate. For transmission of FSK and MSK it is required that the synthesizer bandwidth must be in the order of the data−rate.

VCO

An on−chip VCO converts the control voltage generated by the charge pump and loop filter into an output frequency. This frequency is used for transmit as well as for receive operation. The frequency can be programmed in 1 Hz steps in the FREQ registers. For operation in the 433 MHz band, the BANDSEL bit in the PLLLOOP register must be programmed.

VCO Auto−Ranging

The AX5051 has an integrated auto−ranging function, which allows to set the correct VCO range for specific frequency generation subsystem settings automatically. Typically it has to be executed after power−up. The function is initiated by setting the RNG_START bit in the PLLRANGING register. The bit is readable and a 0 indicates the end of the ranging process. The RNGERR bit indicates the correct execution of the auto−ranging.

Loop Filter and Charge Pump

The AX5051 internal loop filter configuration together with the charge pump current sets the synthesizer loop band width. The loop−filter has three configurations that can be programmed via the register bits FLT[1:0] in register PLLLOOP, the charge pump current can be programmed using register bits PLLCPI[1:0] also in register PLLLOOP. Synthesizer bandwidths are typically 50 – 500 kHz depending on the PLLLOOP settings, for details see the section: AC Characteristics.

Registers

Table 12. REGISTERS

Register	Bits	Purpose
PLLLOOP	FLT[1:0]	Synthesizer loop filter bandwidth, recommended usage is to increase the bandwidth for faster settling time, bandwidth increases of factor 2 and 5 are possible.
	PLLCPI[2:0]	Synthesizer charge pump current, recommended usage is to decrease the bandwidth (and improve the phase−noise) for low data−rate transmissions.
	BANDSEL	Switches between 868 MHz / 915 MHz and 433 MHz bands
FREQ		Programming of the carrier frequency
IFFREQHI, IFFREQLO		Programming of the IF frequency
PLLRANGING		Initiate VCO auto−ranging and check results

RF Input and Output Stage (ANTP/ANTN)

The AX5051 uses fully differential antenna pins. RX/TX switching is handled internally; an external RX/TX switch is not required.

LNA

The LNA amplifies the differential RF signal from the antenna and buffers it to drive the I/Q mixer. An external matching network is used to adapt the antenna impedance to the IC impedance. A DC feed to the regulated supply voltage VREG must be provided at the antenna pins. For recommendations see section: Application Information.

I/Q Mixer

The RF signal from the LNA is mixed down to an IF of typically 1 MHz. I− and Q−IF signals are buffered for the analog IF filter.

PA

In TX mode the PA drives the signal generated by the frequency generation subsystem out to the differential antenna terminals. The output power of the PA is programmed via bits TXRNG[3:0] in the register TXPWR. Output power as well as harmonic content will depend on the external impedance seen by the PA, recommendations are given in the section: Application Information.

Analog IF Filter

The mixer is followed by a complex band−pass IF filter, which suppresses the down−mixed image while the wanted signal is amplified. The center frequency of the filter is 1 MHz, with a pass−band width of 1 MHz. The RF frequency generation subsystem must be programmed in such a way that for all possible modulation schemes the IF frequency spectrum fits into the pass−band of the analog filter.

Digital IF Channel Filter and Demodulator

The digital IF channel filter and the demodulator extract the data bit−stream from the incoming IF signal. They must be programmed to match the modulation scheme as well as the data rate. Inaccurate programming will lead to loss of sensitivity.

The channel filter offers bandwidths of 40 kHz up to 600 kHz.

For detailed instructions how to program the digital channel filter and the demodulator see the AX5051 Programming Manual, an overview of the registers involved is given in the following table. The register setups typically must be done once at power−up of the device.

Table 13. REGISTERS

Register	Remarks
CICDEC	This register programs the bandwidth of the digital channel filter.
DATARATEHI, DATARATELO	These registers specify the receiver bit rate, relative to the channel filter bandwidth.
TMGGAINHI, TMGGAINLO	These registers specify the aggressiveness of the receiver bit timing recovery. More aggressive settings allow the receiver to synchronize with shorter preambles, at the expense of more timing jitter and thus a higher bit error rate at a given signal−to−noise ratio.
MODULATION	This register selects the modulation to be used by the transmitter and the receiver, i.e. whether ASK, PSK , FSK, MSK or OQPSK should be used.
PHASEGAIN, FREQGAIN, FREQGAIN2, AMPLGAIN	These registers control the bandwidth of the phase, frequency offset and amplitude tracking loops. Recommended settings are provided in the Programming Manual.
AGCATTACK, AGCDECAY	These registers control the AGC (automatic gain control) loop slopes, and thus the speed of gain adjustments. The faster the bit rate, the faster the AGC loop should be. Recommended settings are provided in the Programming Manual.
TXRATE	These registers control the bit rate of the transmitter.
FSKDEV	These registers control the frequency deviation of the transmitter in FSK mode. The receiver does not explicitly need to know the frequency deviation, only the channel filter bandwidth has to be set wide enough for the complete modulation to pass.

Encoder

The encoder is located between the Framing Unit, the Demodulator and the Modulator. It can optionally transform the bit−stream in the following ways:

- It can invert the bit stream.
- It can perform differential encoding. This means that a zero is transmitted as no change in the level, and a one is transmitted as a change in the level. Differential encoding is useful for PSK, because PSK transmissions can be received either as transmitted or inverted, due to the uncertainty of the initial phase. Differential encoding / decoding removes this uncertainty.
- It can perform Manchester encoding. Manchester encoding ensures that the modulation has no DC content and enough transitions (changes from 0 to 1 and from 1 to 0) for the demodulator bit timing recovery to function correctly, but does so at a doubling of the data rate.
- It can perform Spectral Shaping. Spectral Shaping removes DC content of the bit stream, ensures

transitions for the demodulator bit timing recovery, and makes sure that the transmitted spectrum does not have discrete lines even if the transmitted data is cyclic. It does so without adding additional bits, i.e. without changing the data rate. Spectral Shaping uses a self−synchronizing feedback shift register.

The encoder is programmed using the register ENCODING, details and recommendations on usage are given in the AX5051 Programming Manual.

Framing and FIFO

Most radio systems today group data into packets. The framing unit is responsible for converting these packets into a bit−stream suitable for the modulator, and to extract packets from the continuous bit−stream arriving from the demodulator.

The Framing unit supports four different modes:

- HDLC
- Raw
- Raw with Preamble Match
- 802.15.4 Compliant

The micro−controller communicates with the framing unit through a 4 level × 10 bit FIFO. The FIFO decouples micro−controller timing from the radio (modulator and demodulator) timing. The bottom 8 bits of the FIFO contain transmit or receive data. The top 2 bit are used to convey meta information in HDLC and 802.15.4 modes. They are unused in Raw and Raw with Preamble Match modes. The meta information consists of packet begin / end information and the result of CRC checks.

The AX5051 contains one FIFO. Its direction is switched depending on whether transmit or receive mode is selected.

The FIFO can be operated in polled or interrupt driven modes. In polled mode, the micro−controller must periodically read the FIFO status register or the FIFO count register to determine whether the FIFO needs servicing.

In interrupt mode EMPTY, NOT EMPTY, FULL, NOT FULL and programmable level interrupts are provided. The AX5051 signals interrupts by asserting (driving high) its IRQ line. The interrupt line is level triggered, active high. Interrupts are acknowledged by removing the cause for the interrupt, i.e. by emptying or filling the FIFO.

Basic FIFO status (EMPTY, FULL, Overrun, Under−run, and the top two bits of the top FIFO word) are also provided during each SPI access on MISO while the micro−controller shifts out the register address on MOSI. See the SPI interface section for details. This feature significantly reduces the number of SPI accesses necessary during transmit and receive.

HDLC Mode

NOTE: HDLC mode follows High−Level Data Link Control (HDLC, ISO 13239) protocol.

HDLC Mode is the main framing mode of the AX5051. In this mode, the AX5051 performs automatic packet delimiting, and optional packet correctness check by inserting and checking a cyclic redundancy check (CRC) field.

The packet structure is given in the following table.

Table 14.

Flag	Address	Control	Information	FCS	(Optional Flag)
8 bit	8 bit	8 or 16 bit	Variable length, 0 or more bits in multiples of 8	16 / 32 bit	8 bit

HDLC packets are delimited with flag sequences of content 0x7E.

In AX5051 the meaning of address and control is user defined. The Frame Check Sequence (FCS) can be programmed to be CRC−CCITT, CRC−16 or CRC−32.

The receiver checks the CRC, the result can be retrieved from the FIFO, the CRC is appended to the received data.

For details on implementing a HDLC communication see the AX5051 Programming Manual.

Raw Mode

In Raw mode, the AX5051 does not perform any packet delimiting or byte synchronization. It simply serializes transmit bytes and de−serializes the received bit−stream and groups it into bytes.

This mode is ideal for implementing legacy protocols in software.

Raw Mode with Preamble Match

Raw mode with preamble match is similar to raw mode. In this mode, however, the receiver does not receive anything until it detects a user programmable bit pattern (called the preamble) in the receive bit−stream. When it detects the preamble, it aligns the de−serialization to it.

The preamble can be between 4 and 32 bits long.

802.15.4 (ZigBee) DSSS

802.15.4 uses binary phase shift keying (PSK) with 300 kbit/s (868 MHz band) or 600 kbit/s (915 MHz band) on the radio. The usable bit rate is only a 15^{th} of the radio bit rate, however. A spreading function in the transmitter expands the user bit rate by a factor of 15, to make the transmission more robust. The despreader function of the receiver undoes that.

In 802.15.4 mode, the AX5051 framing unit performs the spreading and despreading function according to the 802.15.4 specification. In receive mode, the framing unit will also automatically search for the 802.15.4 preamble, meaning that no interrupts will have to be serviced by the micro−controller until a packet start is detected.

The 802.15.4 is a universal DSSS mode, which can be used with any modulation or data rate as long as it does not violate the maximum data rate of the modulation being used. Therefore the maximum DSSS data rate is 16 kbps for FSK and 40 kbps for ASK and PSK.

RX AGC and RSSI

AX5051 features two receiver signal strength indicators (RSSI):

1. RSSI before the digital IF channel filter.
   The gain of the receiver is adjusted in order to keep the analog IF filter output level inside the working range of the ADC and demodulator. The register AGCCOUNTER contains the current value of the AGC and can be used as an RSSI. The step size of this RSSI is 0.625 dB. The value can be used as soon as the RF frequency generation sub−system has been programmed.
2. RSSI behind the digital IF channel filter.
   The demodulator also provides amplitude information in the TRK_AMPLITUDE register. By combining both the AGCCOUNTER and the TRK_AMPLITUDE registers, a high resolution (better than 0.1 dB) RSSI value can be computed at the expense of a few arithmetic operations on the micro−controller. Formulas for this computation can be found in the AX5051 Programming Manual.

Modulator

Depending on the transmitter settings the modulator generates various inputs for the PA (see Table 15):

Table 15.

Modulation	Bit = 0	Bit = 1	Main Lobe Bandwidth	Max. Bitrate
ASK	PA off	PA on	BW = BITRATE	600 kBit/s
FSK/MSK	$\Delta f = -f_{deviation}$	$\Delta f = +f_{deviation}$	BW = (1 + h) ·BITRATE	350 kBit/s
PSK	$\Delta\Phi = 0°$	$\Delta\Phi = 180°$	BW = BITRATE	600 kBit/s

Table 16.

h	Modulation index. It is the ratio of the deviation compared to the bit−rate. AX5051 can demodulate signals with h < 32.
$f_{deviation}$	0.5·h·BITRATE
ASK	Amplitude shift keying
FSK	Frequency shift keying
MSK	Minimum shift keying. MSK is a special case of FSK, where h = 0.5, and therefore $f_{deviation}$ = 0.25·BITRATE; the advantage of MSK over FSK is that it can be demodulated more robustly.
PSK	Phase shift keying
OQPSK	Offset quadrature shift keying. The AX5051 supports OQPSK. However, unless compatibility to an existing system is required, MSK should be preferred.

All modulation schemes are binary.

Automatic Frequency Control (AFC)

The AX5051 has a frequency tracking register TRKFREQ to synchronize the receiver frequency to a carrier signal. For AFC adjustment, the frequency offset can be computed with the following formula:

$$\Delta f = \frac{TRKFREQ}{2^{16}} BITRATE \times FSKMUL$$

FSKMUL is the FSK oversampling factor, it depends on the FSK bit−rate and deviation used. To determine it for a specific case, see the AX5051 Programming Manual. For modulations other than FSK, FSKMUL = 1.

PWRMODE Register

The PWRMODE register controls, which parts of the chip are operating.

Table 17. PWRMODE REGISTER

PWRMODE Register	Name	Description	Typical Idd
0000	POWERDOWN	All digital and analog functions, except the register file, are disabled. The core supply voltage is reduced to conserve leakage power. SPI registers are still accessible, but at a slower speed.	0.5 μA
0100	VREGON	All digital and analog functions, except the register file, are disabled. The core voltage, however is at its nominal value for operation, and all SPI registers are accessible at the maximum speed.	200 μA

Table 17. PWRMODE REGISTER

PWRMODE Register	Name	Description	Typical Idd
0101	STANDBY	The crystal oscillator is powered on; receiver and transmitter are off.	650 μA
1000	SYNTHRX	The synthesizer is running on the receive frequency. Transmitter and receiver are still off. This mode is used to let the synthesizer settle on the correct frequency for receive.	11 mA
1001	FULLRX	Synthesizer and receiver are running.	17 – 19 mA
1100	SYNTHTX	The synthesizer is running on the transmit frequency. Transmitter and receiver are still off. This mode is used to let the synthesizer settle on the correct frequency for transmit.	10 mA
1101	FULLTX	Synthesizer and transmitter are running. Do not switch into this mode before the synthesizer has completely settled on the transmit frequency (in SYNTHTX mode), otherwise spurious spectral transmissions will occur.	11 – 45 mA

Table 18. A TYPICAL PWRMODE SEQUENCE FOR A TRANSMIT SESSION

Step	PWRMODE	Remarks
1	POWERDOWN	
2	STANDBY	The settling time is dominated by the crystal used, typical value 3 ms.
3	SYNTHTX	The synthesizer settling time is 5 – 50 μs depending on settings, see section AC Characteristics
4	FULLTX	Data transmission
5	SYNTHTX	**This step must be programmed after FULLTX mode, or the device will not enter POWERDOWN or STANDBY mode.**
6	POWERDOWN	

Table 19. A TYPICAL PWRMODE SEQUENCE FOR A RECEIVE SESSION

Step	PWRMODE [3:0]	Remarks
1	POWERDOWN	
2	STANDBY	The settling time is dominated by the crystal used, typical value 3 ms.
3	SYNTHRX	The synthesizer settling time is 5 – 50 μs depending on settings, see section AC Characteristics
4	FULLRX	Data reception
5	POWERDOWN	

Serial Peripheral Interface

The AX5051 can be programmed via a four wire serial interface according SPI using the pins CLK, MOSI, MISO and SEL. Registers for setting up the AX5051 are programmed via the serial peripheral interface in all device modes.

When the interface signal SEL is pulled low, a 16−bit configuration data stream is expected on the input signal pin MOSI, which is interpreted as D0...D7, A0...A6, R_N/W. Data read from the interface appears on MISO.

Figure 3 shows a write/read access to the interface. The data stream is built of an address byte including read/write information and a data byte. Depending on the R_N/W bit and address bits A[6..0], data D[7..0] can be written via MOSI or read at the pin MISO.

R_N/W = 0 means read mode, R_N/W = 1 means write mode.

The read sequence starts with 7 bits of status information S[6..0] followed by 8 data bits.

The status bits contain the following information:

Table 20.

S6	S5	S4	S3	S2	S1	S0
PLL LOCK	FIFO OVER	FIFO UNDER	FIFO FULL	FIFO EMPTY	FIFOSTAT(1)	FIFOSTAT(0)

SPI Timing

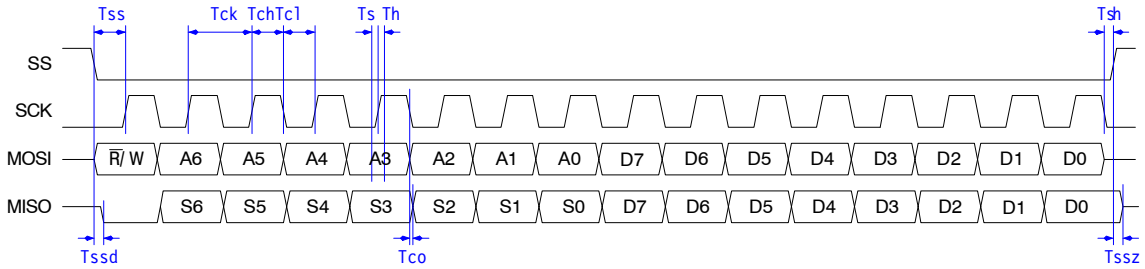


Figure 3. Serial Peripheral Interface Timing

REGISTER BANK DESCRIPTION

This section describes the bits of the register bank in detail. The registers are grouped by functional block to facilitate programming.

No checks are made whether the programmed combination of bits makes sense! Bit 0 is always the LSB.

NOTES: Whole registers or register bits marked as reserved should be kept at their default values. All addresses not documented here must not be accessed, neither in reading nor in writing.

Table 21. CONTROL REGISTER MAP

Addr	Name	Dir	Reset	Bit 7	6	5	4	3	2	1	0	Description
Revision & Interface Probing												
0	REVISION	R	00010100	SILICONREV(7:0)								Silicon Revision
1	SCRATCH	RW	11000101	SCRATCH(7:0)								Scratch Register
Operating Mode												
2	PWRMODE	RW	0–––0000	RST	–	–	–	PWRMODE(3:0)				Power Mode
Crystal Oscillator, Part 1												
3	XTALOSC	RW	––––0010	–	–	–	–	XTALOSCGM(3:0)				GM of Crystal Oscillator
FIFO, Part 1												
4	FIFOCTRL	RW	––––––11	FIFOSTAT(1:0)		FIFO OVER	FIFO UNDER	FIFO FULL	FIFO EMPTY	FIFOCMD(1:0)		FIFO Control
5	FIFODATA	RW	––––––––	FIFODATA(7:0)								FIFO Data
Interrupt Control												
6	IRQMASK	RW	––000000	–	–	IRQMASK(5:0)						IRQ Mask
7	IRQREQUEST	R	––––––––	–	–	IRQREQUEST(5:0)						IRQ Request
Interface & Pin Control												
8	IFMODE	RW	––––0011	–	–	–	–	IFMODE(3:0)				Interface Mode **Must be set to 0000**
0C	PINCFG1	RW	11111000	reserved		IRQZ	reserved	SYSCLK(3:0)				Pin Configuration 1
0D	PINCFG2	RW	00000000	TST_PINS		IRQE	reserved	reserved		IRQI	reserved	Pin Configuration 2 **TST_PINS(1:0) must be set to 11**
0E	PINCFG3	R	––––––––	–	–	–	SYSCLKR	reserved		IRQR	reserved	Pin Configuration 3
0F	IRQINVERSION	RW	––000000	–	–	IRQINVERSION(5:0)						IRQ Inversion
Modulation & Framing												
10	MODULATION	RW	–0000010	–	MODULATION(6:0)							Modulation
11	ENCODING	RW	––––0010	–	–	–	–	ENC MANCH	ENC SCRAM	ENC DIFF	ENC INV	Encoder/Decoder Settings
12	FRAMING	RW	–0000000	FRMRX	HSUPP	CRCMODE(1:0)		FRMMODE(2:0)			FABORT	Framing settings
14	CRCINIT3	RW	11111111	CRCINIT(31:24)								CRC Initialization Data or Preamble
15	CRCINIT2	RW	11111111	CRCINIT(23:16)								CRC Initialization Data or Preamble
16	CRCINIT1	RW	11111111	CRCINIT(15:8)								CRC Initialization Data or Preamble
17	CRCINIT0	RW	11111111	CRCINIT(7:0)								CRC Initialization Data or Preamble
Voltage Regulator												
1B	VREG	R	––––––––	–	–	–	–	SSDS	SSREG	SDS	SREG	Voltage Regulator Status

Table 21. CONTROL REGISTER MAP

Addr	Name	Dir	Reset	Bit 7	6	5	4	3	2	1	0	Description
Synthesizer												
20	FREQ3	RW	00111001	FREQ(31:24)								Synthesizer Frequency
21	FREQ2	RW	00110100	FREQ(23:16)								Synthesizer Frequency
22	FREQ1	RW	11001100	FREQ(15:8)								Synthesizer Frequency
23	FREQ0	RW	11001101	FREQ(7:0)								Synthesizer Frequency
25	FSKDEV2	RW	00000010	FSKDEV(23:16)								FSK Frequency Deviation
26	FSKDEV1	RW	01100110	FSKDEV(15:8)								FSK Frequency Deviation
27	FSKDEV0	RW	01100110	FSKDEV(7:0)								FSK Frequency Deviation
28	IFFREQHI	RW	00100000	IFFREQ(15:8)								2nd LO / IF Frequency
29	IFFREQLO	RW	00000000	IFFREQ(7:0)								2nd LO / IF Frequency
2C	PLLLOOP	RW	–0011101	–	reserved	BANDSEL	PLLCPI(2:0)			FLT(1:0)		Synthesizer Loop Filter Settings
2D	PLLRANGING	RW	00001000	STICKY LOCK	PLL LOCK	RNGERR	RNG START	VCOR(3:0)				Synthesizer VCO Auto−Ranging
Transmitter												
30	TXPWR	RW	––––1000	–	–	–	–	TXRNG(3:0)				Transmit Power
31	TXRATEHI	RW	00001001	TXRATE(23:16)								Transmitter Bitrate
32	TXRATEMID	RW	10011001	TXRATE(15:8)								Transmitter Bitrate
33	TXRATELO	RW	10011010	TXRATE(7:0)								Transmitter Bitrate
34	MODMISC	RW	––––––11	–	–	–	–	–	–	reserved	PTTCLK GATE	Misc RF Flags
FIFO, Part 2												
35	FIFOCOUNT	R	––––––––	–	–	–	–	–	FIFOCOUNT(2:0)			FIFO Fill state
36	FIFOTHRESH	RW	–––––000	–	–	–	–	–	FIFOTHRESH(2:0)			FIFO Threshold
37	FIFOCONTROL2	RW	0–––––00	CLEAR	–	–	–	–	–	STOPONERR(1:0)		Additional FIFO control
Receiver												
3A	AGCATTACK	RW	00010110	–	–	–	AGCATTACK(4:0)					AGC Attack
3B	AGCDECAY	RW	0–010011	reserved	–	reserved	AGCDECAY(4:0)					AGC Decay
3C	AGCCOUNTER	R	––––––––	AGCCOUNTER(7:0)								AGC Current Value
3D	CICSHIFT	R	––000100	–	–	reseved	CICSHIFT(4:0)					CIC Shift Factor
3F	CICDEC	RW	00000100	–	–	CICDEC(5:0)						CIC Decimation Factor
40	DATARATEHI	RW	00011010	DATARATE(15:8)								Datarate
41	DATARATELO	RW	10101011	DATARATE(7:0)								Datarate
42	TMGGAINHI	RW	00000000	TIMINGGAIN(15:8)								Timing Gain
43	TMGGAINLO	RW	11010101	TIMINGGAIN(7:0)								Timing Gain
44	PHASEGAIN	RW	00––0011	reserved		–	–	PHASEGAIN(3:0)				Phase Gain
45	FREQGAIN	RW	00001010	reserved				FREQGAIN(3:0)				Frequency Gain
46	FREQGAIN2	RW	––––1010	–	–	–	–	FREQGAIN2(3:0)				Frequency Gain 2

Table 21. CONTROL REGISTER MAP

Addr	Name	Dir	Reset	Bit 7	6	5	4	3	2	1	0	Description
47	AMPLGAIN	RW	––00110	–	–	–	reserved	AMPLGAIN(3:0)				Amplitude Gain
48	TRKAMPLHI	R	————	TRKAMPL(15:8)								Amplitude Tracking
49	TRKAMPLLO	R	————	TRKAMPL(7:0)								Amplitude Tracking
4A	TRKPHASEHI	R	————	–	–	–	–	TRKPHASE(11:8)				Phase Tracking
4B	TRKPHASELO	R	————	TRKPHASE(7:0)								Phase Tracking
4C	TRKFREQHI	R	————	TRKFREQ(15:8)								Frequency Tracking
4D	TRKFREQLO	R	————	TRKFREQ(7:0)								Frequency Tracking
Crystal Oscillator, Part 2												
4F	XTALCAP	RW	––000000	–	–	XTALCAP(5:0)						Crystal oscillator tuning capacitance
Misc												
72	PLLVCOI	RW	––000100	–	–	reserved		VCO_I[2:0]				Synthesizer VCO current **Must be set to 001**
7A	LOCURST	RW	00110000	LOCURST	reserved							LOCURST **Must be set to 1**
7C	rEF	RW	––100011	–	–	reserved		REF_I[2:0]				Reference adjust
7D	RXMISC	RW	––110110	–	–	reserved			RXIMIX(1:0)			Misc RF settings RXIMIX(1:0) must be set to 01

APPLICATION INFORMATION

Typical Application Diagram

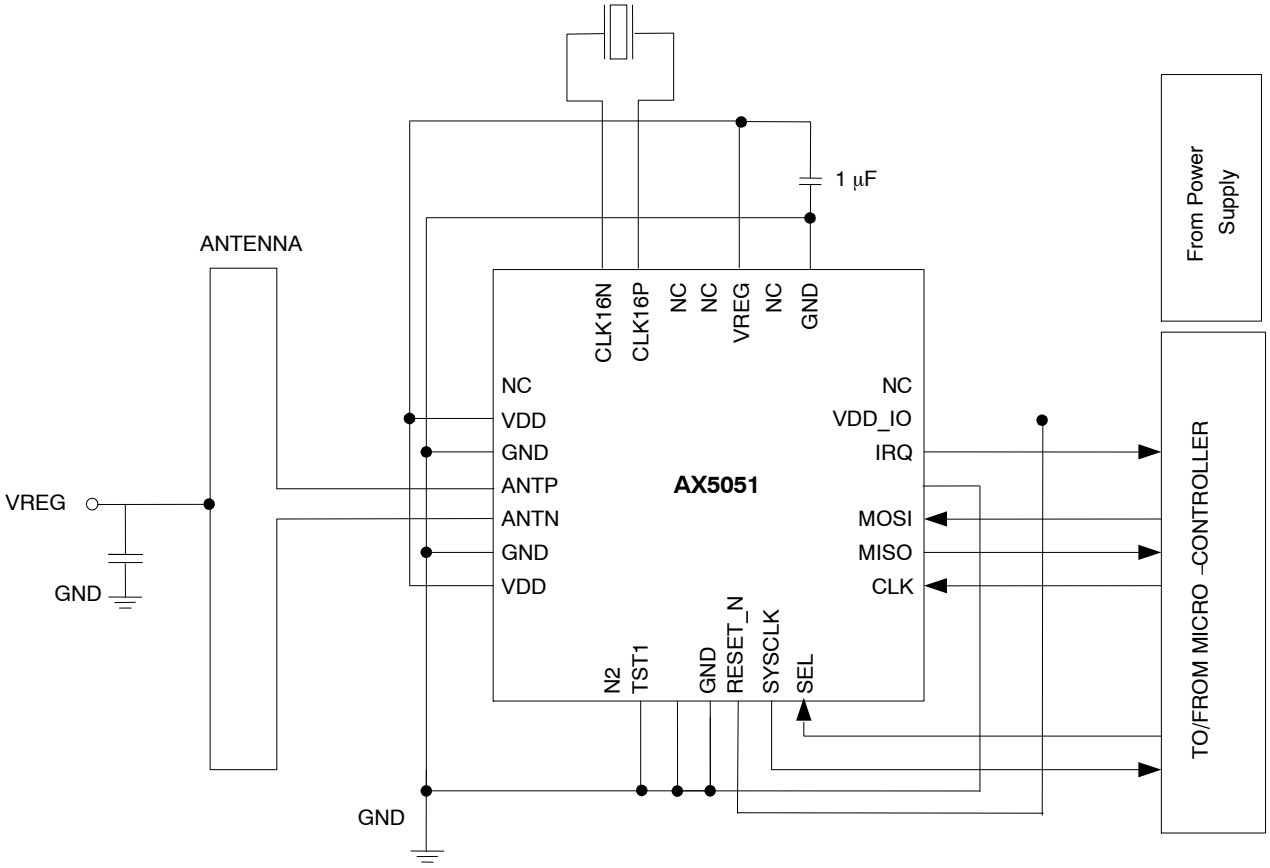


Figure 4. Typical Application Diagram

It is mandatory to add 1 μF (low ESR) between VREG and GND.

Decoupling capacitors are not all drawn. It is recommended to add 100 nF decoupling capacitor for every VDD and VDD_IO pin. In order to reduce noise on the antenna inputs it is recommended to add 27 pF on the VDD pins close to the antenna interface.

Antenna Interface Circuitry

The ANTP and ANTN pins provide RF input to the LNA when AX5051 is in receiving mode, and RF output from the PA when AX5051 is in transmitting mode. A small antenna can be connected with an optional translation network. The network must provide DC power to the PA and LNA. A biasing to VREG is necessary.

Beside biasing and impedance matching, the proposed networks also provide low pass filtering to limit spurious emission.

Single−ended Antenna Interface

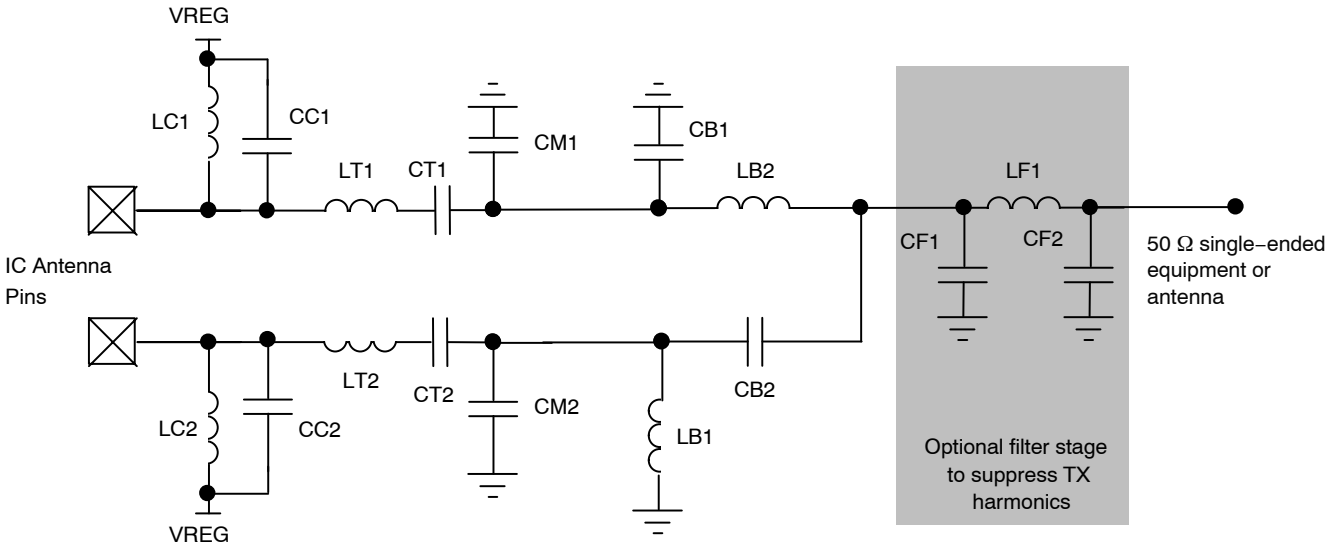


Figure 5. Structure of the Antenna Interface to 50 Ω Single−ended Equipment or Antenna

Table 22.

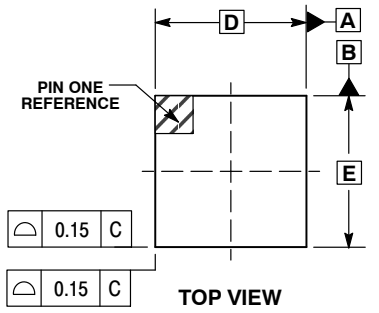
Frequency Band	LC1,2 [nH]	CC1,2 [pF]	LT1,2 [nH]	CT1,2 [pF]	CM1,2 [pF]	LB1,2 [nH]	CB1,2 [pF]	LF1 [nH]	CF1,2 [pF]
868 / 915 MHz	68	0.9	12	18	2.4	12	2.7	0 Ω	NC
433 MHz	120	2.2	39	7.5	6.0	27	5.2	0 Ω	NC

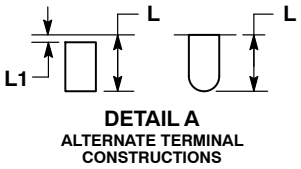
Voltage Regulator

The AX5051 has an integrated voltage regulator, which generates a stable supply voltage VREG from the voltage applied at VDD_IO. Use VREG to supply all the VDD supply pins.

QFN28 PACKAGE INFORMATION

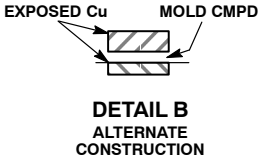
QFN28 5x5, 0.5P
CASE 485EF
ISSUE A

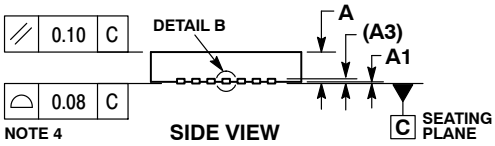


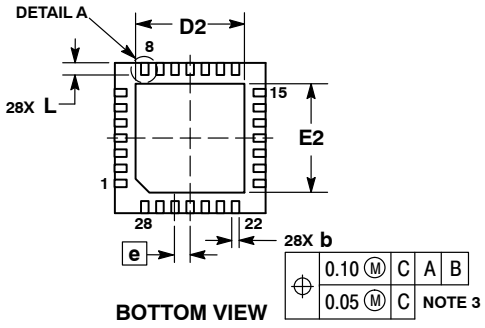


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

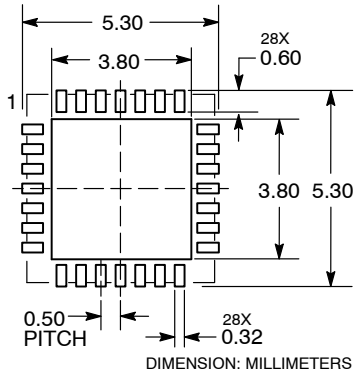
DIM	MILLIMETERS MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	3.45	3.75
E	5.00 BSC	
E2	3.45	3.75
e	0.50 BSC	
L	0.35	0.45
L1	---	0.15







RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

QFN28 Soldering Profile

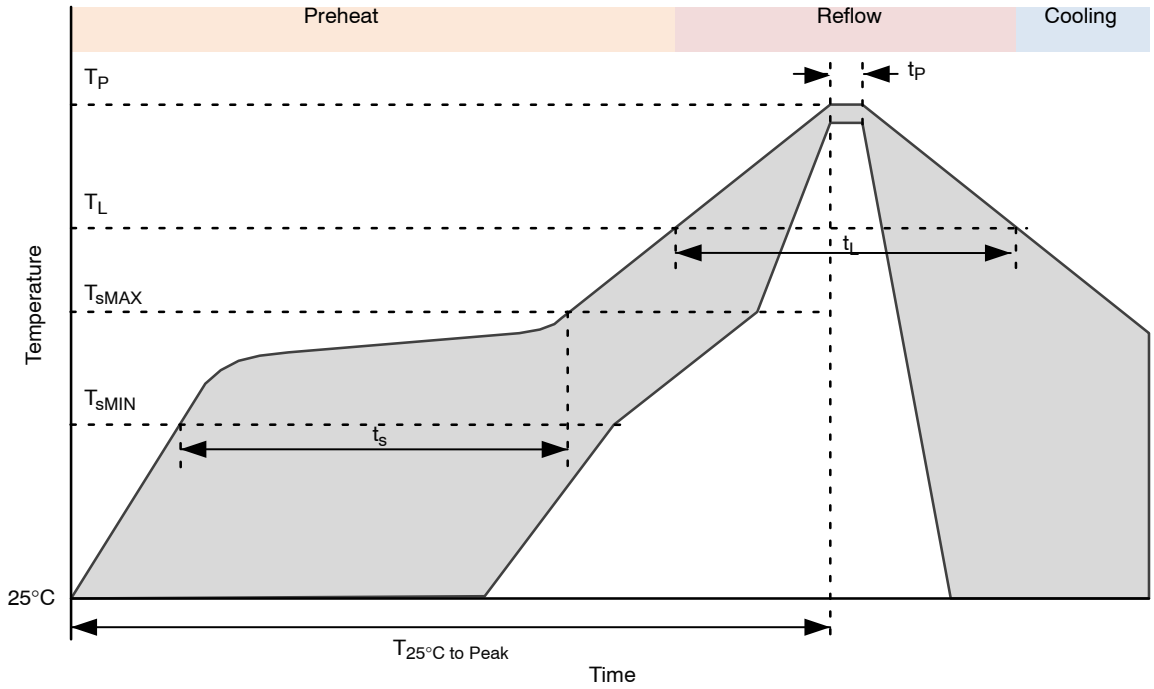


Figure 6. QFN28 Soldering Profile

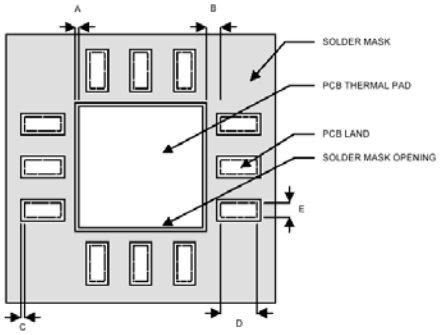
Table 23.

Profile Feature		Pb−Free Process
Average Ramp−Up Rate		3°C/s max.
Preheat Preheat		
Temperature Min	T_{sMIN}	150°C
Temperature Max	T_{sMAX}	200°C
Time (T_{sMIN} to T_{sMAX})	t_s	60 − 180 sec
Time 25°C to Peak Temperature	$T_{25°C\ to\ Peak}$	8 min max.
Reflow Phase		
Liquidus Temperature	T_L	217°C
Time over Liquidus Temperature	t_L	60 − 150 s
Peak Temperature	t_p	260°C
Time within 5°C of actual Peak Temperature	T_p	20 − 40 s
Cooling Phase		
Ramp−down rate		6°C/s max.

1. All temperatures refer to the top side of the package, measured on the package body surface.

QFN28 Recommended Pad Layout

1. PCB land and solder masking recommendations are shown in Figure 7.



A = Clearance from PCB thermal pad to solder mask opening, 0.0635 mm minimum
B = Clearance from edge of PCB thermal pad to PCB land, 0.2 mm minimum
C = Clearance from PCB land edge to solder mask opening to be as tight as possible to ensure that some solder mask remains between PCB pads.
D = PCB land length = QFN solder pad length + 0.1 mm
E = PCB land width = QFN solder pad width + 0.1 mm

Figure 7. PCB Land and Solder Mask Recommendations

2. Thermal vias should be used on the PCB thermal pad (middle ground pad) to improve thermal conductivity from the device to a copper ground plane area on the reverse side of the printed circuit board. The number of vias depends on the package thermal requirements, as determined by thermal simulation or actual testing.
3. Increasing the number of vias through the printed circuit board will improve the thermal conductivity to the reverse side ground plane and external heat sink. In general, adding more metal through the PC board under the IC will improve operational heat transfer, but will require careful attention to uniform heating of the board during assembly.

Assembly Process

Stencil Design & Solder Paste Application

1. Stainless steel stencils are recommended for solder paste application.
2. A stencil thickness of 0.125 – 0.150 mm (5 – 6 mils) is recommended for screening.
3. For the PCB thermal pad, solder paste should be printed on the PCB by designing a stencil with an array of smaller openings that sum to 50% of the QFN exposed pad area. Solder paste should be applied through an array of squares (or circles) as shown in Figure 8.
4. The aperture opening for the signal pads should be between 50−80% of the QFN pad area as shown in Figure 9.
5. Optionally, for better solder paste release, the aperture walls should be trapezoidal and the corners rounded.
6. The fine pitch of the IC leads requires accurate alignment of the stencil and the printed circuit board. The stencil and printed circuit assembly should be aligned to within + 1 mil prior to application of the solder paste.
7. No−clean flux is recommended since flux from underneath the thermal pad will be difficult to clean if water−soluble flux is used.

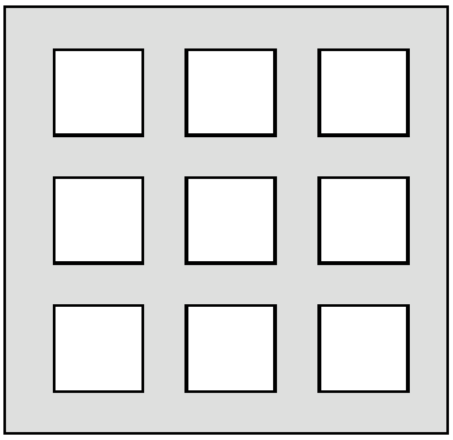


Figure 8. Solder Paste Application on Exposed Pad

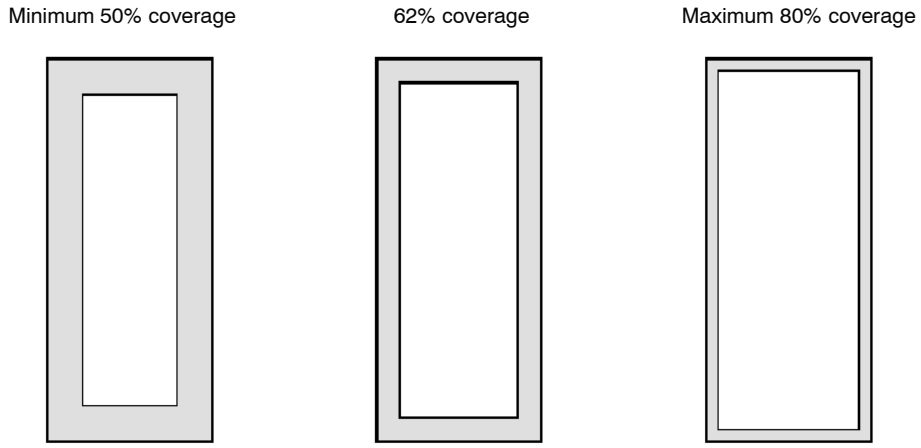


Figure 9. Solder Paste Application on Pins

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