PCE85176AUG

4 × 40 LCD segment driver for Chip-On-Glass

Rev. 1 — 12 January 2015 Product data sheet

1. General description

The PCE85176AUG is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The PCE85176AUG is compatible with most microcontrollers and communicates via the two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing and by display memory switching (static and duplex drive modes).

For a selection of NXP LCD segment drivers, see Table 31 on page 40.

2. Features and benefits

- Single chip LCD controller and driver
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static, ½, or ⅓
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives:
  - Up to 20 7-segment alphanumeric characters
  - Up to 10 14-segment alphanumeric characters
  - Any graphics of up to 160 elements
- 40 × 4-bit RAM for display data storage
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- Independent supplies possible for LCD and logic voltages
- Wide power supply range: from 1.8 V to 5.5 V
- Wide logic LCD supply range:
  - From 2.5 V for low-threshold LCDs
  - Up to 5.5 V for high-threshold twisted nematic LCDs
- Low power consumption
- 400 kHz I^2C-bus interface
- No external components required
- Compatible with Chip-On-Glass (COG) technology

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 19.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCE85176AUG	bare die	59 bumps	PCE85176AUG

3.1 Ordering options

Table 2. Ordering options

Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCE85176AUG/DA	PCE85176AUG/DAKP	935304709026	chip with gold bumps in tray	1

4. Marking

Table 3. Marking codes

Product type number	Marking code
PCE85176AUG/DA	PC85176A-1

5. Block diagram

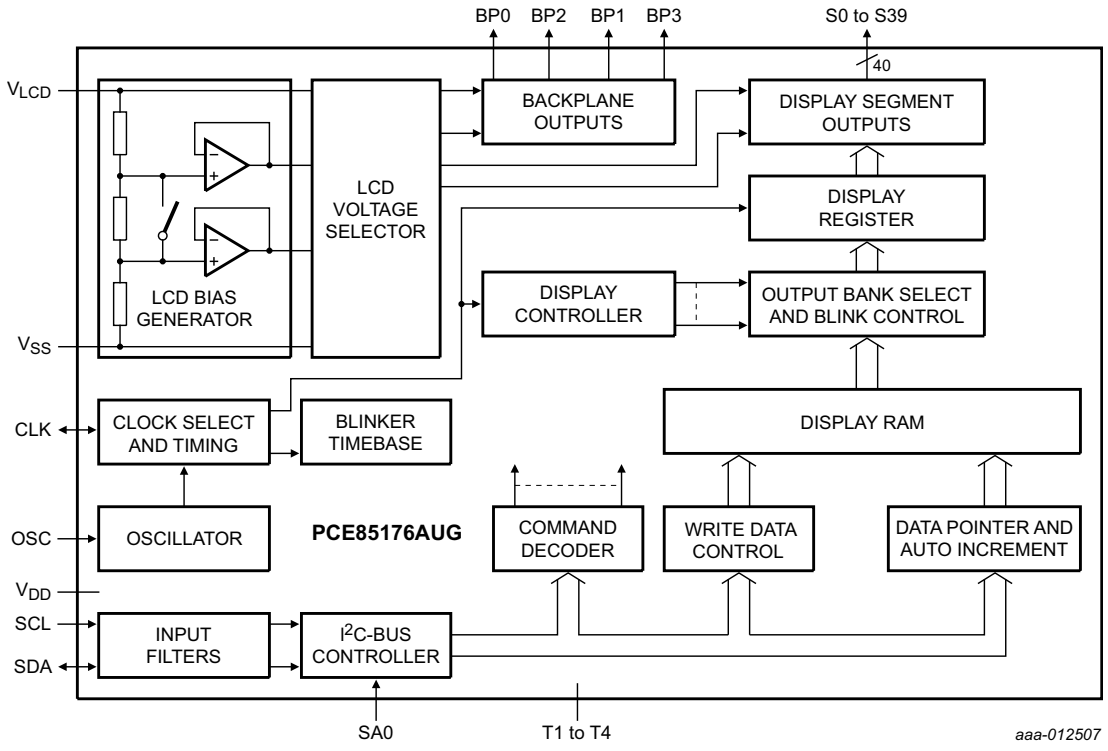
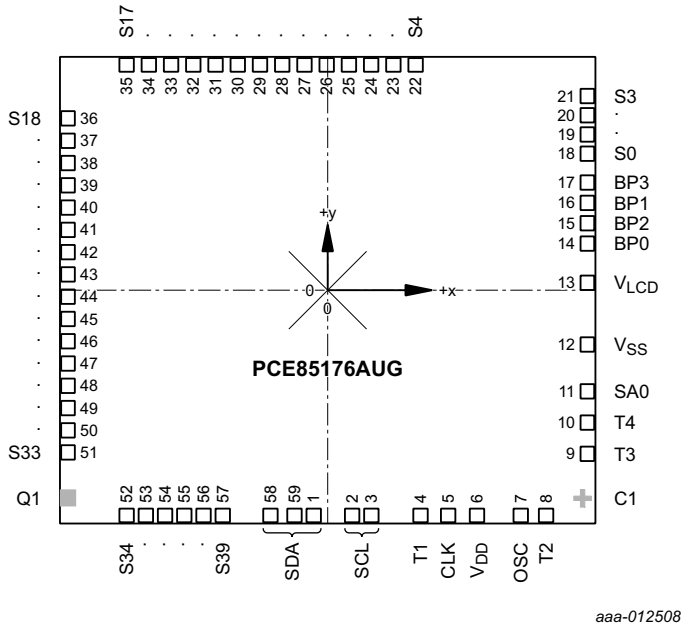


Fig 1. Block diagram of PCE85176AUG

6. Pinning information

6.1 Pinning



Viewed from active side. For mechanical details, see Figure 27.

Fig 2. Pinning diagram for PCE85176AUG (bare die)

6.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Type	Description
SDA	1, 58, 59	input/output	I²C-bus serial data line
SCL	2, 3	input	I²C-bus serial clock
T1	4	input/output	test pin; must be left open
CLK	5	input/output	clock line
V_{DD}	6	supply	supply voltage
OSC	7	input	internal oscillator enable
T2 to T4	8 to 10	input	test pins; must be tied to V_{SS}
SA0	11	input	I²C-bus address input
V_{SS}	12	supply	ground supply voltage
V_{LCD}	13	supply	LCD supply voltage
BP0, BP2, BP1, BP3	14 to 17	output	LCD backplane outputs
S0 to S39	18 to 57	output	LCD segment outputs

7. Functional description

The PCE85176AUG is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot matrix displays (see Figure 9). It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments.

7.1 Commands of PCE85176AUG

The commands available to the PCE85176AUG are defined in Table 5.

Table 5. Definition of PCE85176AUG commands

Bit position labeled as - is not used.

Command	Operation Code								Reference
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
mode-set	C	1	0	-	E	B	M[1:0]		Table 8
load-data-pointer	C	0	P[5:0]						Table 10
initialize-RAM	C	1	1	0	0	0	0	0	Table 12
bank-select	C	1	1	1	1	0	I	O	Table 14
blink-select	C	1	1	1	0	AB	BF[1:0]		Table 16

All available commands carry a continuation bit C in their most significant bit position as shown in Figure 22. When this bit is set logic 1, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is set logic 0, it indicates that the command byte is the last in the transfer. Further bytes are regarded as display data (see Table 6).

Table 6. C bit description

Bit	Symbol	Value	Description
7	C		**continue bit**
		0	last control byte in the transfer; next byte will be regarded as display data
		1	control bytes continue; next byte will be a command as well

7.1.1 Command: mode-set

The mode-set command allows configuring the multiplex mode, the bias levels and enabling or disabling the display.

Table 7. Mode-set command bit allocation

Bit position labeled as - is not used.

Bit	7	6	5	4	3	2	1	0
Symbol	C	1	0	-	E	B	M[1:0]	

Table 8. Mode-set command bit description

Bit position labeled as - is not used.

Bit	Symbol	Value	Description
7	C	0, 1	see Table 6
6, 5	-	10	fixed value
4	-	-	unused
3	E		**display status**[1]
		0	disabled (blank)[2]
		1	enabled
2	B		**LCD bias configuration**[3]
		0	$\frac{1}{3}$ bias
		1	$\frac{1}{2}$ bias
1 to 0	M[1:0]		**LCD drive mode selection**
		01	static; BP0
		10	1:2 multiplex; BP0, BP1
		11	1:3 multiplex; BP0, BP1, BP2
		00	1:4 multiplex; BP0, BP1, BP2, BP3

[1] The possibility to disable the display allows implementation of blinking under external control.

[2] The display is disabled by setting all backplane and segment outputs to V_{LCD}.

[3] Not applicable for static drive mode.

7.1.2 Command: load-data-pointer

The load-data-pointer command defines the display RAM address where the following display data is sent to.

Table 9. Load-data-pointer command bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	C	0	P[5:0]					

Table 10. Load-data-pointer command bit description

See Section 7.3.1.

Bit	Symbol	Value	Description
7	C	0, 1	see Table 6
6	0	0	fixed value
5 to 0	P[5:0]	000000 to 100111	6-bit binary value, 0 to 39; transferred to the data pointer to define one of 40 display RAM addresses

7.1.3 Command: Initialize-RAM

Table 11. Initialize-RAM command bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	C	1	1	0	0	0	0	0

Table 12. Initialize-RAM command bit description

See Section 7.3.1.

Bit	Symbol	Value	Description
7	C	0, 1	see Table 6
6 to 0	-	1100000	initializing the RAM access

7.1.4 Command: bank-select

The bank-select command controls where data is written to RAM and where it is displayed from.

Table 13. Bank-select command bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	C	1	1	1	1	0	I	O

Table 14. Bank-select command bit description

See Section 7.3.4.

Bit	Symbol	Value	Description	
			Static	1:2 multiplex[1]
7	C	0, 1	see Table 6	
6 to 2	-	11110	fixed value	
1	I		**input bank selection**; storage of arriving display data	
		0	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3
0	O		**output bank selection**; retrieval of LCD display data	
		0	RAM row 0	RAM rows 0 and 1
		1	RAM row 2	RAM rows 2 and 3

[1] The bank-select command has no effect in 1:3 and 1:4 multiplex drive modes.

7.1.5 Command: blink-select

The blink-select command allows configuring the blink mode and the blink frequency.

Table 15. Blink-select command bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	C	1	1	1	0	AB	BF[1:0]	

Table 16. Blink-select command bit description

See Section 7.2.4.

Bit	Symbol	Value	Description
7	C	0, 1	see Table 6
6 to 3	-	1110	fixed value
2	AB		**blink mode selection**
		0	normal blinking[1]
		1	alternate RAM bank blinking[2]
1 to 0	BF[1:0]		**blink frequency selection** (see Table 17)
		00	off
		01	1
		10	2
		11	3

[1] Normal blinking is assumed when the LCD multiplex drive modes 1:3 or 1:4 are selected.

[2] Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

7.2 Clock and frame frequency

7.2.1 Internal clock

The internal logic of the PCE85176AUG and its LCD drive signals are timed either by its internal oscillator or by an external clock. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}.

7.2.2 External clock

Pin CLK is enabled as an external clock input by connecting pin OSC to V_{DD}.

Remark: A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

7.2.3 Timing

The PCE85176AUG timing controls the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. The timing also generates the LCD frame signal whose frequency is derived from the clock frequency. The frame signal frequency is a fixed division of the clock frequency from either the internal or an external clock: $f_{fr} = \frac{f_{clk}}{24}$

7.2.4 Blinking

The display blinking capabilities of the PCE85176AUG are very versatile. The whole display can blink at frequencies selected by the blink-select command (see Table 16). The blink frequencies are derived from the clock frequency. The ratio between the clock and blink frequencies depends on the selected blink mode (see Table 17).

An additional feature is for an arbitrary selection of LCD elements to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. With the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command.

In the 1:3 and 1:4 multiplex modes, where no alternative RAM bank is available, groups of LCD elements can blink by selectively changing the display RAM data at fixed time intervals.

The entire display can blink at a frequency other than the nominal blink frequency. This can be effectively performed by resetting and setting the display enable bit E at the required rate using the mode-set command (see Table 8).

Table 17. Blink frequencies

Blink mode	Blink frequency[1]
off	-
1	$f_{blink} = \frac{f_{clk}}{768}$
2	$f_{blink} = \frac{f_{clk}}{1536}$
3	$f_{blink} = \frac{f_{clk}}{3072}$

[1] The blink frequency is proportional to the clock frequency (f_{clk}). For the range of the clock frequency, see Table 25.

7.3 Display RAM

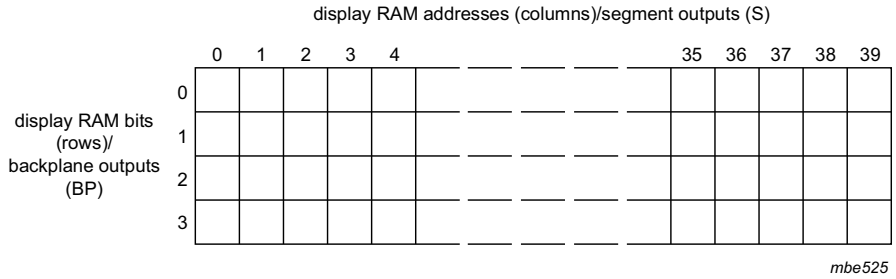
The display RAM is a static 40 × 4-bit RAM which stores LCD data.

There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

A logic 1 in the RAM bitmap indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state.

The display RAM bitmap, Figure 3, shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 39 which correspond with the segment outputs S0 to S39. In multiplexed LCD applications the segment data of the first, second, third and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3 respectively.

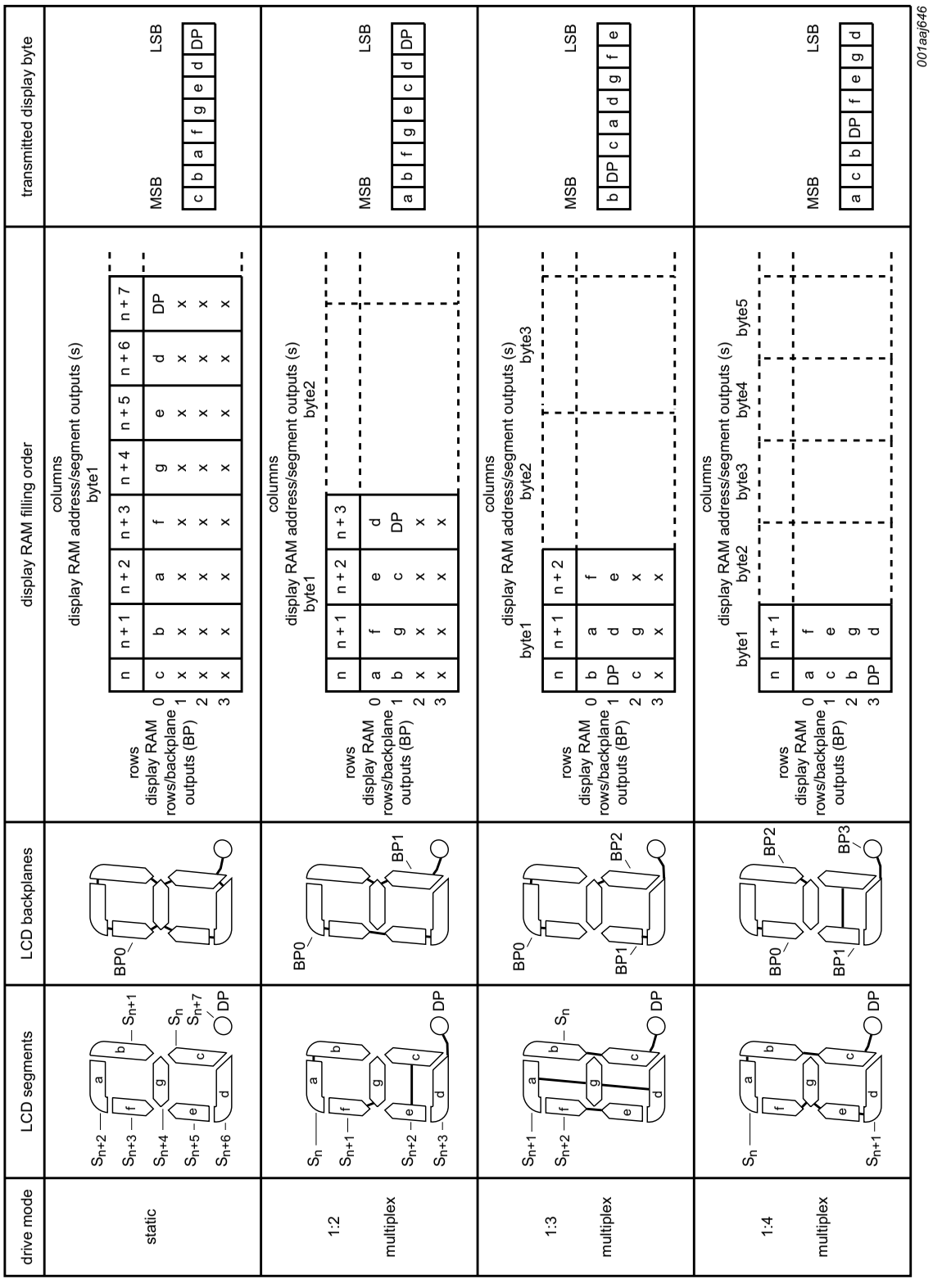


The display RAM bitmap shows the direct relationship between the display RAM column and the segment outputs; and between the bits in a RAM row and the backplane outputs.

Fig 3. Display RAM bitmap

When display data is transmitted to the PCE85176AUG, the received display bytes are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and depending on the current multiplex drive mode the bits are stored singularly, in pairs, triples, or quadruples. To illustrate the filling order, an example of a 7-segment display showing all drive modes is given in Figure 4; the RAM filling organization depicted applies equally to other LCD types.

- In static drive mode the eight transmitted data bits are placed into row 0 as one byte
- In 1:2 multiplex drive mode the eight transmitted data bits are placed in pairs into row 0 and 1 as two successive 4-bit RAM words
- In 1:3 multiplex drive mode the eight bits are placed in triples into row 0, 1, and 2 as three successive 3-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address, but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted (see Section 7.3.2)
- In 1:4 multiplex drive mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 as two successive 4-bit RAM words



x = data bit unchanged.

Fig 4. Relationship between LCD layout, drive mode, display RAM filling order, and display data transmitted over the I²C-bus

7.3.1 Writing to RAM

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM.

The sequence always commences with the initialize-RAM command (see Table 12). Following this command, the data pointer has to be set to the desired RAM address using the load-data-pointer command (see Table 10). After this an arriving data byte is stored at the display RAM address indicated by the data pointer. The RAM writing procedure is illustrated in Figure 5 and the filling order of the RAM is shown in Figure 4.

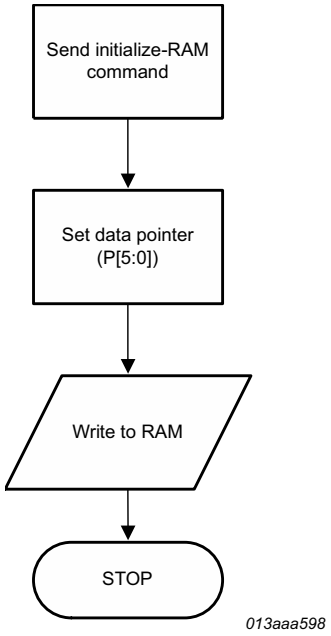


Fig 5. RAM writing procedure

After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight.
- In 1:2 multiplex drive mode by four.
- In 1:3 multiplex drive mode by three.
- In 1:4 multiplex drive mode by two.

If an I^2C-bus data access terminates early, then the state of the data pointer is unknown. So, the data pointer must be rewritten before further RAM accesses.

7.3.2 Writing to RAM in 1:3 multiplex drive mode

In 1:3 multiplex drive mode, the RAM is written as shown in Table 18 (see Figure 4 as well).

Table 18. Standard RAM filling in 1:3 multiplex drive mode

*Assumption: BP2/S2, BP2/S5, BP2/S8 etc. **are not connected** to any elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	1	2	3	4	5	6	7	8	9	:
0	a7	a4	a1	b7	b4	b1	c7	c4	c1	d7	:
1	a6	a3	a0	b6	b3	b0	c6	c3	c0	d6	:
2	a5	a2	-	b5	b2	-	c5	c2	-	d5	:
3	-	-	-	-	-	-	-	-	-	-	:

If the bit at position BP2/S2 would be written by a second byte transmitted, then the mapping of the segment bits would change as illustrated in Table 19.

Table 19. Entire RAM filling by rewriting in 1:3 multiplex drive mode

*Assumption: BP2/S2, BP2/S5, BP2/S8 etc. **are connected** to elements on the display.*

Display RAM bits (rows)/ backplane outputs (BPn)	Display RAM addresses (columns)/segment outputs (Sn)										
	0	1	2	3	4	5	6	7	8	9	:
0	a7	a4	a1/b7	b4	b1/c7	c4	c1/d7	d4	d1/e7	e4	:
1	a6	a3	a0/b6	b3	b0/c6	c3	c0/d6	d3	d0/e6	e3	:
2	a5	a2	b5	b2	c5	c2	d5	d2	e5	e2	:
3	-	-	-	-	-	-	-	-	-	-	:

In the case described in Table 19 the RAM has to be written entirely and BP2/S2, BP2/S5, BP2/S8 etc. have to be connected to elements on the display. This can be achieved by a combination of writing and rewriting the RAM like follows:

- In the first write to the RAM, bits a7 to a0 are written.
- The data-pointer (see Section 7.3.1 on page 11) has to be set to the address of bit a1
- In the second write, bits b7 to b0 are written, overwriting bits a1 and a0 with bits b7 and b6.
- The data-pointer has to be set to the address of bit b1
- In the third write, bits c7 to c0 are written, overwriting bits b1 and b0 with bits c7 and c6.

Depending on the method of writing to the RAM (standard or entire filling by rewriting), some elements remain unused or can be used. But it has to be considered in the module layout process as well as in the driver software design.

7.3.3 Writing over the RAM address boundary

In all multiplex drive modes, depending on the setting of the data pointer, it is possible to fill the RAM over the RAM address boundary. In this case, the additional bits will be discarded.

7.3.4 Bank selection

7.3.4.1 Output bank selector

The output bank selector (see Table 14) selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the selected LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, these are followed by the contents of row 1, 2, and then 3
- In 1:3 multiplex mode, rows 0, 1, and 2 are selected sequentially
- In 1:2 multiplex mode, rows 0 and 1 are selected
- In static mode, row 0 is selected

The PCE85176AUG includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 multiplex mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

7.3.4.2 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command (see Table 14). The input bank selector functions independently to the output bank selector.

7.3.4.3 RAM bank switching

The PCE85176AUG includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. A bank can be thought of as one RAM row or a collection of RAM rows (see Figure 6). The RAM bank switching gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is complete.

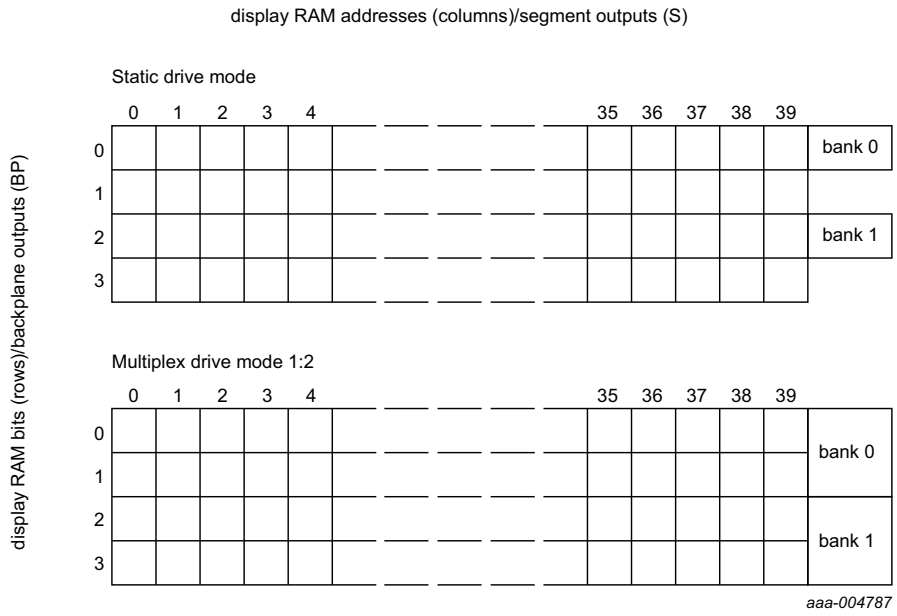


Fig 6. RAM banks in static and multiplex driving mode 1:2

There are two banks; bank 0 and bank 1. Figure 6 shows the location of these banks relative to the RAM map. Input and output banks can be set independently from one another with the Bank-select command (see Table 14). Figure 7 shows the concept.

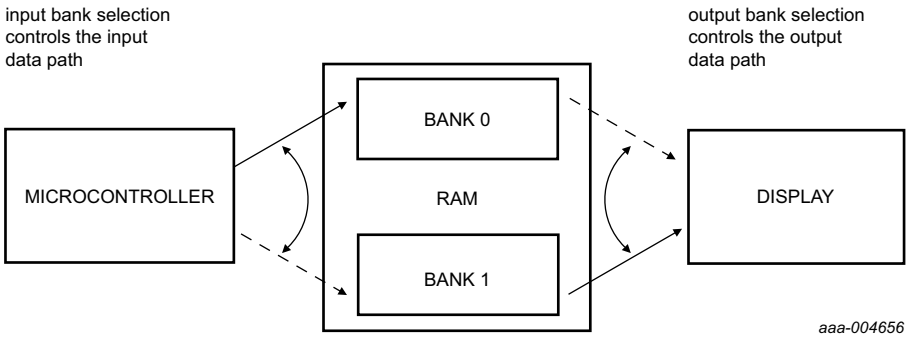


Fig 7. Bank selection

In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of row 0. In the 1:2 multiplex mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

In Figure 8 an example is shown for 1:2 multiplex drive mode where the displayed data is read from the first two rows of the memory (bank 0), while the transmitted data is stored in the second two rows of the memory (bank 1).

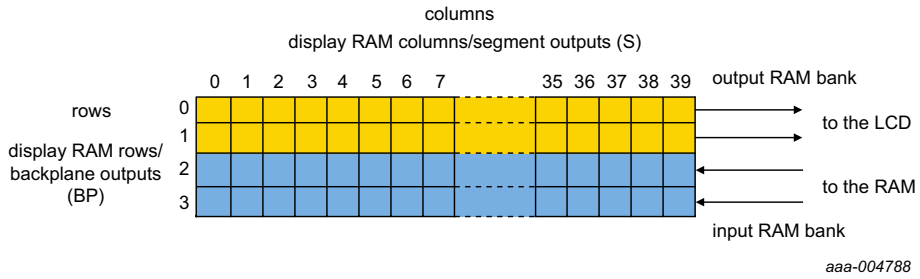


Fig 8. Example of the Bank-select command with multiplex drive mode 1:2

7.4 Initialization

At power-on the status of the I²C-bus and the registers of the PCE85176AUG is undefined. Therefore the PCE85176AUG should be initialized as quickly as possible after power-on to ensure a proper bus communication and to avoid display artifacts. The following instructions should be accomplished for initialization:

- I²C-bus (see Section 8) initialization
  - generating a START condition
  - sending 0h and ignoring the acknowledge
  - generating a STOP condition
- Mode-set command (see Table 8), setting
  - bit E = 0
  - bit B to the required LCD bias configuration
  - bits M[1:0] to the required LCD drive mode
- Load-data-pointer command (see Table 10), setting
  - bits P[5:0] to 0h (or any other required address)
- Initialize-RAM command (see Table 12)
- Bank-select command (see Table 14), setting
  - bit I to 0
  - bit O to 0
- Blink-select command (see Table 16), setting
  - bit AB to 0 or 1
  - bits BF[1:0] to 00 (or to a desired blinking mode)
- writing meaningful information (for example, a logo) into the display RAM

After the initialization, the display can be switched on by setting bit E = 1 with the mode-set command.

7.5 Possible display configurations

The possible display configurations of the PCE85176AUG is depending on the number of active backplane outputs required. A selection of display configurations is shown in Table 20. All of these configurations can be implemented in the typical system shown in Figure 10.

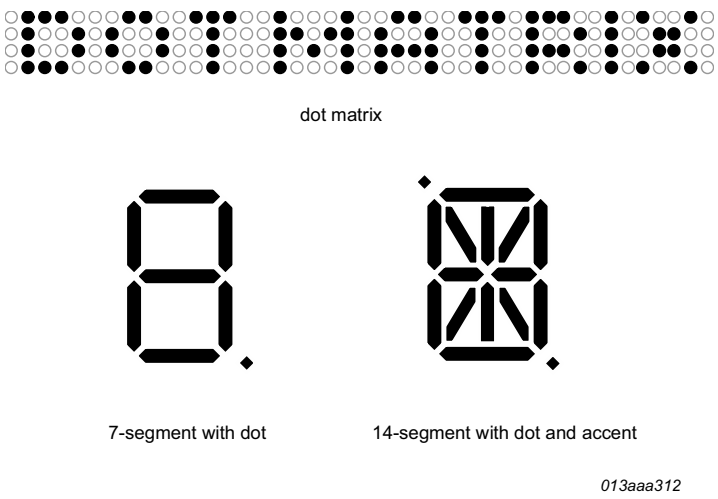


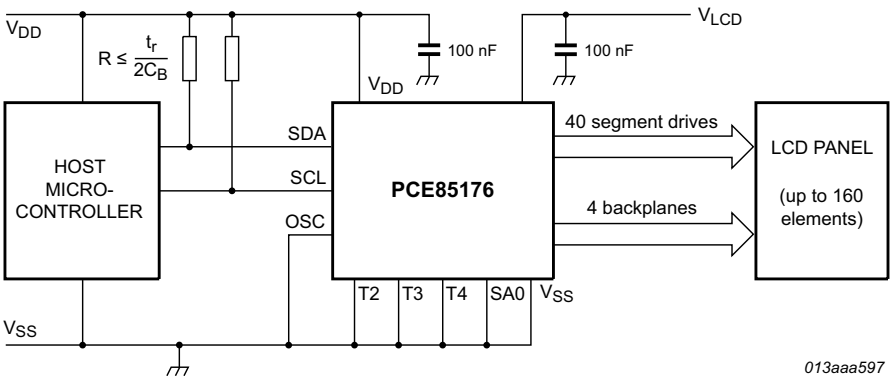
Fig 9. Example of displays suitable for PCE85176AUG

Table 20. Selection of possible display configurations

Number of				
Backplanes	**Icons**	**Digits/Characters**		**Dot matrix/ Elements**
		7-segment[1]	**14-segment[2]**	
4	160	20	10	160 (4 × 40)
3	120	15	7	120 (3 × 40)
2	80	10	5	80 (2 × 40)
1	40	5	2	40 (1 × 40)

[1] 7 segment display has 8 elements including the decimal point.

[2] 14 segment display has 16 elements including decimal point and accent dot.



The resistance of the power lines must be kept to a minimum.

Fig 10. Typical system configuration

The host microcontroller maintains the 2-line I²C-bus communication channel with the PCE85176AUG. The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the power supplies (V_{DD}, V_{SS}, and V_{LCD}) and the LCD panel chosen for the application.

7.5.1 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of three impedances connected between pins V_{LCD} and V_{SS}. The center impedance is bypassed by switch if the ½ bias voltage level for the 1:2 multiplex drive mode configuration is selected.

7.5.2 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

7.5.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D) are given in Table 21.

Table 21. Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\frac{V_{off(RMS)}}{V_{LCD}}$	$\frac{V_{on(RMS)}}{V_{LCD}}$	$D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	Levels				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	½	0.354	0.791	2.236
1:2 multiplex	2	4	⅓	0.333	0.745	2.236
1:3 multiplex	3	4	⅓	0.333	0.638	1.915
1:4 multiplex	4	4	⅓	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode, a suitable choice is $V_{LCD} > 3V_{th(off)}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 1:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1+a)^2}} \quad (1)$$

where the values for n are

n = 1 for static drive mode

n = 2 for 1:2 multiplex drive mode

n = 3 for 1:3 multiplex drive mode

n = 4 for 1:4 multiplex drive mode

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (2)$$

Discrimination is a term which is defined as the ratio of the on and off RMS voltages ($V_{on(RMS)}$ to $V_{off(RMS)}$) across a segment. It can be thought of as a measurement of contrast. Discrimination is determined from Equation 3:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a^2 + 2a + n}{a^2 - 2a + n}} \quad (3)$$

Using Equation 3, the discrimination for an LCD drive mode of 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(RMS)}$

These compare with $V_{LCD} = 3V_{off(RMS)}$ when ⅓ bias is used.

V_{LCD} is sometimes referred as the LCD operating voltage.

7.5.3.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel is switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 11. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (4)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (5)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 1 to Equation 3) and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

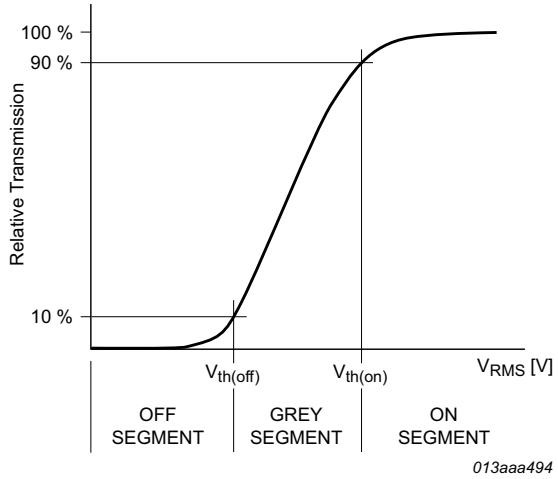
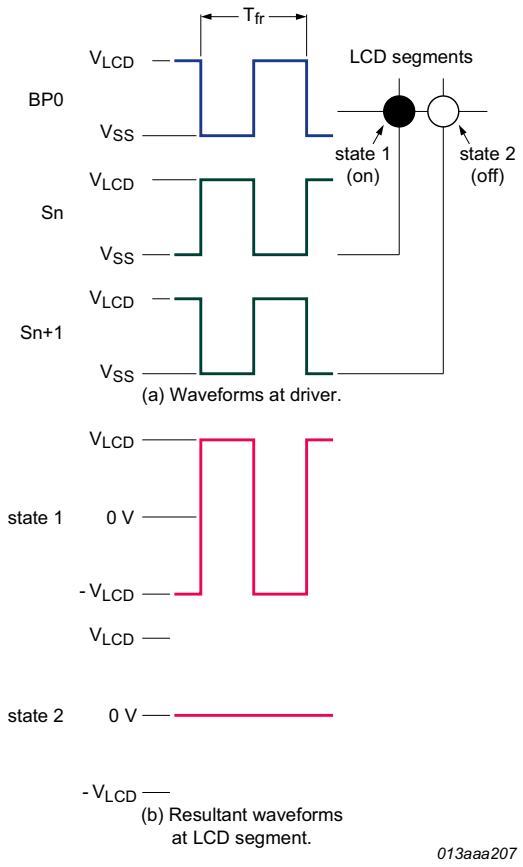


Fig 11. Electro-optical characteristic: relative transmission curve of the liquid

7.5.4 LCD drive mode waveforms

7.5.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. The backplane (BPn) and segment (Sn) drive waveforms for this mode are shown in Figure 12.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = V_{LCD}$.

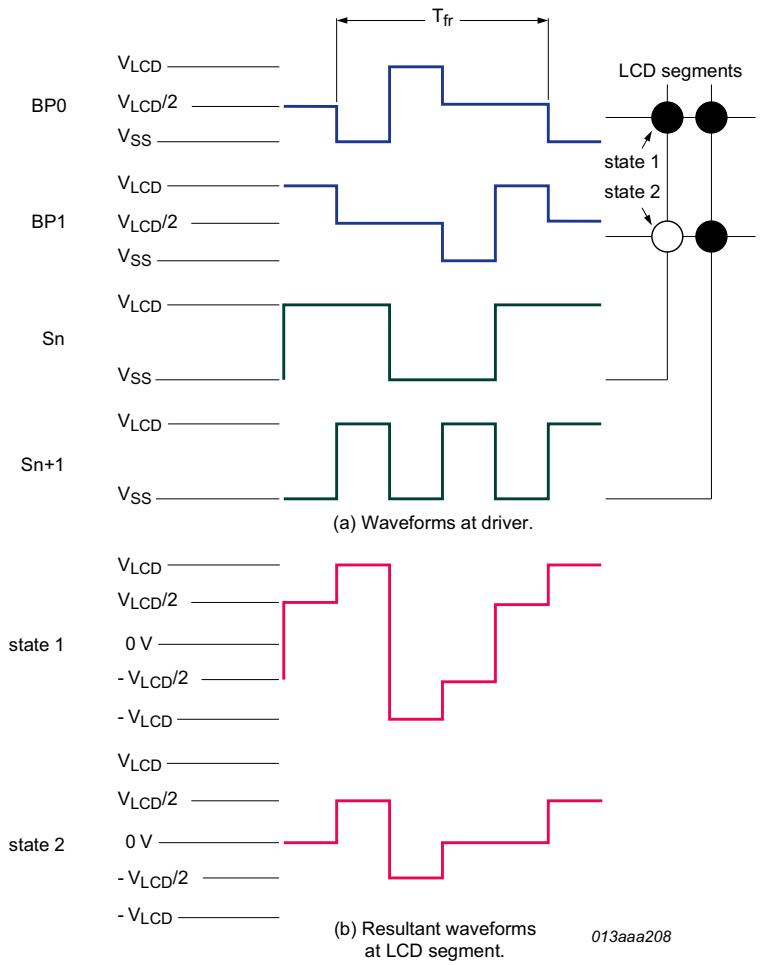
$V_{state2}(t) = V_{(Sn + 1)}(t) - V_{BP0}(t)$.

$V_{off(RMS)} = 0$ V.

Fig 12. Static drive mode waveforms

7.5.4.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCE85176AUG allows the use of ½ bias or ⅓ bias in this mode as shown in Figure 13 and Figure 14.



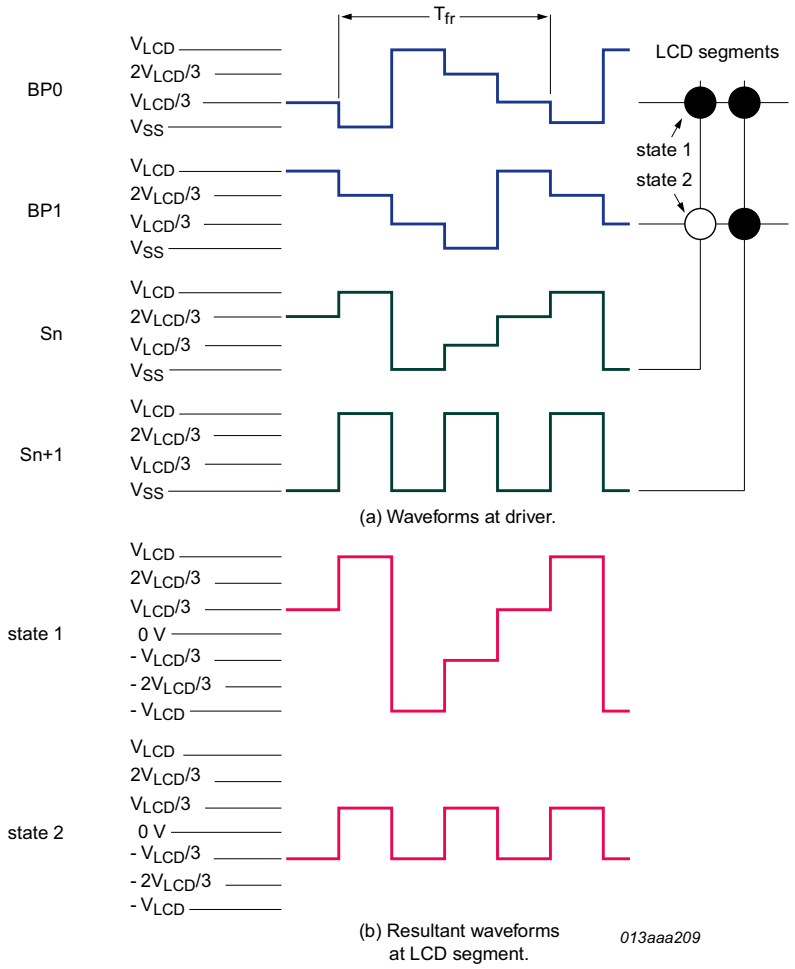
$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.791V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.354V_{LCD}$.

Fig 13. Waveforms for the 1:2 multiplex drive mode with ½ bias



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$.

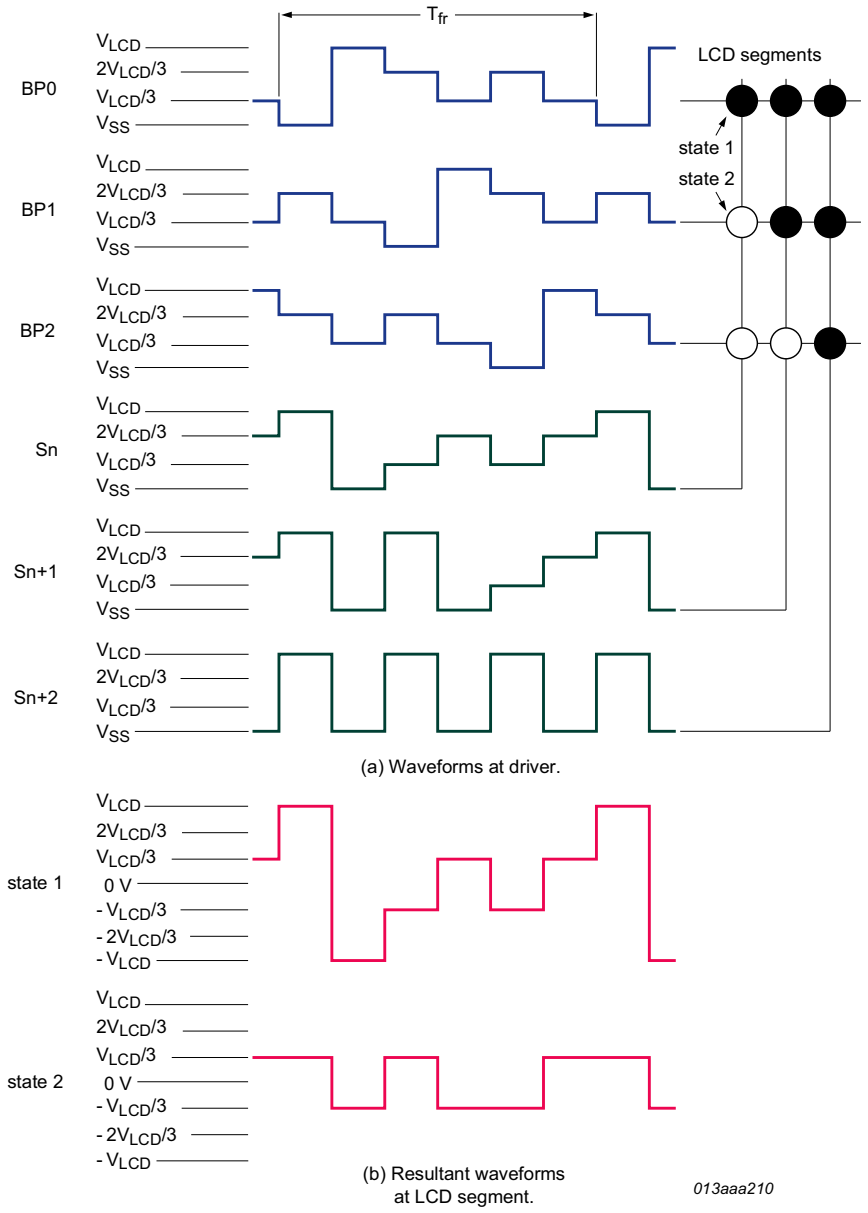
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 14. Waveforms for the 1:2 multiplex drive mode with ⅓ bias

7.5.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in Figure 15.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

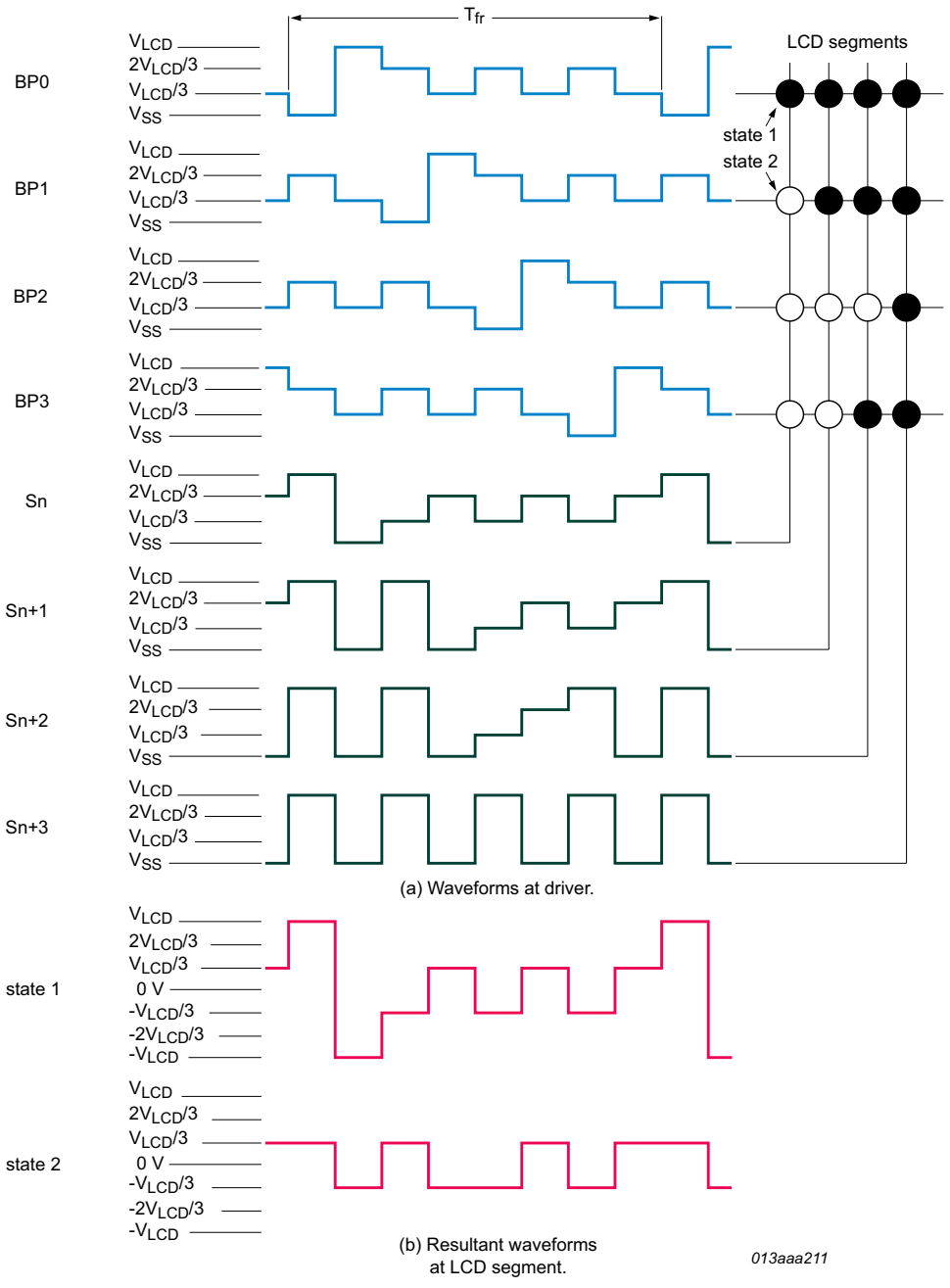
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 15. Waveforms for the 1:3 multiplex drive mode with ⅓ bias

7.5.4.4 1:4 Multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies as shown in Figure 16.



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 16. Waveforms for the 1:4 multiplex drive mode with ⅓ bias

7.6 Backplane and segment outputs

7.6.1 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which must be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required, the unused outputs can be left open-circuit.

- In 1:3 multiplex drive mode, BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode, BP0 and BP2, respectively, BP1 and BP3 all carry the same signals and may also be paired to increase the drive capabilities.
- In static drive mode, the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

7.6.2 Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display register. When less than 40 segment outputs are required, the unused segment outputs should be left open-circuit.

8. Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as a control signal (see Figure 17).

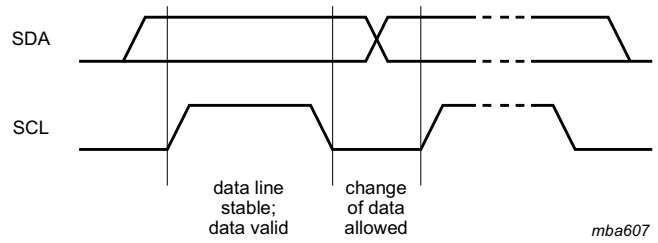


Fig 17. Bit transfer

8.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition - S.

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition - P.

The START and STOP conditions are illustrated in Figure 18.

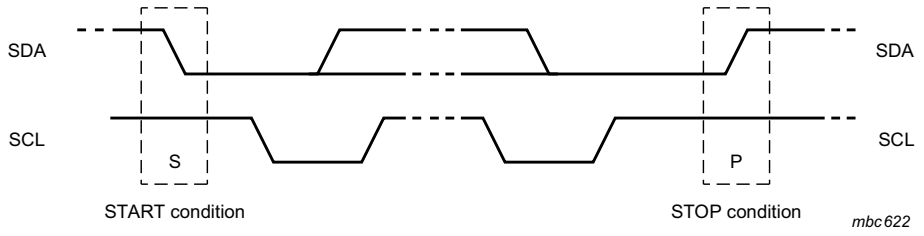


Fig 18. Definition of START and STOP conditions

8.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves. The system configuration is shown in Figure 19.

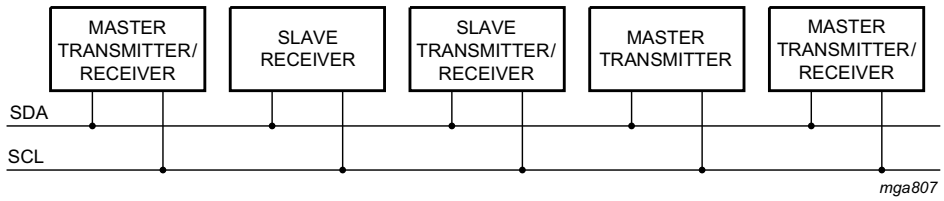


Fig 19. System configuration

8.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^{2}C-bus is illustrated in Figure 20.

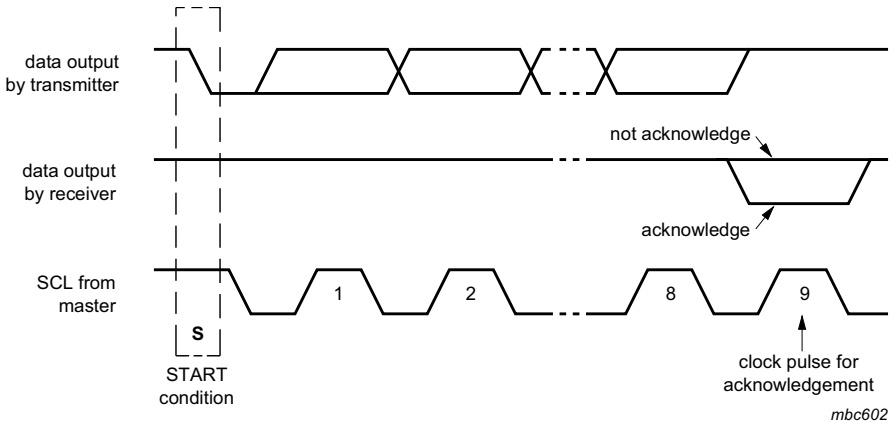


Fig 20. Acknowledgement of the I^{2}C-bus

8.5 I^{2}C-bus controller

The PCE85176AUG acts as an I^{2}C-bus slave receiver. It does not initiate I^{2}C-bus transfers or transmit data to an I^{2}C-bus master receiver. The only data outputs from the PCE85176AUG are the acknowledge signals.

8.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

8.7 I²C-bus protocol

Two I²C-bus slave addresses (0111 000 and 0111 001) are used to address the PCE85176AUG. The entire I²C-bus slave address byte is shown in Table 22.

Table 22. I²C slave address byte

	Slave address							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	MSB							**LSB**
	0	1	1	1	0	0	SA0	R/$\overline{W}$

The PCE85176AUG is a write-only device and will not respond to a read access, therefore bit 0 should always be logic 0. Bit 1 of the slave address byte that a PCE85176AUG responds to, is defined by the level tied to its SA0 input (V_{SS} for logic 0 and V_{DD} for logic 1).

The I²C-bus protocol is shown in Figure 21. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of two possible PCE85176AUG slave addresses available.

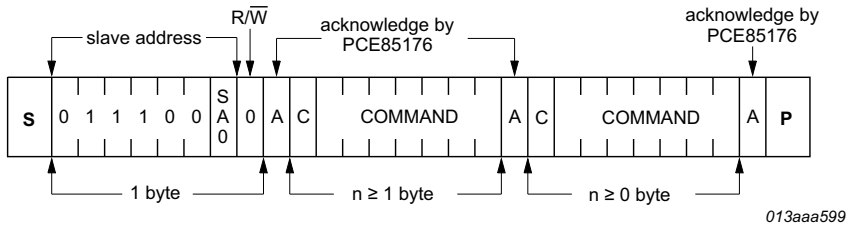


Fig 21. I²C-bus protocol

The last command byte sent is identified by resetting its most significant bit, continuation bit C (see Figure 22).

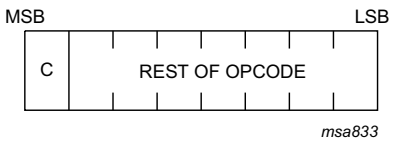
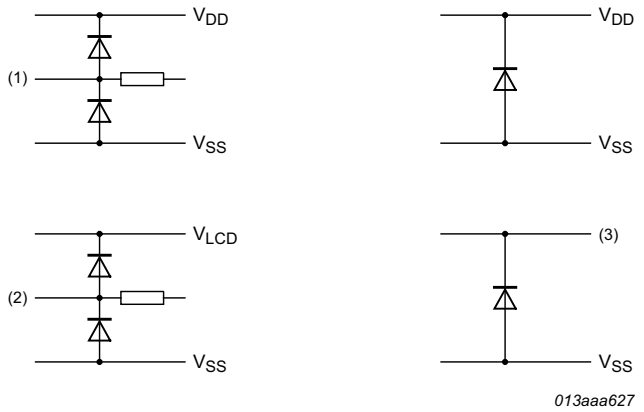


Fig 22. Format of command byte

9. Internal circuitry



(1) SA0, CLK, OSC, T1 to T4.

(2) BP0 to BP3, S0 to S39.

(3) V_{LCD}, SCL, SDA.

Fig 23. Device protection diagram

10. Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

CAUTION

Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.

11. Limiting values

Table 23. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6.5	V
V_{LCD}	LCD supply voltage		–0.5	+6.5	V
V_I	input voltage	on each of the pins CLK, SDA, SCL, T1 to T4, SA0, OSC	–0.5	+6.5	V
V_O	output voltage	on each of the pins S0 to S39, BP0 to BP3	–0.5	+6.5	V
I_I	input current		–10	+10	mA
I_O	output current		–10	+10	mA
I_{DD}	supply current		–50	+50	mA
$I_{DD(LCD)}$	LCD supply current		–50	+50	mA
I_{SS}	ground supply current		–50	+50	mA
P_{tot}	total power dissipation		-	400	mW
P_o	output power		-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM [1]	-	±3500	V
I_{lu}	latch-up current	[2]	-	100	mA
T_{stg}	storage temperature	[3]	–55	+150	°C
T_{amb}	ambient temperature	operating device	–40	+85	°C

[1] Pass level; Human Body Model (HBM), according to Ref. 9 “JESD22-A114”

[2] Pass level; latch-up testing according to Ref. 10 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[3] According to the store and transport requirements (see Ref. 14 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

12. Static characteristics

Table 24. Static characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 5.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage		1.8	-	5.5	V
V_{LCD}	LCD supply voltage	[1]	2.5	-	5.5	V
I_{DD}	supply current	$f_{clk(ext)}$ = 1536 Hz [2]	-	3.5	7	µA
		V_{DD} = 3.0 V; T_{amb} = 25 °C	-	2.7	-	µA
$I_{DD(LCD)}$	LCD supply current	$f_{clk(ext)}$ = 1536 Hz [2]	-	23	32	µA
		V_{LCD} = 3.0 V; T_{amb} = 25 °C	-	13	-	µA
Logic[3]						
V_{IL}	LOW-level input voltage	on pins CLK, T2 to T4, OSC, SA0, SCL, SDA	V_{SS}	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	on pins CLK, OSC, T2 to T4, SA0, SCL, SDA [4][5]	$0.7V_{DD}$	-	V_{DD}	V
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD} = 5 V				
		on pin CLK	1	-	-	mA
		on pin SDA	3	-	-	mA
$I_{OH(CLK)}$	HIGH-level output current on pin CLK	output source current; V_{OH} = 4.6 V; V_{DD} = 5 V	1	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}; on pins CLK, SCL, SDA, T2 to T4 and SA0	−1	-	+1	µA
$I_{L(OSC)}$	leakage current on pin OSC	$V_I = V_{DD}$	−1	-	+1	µA
C_I	input capacitance	[6]	-	-	7	pF
LCD outputs						
ΔV_O	output voltage variation	on pins BP0 to BP3 and S0 to S39	−100	-	+100	mV
R_O	output resistance	V_{LCD} = 5 V [7]				
		on pins BP0 to BP3	-	1.5	-	kΩ
		on pins S0 to S39	-	6.0	-	kΩ

[1] $V_{LCD} > 3$ V for ⅓ bias.

[2] LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; external clock with 50 % duty factor; I^2C-bus inactive.

[3] The I^2C-bus interface of PCE85176AUG is 5 V tolerant.

[4] When tested, I^2C pins SCL and SDA have no diode to V_{DD} and may be driven to the V_I limiting values given in Table 23 (see Figure 23 as well).

[5] Propagation delay of driver between clock (CLK) and LCD driving signals.

[6] Periodically sampled, not 100 % tested.

[7] Outputs measured one at a time.

13. Dynamic characteristics

Table 25. Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 2.5 V to 5.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock						
$f_{clk(int)}$	internal clock frequency	[1]	1440	1850	2640	Hz
$f_{clk(ext)}$	external clock frequency		960	-	2640	Hz
f_{fr}	frame frequency	internal clock	60	77	110	Hz
		external clock	40	-	110	Hz
$t_{clk(H)}$	HIGH-level clock time		60	-	-	µs
$t_{clk(L)}$	LOW-level clock time		60	-	-	µs
$t_{PD(drv)}$	driver propagation delay	V_{LCD} = 5 V [2]	-	-	30	µs
I^2C-bus[3]						
Pin SCL						
f_{SCL}	SCL clock frequency		-	-	400	kHz
t_{LOW}	LOW period of the SCL clock		1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock		0.6	-	-	µs
Pin SDA						
$t_{SU;DAT}$	data set-up time		100	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
Pins SCL and SDA						
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	-	-	µs
t_r	rise time of both SDA and SCL signals	f_{SCL} = 400 kHz	-	-	0.3	µs
		f_{SCL} < 125 kHz	-	-	1.0	µs
t_f	fall time of both SDA and SCL signals		-	-	0.3	µs
C_b	capacitive load for each bus line		-	-	400	pF
$t_{w(spike)}$	spike pulse width	on the I^2C-bus	-	-	50	ns

[1] Typical output duty factor: 50 % measured at the CLK output pin.

[2] Not tested in production.

[3] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

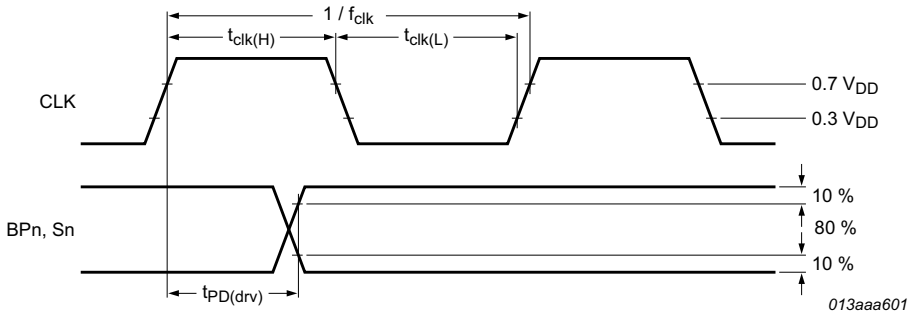


Fig 24. Driver timing waveforms

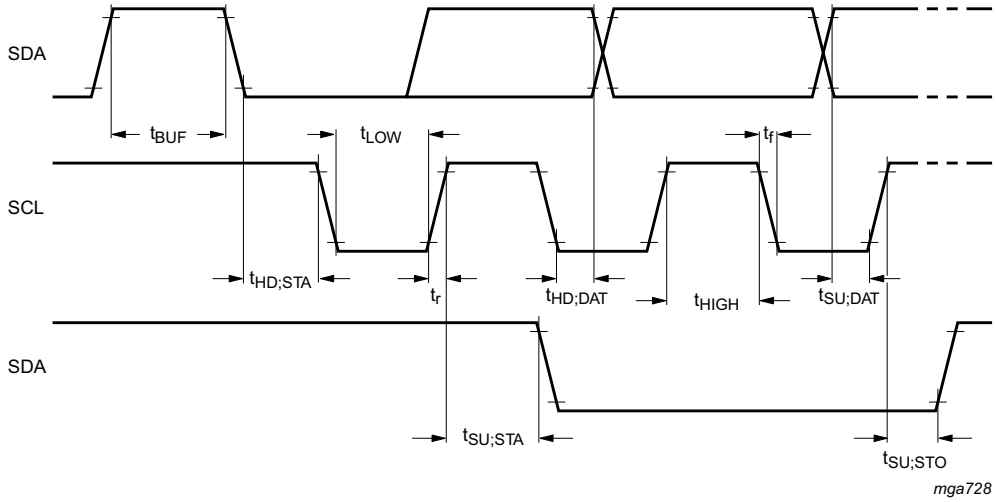
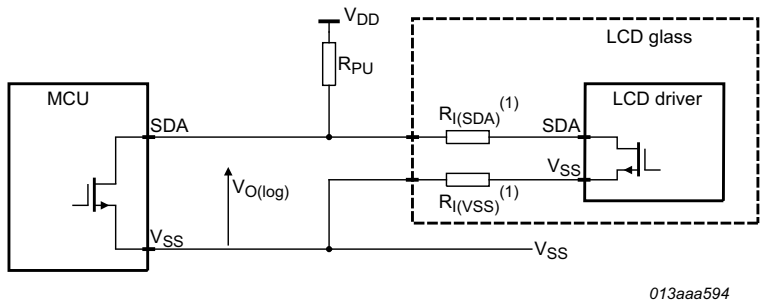


Fig 25. I²C-bus timing waveforms

14. Application information

14.1 Track resistance on the I²C-bus lines

The SDA line of an I²C device is an open-drain output which therefore needs an external pull-up resistor (R_{PU}). In Chip-On Glass (COG) applications, the track resistance (R_{ITO}) from the SDA pin to the SDA system line can be significant. For this reason, it is possible that the two resistances are forming a voltage divider. Such a divider could prevent that the acknowledge cycle generated by the PCE85176AUG can be interpreted as logic 0 by the master. To guarantee a valid LOW level, it is necessary that the R_{ITO} from the SDA pin to the SDA system line is minimized.



(1) Includes track resistance R_{ITO}.

Fig 26. Track resistances on the SDA and V_{SS} line

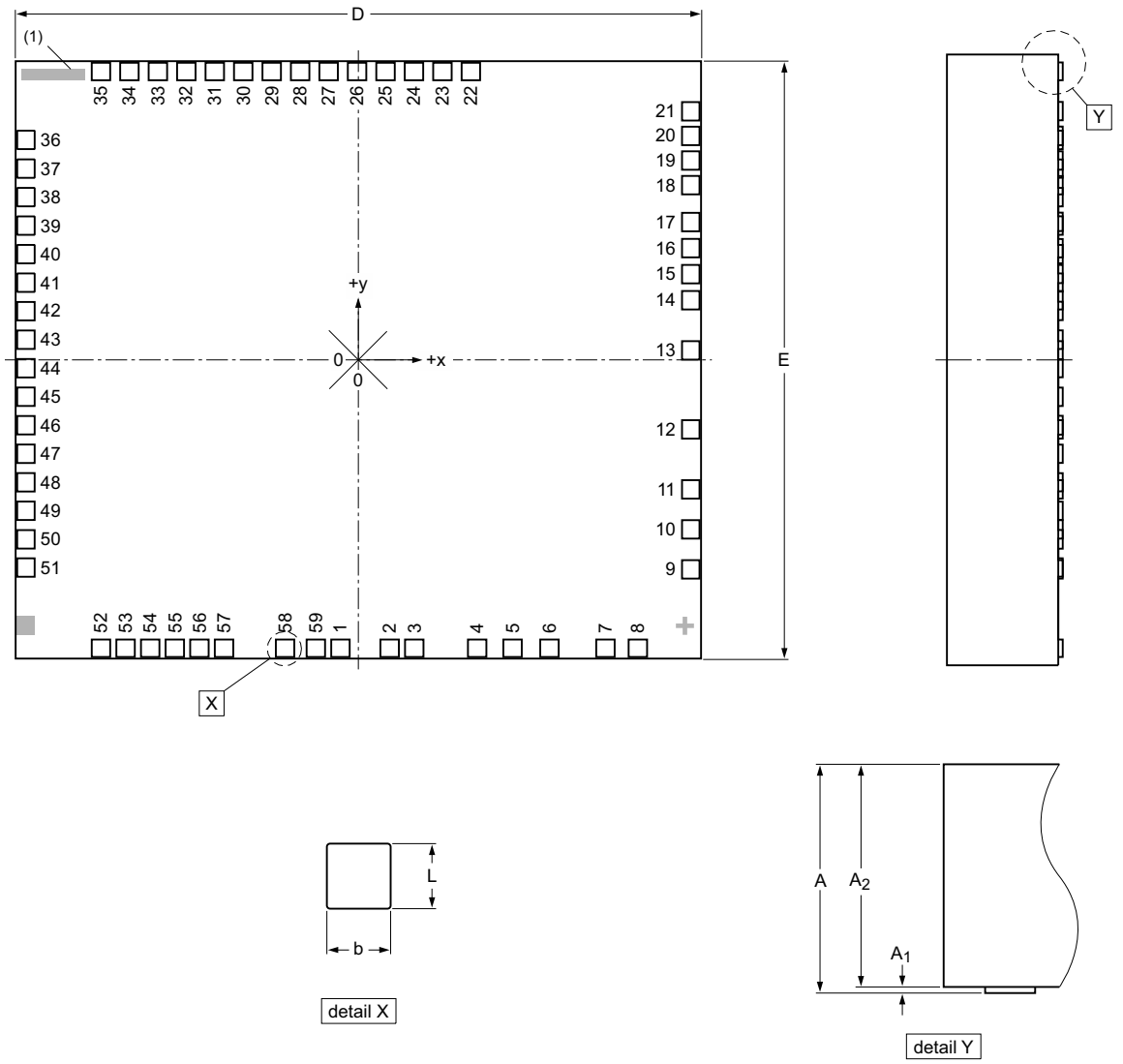
The logic output voltage is calculated with Equation 6:

$$V_{O(log)} = \frac{R_{I(SDA)} + R_{I(VSS)}}{R_{PU} + R_{I(SDA)} + R_{I(VSS)}} \times V_{DD} \quad (6)$$

For further information on this topic, see Ref. 1 “AN10170”.

15. Bare die outline

Bare die; 59 bumps **PCE85176AUG**



Notes
1. Marking code: PC85176A-1
Figure not drawn to scale.

pce85176aug_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCE85176AUG						~~14-04-08~~ 14-04-15

Fig 27. Bare die outline of PCE85176AUG

Table 26. Dimensions of PCE85176AUG

Original dimensions are in mm.

Unit (mm)	A	A_1	A_2	b	D	E	L
max	-	-	-	-	-	-	-
nom	0.40	0.015	0.38	0.051	2.1	1.8	0.054
min	-	-	-	-	-	-	-

Table 27. Bump location for PCE85176AUG

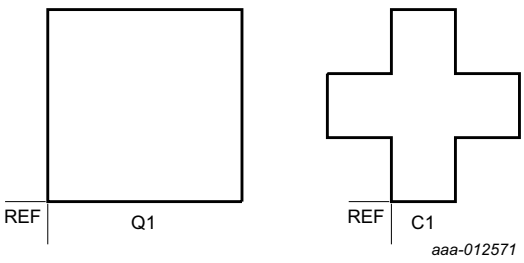
All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip (see Figure 27).

Symbol	Bump	Location		Pitch		Description
		X (μm)	Y (μm)	X (μm)	Y (μm)	
SDA	1	–52.4	–843.7	-	-	I^2C-bus serial data input/output
SCL	2	91.5	–843.7	143.9	0	I^2C-bus serial clock input
SCL	3	163.5	–843.7	72	0	
T1	4	347.6	–843.7	184.1	0	test pin
CLK	5	451.1	–843.7	103.5	0	external clock input/output
V_{DD}	6	559.1	–843.7	108	0	supply voltage
OSC	7	722.9	–843.7	163.8	0	internal oscillator enable input
T2	8	817.8	–843.7	94.9	0	test pins
T3	9	972.5	–612.9	-	-	
T4	10	972.5	–495.9	0	117	
SA0	11	972.5	–378.9	0	117	I^2C-bus address input; bit 0
V_{SS}	12	972.5	–203.4	0	175.5	ground supply voltage
V_{LCD}	13	972.5	27.8	0	231.2	LCD supply voltage
BP0	14	972.5	174.5	0	146.7	LCD backplane outputs
BP2	15	972.5	250.8	0	76.3	
BP1	16	972.5	327.0	0	76.2	
BP3	17	972.5	403.2	0	76.2	
S0	18	972.5	511.2	0	108	LCD segment outputs
S1	19	972.5	583.2	0	72	
S2	20	972.5	655.2	0	72	
S3	21	972.5	727.2	0	72	
S4	22	329.2	843.7	-	-	
S5	23	246.0	843.7	83.2	0	
S6	24	162.7	843.7	83.3	0	
S7	25	79.5	843.7	83.2	0	
S8	26	–3.8	843.7	83.3	0	
S9	27	–87.0	843.7	83.2	0	
S10	28	–170.3	843.7	83.3	0	
S11	29	–253.5	843.7	83.2	0	
S12	30	–336.8	843.7	83.3	0	
S13	31	–420.0	843.7	83.2	0	
S14	32	–503.3	843.7	83.3	0	

Table 27. Bump location for PCE85176AUG *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip (see Figure 27).

Symbol	Bump	Location		Pitch		Description
		X (μm)	Y (μm)	X (μm)	Y (μm)	
S15	33	–586.5	843.7	83.2	0	LCD segment outputs
S16	34	–669.8	843.7	83.3	0	
S17	35	–753.0	843.7	83.2	0	
S18	36	–972.5	643.6	-	-	
S19	37	–972.5	559.6	0	84	
S20	38	–972.5	476.2	0	83.4	
S21	39	–972.5	392.8	0	83.4	
S22	40	–972.5	309.4	0	83.4	
S23	41	–972.5	225.9	0	83.5	
S24	42	–972.5	142.5	0	83.4	
S25	43	–972.5	59.1	0	83.4	
S26	44	–972.5	–24.4	0	83.5	
S27	45	–972.5	–107.8	0	83.4	
S28	46	–972.5	–191.2	0	83.4	
S29	47	–972.5	–274.7	0	83.5	
S30	48	–972.5	–358.1	0	83.4	
S31	49	–972.5	–441.5	0	83.4	
S32	50	–972.5	–525.0	0	83.5	
S33	51	–972.5	–607.6	0	82.6	
S34	52	–753.0	–843.7	-	-	
S35	53	–681.0	–843.7	72	0	
S36	54	–609.0	–843.7	72	0	
S37	55	–537.0	–843.7	72	0	
S38	56	–465.0	–843.7	72	0	
S39	57	–393.0	–843.7	72	0	
SDA	58	–214.4	–843.7	178.6	0	I^2C-bus serial data input/output
SDA	59	–124.4	–843.7	90	0	



The approximate positions of the alignment marks are shown in Figure 27.

Fig 28. Alignment marks of PCE85176AUG

Table 28. Alignment marks

All x/y coordinates represent the position of the REF point (see Figure 28) with respect to the center (x/y = 0) of the chip (see Figure 2, and Figure 27).

Symbol	Location		Dimension (μm)
	X (μm)	Y (μm)	
Q1	−987.1	−778.0	45 × 45
C1	955.4	−778.0	45 × 45

Table 29. Gold bump hardness

Type number	Min	Max	Unit[1]
PCE85176AUG/DA	60	120	HV

[1] Pressure of diamond head: 10 g to 50 g.

16. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

17. Packing information

17.1 Tray information for PCE85176AUG

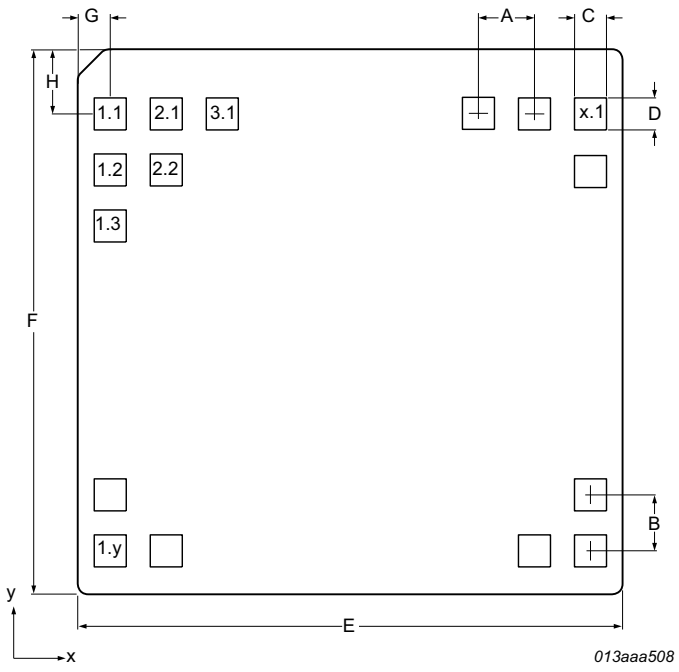


Fig 29. Tray details for PCE85176AUG

Table 30. Dimensions of tray for PCE85176AUG

See Figure 29.

Symbol	Description	Value
A	pocket pitch in x direction	3.2 mm
B	pocket pitch in y direction	3.0 mm
C	pocket width in x direction	2.2 mm
D	pocket width in y direction	1.9 mm
E	tray width in x direction	50.8 mm
F	tray width in y direction	50.8 mm
G	pitch from edge of tray to pocket center in x direction	4.6 mm
H	pitch from edge of tray to pocket center in y direction	4.4 mm
N	number of pockets, x direction	14
M	number of pockets, y direction	15

The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray (see Figure 30). Refer to the bare die outline drawing (see Figure 27) for the orientation and position of the type name on the die surface.

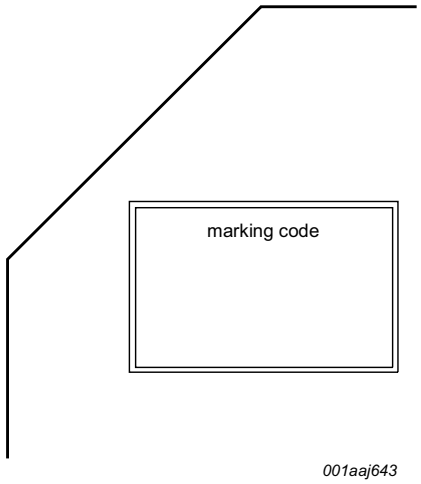


Fig 30. Tray alignment for PCE85176AUG tray

18. Appendix

18.1 LCD segment driver selection

Table 31. Selection of LCD segment drivers

Type name	Number of elements at MUX							V_{DD} (V)	V_{LCD} (V)	f_{fr} (Hz)	V_{LCD} (V) charge pump	V_{LCD} (V) temperature compensat.	T_{amb} (°C)	Interface	Package	AEC-Q100
	1:1	1:2	1:3	1:4	1:6	1:8	1:9									
PCA8553DTT	40	80	120	160	-	-	-	1.8 to 5.5	1.8 to 5.5	32 to 256[1]	N	N	–40 to 105	I^2C / SPI	TSSOP56	Y
PCA8546ATT	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	I^2C	TSSOP56	Y
PCA8546BTT	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	SPI	TSSOP56	Y
PCA8547AHT	44	88	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 95	I^2C	TQFP64	Y
PCA8547BHT	44	88	-	176	-	-	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 95	SPI	TQFP64	Y
PCF85134HL	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 6.5	82	N	N	–40 to 85	I^2C	LQFP80	N
PCA85134H	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 8	82	N	N	–40 to 95	I^2C	LQFP80	Y
PCA8543AHL	60	120	-	240	-	-	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 105	I^2C	LQFP80	Y
PCF8545ATT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	60 to 300[1]	N	N	–40 to 85	I^2C	TSSOP56	N
PCF8545BTT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	60 to 300[1]	N	N	–40 to 85	SPI	TSSOP56	N
PCF8536AT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 85	I^2C	TSSOP56	N
PCF8536BT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 85	SPI	TSSOP56	N
PCA8536AT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	I^2C	TSSOP56	Y
PCA8536BT	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	N	N	–40 to 95	SPI	TSSOP56	Y
PCF8537AH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 85	I^2C	TQFP64	N
PCF8537BH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 85	SPI	TQFP64	N
PCA8537AH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 95	I^2C	TQFP64	Y
PCA8537BH	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 95	SPI	TQFP64	Y
PCA9620H	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 105	I^2C	LQFP80	Y
PCA9620U	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	60 to 300[1]	Y	Y	–40 to 105	I^2C	Bare die	Y
PCF8576DU	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	77	N	N	–40 to 85	I^2C	Bare die	N
PCF8576EUG	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	77	N	N	–40 to 85	I^2C	Bare die	N
PCA8576FUG	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 8	200	N	N	–40 to 105	I^2C	Bare die	Y
PCF85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 6.5	82, 110[2]	N	N	–40 to 85	I^2C	Bare die	N
PCA85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 8	82, 110[2]	N	N	–40 to 95	I^2C	Bare die	Y

Table 31. Selection of LCD segment drivers *...continued*

Type name	Number of elements at MUX							V_{DD} (V)	V_{LCD} (V)	f_{fr} (Hz)	V_{LCD} (V) charge pump	V_{LCD} (V) temperature compensat.	T_{amb} (°C)	Interface	Package	AEC-Q100
	1:1	1:2	1:3	1:4	1:6	1:8	1:9									
PCA85233UG	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 8	150, 220[2]	N	N	–40 to 105	I^2C	Bare die	Y
PCF85132U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	60 to 90[1]	N	N	–40 to 85	I^2C	Bare die	N
PCA8530DUG	102	204	-	408	-	-	-	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y	–40 to 105	I^2C / SPI	Bare die	Y
PCA85132U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	60 to 90[1]	N	N	–40 to 95	I^2C	Bare die	Y
PCA85232U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	117 to 176[1]	N	N	–40 to 95	I^2C	Bare die	Y
PCF8538UG	102	204	-	408	612	816	918	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y	–40 to 85	I^2C / SPI	Bare die	N
PCA8538UG	102	204	-	408	612	816	918	2.5 to 5.5	4 to 12	45 to 300[1]	Y	Y	–40 to 105	I^2C / SPI	Bare die	Y

[1] Software programmable.

[2] Hardware selectable.

19. Abbreviations

Table 32. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DC	Direct Current
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MSB	Most Significant Bit
RAM	Random Access Memory
RC	Resistance and Capacitance
RMS	Root Mean Square
SCL	Serial CLock line
SDA	Serial DAta Line

20. References

[1] **AN10170 —** Design guidelines for COG modules with NXP monochrome LCD drivers

[2] **AN10365 —** Surface mount reflow soldering description

[3] **AN10439 —** Wafer Level Chip Size Package

[4] **AN10706 —** Handling bare die

[5] **AN10853 —** ESD and EMC sensitivity of IC

[6] **AN11267 —** EMC and system level ESD design guidelines for LCD drivers

[7] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[8] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[9] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[10] **JESD78 —** IC Latch-Up Test

[11] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[12] **R_10015 —** Chip-On-Glass (COG) - a cost-effective and reliable technology for LCD displays

[13] **UM10204 —** I^2C-bus specification and user manual

[14] **UM10569 —** Store and transport requirements

21. Revision history

Table 33. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCE85176AUG v.1	20150112	Product data sheet	-	-

22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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24. Tables

25. Figures

26. Contents

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- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

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