

## Serial EEPROM Series Automotive EEPROM

## 125°C Operation SPI BUS EEPROM

# **BR25H640-2AC**

## **General Description**

BR25H640-2AC is a 64Kbit Serial EEPROM of SPI BUS interface method.

#### **Features**

■ SPI BUS interface (CPOL, CPHA)=(0,0), (1,1)

Voltage Range
 ∴ 2.5V to 5.5V
 ∴ -40°C to +125°C
 ∴ Clock Frequency
 ∴ Write Time
 ∴ 4ms(Max)
 ∴ Page Size
 ∴ 32bytes
 → Bit Format
 ∴ 8192 x 8bit

■ 32bytes Write Lockable Identification Page (ID Page)

■ Address Auto Increment Function at Read Operation

■ Auto Erase and Auto End Function at Data Rewrite

■ Write Protect Block Setting by Software Memory Array 1/4, 1/2, Whole

■ HOLD Function by HOLDB Pin

■ Low Supply Current

Write Operation (5V) : 1.0mA (Typ) Read Operation (5V) : 1.2mA (Typ) Standby State(5V) : 0.1µA (Typ)

Prevention of Write Mistake

Write prohibition at Power On Write prohibition by WPB Pin Write prohibition Block Setting

Prevention of Write Mistake at Low Voltage

■ Write Cycles : 1,000,000 Write Cycles (Ta≤85°C)

500,000 Write Cycles (Ta≤105°C) 300,000 Write Cycles (Ta≤125°C)

■ Data Retention : 100 Years (Ta≤25°C) : 60 Years (Ta≤105°C)

: 50 Years (Ta≤125°C)

■ Data at Shipment

Memory Array : FFh

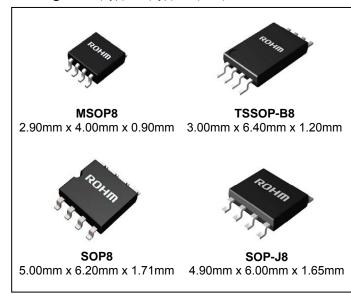
ID Page First 3 Addresses : 2Fh, 00h, 0Dh

Other Addresses : FFh
Status Register WPEN, BP1, BP0 : 0, 0, 0
Lock Status LS : 0

■ MSOP8, TSSOP-B8, SOP8, SOP-J8 Packages

■ AEC-Q100 Qualified

## Packages W(Typ) x D(Typ) x H(Max)



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit	
Supply Voltage	Vcc	-0.3 to +6.5	V	
		0.38 (MSOP8) (Note1)		
Danies Dississation	Dd	0.41 (TSSOP-B8) (Note2)	10/	
Power Dissipation	Pd	0.56 (SOP8) (Note3)	W	
		0.56 (SOP-J8) (Note4)		
Storage Temperature Range	Tstg	-65 to +150	°C	
Operating Temperature Range	Topr	-40 to +125	°C	
Terminal Voltage	_	-0.3 to +6.5	V	
Maximum Junction Temperature	Tjmax	150	°C	
Electrostatic Discharge Voltage (Human Body Model)	V <sub>ESD</sub>	-6000 to +6000	V	

(Note1) Derate by 3.1mW/°C when operating above Ta=25°C

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Memory Cell Characteristics (Vcc=2.5V to 5.5V)

Parameter		Limit	Unit	Condition	
Farameter	Min	Тур	Max	Offic	Condition
	1,000,000	_	_	Cycles	Ta≤85°C
Write Cycles (Note5, 6)	500,000	_	_	Cycles	Ta≤105°C
	300,000	_	_	Cycles	Ta≤125°C
	100	_	_	Years	Ta≤25°C
Data Retention (Note5)	60	_	_	Years	Ta≤105°C
	50	_	_	Years	Ta≤125°C

(Note5) Not 100% TESTED

(Note6) The Write Cycles is defined for unit of 4 data bytes with the same address bits of A12 to A2.

**Recommended Operating Ratings** 

Parameter	Symbol	Ra	Unit	
Farameter	Symbol	Min	Max	UTIIL
Supply Voltage	Vcc	2.5	5.5	V
Input Voltage	VIN	0	Vcc	V
Bypass Capacitor	С	0.1	_	μF

Input / Output Capacitance (Ta=25°C, Frequency=5MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Capacitance (Note7)	Cin	V <sub>IN</sub> =GND	_	8	pF
Output Capacitance (Note7)	Соит	V <sub>OUT</sub> =GND	_	8	pF

(Note7) Not 100% TESTED

<sup>(</sup>Note2) Derate by 3.3mW/°C when operating above Ta=25°C.

<sup>(</sup>Note3) Derate by 4.5mW/°C when operating above Ta=25°C.

<sup>(</sup>Note4) Derate by 4.5mW/°C when operating above Ta=25°C.

DC Characteristics (Unless otherwise specified, Ta=-40°C to +125°C, Vcc=2.5V to 5.5V)

Parameter	Symbol	Limit			Unit	Conditions
न् वावागि <del>द्</del> दा	Symbol	Min	Тур	Max	Offic	Conditions
Input High Voltage	V <sub>IH</sub>	0.7 Vcc	_	Vcc+0.3	٧	2.5V≤Vcc≤5.5V
Input Low Voltage	VIL	-0.3	_	0.3 Vcc	٧	2.5V≤Vcc≤5.5V
Output Low Voltage	Vol	0	_	0.4	٧	I <sub>OL</sub> =2.1mA
Output High Voltage	Vон	0.8 Vcc	-	Vcc	<b>V</b>	I <sub>OH</sub> =-2.0mA
Input Leakage Current	ILI	-2	_	+2	μΑ	V <sub>IN</sub> =0V to Vcc
Output Leakage Current	I <sub>LO</sub>	-2	_	+2	μΑ	V <sub>OUT</sub> =0V to Vcc, CSB=Vcc
Supply Current	Icc1	_	-	2.5	mA	Vcc=2.5V, f <sub>SCK</sub> =5MHz, t <sub>EW</sub> =4ms V <sub>IH</sub> /V <sub>IL</sub> =0.9Vcc/0.1Vcc, SO=OPEN
(WRITE)	I <sub>CC2</sub>	_	_	5.5	mA	Vcc=5.5V, f <sub>SCK</sub> =5 or 10 MHz, t <sub>E/W</sub> =4ms V <sub>IH</sub> /V <sub>IL</sub> =0.9Vcc/0.1Vcc, SO=OPEN
	Іссз	_	_	1.5	mA	Vcc=2.5V, f <sub>SCK</sub> =5MHz V <sub>IH</sub> /V <sub>IL</sub> =0.9Vcc/0.1Vcc, SO=OPEN
Supply Current (READ)	Icc4	_	_	2.0	mA	Vcc=5.5V, f <sub>SCK</sub> =5MHz V <sub>IH</sub> /V <sub>IL</sub> =0.9Vcc/0.1Vcc, SO=OPEN
	I <sub>CC5</sub>	_	-	4.0	mA	Vcc=5.5V, f <sub>SCK</sub> =10MHz V <sub>IH</sub> /V <sub>IL</sub> =0.9Vcc/0.1Vcc, SO=OPEN
Standby Current	I <sub>SB</sub>	_	-	10	μΑ	Vcc=5.5V CSB=HOLDB=WPB=Vcc, SCK=SI=Vcc or 0V, SO=OPEN

AC Characteristics (Ta=-40°C to +125°C, unless otherwise specified, load capacitance C<sub>L1</sub>=100pF)

Parameter	Symbol	2.5	V≤Vcc≤5	5.5V	4.5V≤Vcc≤5.5V			Unit
Parameter	Symbol	Min	Тур	Max	Min	Тур	Max	Onit
SCK Frequency	f <sub>SCK</sub>	0.01	_	5	0.01	_	10	MHz
SCK High Time	tscкwн	85	_	_	40	_	_	ns
SCK Low Time	tsckwl	85	_	_	40	_	_	ns
CSB High Time	t <sub>CS</sub>	85	_	_	40	_	_	ns
CSB Setup Time	tcss	90	_	_	30	_	_	ns
CSB Hold Time	t <sub>сsн</sub>	85	_	_	30	_	_	ns
SCK Setup Time	tscks	90	_	_	30	_	_	ns
SCK Hold Time	tscкн	90	_	_	30	_	_	ns
SI Setup Time	t <sub>DIS</sub>	20	_	_	10	_	_	ns
SI Hold Time	tын	30	_	_	10	_	_	ns
Data Output Delay Time1	t <sub>PD1</sub>	_	_	60	_	_	40	ns
Data Output Delay Time2 (C <sub>L2</sub> =30pF)	t <sub>PD2</sub>	_	_	50	_	_	30	ns
Output Hold Time	tон	0	_	_	0	_	_	ns
Output Disable Time	toz	_	_	100	_	_	40	ns
HOLDB Setting Setup Time	t <sub>HFS</sub>	0	_	_	0	_	_	ns
HOLDB Setting Hold Time	t <sub>HFH</sub>	40	_	_	30	_	_	ns
HOLDB Release Setup Time	thrs	0	_	_	0	_	_	ns
HOLDB Release Hold Time	t <sub>HRH</sub>	70	_	_	30	_	_	ns
Time from HOLDB to Output High-Z	tноz	_	_	100	_	_	40	ns
Time from HOLDB to Output Change	<b>t</b> HPD	_	_	60	_	_	40	ns
SCK Rise Time (Note1)	t <sub>RC</sub>	_	_	2	_	_	2	μs
SCK Fall Time (Note1)	t <sub>FC</sub>	_	_	2	_	_	2	μs
Output Rise Time (Note1)	t <sub>RO</sub>	_	_	40	_	_	20	ns
Output Fall Time (Note1)	t <sub>FO</sub>	_	_	40	_	_	20	ns
Write Time	t⊨∕w	_	_	4	_	_	4	ms

(Note1) NOT 100% TESTED

## **AC Measurement Conditions**

moded official contactions								
Parameter	Symbol		Unit					
Farameter	Symbol	Min	Тур	Max	Offic			
Load Capacitance1	C <sub>L1</sub>	_	_	100	pF			
Load Capacitance2	C <sub>L2</sub>	_	_	30	pF			
Input Rise Time	_	_	_	50	ns			
Input Fall Time	_	_	_	50	ns			
Input Voltage	_	0.2 Vcc / 0.8 Vcc			V			
Input / Output Judgment Voltage	_	0.3 Vcc / 0.7 Vcc			V			

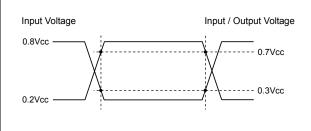


Figure 1. Input / Output Judgment Voltage

## **Serial Input / Output Timing**

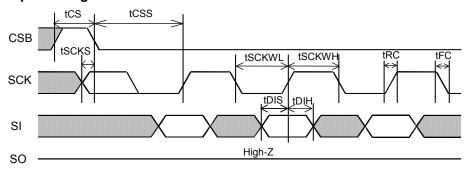


Figure 2. Input Timing

SI is taken into IC inside in sync with data rise edge of SCK. Input address and data from the Most Significant Bit MSB.

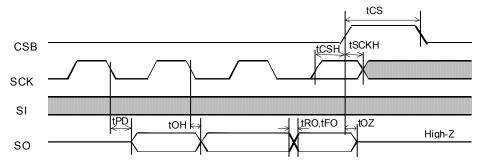
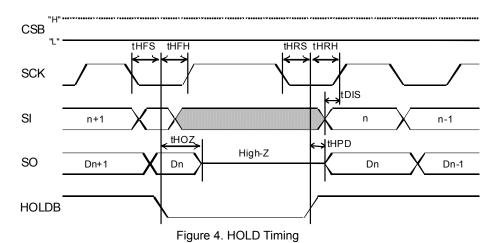


Figure 3. Input / Output Timing

SO is output in sync with data fall edge of SCK. Data is output from the Most Significant Bit MSB.



## **Block Diagram**

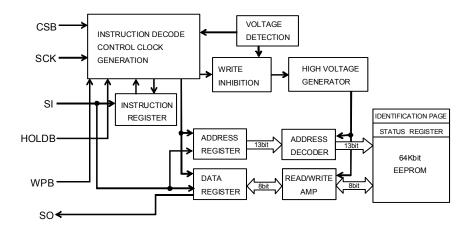


Figure 5. Block Diagram

## **Pin Configuration**

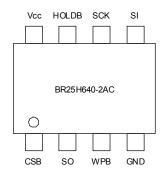


Figure 6. Pin Assignment Diagram

## **Pin Description**

Pin Number	Pin Name	Input / Output	Function
1	CSB	Input	Chip Select Input
2	SO	Output	Serial Data Output
3	WPB	Input	Write Protect Input Write Status Register Command is prohibited.
4	GND	_	All Input / Output Reference Voltage, 0V
5	SI	Input	Serial Data Input Start Bit, Instruction Code, Address and Data Input
6	SCK	Input	Serial Clock Input
7	HOLDB	Input	Hold Input Serial Communications may be suspended temporarily (HOLD State).
8	Vcc	_	Supply Voltage

## **Typical Performance Curves**

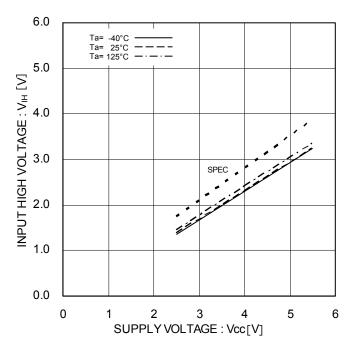


Figure 7. Input High Voltage V<sub>IH</sub> (CSB, SCK, SI, HOLDB, WPB)

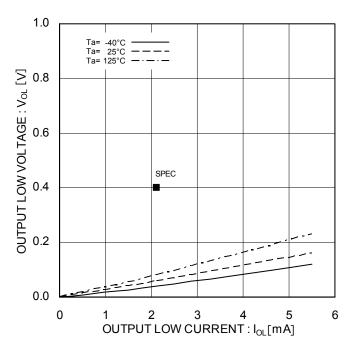


Figure 9. Output Low Voltage Vol., Iol (Vcc=2.5V)

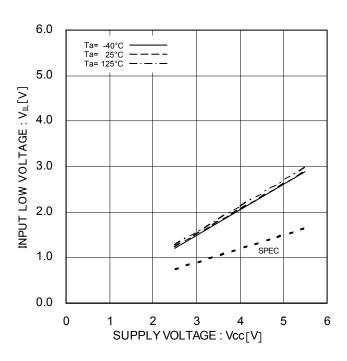


Figure 8. Input Low Voltage V<sub>IL</sub> (CSB, SCK, SI, HOLDB, WPB)

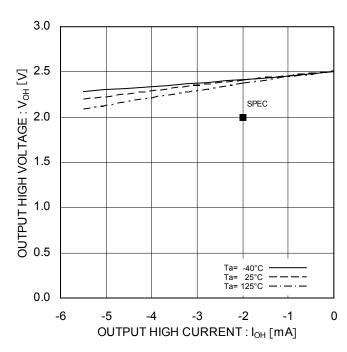


Figure 10. Output High Voltage Voh, Ioh (Vcc=2.5V)

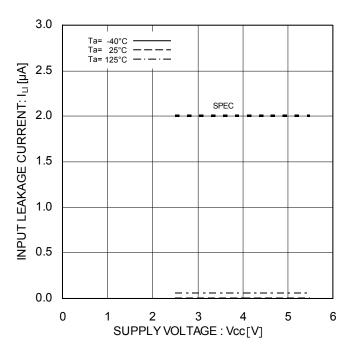


Figure 11. Input Leakage Current ILI (CSB, SCK, SI, HOLDB, WPB)

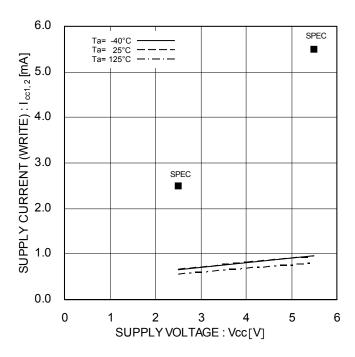


Figure 13. Supply Current (WRITE) ICC1,2

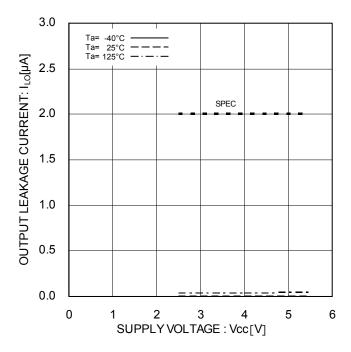


Figure 12. Output Leakage Current I<sub>LO</sub> (SO)

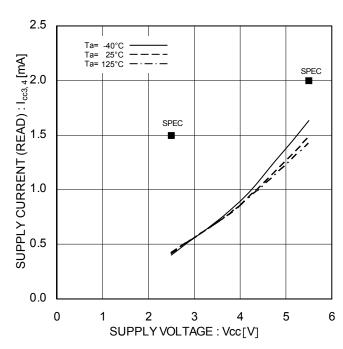


Figure 14. Supply Current (READ) Icc3,4

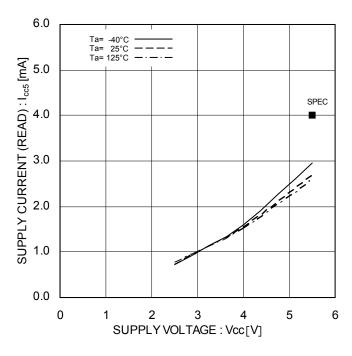


Figure 15. Supply Current (READ) Iccs

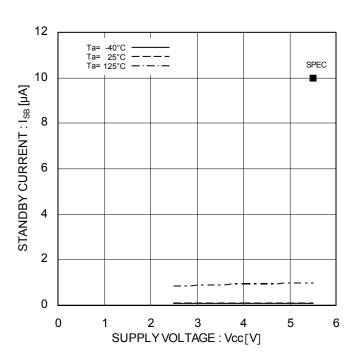


Figure 16. Standby Current ISB

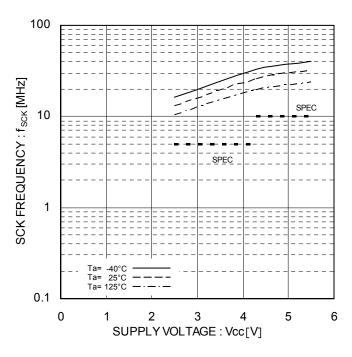


Figure 17. SCK Frequency fsck

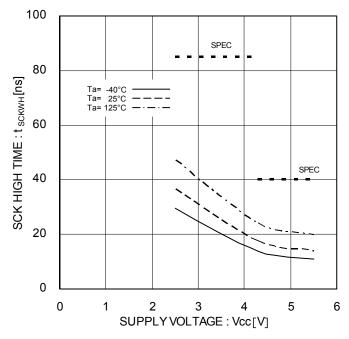


Figure 18. SCK High Time tsckwh

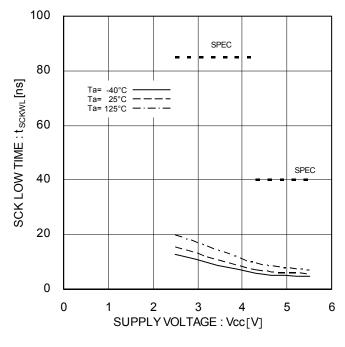


Figure 19. SCK Low Time tsckwL

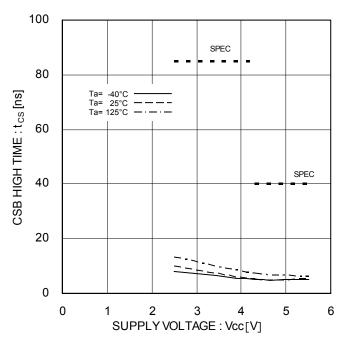


Figure 20. CSB High Time tcs

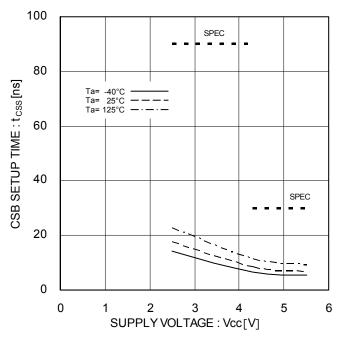


Figure 21. CSB Setup Time tcss

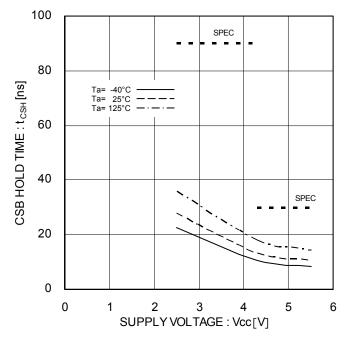


Figure 22. CSB Hold Time tcsh

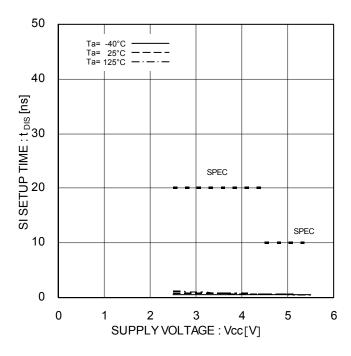


Figure 23. SI Setup Time tols

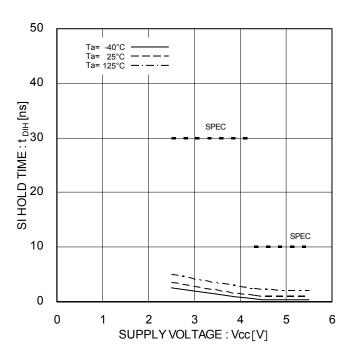


Figure 24. SI Hold Time tolh

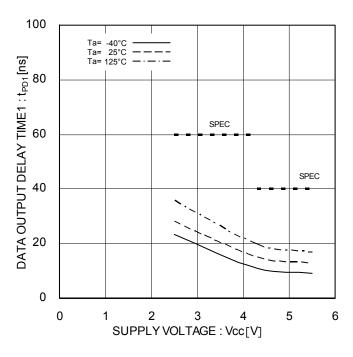


Figure 25. Data Output Delay Time1 t<sub>PD1</sub> (C<sub>L1</sub>=100pF)

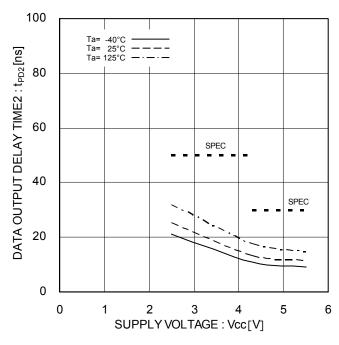


Figure 26. Data Output Delay Time2 tpD2 (CL2=30pF)

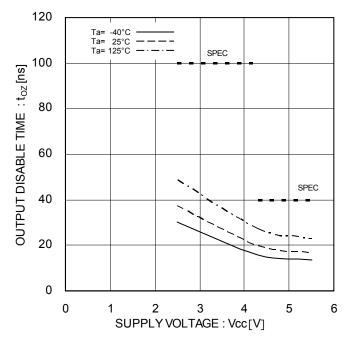


Figure 27. Output Disable Time toz

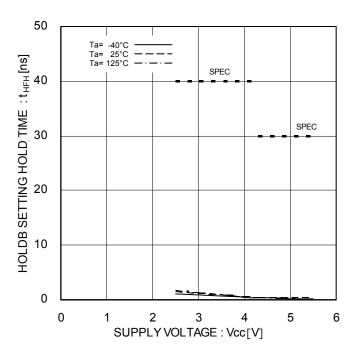


Figure 28. HOLDB Setting Hold Time theh

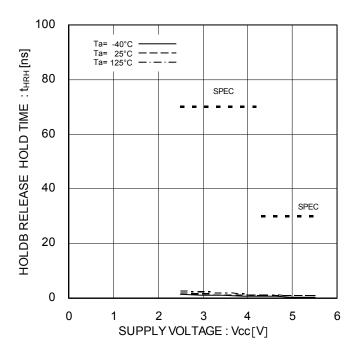


Figure 29. HOLDB Release Hold Time three

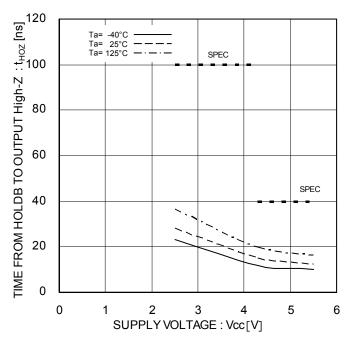


Figure 30. Time from HOLDB to Output High-Z thoz

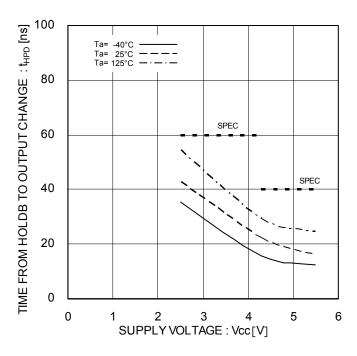


Figure 31. Time from HOLDB to Output Change then

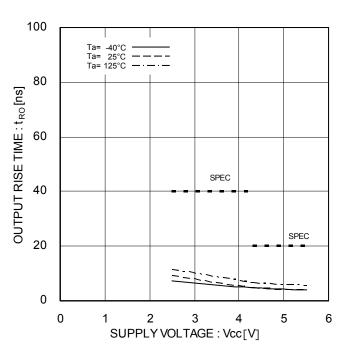


Figure 32. Output Rise Time tRO

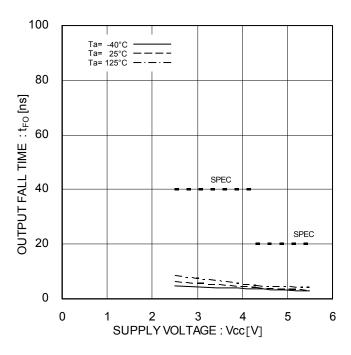


Figure 33. Output Fall Time  $t_{FO}$ 

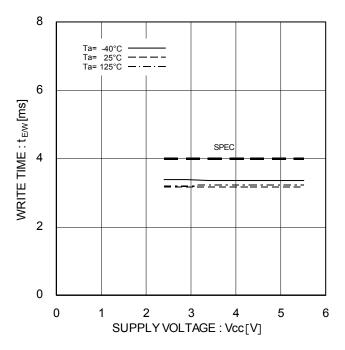


Figure 34. Write Time  $t_{E/W}$ 

#### 1. Features

## (1) Status Register

This IC has the Status Registers. Status Registers are of 8 bits and express the following parameters.

WPEN, BP0 and BP1 can be set by Write Status Register command. These 3 bits are memorized into the EEPROM, therefore are valid even when supply voltage is turned off.

Write Cycles and Data Retention of Status Registers are same as characteristics of the EEPROM.

WEN can be set by Write Enable command and Write Disable command. WEN becomes write disable status when supply voltage is turned off.  $\overline{R}/B$  is for write confirmation, therefore cannot be set externally.

The values of Status Register can be read by Read Status Register command.

Table 1. Status Register

D7	D6	D5	D4	D3	D2	D1	D0
WPEN	0	0	0	BP1	BP0	WEN	R/B

Table 2. Function of Status Register

bit	Memory Location	Function	Content
WPEN	EEPROM	Pin Enable / Disable designation bit for WPB pin WPEN=0=Invalid, WPEN=1=Valid	WPEN bit enables / disables the function of WPB pin.
BP1 BP0	EEPROM	EEPROM Write Disable Block designation bit	BP1 and BP0 bits designate the Write Disable Block of EEPROM. Refer Table 3. Write Disable Block Setting.
WEN	Register	Write Enable/Write Disable Confirmation bit for WRITE, WRSR, WRID and LID WEN=0=Prohibited, WEN=1=Permitted	WEN bit indicates the status of write enable or write disable for WRITE, WRSR, WRID, LID.
R/B	Register	Write Cycle Status(READY/BUSY) Confirmation bit R/B=0=READY, R/B=1=BUSY	R/B bit indicates the status of READY or BUSY of the write cycle.

Table 3. Write Disable Block Setting

Status I	Register	Protected Block	Protected Addresses		
BP1	BP0	Protected Block	Frolected Addresses		
0	0	None	None		
0	1	Upper 1/4	1800h to 1FFFh		
1	0	Upper 1/2	1000h to 1FFFh		
1	1	Whole Memory	0000h to 1FFFh, ID Page		

#### (2) Write Protect Mode by WPB pin

By setting WPB = Low with WPEN = 1, Write Status Register command is disabled. Only when WPEN bit is set "1", the WPB pin functions become valid. However, when write cycle is in execution, no interruption can be made.

Table 4. Write Protect Mode

WPEN bit	WDD nin	Instruction		
VVP EIN DIL	WPB pin	WRSR	WRITE/WRID/LID	
0	Х	Writable	Writable	
1	1	Writable	Writable	
1	0	Write Protected	Writable	

WPB is normally fixed to High or Low for use, but when WPB is controlled so as to cancel Write Status Register command, pay attention to the following WPB Valid Timing.

Write Status Register command is executed, by setting WPB = Low in cancel valid area, command can be cancelled. The Data area (from 7th fall of SCK to 16th rise of SCK) becomes the cancel valid area. However, once write is started, any input cannot be cancelled. WPB input becomes Don't Care, and cancellation becomes invalid.

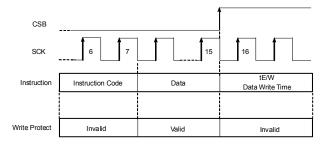


Figure 35. WPB Valid Timing (WRSR)

## (3) Hold Mode by HOLDB pin

By the HOLDB pin, serial communication can be stopped temporarily (HOLD status). HOLDB pin carries out serial communications normally when it is High. To get in HOLD status, at serial communication, when SCK = Low, set the HOLDB pin Low. At HOLD status, SCK and SI become Don't Care, and SO becomes high impedance (High-Z). To release the HOLD status, set the HOLDB pin High when SCK = Low. After that, communication can be restarted from the point before the HOLD status. For example, when HOLD status is made after A5 address input at Read command, after release of HOLD status, by starting A4 address input, Read command can be restarted. When in HOLD status, leave CSB = Low. When it is set CSB = High in HOLD status, the IC is reset, therefore communication after that cannot be restarted.

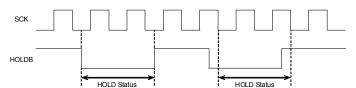


Figure 36. HOLD Status

#### (4) ID Page

This IC has 32 bytes Write lockable Identification Page (ID Page) in addition to Memory Array.

The data in the first 3 addresses are for device identification. These data are over written by Write ID Page command.

Table 5. Data in the first 3 addresses

ID Page Address	Data	Content
00h	2Fh	Manufacturer Code (ROHM)
01h	00h	Interface Method (SPI)
02h	0Dh	Memory Density (64Kbit)

By setting Lock Status (LS) bit to "1" with Lock ID Page command, it is prohibited to write to ID page permanently. It is not reversible to set from ID Page Lock Status (LS="1") to ID Page Lock Release status (LS="0").

Table 6. Function of Lock Status

bit	Memory Location	Function	Content
LS	EEPROM	ID Page Lock/ Lock Release Status designation bit LS=0=ID Page Lock Release LS=1=ID Page Lock	LS bit can set Lock Status to ID Page.

## (5) ECC Function

This IC has ECC bits for Error Correction to each 4 data bytes with the same address bits of A12 to A2. In the Read operation, even if there is 1 bit data error in the 4 bytes, IC corrects to correct data by ECC function and outputs data corrected. Even if write operation is started with only 1 byte data input, this IC rewrites the data of 4 bytes with the same address bits of A12 to A2 and the data of ECC bits added to these 4 bytes data. In order to maximize Write Cycles specified, it is recommended to write with data input of each 4 bytes with the same address bits of A12 to A2.

Table 7. Example of 4 data bytes with the same address bits of A12 to A2 (Address 0000h,0001h,0002h,0003h)

	Same Address Bits from A12 to A2									Non- Common		Address	
A12	A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2							A1	A0				
0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
0	0	0	0	0	0	0	0	0	0	0	0	1	0001h
0	0	0	0	0	0	0	0	0	0	0	1	0	0002h
0	0	0	0	0	0	0	0	0	0	0	1	1	0003h

## 2. Instruction Mode

After setting CSB pin from High to Low, to execute each command, input Instruction Code, Address and Data from the Most Significant Bit MSB.

Table 8. Instruction Mode

iable o. ilistit	dollott Mode				
Instruction	Content	Instruction Code (8bit)	Address(MSB) / Data (8bit)	Address (LSB) (8bit)	Data (8bit)
WREN	Write Enable	0000 0110	-	-	-
WRDI	Write Disable	0000 0100	-	-	-
READ	Read	0000 0011	A15 to A8 (Note1)	A7 to A0	D7 to D0 Output
WRITE	Write	0000 0010	A15 to A8 (Note1)	A7 to A0	D7 to D0 Input
RDSR	Read Status Register	0000 0101	D7 to D0 Output (Note2)	-	-
WRSR	Write Status Register	0000 0001	D7 to D0 Input (Note2)	-	-
RDID	Read ID Page	1000 0011	0000 0000	00A4 to A0	D7 to D0 Output
WRID	Write ID Page	1000 0010	0000 0000	00A4 to A0	D7 to D0 Input
RDLS	Read Lock Status	1000 0011	0000 0100	0000 0000	D7 to D0 Output
LID	Lock ID page	1000 0010	0000 0100	0000 0000	D7 to D0 Input (Note3)

<sup>(</sup>Note1) Address bit A15, A14, A13 = Don't Care

<sup>(</sup>Note2) Refer Figure 43. , Figure 44.. (Note3) Refer Figure 47. , Figure 48..

#### 3. Timing Chart

## (1) Write Enable Command (WREN)

It is set to write enable status by Write Enable command. As for this command, set CSB to Low, and then input the Instruction Code of Write Enable command. This command is accepted at the 7th rise of SCK. Even with input over 7 clocks, command becomes valid.

Before carrying out Write command, Write Status Register command, Write ID Page command and Lock ID Page command, it is necessary to set write enable status by the Write Enable command.

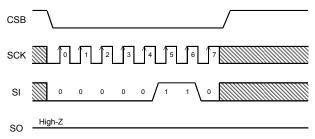


Figure 37. Write Enable Command

## (2) Write Disable Command (WRDI)

It is set to write disable status, WEN bit becomes to "0", by Write Disable command. As for this command, set CSB to Low, and then input the Instruction Code of Write Disable command. This command is accepted at the 7th rise of SCK. Even with input over 7 clocks, command becomes valid.

If Write command, Write Status Register command, Write ID Page command or Lock ID Page command is input in the write disable status, commands are cancelled. And even in the write enable status, once Write command, Write Status Register command, Write ID Page command or Lock ID Page is executed, it gets in the write disable status. After power on, this IC is in write disable status.

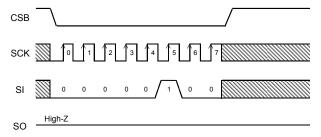


Figure 38. Write Disable Command

#### (3) Read Command (READ)

By Read command, data of EEPROM can be read. As for this command, set CSB to Low, then input address after Instruction Code of Read command. This IC starts data output of the designated address. Data output is started from SCK fall of 23 clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8bits), by continuing input of SCK, data of the next address can be read. Increment read can read all the addresses of EEPROM Array. After reading data of the most significant address, by continuing increment read, data of the least significant address is read.

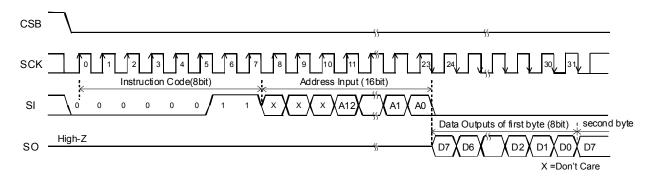


Figure 39. Read Command

#### (4) Write Command (WRITE)

By Write command, data of EEPROM can be written. As for this command, set CSB to Low, then input address and data after Instruction Code of Write command. Then, by making CSB to High, the IC starts write operation. The write time of EEPROM requires time of  $t_{EW}$  (Max 4ms). To start write operation, set CSB Low to High after taking the last data (D0), and before the next SCK clock starts. At other timing, Write command is not executed, and this Write command is cancelled.

During write operation, other than Read Status Register command is not accepted.

This IC has Page Write function, and after input of data for 1 byte (8bits), by continuing data input without setting CSB Low to High, data up to 32 bytes can be written for one tew. In Page Write, the addressed lower 5 address bits are incremented internally at every time when data of 1 byte is inputted and data is written to respective addresses. When the data input exceeds the last address byte of the page, address rolls over to the first address byte of the same page. It is not recommended to input data over 32 bytes, it is recommended to input data in 32 bytes. In case of the data input over 32 bytes, it is explained in Table 10.

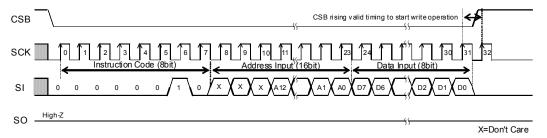


Figure 40. Write Command (Byte Write)

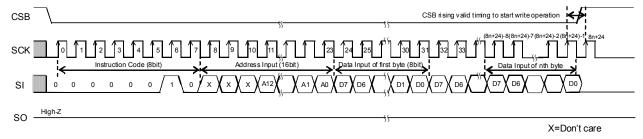


Figure 41. Write Command (Page Write)

#### (a) Page Write Function

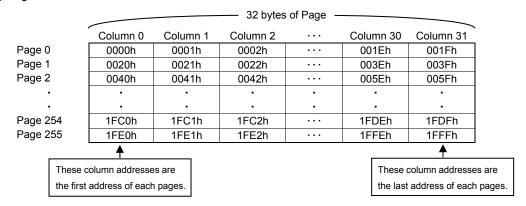


Figure 42. EEPROM physical address for Page Write command (32Byte)

In case of Page Write command with lower than 32 bytes data input

Table 9. Example of Page Write with 2 bytes data input

No.	4 bytes group		Gro	up 0			··· Group 7			up 7	
INO.	Addresses of Page 0	0000h	0001h	0002h	0003h	0004h		001Ch	001Dh	001Eh	001Fh
1	Previous Data	00h	01h	02h	03h	04h		1Ch	1Dh	1Eh	1Fh
2	Input data for Page Write (2 bytes)	AAh	55h	-	-	-		-	-	-	-
3	The Data after Write operation	AAh	55h	02h	03h	04h		1Ch	1Dh	1Eh	1Fh

- No. 1 : These data are EEPROM data before Write operation.
- No.2 : Inputted 2 bytes data AAh, 55h from address 0000h.
- No.③ : If Write operation is executed with the data of No.②, the data are changed from the data of No.① to the data of No.③.

The data of address 0000h, 0001h are changed to data AAh, 55h, the data of address 0002h, 0003h, the 4 bytes group of Group 0, are over-written to data 02h, 03h.

When Write command is cancelled, EEPROM data keep No.1.

In case of Page Write command with more than 32 bytes data input

Table 10. Example of Page Write with 34 bytes data input

No.	4 bytes group		Gro	up 0			 Group 7			
INO.	Addresses of Page 0	0000h	0001h	0002h	0003h	0004h	 001Ch	001Dh	001Eh	001Fh
1	Previous Data	00h	01h	02h	03h	04h	 1Ch	1Dh	1Eh	1Fh
2	Input data for Page Write (34 bytes)	55h	AAh	55h	AAh	55h	 55h	AAh	55h	AAh
		FFh	00h	-	-	-	 -	-	-	-
3	The Data after Write operation	FFh	00h	02h	03h	55h	 55h	AAh	55h	AAh

- No. 1 : These data are EEPROM data before Write operation.
- No.② : Inputted 34 bytes data 55h, AAh, ..., 55h, AAh, FFh, 00h from address 0000h.

  The data of address 0000h, 0001h are set to data 55h, AAh first. The data of address 0002h, 0003h are set to data 55h, AAh. After inputting data to Maximum byte (001Fh), the data address 0000h, 0001h are set to data FFh, 00h again. No data input to address 0002h, 0003h again.
- No.③ : If Write operation is executed with the data of No.②, the data are changed from the data of No.① to the data of No.③.

The data of address 0000h, 0001h are changed to FFh, 00h inputted data later, not to 55h, AAh inputted data first. The data of address 0002h, 0003h, the 4 bytes group of Group 0, are over-written to 02h, 03h of Previous Data, not to 55h, AAh inputted data first. The data of other addresses are changed to 55h, AAh..., 55h, AAh.

When Write command is cancelled, EEPROM data keep No. 1.

#### Roll Over

In Page Write command, when data is set to the last address of a page (e.g. address "001Fh" of page 0), the next data will be set to the first address of the same page (e.g. address "0000h" of page 0). This is why Page Write address increment is available in the same page.

#### (5) Read Status Register Command (RDSR)

By Read Status register command, data of status register can be read. As for this command, set CSB to Low, then input Instruction Code of Read Status Register command. This IC starts data output of the status register. Data output is started from SCK fall of 7 clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8bits), by continuing input of SCK, this IC repeats to output data of the status register. Even if in write operation, Read Status Register command can be executed.

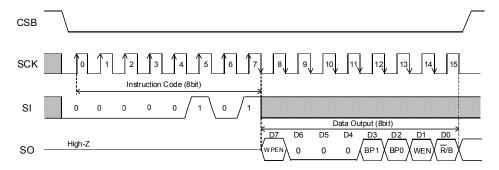


Figure 43. Read Status Register Command

## (6) Write Status Register Command (WRSR)

Write Status Register command can write status register data. The data can be written by this command are 3 bits, that is, WPEN (D7), BP1 (D3) and BP0 (D2) among 8 bits of status register. As for this command, set CSB to Low, and input Instruction Code of Write Status Register command, and input data. Then, by making CSB to High, this IC starts write operation. Write Time requires time of t<sub>EW</sub> as same as Write command. As for CSB rise, start CSB after taking the last data bit (D0), and before the next SCK clock starts. At other timing, command is cancelled. To the write disabled block, write cannot be made, and only read can be made. During write operation, other than Read Status Register command is not accepted.

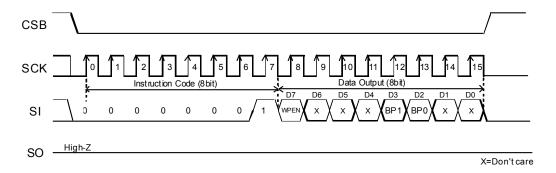


Figure 44. Write Status Register Command

#### (7) Read ID Page Command (RDID)

By Read ID Page command, data of ID Page can be read. As for this command, set CSB to Low, then input address after Instruction Code of Read ID Page command. Input address bit A10 as "0", other upper address bits A12 to A6 as "0". By inputting lower address bits A4 to A0, it is possible to address to 32 bytes ID Page. Data output is started from SCK fall of 23 clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8bits), by continuing input of SCK, data of the next address can be read. After reading data of the most significant address of ID Page, by continuing increment read, data of the least significant address of ID Page is read.

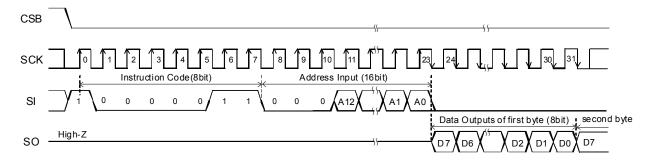


Figure 45. Read ID Page Command

## (8) Write ID Page Command (WRID)

By Write ID Page command, data of ID Page can be written. As for this command, set CSB to Low, then input address and data after Instruction Code of Write ID Page command. Input address bit A10 as "0", other upper address bits A12 to A6 as "0". By inputting lower address bits A4 to A0, it is possible to address to 32 bytes ID Page. Then, by making CSB to High, the IC starts write operation. To start write operation, set CSB Low to High after taking the last data (D0), and before the next SCK clock starts. At other timing, Write ID Page command is not executed, and this Write ID Page command is cancelled. The write time of EEPROM requires time of tew (Max 4ms). During write operation, other than Read Status Register command is not accepted. In case of Lock Status (LS) bit "1", Write ID Page command can't be executed.

Write ID Page command has Page Write Function same as Write command.

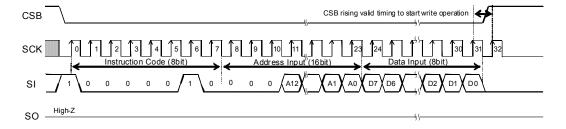


Figure 46. Write ID Page Command

#### (9) Read Lock Status Command (RDLS)

By Read Lock Status command, data of Lock Status can be read. As for this command, set CSB to Low, then input address after Instruction Code of Read Lock Status command. Input address bit A10 as "1", other address bits A12 to A0 as "0". Data output is started from SCK fall of 23 clock, and from D7 to D0 sequentially. The data D0 indicates Lock Status bit. The data D7 to D1 are Don't Care. This IC has increment read function. After output of data for 1 byte (8bits), by continuing input of SCK, this IC repeats to output data of the Lock Status byte. In case of Lock Status (LS) bit "1", ID Page is locked, Write ID Page command can't be executed. In case of LS bit "0", ID Page is released to lock, Write ID Page command can be executed.

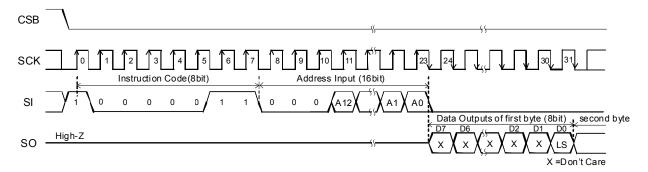


Figure 47. Read Lock Status Command

## (10) Lock ID Page Command (LID)

By Lock ID Page command, data of Lock Status can be written. In case of Lock Status (LS) bit "1", Lock ID Page command can't be executed permanently. As for this command, set CSB to Low, then input address and data after Instruction Code of Lock ID Page command. Input address bit A10 as "1", other address bits A12 to A0 as "0". The data D1 is for LS bit, other data bits are Don't Care. Then, by making CSB to High, the IC starts write operation. To start write operation, set CSB Low to High after taking the last data (D0), and before the next SCK clock starts. At other timing, Lock ID Page command is not executed, and this Lock ID Page command is cancelled. The write time of EEPROM requires time of  $t_{\rm EW}$  (Max 4ms).

During write operation, other than Read Status Register command is not accepted.

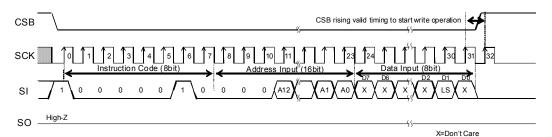


Figure 48. Lock ID Page Command

## At Standby State

## 1. Standby Current

Set CSB = High, and be sure to set SCK, SI, WPB and HOLDB inputs = Low or High. Do not input intermediate electric potential.

#### 2. Timing

As shown in Figure.49, at standby, when SCK is High, even if CSB is fallen, SI status is not read at fall edge. SI status is read at SCK rise edge after fall of CSB. At standby and at power ON/OFF, set CSB = High status.

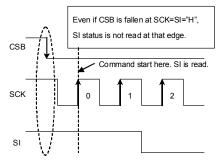


Figure 49. Operating Timing

#### Method to cancel each command

- 1. READ, RDID, RDLS
- · Method to cancel: cancel by CSB = High

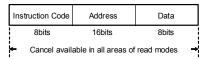


Figure 50. READ, RDID, RDLS Cancel Valid Timing

#### 2. RDSR

Method to cancel: cancel by CSB = High

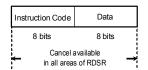


Figure 51. RDSR Cancel Valid Timing

#### 3. WRITE, WRID, LID

- a : Instruction Code, Address Input Area Cancellation is available by CSB = High.
- b : Data Input Area (D7 to D1 input area) Cancellation is available by CSB = High.
- c : Data Input Area (D0 area)
   When CSB is started, write starts.
   After CSB rise, cancellation cannot be made by any means.

# d: t<sub>E/W</sub> Area Cancellation is available by CSB = High. However, when write starts (CSB is started) in the area c, cancellation cannot be made by any means. And by inputting on SCK clock, cancellation cannot be made. In page write mode, there is write enable area at every 8 clocks

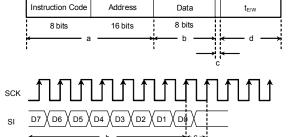


Figure 52. WRITE, WRID, LID Cancel Valid Timing

- Note 1) If V<sub>CC</sub> is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.
- Note 2) If CSB is started at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to fall in SCK = Low area. As for SCK rise, assure timing of tcss / tcsh or higher.

#### 4. WRSR

- a : From Instruction code to 15th rising of SCK Cancel by CSB = High.
- b : From 15th rising of SCK to 16th rising of SCK (write enable area) When CSB is started, write starts.
- c: After 16th rising of SCK
  Cancel by CSB = High.
  However, when write starts (CSB is started) in the area b, cancellation cannot be made by any means.
  And, by inputting on SCK clock, cancellation cannot be made.

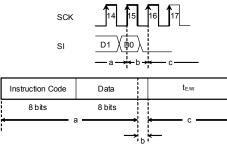


Figure 53. WRSR Cancel Valid Timing

- Note 1) If V<sub>CC</sub> is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.
- Note 2) If CSB is started at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to fall in SCK = Low area. As for SCK rise, assure timing of toss / tosh or higher.

## 5. WREN/WRDI

- a : From instruction code to 7th rising of SCK Cancel by CSB = High.
- b : Cancellation is not available when CSB is started after 7th clock.

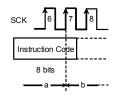


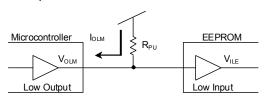
Figure 54. WREN/WRDI Cancel Valid Timing

#### High speed operation

In order to realize stable high speed operations, pay attention to the following input / output pin conditions.

1. Pull Up, Pull Down Resistance for Input Pins
When to attach pull up, pull down resistance to EEPROM input pins, select an appropriate value for the microcontroller V<sub>OL</sub>, I<sub>OL</sub> from V<sub>IL</sub> characteristics of this IC.

## 2. Pull Up Resistance



V<sub>ILE</sub> : V<sub>IL</sub> specifications of EEPROM
 V<sub>OLM</sub> : V<sub>OL</sub> specifications of Microcontroller

• Iolm : Iol specifications of Microcontroller

Figure 55. Pull Up Resistance

$$R_{PU} \ge \frac{V_{CC} - V_{OLM}}{I_{OLM}}$$
 ... ①
 $V_{OLM} \le V_{ILE}$  ... ②

Example) When Vcc=5V,  $V_{ILE}$ =1.5V,  $V_{OLM}$ =0.4V,  $I_{OLM}$ =2mA, from the equation ①.

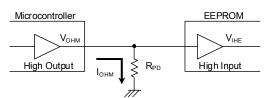
$$R_{PU} \ge \frac{5 - 0.4}{2 \times 10^{-3}}$$

$$\therefore R_{PU} \leq 2.3 \ \lceil k\Omega \rceil$$

With the value of R<sub>PU</sub> to satisfy the above equation,  $V_{OLM}$  becomes 0.4V or lower, and with  $V_{ILE}$  (=1.5V), the equation ② is also satisfied.

And, in order to prevent malfunction, mistake write at power ON/OFF, be sure to make CSB pull up.

#### 3. Pull Down Resistance



V<sub>IHE</sub> : V<sub>IH</sub> specifications of EEPROMV<sub>OH</sub> specifications of Microcontroller

• I<sub>OHM</sub> : I<sub>OH</sub> specifications of Microcontroller

$$R_{PD} \ge \frac{V_{OHM}}{I_{OHM}}$$
 ... 3

Example) When  $V_{CC}$ =5V,  $V_{OHM}$ = $V_{CC}$ -0.5V,  $I_{OHM}$ =0.4mA,  $V_{IHE}$ = $V_{CC}$ ×0.7V, from the equation ③,

$$RPD \ge \frac{5 - 0.5}{0.4 \times 10^{-3}}$$

$$\therefore R_{PU} \ge 11.3 \quad [k\Omega]$$

Further, by amplitude  $V_{\text{IHE}}$ ,  $V_{\text{ILE}}$  of signal input to EEPROM, operation speed changes. By inputting signal of amplitude of Vcc / GND level to input, more stable high speed operations can be realized. On the contrary, when amplitude of 0.8Vcc / 0.2Vcc is input, operation speed becomes slow. (Note1)

In order to realize more stable high speed operation, it is recommended to make the values of R<sub>PU</sub>, R<sub>PD</sub> as large as possible, and make the amplitude of signal input to EEPROM close to the amplitude of Vcc / GND level. (Note1) At this moment, operating timing guaranteed value is guaranteed.

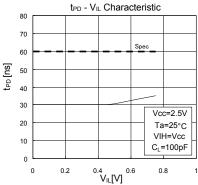


Figure 57. VIL dependency of Data Output Delay Time tPD

#### 4. SO Load Capacitance Condition

Load capacitance of SO Pin affects upon delay characteristic of SO output. (Data Output Delay Time, Time from HOLDB to High-Z) In order to make output delay characteristic into higher speed, make SO load capacitance small. In concrete, "Do not connect many devices to SO bus", "Make the wire between the controller and EEPROM short", and so forth.

## 5. Other cautions

Make the wire length from the Microcontroller to EEPROM input signal same length, in order to prevent setup / hold violation to EEPROM, owing to difference of wire length of each input.

## I/O Equivalence Circuit

## 1. Output Circuit

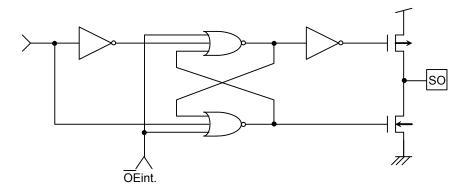


Figure 58. SO Output Equivalent Circuit

## 2. Input Circuit

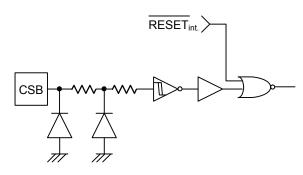


Figure 59. CSB Input Equivalent Circuit

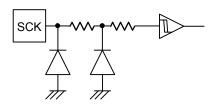


Figure 60. SCK Input Equivalent Circuit

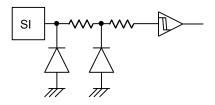


Figure 61. SI Input Equivalent Circuit

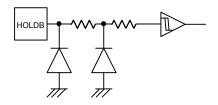


Figure 62. HOLDB Input Equivalent Circuit

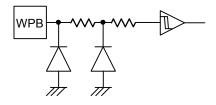


Figure 63. WPB Input Equivalent Circuit

#### Power-Up/Down conditions

## 1. At power ON/OFF, set CSB = High (=Vcc).

When CSB is Low, this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, mistake write or so. To prevent these, at power ON, set CSB = High. (When CSB is in High status, all inputs are canceled.)

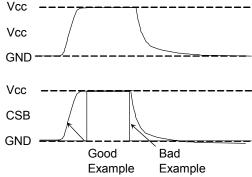


Figure 64. CSB Timing at power ON / OFF

## (Good example) CSB Pin is pulled up to Vcc.

At power OFF, take 10ms or higher before supply. If power is turned on without observing this condition, the IC internal circuit may not be reset, which please note.

## (Bad example) CSB Pin is Low at power ON/OFF.

In this case, CSB always becomes Low (active status), and EEPROM may have malfunction, mistake write owing to noises and the likes.

Even when CSB input is High-Z, the status becomes like this case, which please note.

#### 2. POR Circuit

This IC has a POR (Power On Reset) circuit as mistake write countermeasure. After POR, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. When power is ON, if the recommended conditions of the following tR, tOFF, and Vbot are not satisfied, it may become write enable status owing to noises and the likes.

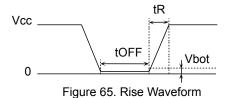


Table 11. Recommended conditions of tR, tOFF, Vbot

tR	tR tOFF		
10ms or below	10ms or higher	0.3V or below	
100ms or below	10ms or higher	0.2V or below	

## 3. LVCC Circuit

LVCC (VCC-Lockout) circuit prevents data rewrite operation at low supply voltage, and prevents wrong write. At LVCC voltage (Typ. =1.9V) or below, it prevent data rewrite.

#### Noise countermeasures

#### 1. Vcc Noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a bypass capacitor (over 0.1µF) between IC Vcc and GND. At that moment, attach it as close to IC as possible. And, it is also recommended to attach a bypass capacitor between board Vcc and GND.

#### 2. SCK Noise

When the rise time ( $t_{RC}$ ) of SCK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SCK input. The hysteresis width of this circuit is set about 0.2V, if noises exist at SCK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time ( $t_{RC}$ ) of SCK 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

#### 3. WPB Noise

During execution of Write Status Register command, if there exist noises on WPB pin, mistake in recognition may occur and forcible cancellation may result, which please note. To avoid this, a Schmitt trigger circuit is built in WPB input. In the same manner, a Schmitt trigger circuit is built in CSB input, SI input and HOLDB input too.

## **Operational Notes**

## 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

## 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

#### 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

#### 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

## 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

#### 6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

## 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

## 8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

#### 9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

#### 10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

## **Operational Notes - continued**

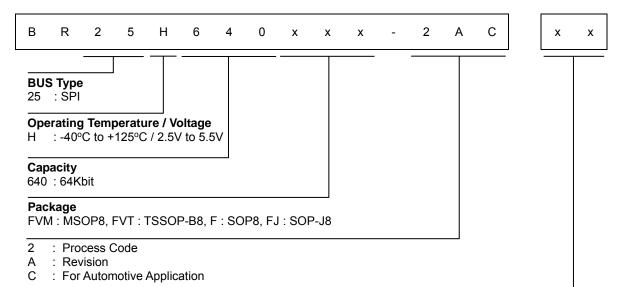
## 11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

## 12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

## **Part Numbering**



## **Packaging and Forming Specification**

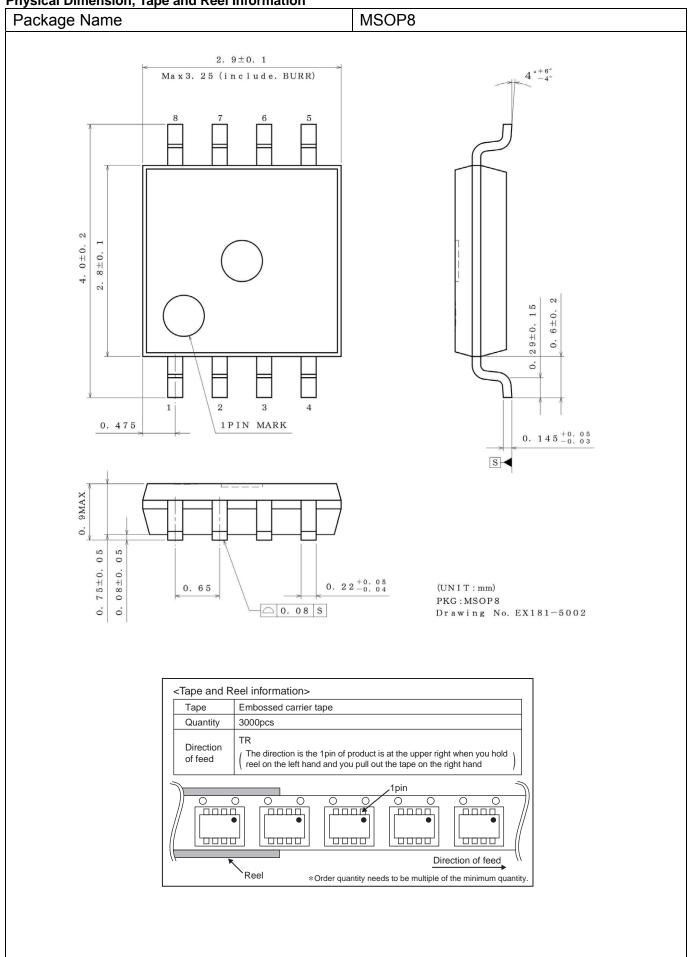
E2 : Embossed tape and reel

TR : Embossed tape and reel (MSOP8 package only)

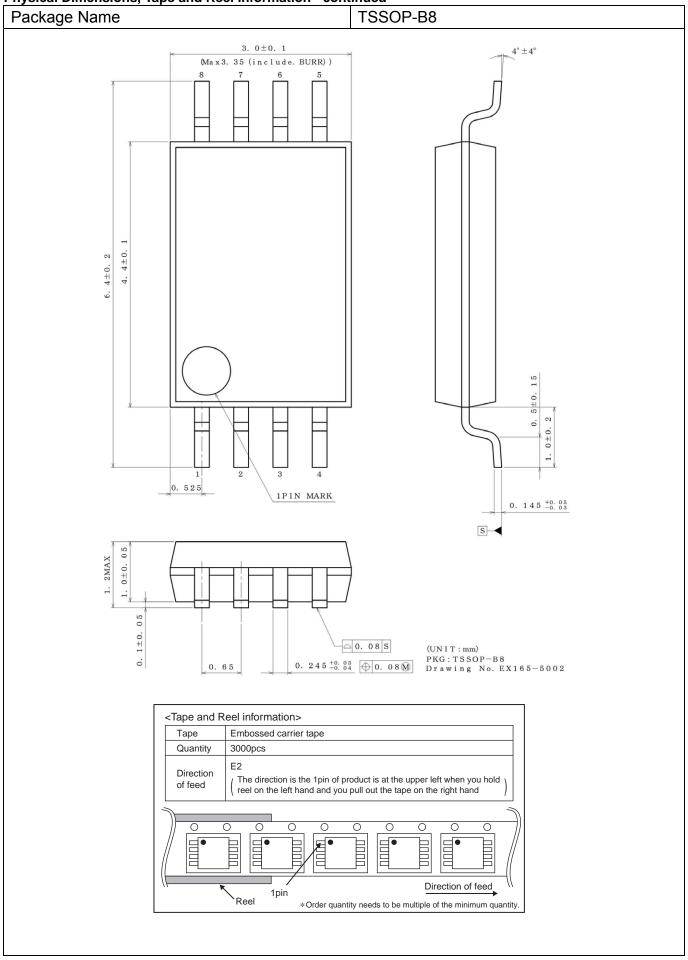
## Lineup

0	Pacl	kage	Orderable Part Number		
Capacity	Type Quantity		Orderable Part Number		
	MSOP8	Reel of 3000	BR25H640FVM	-2ACTR	
64Kbit	TSSOP-B8	Reel of 3000	BR25H640FVT	-2ACE2	
04NDIL	SOP8	Reel of 2500	BR25H640F	-2ACE2	
	SOP-J8	Reel of 2500	BR25H640FJ	-2ACE2	

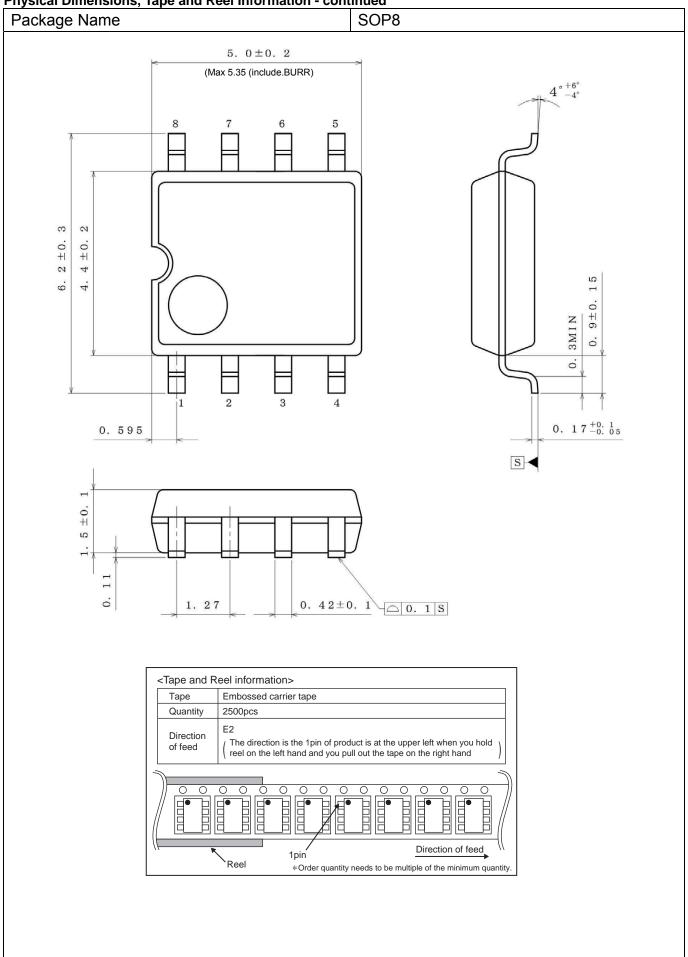
**Physical Dimension, Tape and Reel Information** 

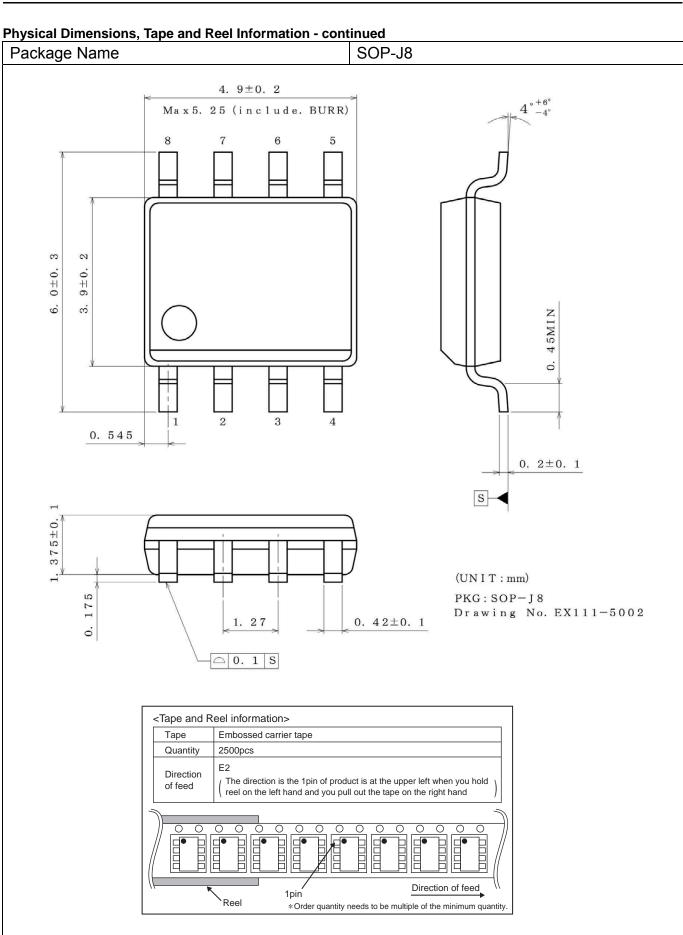


Physical Dimensions, Tape and Reel Information - continued

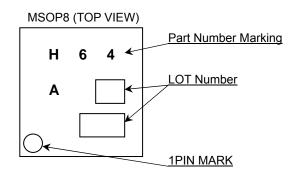


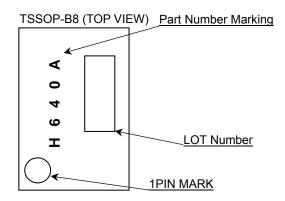
Physical Dimensions, Tape and Reel Information - continued

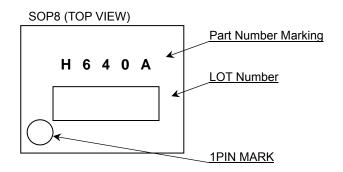


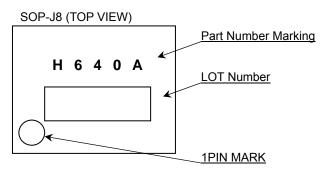


## **Marking Diagrams (TOP VIEW)**









## **Revision History**

Date	Revision	Changes				
01.Oct.2014	001	New Release				
16.Feb.2016	002	P4 Indicated Limit of t <sub>FO</sub> . P19 Modified Sentence in (4) Write Command. P20 Modified Figure 42				

# **Notice**

## **Precaution on using ROHM Products**

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

Ī	JAPAN	USA	EU	CHINA
ĺ	CLASSⅢ	CLACCIII	CLASS II b	СГУССШ
Ī	CLASSIV	CLASSⅢ	CLASSⅢ	CLASSⅢ

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  - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
  - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
  - [f] Sealing or coating our Products with resin or other coating materials
  - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - [h] Use of the Products in places subject to dew condensation
- 4. The Products are not subject to radiation-proof design.
- 5. Please verify and confirm characteristics of the final or mounted products in using the Products.
- 6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- 7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- 8. Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

- 1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- 2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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- 1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of lonizer, friction prevention and temperature / humidity control).

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- 1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
- Even under ROHM recommended storage condition, solderability of products out of recommended storage time period
  may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is
  exceeding the recommended storage time period.
- 3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
- 4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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