

## 7 x 17 Dots Matrix LED Driver LSI

### FEATURES

- 7 x 17 LED Matrix Driver  
(Total LED that can be driven = 119)
- Internal memory RAM (2-side)
- LDO (1-ch.)
- I<sup>2</sup>C interface + SPI interface
- 50 pin Wafer Level Chip Size Package (WLCSP)

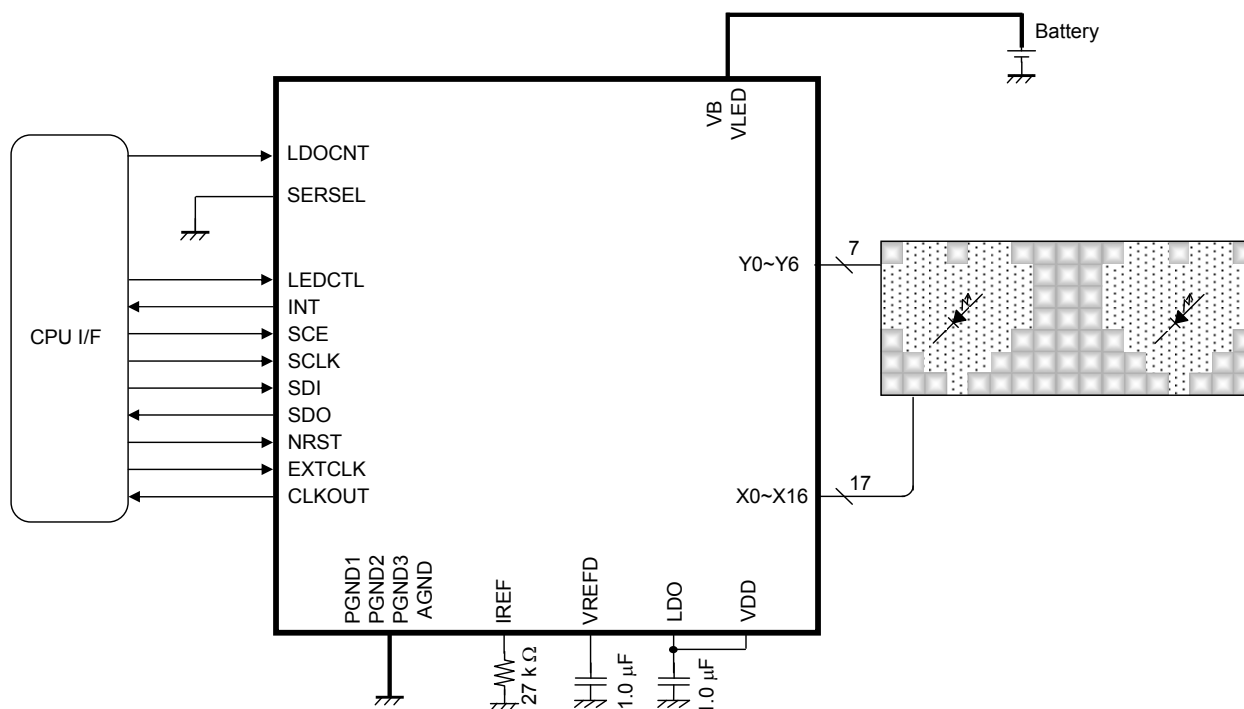
### DESCRIPTION

AN32054B is a 7 x 17 LED Matrix Driver equipped with RAM.

### APPLICATIONS

- Mobile Phone
- Smart Phone
- PCs
- Game Consoles
- Home Appliances etc.

### TYPICAL APPLICATION



Note)

The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

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**ABSOLUTE MAXIMUM RATINGS**

| Parameter                      | Symbol  | Rating        | Unit | Note |
|--------------------------------|---|---------------|------|------|
| Supply voltage                 | VDD <sub>MAX</sub>  | 4.3           | V    | *1   |
|                                | VB <sub>MAX</sub>   | 6.0           | V    | *1   |
|                                | VLED <sub>MAX</sub>   | 6.5           | V    | *1   |
| Operating ambience temperature | T <sub>opr</sub>  | -30 to + 85   | °C   | *2   |
| Operating junction temperature | T <sub>j</sub>  | - 30 to + 125 | °C   | *2   |
| Storage temperature            | T <sub>stg</sub>  | - 55 to + 125 | °C   | *2   |
| Input Voltage Range            | NRST, SCLK, SDI   | - 0.3 to 4.3  | V    | —    |
|                                | SERSEL, EXTCLK,<br>LDOCNT, SCE, LEDCTL  | - 0.3 to 6.0  | V    | —    |
| Output Voltage Range           | SDO, CLKOUT, INT  | - 0.3 to 4.3  | V    | —    |
|                                | LDO   | - 0.3 to 6.0  | V    | —    |
|                                | X0, X1, X2, X3, X4, X5,<br>X6, X7, X8, X9, X10, X11,<br>X12, X13, X14, X15, X16<br>Y0, Y1, Y2, Y3, Y4, Y5, Y6 | - 0.3 to 6.5  | V    | —    |
| ESD                            | HBM   | 1.5 to 2.0    | kV   | —    |

Note) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

\*1: VB<sub>MAX</sub> = VB, VDD<sub>MAX</sub> = VDD, VLED<sub>MAX</sub> = VLED, the values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

\*2: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T<sub>a</sub> = 25°C.

**POWER DISSIPATION RATING**

| PACKAGE                                      | θ <sub>JA</sub> | P <sub>D</sub> (Ta=25 °C) | P <sub>D</sub> (Ta=85 °C) |
|--|-----------------|---------------------------|---------------------------|
| 50 pin Wafer Level Chip Size Package (WLCSP) | 107.3 °C /W     | 0.932 W                   | 0.373 W                   |

Note) For the actual usage, please refer to the P<sub>D</sub>-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.



**CAUTION**

Although this LSI has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

**RECOMMENDED OPERATING CONDITIONS**

| Parameter            | Symbol  | Min.  | Typ. | Max.       | Unit | Note |
|----------------------|---|-------|------|------------|------|------|
| Supply voltage range | VDD   | 1.7   | 1.85 | 3.5        | V    | *1   |
|                      | VB  | 3.1   | 3.7  | 4.6        | V    | *1   |
|                      | VLED  | 3.1   | 5.0  | 5.6        | V    | *1   |
| Input Voltage Range  | NRST, SCLK, SDI   | - 0.3 | —    | VDD + 0.3  | V    | *2   |
|                      | SERSEL, EXTCLK,<br>LDOCNT, SCE, LEDCTL  | - 0.3 | —    | VB + 0.3   | V    | *2   |
| Output Voltage Range | SDO, CLKOUT, INT  | - 0.3 | —    | VDD + 0.3  | V    | *2   |
|                      | LDO   | - 0.3 | —    | VB + 0.3   | V    | *2   |
|                      | X0, X1, X2, X3, X4, X5,<br>X6, X7, X8, X9, X10, X11,<br>X12, X13, X14, X15, X16<br>Y0, Y1, Y2, Y3, Y4, Y5, Y6 | - 0.3 | —    | VLED + 0.3 | V    | *2   |

Note) \*1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

Do not apply external currents and voltages to any pin not specifically mentioned.

Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND, PGND1, PGND2 and PGND3.

VDD is voltage for VDD. VB is voltage for VB. VLED is voltage for VLED.

\*2: ( VDD + 0.3 ) V must not exceed 4.3 V. ( VB + 0.3 ) V must not exceed 6 V.

( VLED + 0.3 ) V must not exceed 6.5 V.

**ELECTRICAL CHARACTERISTICS**

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) Ta = 25 °C ± 2 °C unless otherwise specified.

| Parameter                                   | Symbol | Condition  | Limits |      |                         | Unit | Note |
|---|--------|--|--------|------|-------------------------|------|------|
|   |        |  | Min    | Typ  | Max                     |      |      |
| <b>Current consumption</b>                  |        |  |        |      |                         |      |      |
| Current consumption (1)<br>Off mode         | ICC1   | LDOCNT = Low   | —      | 0    | 1                       | μA   | —    |
| Current consumption (2)<br>Normal mode      | ICC2   | LDOCNT = High<br>ILOAD = 0 μA  | —      | 14   | 20                      | μA   | —    |
| <b>Reference voltage source</b>             |        |  |        |      |                         |      |      |
| Output voltage                              | VREF   | I <sub>VREF</sub> = 0 μA   | 1.21   | 1.24 | 1.27                    | V    | —    |
| <b>Reference current source</b>             |        |  |        |      |                         |      |      |
| Output voltage                              | VIREF  | Connect the register of 39 kΩ<br>between IREF and GND.<br>I <sub>IREF</sub> = 0 μA | 0.2    | 0.3  | 0.4                     | V    | —    |
| <b>EXTCLK, NRST, LDOCNT, SERSEL, LEDCTL</b> |        |  |        |      |                         |      |      |
| High-level input voltage range              | VIH1   | High-level recognition voltage of<br>EXTCLK, NRST, LDOCNT,<br>SERSEL, LEDCTL       | 1.4    | —    | V <sub>B</sub><br>+ 0.3 | V    | —    |
| Low-level input voltage range               | VIL1   | Low-level recognition voltage of<br>EXTCLK, NRST, LDOCNT,<br>SERSEL, LEDCTL        | −0.3   | —    | 0.4                     | V    | —    |
| High-level input current                    | IIH1   | V <sub>EXTCLK, NRST, LDOCNT, SERSEL, LEDCTL</sub><br>= 1.85 V                      | —      | 0    | 1                       | μA   | —    |
| Low-level input current                     | IIL1   | V <sub>EXTCLK, NRST, LDOCNT, SERSEL, LEDCTL</sub><br>= 0 V                         | —      | 0    | 1                       | μA   | —    |

**ELECTRICAL CHARACTERISTICS (continued)**

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T<sub>a</sub> = 25 °C ± 2 °C unless otherwise specified.

| Parameter                      | Symbol           | Condition   | Limits    |     |                          | Unit | Note |
|--------------------------------|------------------|---|-----------|-----|--------------------------|------|------|
|                                |                  |   | Min       | Typ | Max                      |      |      |
| <b>SCE, SCLK, SDI</b>          |                  |   |           |     |                          |      |      |
| High-level input voltage range | VIH2             | High-level recognition voltage of SCE, SCLK, SDI            | 0.7 × VDD | —   | VDD <sub>max</sub> + 0.5 | V    | —    |
| Low-level input voltage range  | VIL2             | Low-level recognition voltage of SCE, SCLK, SDI             | -0.5      | —   | 0.3 × VDD                | V    | —    |
| High-level input current       | I <sub>IH2</sub> | V <sub>SCE, SCLK, SDI</sub> = 1.85 V                        | —         | 0   | 1                        | μA   | —    |
| Low-level input current        | I <sub>IL2</sub> | V <sub>SCE, SCLK, SDI</sub> = 0 V                           | —         | 0   | 1                        | μA   | —    |
| Low-level output voltage (1)   | VOL1             | I <sub>SDI</sub> = 3 mA, VDD > 2 V, VOL1 = V <sub>SDI</sub> | 0         | —   | 0.4                      | V    | —    |
| Low-level output voltage (2)   | VOL2             | I <sub>SDI</sub> = 3 mA, VDD < 2 V, VOL2 = V <sub>SDI</sub> | 0         | —   | 0.2 × VDD                | V    | —    |
| <b>SDO, INT, CLKOUT</b>        |                  |   |           |     |                          |      |      |
| High-level output voltage      | VOH1             | I <sub>SDO, INT, CLKOUT</sub> = -2 mA                       | VDD × 0.8 | —   | —                        | V    | —    |
| Low-level output voltage       | VOL3             | I <sub>SDO, INT, CLKOUT</sub> = 2 mA                        | —         | —   | VDD × 0.2                | V    | —    |

**ELECTRICAL CHARACTERISTICS (continued)**

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T<sub>a</sub> = 25 °C ± 2 °C unless otherwise specified.

| Parameter                                 | Symbol | Condition   | Limits |       |       | Unit | Note  |
|---|--------|---|--------|-------|-------|------|-------|
|   |        |   | Min    | Typ   | Max   |      |       |
| <b>Current generator (for matrix LED)</b> |        |   |        |       |       |      |       |
| Output current (1)                        | IMX1   | At 1.333 mA setup<br>V <sub>X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16</sub> = 1 V<br>IMX1 = I <sub>X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16</sub>      | 1.226  | 1.333 | 1.440 | mA   | *1, 2 |
| Output current (2)                        | IMX2   | At 2.666 mA setup<br>V <sub>X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16</sub> = 1 V<br>IMX2 = I <sub>X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16</sub>      | 2.452  | 2.666 | 2.879 | mA   | *1, 2 |
| Output current (3)                        | IMX4   | At 5.332 mA setup<br>V <sub>X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16</sub> = 1 V<br>IMX4 = I <sub>X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16</sub>      | 4.905  | 5.332 | 5.759 | mA   | *1, 2 |
| Output current (4)                        | IMX8   | At 10.66 mA setup<br>V <sub>X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16</sub> = 1 V<br>IMX8 = I <sub>X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16</sub>      | 9.81   | 10.66 | 11.52 | mA   | *1, 2 |
| Output current (5)                        | IMX15  | At 20.00 mA setup<br>V <sub>X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16</sub> = 1 V<br>IMX15 = I <sub>X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16</sub>     | 18.40  | 20.00 | 21.60 | mA   | *1, 2 |
| Leak current at the time of OFF           | IMXOFF | Current OFF setup<br>V <sub>X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16</sub> = 4.75 V<br>IMXOFF = I <sub>X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16</sub> | —      | —     | 1     | μA   | —     |
| The error between channels                | IMXCH  | Difference current between the average of all channels and each channel.  | - 5    | —     | 5     | %    | *2    |

Note) \*1: Values when recommended parts (ERJ2RHD393X) are used for IREF pin. The other current settings are combination of above items.

\*2: All of the setting values of matrix block are with absolute accuracy of ± 8 %, the error between channels of ± 5 %.

**ELECTRICAL CHARACTERISTICS (continued)**

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) Ta = 25 °C ± 2 °C unless otherwise specified.

| Parameter                        | Symbol | Condition  | Limits |      |      | Unit | Note |
|----------------------------------|--------|--|--------|------|------|------|------|
|                                  |        |  | Min    | Typ  | Max  |      |      |
| <b>SCAN Switch</b>               |        |  |        |      |      |      |      |
| Resistance at the switch ON      | RSCAN  | $I_{Y0, Y1, Y2, Y3, Y4, Y5, Y6} = -5 \text{ mA}$<br>RSCAN<br>$= V_{Y0, Y1, Y2, Y3, Y4, Y5, Y6} / 5 \text{ mA}$                     | —      | 1    | 2    | Ω    | —    |
| <b>Voltage regulator ( LDO)</b>  |        |  |        |      |      |      |      |
| Output voltage                   | VL1    | $I_{LDO} = -30 \text{ mA}$   | 1.79   | 1.85 | 1.91 | V    | —    |
| Short current protection current | IPT1   | LDOCNT = High<br>REG18 = [1]<br>$V_{LDO} = 0 \text{ V}$  | 50     | 100  | 200  | mA   | —    |
| Ripple rejection ratio (1)       | PSL11  | $V_B = 3.6 \text{ V} + 0.2 \text{ V[p-p]}$<br>$f = 1 \text{ kHz}$<br>$I_{LDO} = -15 \text{ mA}$<br>$PSL11 = 20\log(acVP31 / 0.2)$  | —      | -45  | -40  | dB   | —    |
| Ripple rejection ratio (2)       | PSL12  | $V_B = 3.6 \text{ V} + 0.2 \text{ V[p-p]}$<br>$f = 10 \text{ kHz}$<br>$I_{LDO} = -15 \text{ mA}$<br>$PSL12 = 20\log(acVP31 / 0.2)$ | —      | -35  | -25  | dB   | —    |
| <b>Oscillation circuit</b>       |        |  |        |      |      |      |      |
| Oscillation frequency            | FOSC   | OSCEN = [1]  | 0.96   | 1.2  | 1.44 | MHz  | —    |



**ELECTRICAL CHARACTERISTICS (continued)**

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

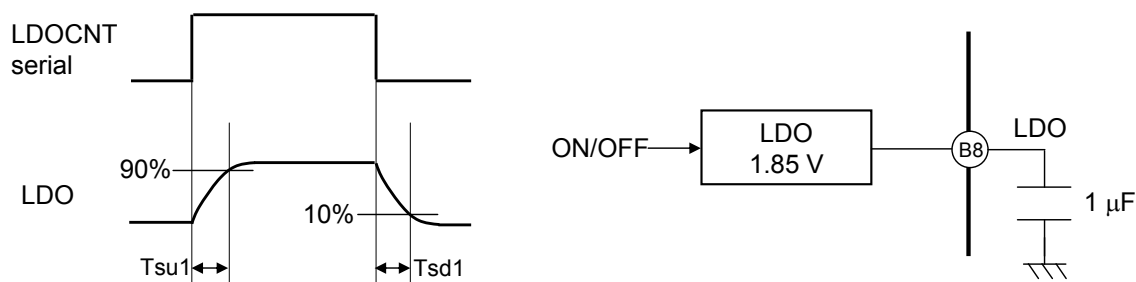
Note)  $T_a = 25\text{ }^\circ\text{C} \pm 2\text{ }^\circ\text{C}$  unless otherwise specified.

| Parameter  | Symbol | Condition  | Limits |      |     | Unit | Note     |
|--|--------|--|--------|------|-----|------|----------|
|  |        |  | Min    | Typ  | Max |      |          |
| <b>TSD (Thermal shutdown circuit)</b>  |        |  |        |      |     |      |          |
| Detection temperature  | Tdet   | Temperature which LDO, Constant current circuit, and Matrix SW turn off.             | —      | 160  | —   | °C   | *3<br>*5 |
| Return temperature   | Tsd11  | Returning temperature  | —      | 110  | —   | °C   | *4<br>*5 |
| <b>Voltage regulator (LDO) Output capacitor 1 <math>\mu\text{F}</math>, Output capacitor's ESR less than 0.1 <math>\Omega</math></b> |        |  |        |      |     |      |          |
| Rise time  | Tsu1   | Time until output voltage reaches 0 V to 90%   | —      | 0.25 | —   | ms   | *5       |
| Fall time  | Tsd1   | Time until output voltage reaches 10%.   | —      | 5    | —   | ms   | *5       |
| Maximum load current   | IOMAX1 | —  | —      | 15   | —   | mA   | *5       |
| Load transient response (1)  | Vtr11  | $I_{LDO} = -50\text{ mA}$<br>$\rightarrow -15\text{ }\mu\text{A}$ (1 $\mu\text{s}$ ) | —      | 70   | —   | mV   | *5       |
| Load transient response (2)  | Vtr12  | $I_{LDO} = -15\text{ mA}$<br>$\rightarrow -50\text{ }\mu\text{A}$ (1 $\mu\text{s}$ ) | —      | 70   | —   | mV   | *5       |

Note) \*3: LDO, Constant current circuit, and Matrix SW are turned off when TSD operates.

\*4: Only LDO returns after ON state of TSD. A logic part will be in Reset state.

\*5: Typical design value.



**ELECTRICAL CHARACTERISTICS (continued)**

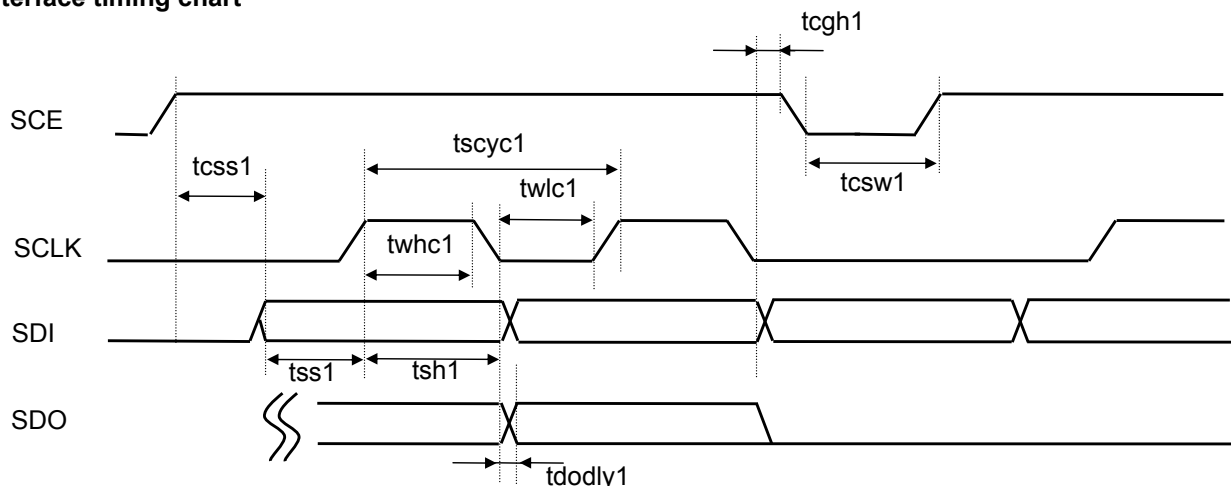
VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) Ta = 25 °C ± 2 °C unless otherwise specified.

| Parameter   | Symbol | Condition      | Limits |     |     | Unit | Note |
|---|--------|----------------|--------|-----|-----|------|------|
|   |        |                | Min    | Typ | Max |      |      |
| <b>Microcomputer interface characteristics (VDD = 1.85 V ± 3 %) Write access timing</b> |        |                |        |     |     |      |      |
| SCLK cycle time   | tscyc1 | —              | —      | 125 | —   | ns   | *5   |
| SCLK cycle time High period   | twhc1  | —              | —      | 60  | —   | ns   | *5   |
| SCLK cycle time Low period  | twlc1  | —              | —      | 60  | —   | ns   | *5   |
| Serial-data setup time  | tss1   | —              | —      | 62  | —   | ns   | *5   |
| Serial-data hold time   | tsh1   | —              | —      | 62  | —   | ns   | *5   |
| Transceiver interval  | tcs1   | —              | —      | 62  | —   | ns   | *5   |
| Chip enable setup time  | tc1    | —              | —      | 5   | —   | ns   | *5   |
| Chip enable hold time   | tch1   | —              | —      | 5   | —   | ns   | *5   |
| <b>Microcomputer interface characteristics (VDD = 1.85 V ± 3 %) Read access timing</b>  |        |                |        |     |     |      |      |
| SCLK cycle time   | tscyc1 | —              | —      | 333 | —   | ns   | *5   |
| SCLK cycle time High period   | twhc1  | —              | —      | 160 | —   | ns   | *5   |
| SCLK cycle time Low period  | twlc1  | —              | —      | 160 | —   | ns   | *5   |
| Serial-data setup time  | tss1   | —              | —      | 125 | —   | ns   | *5   |
| Serial-data hold time   | tsh1   | —              | —      | 125 | —   | ns   | *5   |
| Transceiver interval  | tcs1   | —              | —      | 125 | —   | ns   | *5   |
| Chip enable setup time  | tc1    | —              | —      | 5   | —   | ns   | *5   |
| Chip enable hold time   | tch1   | —              | —      | 5   | —   | ns   | *5   |
| DC delay time   | td1    | Only read mode | —      | 100 | —   | ns   | *5   |

Note) \*5: Typical design value

**Interface timing chart**



**ELECTRICAL CHARACTERISTICS (continued)**

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) Ta = 25 °C ± 2 °C unless otherwise specified.

| Parameter   | Symbol | Condition   | Limits     |     |     | Unit | Note     |
|---|--------|---|------------|-----|-----|------|----------|
|   |        |   | Min        | Typ | Max |      |          |
| <b>I<sup>2</sup>C I/F</b>                             |        |   |            |     |     |      |          |
| Input voltage hysteresis(1)                           | Vhys1  | Hysteresis voltages of Pad No.37, 38<br>VDD > 2 V | 0.05 × VDD | —   | —   | mV   | *6<br>*7 |
| Input voltage hysteresis(2)                           | Vhys2  | Hysteresis voltages of Pad No.37, 38<br>VDD < 2 V | 0.1 × VDD  | —   | —   | mV   | *6<br>*7 |
| Output fall time                                      | Tof    | Bus's capacitance<br>10 pF to 400 pF<br>Ip < 6 mA | 20 + 0.1Cb | —   | 250 | ns   | *6<br>*7 |
| Pulse width of the spike oppressed by an input filter | Tsp    | —   | 0          | —   | 50  | ns   | *6<br>*7 |
| I/O pin's capacitance                                 | Ci     | Bus's capacitance<br>10 pF to 400 pF              | —          | —   | 10  | pF   | *6<br>*7 |

Note) \*6: The timing of Fast-mode and Normal mode devices in I<sup>2</sup>C-bus is specified in Page.13. All values referred to V<sub>IHMIN</sub> and V<sub>ILMAX</sub> level.

\*7: These are values checked by design but not production tested.

**ELECTRICAL CHARACTERISTICS (continued)**

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) Ta = 25 °C ± 2 °C unless otherwise specified.

| Parameter  | Symbol              | Condition  | Limits     |     |     | Unit | Note     |
|--|---------------------|--|------------|-----|-----|------|----------|
|  |                     |  | Min        | Typ | Max |      |          |
| <b>I<sup>2</sup>C I/F (continued)</b>                    |                     |  |            |     |     |      |          |
| Hold period (repeat)                                     | t <sub>HD:STA</sub> | The first clock pulse is generated after t <sub>HD:STA</sub> . | 0.6        | —   | —   | μs   | *6<br>*7 |
| SCLK clock Low period                                    | t <sub>LOW</sub>    | —  | 1.3        | —   | —   | μs   | *6<br>*7 |
| SCLK clock High period                                   | t <sub>HIGH</sub>   | —  | 0.6        | —   | —   | μs   | *6<br>*7 |
| Repeated start condition setup time                      | t <sub>SU:STA</sub> | —  | 0.6        | —   | —   | μs   | *6<br>*7 |
| Data hold time   | t <sub>HD:DAT</sub> | —  | 0          | —   | 0.9 | μs   | *6<br>*7 |
| Data setup time  | t <sub>SU:DAT</sub> | —  | 100        | —   | —   | ns   | *6<br>*7 |
| Rise time of both SDA and SCL signals                    | tr                  | —  | 20 + 0.1Cb | —   | 300 | ns   | *6<br>*7 |
| Fall time of both SDA and SCL signals                    | t <sub>f</sub>      | —  | 20 + 0.1Cb | —   | 300 | ns   | *6<br>*7 |
| STOP condition setup time                                | t <sub>SU:STO</sub> | —  | 0.6        | —   | —   | μs   | *6<br>*7 |
| Bus free time between STOP condition and START condition | t <sub>BUF</sub>    | —  | 1.3        | —   | —   | μs   | *6<br>*7 |
| Bus line capacitive load                                 | C <sub>b</sub>      | —  | —          | —   | 400 | pF   | *6<br>*7 |
| Low-level noise margin of the connected device           | V <sub>aL</sub>     | —  | 0.1 × VDD  | —   | —   | V    | *6<br>*7 |
| High-level noise margin of the connected device          | V <sub>aH</sub>     | —  | 0.2 × VDD  | —   | —   | V    | *6<br>*7 |

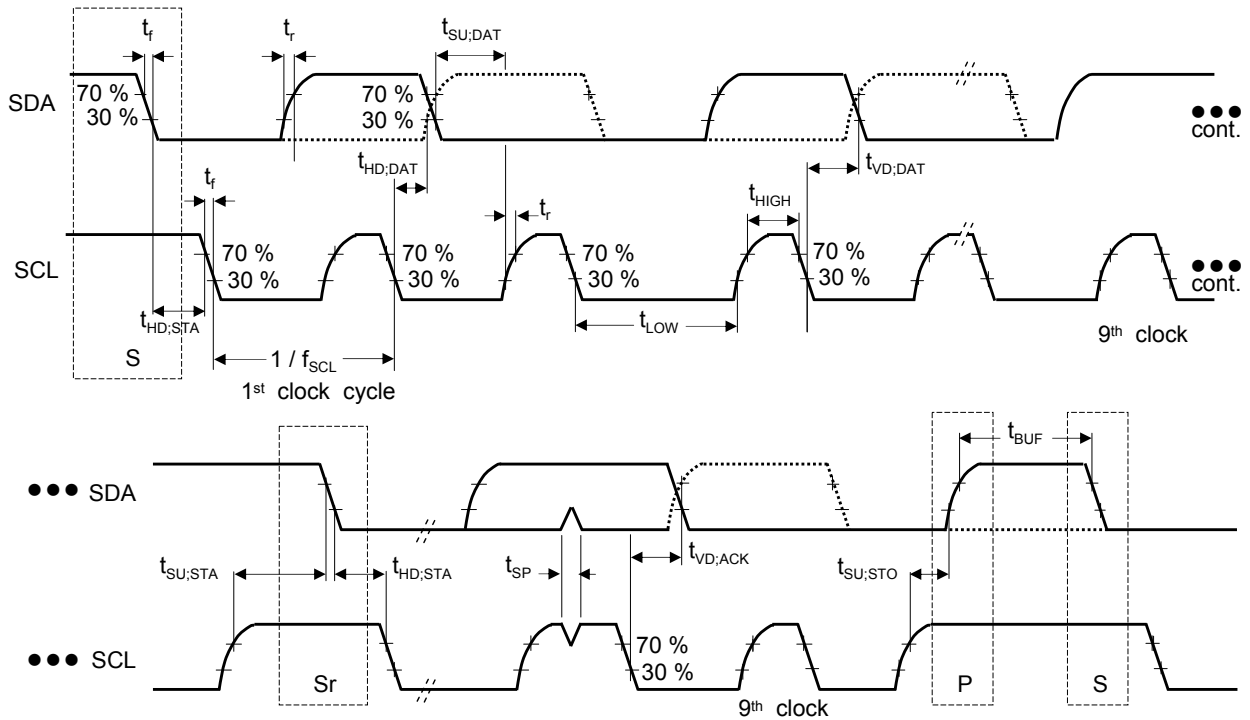
Note) \*6: The timing of Fast-mode and Normal mode devices in I<sup>2</sup>C-bus is specified in Page.13. All values referred to V<sub>IHMIN</sub> and V<sub>ILMAX</sub> level.

\*7: These are values checked by design but not production tested.

**ELECTRICAL CHARACTERISTICS (continued)**

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) Ta = 25 °C ± 2 °C unless otherwise specified.



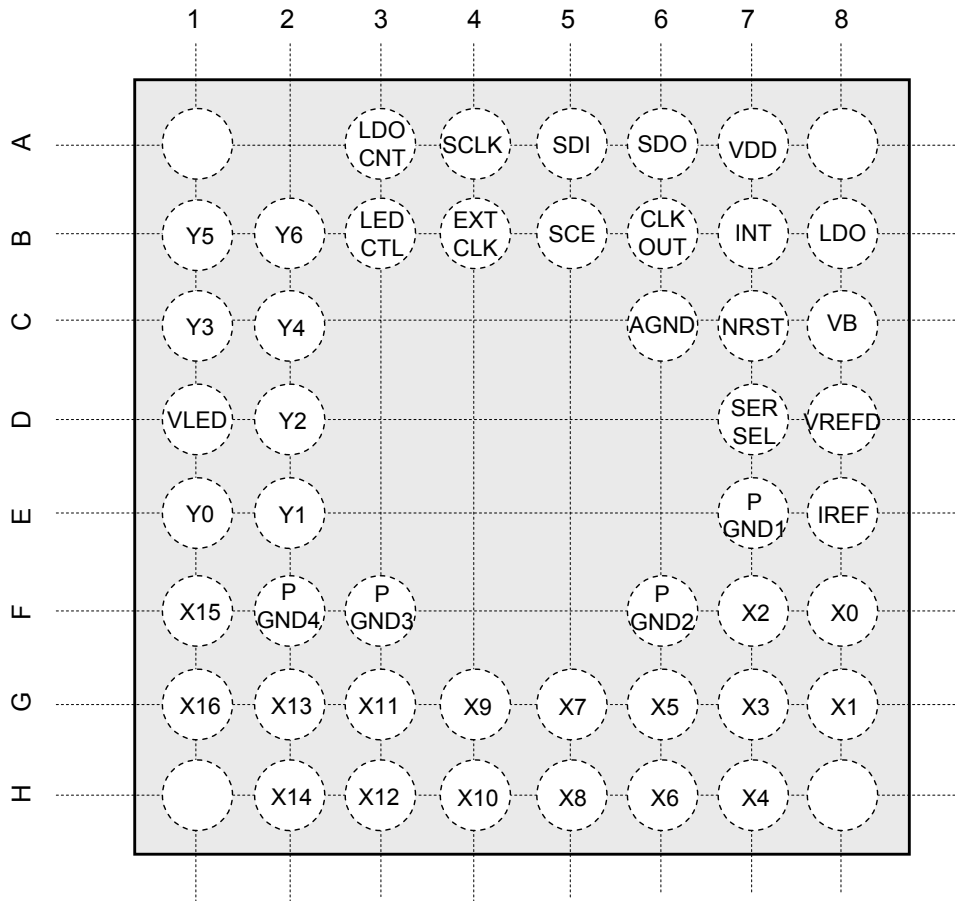
$V_{ILMAX} = 0.3 V_{DD}$

$V_{IHMIN} = 0.7 V_{DD}$

- S : START condition
- Sr : Repeat START condition
- P : STOP condition

**PIN CONFIGURATION**

TOP VIEW



**PIN FUNCTIONS**

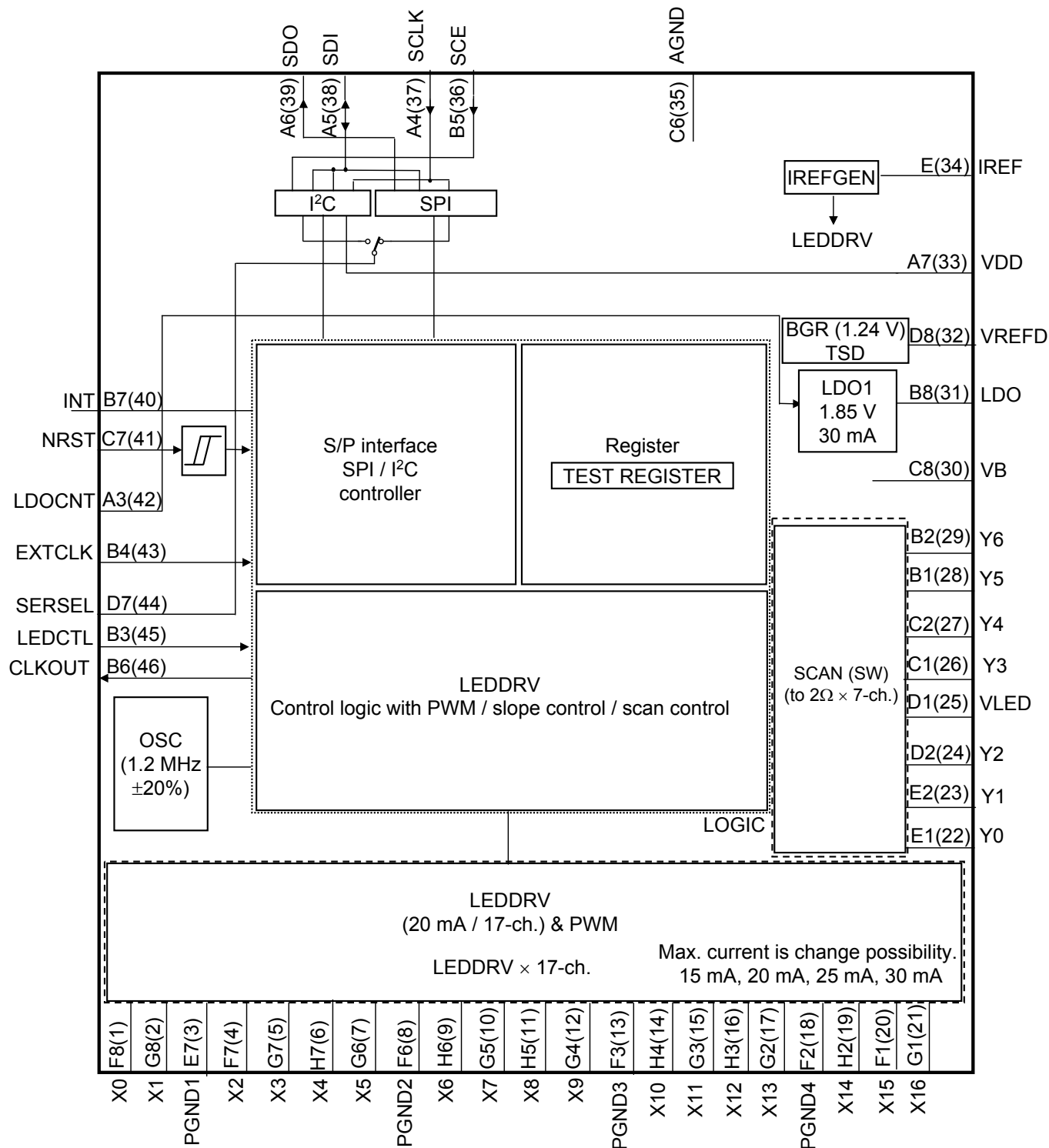
| Pin No.                            | Pin name                         | Type   | Description   |
|------------------------------------|----------------------------------|--------|---|
| F8(1)                              | X0                               | Output | The output pin of PWM control with constant current circuit. It connects with A column of matrix LED. |
| G8(2)                              | X1                               | Output | The output pin of PWM control with constant current circuit. It connects with B column of matrix LED. |
| E7(3)<br>F6(8)<br>F3(13)<br>F2(18) | PGND1<br>PGND2<br>PGND3<br>PGND4 | Ground | GND for matrix LED  |
| F7(4)                              | X2                               | Output | The output pin of PWM control with constant current circuit. It connects with C column of matrix LED. |
| G7(5)                              | X3                               | Output | The output pin of PWM control with constant current circuit. It connects with D column of matrix LED. |
| H7(6)                              | X4                               | Output | The output pin of PWM control with constant current circuit. It connects with E column of matrix LED. |
| G6(7)                              | X5                               | Output | The output pin of PWM control with constant current circuit. It connects with F column of matrix LED. |
| H6(9)                              | X6                               | Output | The output pin of PWM control with constant current circuit. It connects with G column of matrix LED. |
| G5(10)                             | X7                               | Output | The output pin of PWM control with constant current circuit. It connects with H column of matrix LED. |
| H5(11)                             | X8                               | Output | The output pin of PWM control with constant current circuit. It connects with I column of matrix LED. |
| G4(12)                             | X9                               | Output | The output pin of PWM control with constant current circuit. It connects with J column of matrix LED. |
| H4(14)                             | X10                              | Output | The output pin of PWM control with constant current circuit. It connects with K column of matrix LED. |
| G3(15)                             | X11                              | Output | The output pin of PWM control with constant current circuit. It connects with L column of matrix LED. |
| H3(16)                             | X12                              | Output | The output pin of PWM control with constant current circuit. It connects with M column of matrix LED. |
| G2(17)                             | X13                              | Output | The output pin of PWM control with constant current circuit. It connects with N column of matrix LED. |
| H2(19)                             | X14                              | Output | The output pin of PWM control with constant current circuit. It connects with O column of matrix LED. |
| F1(20)                             | X15                              | Output | The output pin of PWM control with constant current circuit. It connects with P column of matrix LED. |
| G1(21)                             | X16                              | Output | The output pin of PWM control with constant current circuit. It connects with Q column of matrix LED. |

**PIN FUNCTIONS (Continued)**

| Pin No. | Pin name | Type           | Description   |
|---------|----------|----------------|---|
| E1(22)  | Y0       | Output         | The output pin of PWM control with constant current circuit. It connects with the 1st row of matrix LED.  |
| E2(23)  | Y1       | Output         | The output pin of PWM control with constant current circuit. It connects with the 2nd row of matrix LED.  |
| D2(24)  | Y2       | Output         | The output pin of PWM control with constant current circuit. It connects with the 3rd row of matrix LED.  |
| D1(25)  | VLED     | Power supply   | Power supply's connect pin for matrix LED<br>Connect with the output of battery or step-up converter to supply sufficient LED voltage.            |
| C1(26)  | Y3       | Output         | The output pin of PWM control with constant current circuit. It connects with the 4th row of matrix LED.  |
| C2(27)  | Y4       | Output         | The output pin of PWM control with constant current circuit. It connects with the 5th row of matrix LED.  |
| B1(28)  | Y5       | Output         | The output pin of PWM control with constant current circuit. It connects with the 6th row of matrix LED.  |
| B2(29)  | Y6       | Output         | The output pin of PWM control with constant current circuit. It connects with the 7th row of matrix LED.  |
| C8(30)  | VB       | Power supply   | Power supply's connect pin for BGR circuit and LDO circuit  |
| B8(31)  | LDO      | Output         | Power supply output pin for the internal serial interface input block and internal logic  |
| D8(32)  | VREFD    | Output         | Band Gap Reference circuit output pin   |
| A7(33)  | VDD      | Power supply   | Power supply's connect pin for interface output   |
| E8(34)  | IREF     | Output         | Resistor connection pin to set up the internal reference constant current   |
| C6(35)  | AGND     | Ground         | GND pin for Analog circuit  |
| B5(36)  | SCE      | Input          | SPI interface chip-enable pin (High active)<br>(Slave address selection control pin in I <sup>2</sup> C mode)                                     |
| A4(37)  | SCLK     | Input          | Common clock input pin in both SPI interface and I <sup>2</sup> C interface   |
| A5(38)  | SDI      | Input / Output | Data input pin for SPI interface<br>Data input/output pin for I <sup>2</sup> C interface  |
| A6(39)  | SDO      | Output         | Data output pin for SPI interface   |
| B7(40)  | INT      | Output         | Interrupt signal output pin to notify IC condition to CPU   |
| C7(41)  | NRST     | Input          | Reset input pin (Low active)  |
| A3(42)  | LDOCNT   | Input          | LDO ON/OFF control pin  |
| B4(43)  | EXTCLK   | Input          | External clock input pin<br>This clock can be used as the reference clock for this IC instead of the internal clock.                              |
| D7(44)  | SERSEL   | Input          | SPI, I <sup>2</sup> C interface selection pin   |
| B3(45)  | LEDCTL   | Input          | External synchronous signal input pin<br>This signal can control LED on/off with the internal register setting.                                   |
| B6(46)  | CLKOUT   | Output         | Internal clock output pin<br>This clock can be used as the reference clock for another AN32054B when more than 2 ICs are used in the application. |



**FUNCTIONAL BLOCK DIAGRAM**



Note) This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

**OPERATION**

**1. Power supply sequence control**

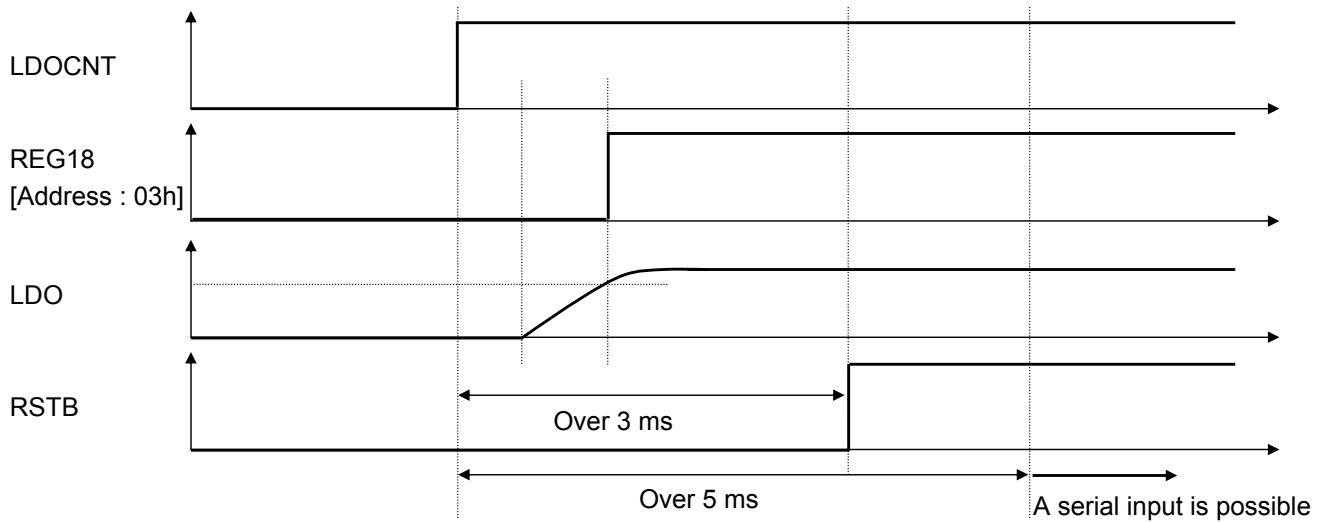
Power supply on/off sequence

| Mode                       | LDOCNT        | REG18 | Note  |
|----------------------------|---------------|-------|---|
| OFF                        | Low           | 0     | <ul style="list-style-type: none"> <li>It is necessary to make it LDOCNT = High for the return from OFF-mode.</li> </ul>  |
| OFF<br>→<br>Normal<br>Mode | Low →<br>High | 0/1   | <ul style="list-style-type: none"> <li>The signal from serial interface is not received in LDOCNT = Low and the state of REG18 = [0]</li> </ul>   |
|                            | High          | 0/1   |   |
| OFF<br>→<br>Normal<br>mode | High →<br>Low | 0     | <ul style="list-style-type: none"> <li>Regardless of the value of REG18, LDO turns on at LDOCNT = High.</li> <li>Serial interface signal is not received at RSTB = Low</li> <li>After more than 5 ms from LDOCNT = High, the IC can recognize the serial interface signal.</li> <li>To activate RSTB, RSTB should be kept low for more than one internal clock period.</li> <li>RSTB terminal prohibits the input signal of those other than a rectangle wave.</li> <li>All register setting become default setting once RSTB = Low.<br/>(The default setting of REG18 is [1].<br/>If RSTB = Low before LDOCNT = Low, LDO can't turn off. )</li> <li>All register setting become default setting when LDO turns off.</li> <li>The correct setting order to set off mode is as following.<br/>REG18 = [0] → LDOCNT = Low → RSTB = Low</li> </ul> |

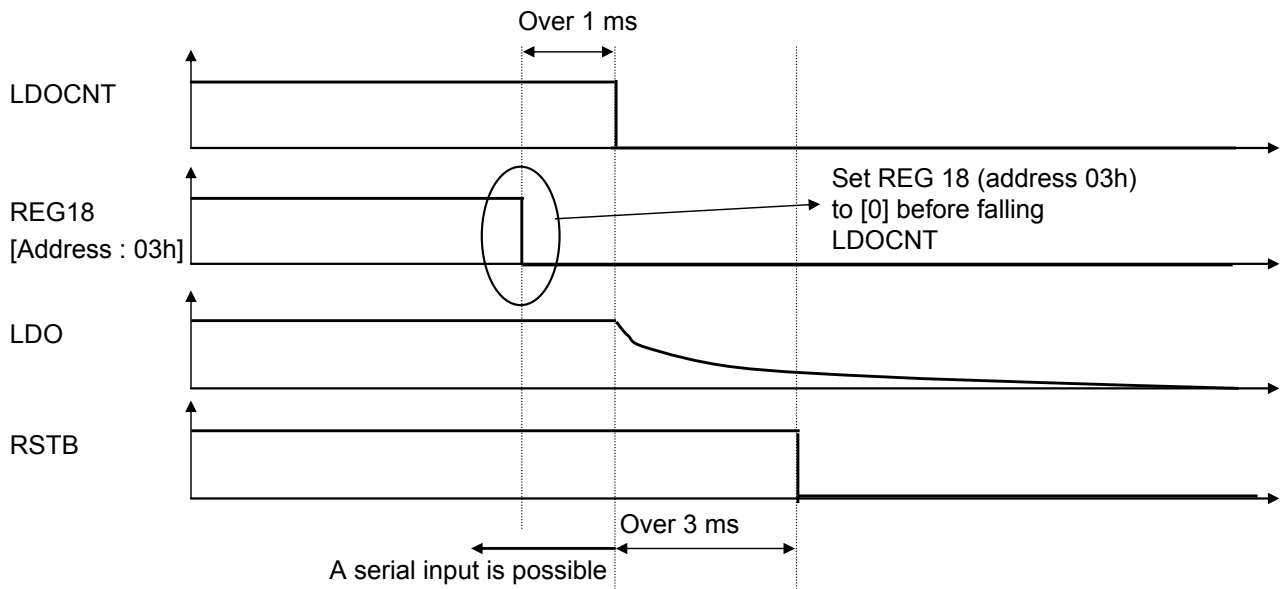
**OPERATION (continued)**

**1. Power supply sequence control (continued)**

Shift to Normal mode from OFF-mode



Shift to OFF-mode from Normal mode



**OPERATION (continued)**

**2. Register Map (1)**

| Sub Address | R/W | Data name | DATA   |        |      |       |      |              |           |              |
|-------------|-----|-----------|--------|--------|------|-------|------|--------------|-----------|--------------|
|             |     |           | D7     | D6     | D5   | D4    | D3   | D2           | D1        | D0           |
| 01h         | R/W | MAPCHG    | —      | —      | —    | —     | —    | —            | —         | MAPCHG<br>*1 |
| 02h         | R/W | POWERCNT  | —      | —      | —    | —     | —    | —            | —         | OSCEN        |
| 03h         | R/W | LDOCNT    | —      | —      | —    | —     | —    | —            | —         | REG18        |
| 04h         | R   | TEST0     | TEST0  |        |      |       |      |              |           |              |
| 05h         | R   | INT       | —      | —      | —    | —     | —    | —            | RAMACT    | FRMINT       |
| 06h         | R/W | OPTION    | LEDACT | DISMTX | —    | —     | —    | —            | CLKOUT    | EXTCLK       |
| 07h         | R/W | MTXON     | —      | —      | —    | —     | —    | —            | —         | MTXON        |
| 08h         | R/W | MTXDATA   | —      | —      | —    | —     | —    | —            | MTXDATA   |              |
| 09h         | R/W | RAMRST    | —      | —      | —    | —     | —    | —            | RAM1      | RAM2         |
| 0Ah         | R/W | SCROLL    | —      | —      | —    | —     | —    | —            | —         | SCOLON       |
| 0Bh         | R/W | SCLMODE   | —      | UP     | DOWN | RIGHT | LEFT | SCLTIME[2:0] |           |              |
| 0Dh         | R/W | RESET     | —      | —      | —    | —     | —    | —            | —         | SRST         |
| 10h         | R/W | XCONST1   | X16    | X15    | X14  | X13   | X12  | X11          | X10       | X9           |
| 11h         | R/W | XCONST2   | X8     | X7     | X6   | X5    | X4   | X3           | X2        | X1           |
| 12h         | R/W | XCONST3   | —      | —      | —    | —     | —    | —            | —         | X0           |
| 13h         | R/W | IMAX      | —      | —      | —    | —     | —    | —            | IMAX[1:0] |              |
| 20h         | R/W | TEST1     | TEST1  |        |      |       |      |              |           |              |
| :           | :   | :         | :      |        |      |       |      |              |           |              |
| :           | :   | :         | :      |        |      |       |      |              |           |              |
| 36h         | R/W | TEST22    | TEST22 |        |      |       |      |              |           |              |
| 40h         | R/W | TEST23    | TEST23 |        |      |       |      |              |           |              |
| 41h         | R/W | TEST24    | TEST24 |        |      |       |      |              |           |              |

Note) Access the address from 20h to 41h is prohibited.

\*1: When 01h D0 is set to "0", Register Map (1) is selected, when 01h D0 is set to "1", Register Map (2) is selected.

**OPERATION (continued)**

**2. Register Map (2)**

| Sub Address | R/W | Data name | DATA      |    |    |    |           |    |           |        |
|-------------|-----|-----------|-----------|----|----|----|-----------|----|-----------|--------|
|             |     |           | D7        | D6 | D5 | D4 | D3        | D2 | D1        | D0     |
| 02h         | R/W | RAMNUM    | —         | —  | —  | —  | —         | —  | —         | RAMNUM |
| 03h         | R/W | A1        | BLA1[3:0] |    |    |    | FRA1[1:0] |    | DLA1[1:0] |        |
| 04h         | R/W | A2        | BLA2[3:0] |    |    |    | FRA2[1:0] |    | DLA2[1:0] |        |
| 05h         | R/W | A3        | BLA3[3:0] |    |    |    | FRA3[1:0] |    | DLA3[1:0] |        |
| 06h         | R/W | A4        | BLA4[3:0] |    |    |    | FRA4[1:0] |    | DLA4[1:0] |        |
| 07h         | R/W | A5        | BLA5[3:0] |    |    |    | FRA5[1:0] |    | DLA5[1:0] |        |
| 08h         | R/W | A6        | BLA6[3:0] |    |    |    | FRA6[1:0] |    | DLA6[1:0] |        |
| 09h         | R/W | A7        | BLA7[3:0] |    |    |    | FRA7[1:0] |    | DLA7[1:0] |        |
| 0Ah         | R/W | B1        | BLB1[3:0] |    |    |    | FRB1[1:0] |    | DLB1[1:0] |        |
| 0Bh         | R/W | B2        | BLB2[3:0] |    |    |    | FRB2[1:0] |    | DLB2[1:0] |        |
| 0Ch         | R/W | B3        | BLB3[3:0] |    |    |    | FRB3[1:0] |    | DLB3[1:0] |        |
| 0Dh         | R/W | B4        | BLB4[3:0] |    |    |    | FRB4[1:0] |    | DLB4[1:0] |        |
| 0Eh         | R/W | B5        | BLB5[3:0] |    |    |    | FRB5[1:0] |    | DLB5[1:0] |        |
| 0Fh         | R/W | B6        | BLB6[3:0] |    |    |    | FRB6[1:0] |    | DLB6[1:0] |        |
| 10h         | R/W | B7        | BLB7[3:0] |    |    |    | FRB7[1:0] |    | DLB7[1:0] |        |
| 11h         | R/W | C1        | BLC1[3:0] |    |    |    | FRC1[1:0] |    | DLC1[1:0] |        |
| 12h         | R/W | C2        | BLC2[3:0] |    |    |    | FRC2[1:0] |    | DLC2[1:0] |        |
| 13h         | R/W | C3        | BLC3[3:0] |    |    |    | FRC3[1:0] |    | DLC3[1:0] |        |
| 14h         | R/W | C4        | BLC4[3:0] |    |    |    | FRC4[1:0] |    | DLC4[1:0] |        |
| 15h         | R/W | C5        | BLC5[3:0] |    |    |    | FRC5[1:0] |    | DLC5[1:0] |        |
| 16h         | R/W | C6        | BLC6[3:0] |    |    |    | FRC6[1:0] |    | DLC6[1:0] |        |
| 17h         | R/W | C7        | BLC7[3:0] |    |    |    | FRC7[1:0] |    | DLC7[1:0] |        |
| 18h         | R/W | D1        | BLD1[3:0] |    |    |    | FRD1[1:0] |    | DLD1[1:0] |        |
| 19h         | R/W | D2        | BLD2[3:0] |    |    |    | FRD2[1:0] |    | DLD2[1:0] |        |
| 1Ah         | R/W | D3        | BLD3[3:0] |    |    |    | FRD3[1:0] |    | DLD3[1:0] |        |
| 1Bh         | R/W | D4        | BLD4[3:0] |    |    |    | FRD4[1:0] |    | DLD4[1:0] |        |
| 1Ch         | R/W | D5        | BLD5[3:0] |    |    |    | FRD5[1:0] |    | DLD5[1:0] |        |
| 1Dh         | R/W | D6        | BLD6[3:0] |    |    |    | FRD6[1:0] |    | DLD6[1:0] |        |
| 1Eh         | R/W | D7        | BLD7[3:0] |    |    |    | FRD7[1:0] |    | DLD7[1:0] |        |
| 1Fh         | R/W | E1        | BLE1[3:0] |    |    |    | FRE1[1:0] |    | DLE1[1:0] |        |
| 20h         | R/W | E2        | BLE2[3:0] |    |    |    | FRE2[1:0] |    | DLE2[1:0] |        |
| 21h         | R/W | E3        | BLE3[3:0] |    |    |    | FRE3[1:0] |    | DLE3[1:0] |        |
| 22h         | R/W | E4        | BLE4[3:0] |    |    |    | FRE4[1:0] |    | DLE4[1:0] |        |
| 23h         | R/W | E5        | BLE5[3:0] |    |    |    | FRE5[1:0] |    | DLE5[1:0] |        |
| 24h         | R/W | E6        | BLE6[3:0] |    |    |    | FRE6[1:0] |    | DLE6[1:0] |        |
| 25h         | R/W | E7        | BLE7[3:0] |    |    |    | FRE7[1:0] |    | DLE7[1:0] |        |

**OPERATION (continued)**

**2. Register Map (2) (continued)**

| Sub Address | R/W | Data name | DATA      |    |    |    |           |    |           |    |
|-------------|-----|-----------|-----------|----|----|----|-----------|----|-----------|----|
|             |     |           | D7        | D6 | D5 | D4 | D3        | D2 | D1        | D0 |
| 26h         | R/W | F1        | BLF1[3:0] |    |    |    | FRF1[1:0] |    | DLF1[1:0] |    |
| 27h         | R/W | F2        | BLF2[3:0] |    |    |    | FRF2[1:0] |    | DLF2[1:0] |    |
| 28h         | R/W | F3        | BLF3[3:0] |    |    |    | FRF3[1:0] |    | DLF3[1:0] |    |
| 29h         | R/W | F4        | BLF4[3:0] |    |    |    | FRF4[1:0] |    | DLF4[1:0] |    |
| 2Ah         | R/W | F5        | BLF5[3:0] |    |    |    | FRF5[1:0] |    | DLF5[1:0] |    |
| 2Bh         | R/W | F6        | BLF6[3:0] |    |    |    | FRF6[1:0] |    | DLF6[1:0] |    |
| 2Ch         | R/W | F7        | BLF7[3:0] |    |    |    | FRF7[1:0] |    | DLF7[1:0] |    |
| 2Dh         | R/W | G1        | BLG1[3:0] |    |    |    | FRG1[1:0] |    | DLG1[1:0] |    |
| 2Eh         | R/W | G2        | BLG2[3:0] |    |    |    | FRG2[1:0] |    | DLG2[1:0] |    |
| 2Fh         | R/W | G3        | BLG3[3:0] |    |    |    | FRG3[1:0] |    | DLG3[1:0] |    |
| 30h         | R/W | G4        | BLG4[3:0] |    |    |    | FRG4[1:0] |    | DLG4[1:0] |    |
| 31h         | R/W | G5        | BLG5[3:0] |    |    |    | FRG5[1:0] |    | DLG5[1:0] |    |
| 32h         | R/W | G6        | BLG6[3:0] |    |    |    | FRG6[1:0] |    | DLG6[1:0] |    |
| 33h         | R/W | G7        | BLG7[3:0] |    |    |    | FRG7[1:0] |    | DLG7[1:0] |    |
| 34h         | R/W | H1        | BLH1[3:0] |    |    |    | FRH1[1:0] |    | DLH1[1:0] |    |
| 35h         | R/W | H2        | BLH2[3:0] |    |    |    | FRH2[1:0] |    | DLH2[1:0] |    |
| 36h         | R/W | H3        | BLH3[3:0] |    |    |    | FRH3[1:0] |    | DLH3[1:0] |    |
| 37h         | R/W | H4        | BLH4[3:0] |    |    |    | FRH4[1:0] |    | DLH4[1:0] |    |
| 38h         | R/W | H5        | BLH5[3:0] |    |    |    | FRH5[1:0] |    | DLH5[1:0] |    |
| 39h         | R/W | H6        | BLH6[3:0] |    |    |    | FRH6[1:0] |    | DLH6[1:0] |    |
| 3Ah         | R/W | H7        | BLH7[3:0] |    |    |    | FRH7[1:0] |    | DLH7[1:0] |    |
| 3Bh         | R/W | I1        | BLI1[3:0] |    |    |    | FRI1[1:0] |    | DLI1[1:0] |    |
| 3Ch         | R/W | I2        | BLI2[3:0] |    |    |    | FRI2[1:0] |    | DLI2[1:0] |    |
| 3Dh         | R/W | I3        | BLI3[3:0] |    |    |    | FRI3[1:0] |    | DLI3[1:0] |    |
| 3Eh         | R/W | I4        | BLI4[3:0] |    |    |    | FRI4[1:0] |    | DLI4[1:0] |    |
| 3Fh         | R/W | I5        | BLI5[3:0] |    |    |    | FRI5[1:0] |    | DLI5[1:0] |    |
| 40h         | R/W | I6        | BLI6[3:0] |    |    |    | FRI6[1:0] |    | DLI6[1:0] |    |
| 41h         | R/W | I7        | BLI7[3:0] |    |    |    | FRI7[1:0] |    | DLI7[1:0] |    |
| 42h         | R/W | J1        | BLJ1[3:0] |    |    |    | FRJ1[1:0] |    | DLJ1[1:0] |    |
| 43h         | R/W | J2        | BLJ2[3:0] |    |    |    | FRJ2[1:0] |    | DLJ2[1:0] |    |
| 44h         | R/W | J3        | BLJ3[3:0] |    |    |    | FRJ3[1:0] |    | DLJ3[1:0] |    |
| 45h         | R/W | J4        | BLJ4[3:0] |    |    |    | FRJ4[1:0] |    | DLJ4[1:0] |    |
| 46h         | R/W | J5        | BLJ5[3:0] |    |    |    | FRJ5[1:0] |    | DLJ5[1:0] |    |
| 47h         | R/W | J6        | BLJ6[3:0] |    |    |    | FRJ6[1:0] |    | DLJ6[1:0] |    |
| 48h         | R/W | J7        | BLJ7[3:0] |    |    |    | FRJ7[1:0] |    | DLJ7[1:0] |    |

**OPERATION (continued)**

**2. Register Map (2) (continued)**

| Sub Address | R/W | Data name | DATA      |    |    |           |    |           |    |    |
|-------------|-----|-----------|-----------|----|----|-----------|----|-----------|----|----|
|             |     |           | D7        | D6 | D5 | D4        | D3 | D2        | D1 | D0 |
| 49h         | R/W | K1        | BLK1[3:0] |    |    | FRK1[1:0] |    | DLK1[1:0] |    |    |
| 4Ah         | R/W | K2        | BLK2[3:0] |    |    | FRK2[1:0] |    | DLK2[1:0] |    |    |
| 4Bh         | R/W | K3        | BLK3[3:0] |    |    | FRK3[1:0] |    | DLK3[1:0] |    |    |
| 4Ch         | R/W | K4        | BLK4[3:0] |    |    | FRK4[1:0] |    | DLK4[1:0] |    |    |
| 4Dh         | R/W | K5        | BLK5[3:0] |    |    | FRK5[1:0] |    | DLK5[1:0] |    |    |
| 4Eh         | R/W | K6        | BLK6[3:0] |    |    | FRK6[1:0] |    | DLK6[1:0] |    |    |
| 4Fh         | R/W | K7        | BLK7[3:0] |    |    | FRK7[1:0] |    | DLK7[1:0] |    |    |
| 50h         | R/W | L1        | BLL1[3:0] |    |    | FRL1[1:0] |    | DLL1[1:0] |    |    |
| 51h         | R/W | L2        | BLL2[3:0] |    |    | FRL2[1:0] |    | DLL2[1:0] |    |    |
| 52h         | R/W | L3        | BLL3[3:0] |    |    | FRL3[1:0] |    | DLL3[1:0] |    |    |
| 53h         | R/W | L4        | BLL4[3:0] |    |    | FRL4[1:0] |    | DLL4[1:0] |    |    |
| 54h         | R/W | L5        | BLL5[3:0] |    |    | FRL5[1:0] |    | DLL5[1:0] |    |    |
| 55h         | R/W | L6        | BLL6[3:0] |    |    | FRL6[1:0] |    | DLL6[1:0] |    |    |
| 56h         | R/W | L7        | BLL7[3:0] |    |    | FRL7[1:0] |    | DLL7[1:0] |    |    |
| 57h         | R/W | M1        | BLM1[3:0] |    |    | FRM1[1:0] |    | DLM1[1:0] |    |    |
| 58h         | R/W | M2        | BLM2[3:0] |    |    | FRM2[1:0] |    | DLM2[1:0] |    |    |
| 59h         | R/W | M3        | BLM3[3:0] |    |    | FRM3[1:0] |    | DLM3[1:0] |    |    |
| 5Ah         | R/W | M4        | BLM4[3:0] |    |    | FRM4[1:0] |    | DLM4[1:0] |    |    |
| 5Bh         | R/W | M5        | BLM5[3:0] |    |    | FRM5[1:0] |    | DLM5[1:0] |    |    |
| 5Ch         | R/W | M6        | BLM6[3:0] |    |    | FRM6[1:0] |    | DLM6[1:0] |    |    |
| 5Dh         | R/W | M7        | BLM7[3:0] |    |    | FRM7[1:0] |    | DLM7[1:0] |    |    |
| 5Eh         | R/W | N1        | BLN1[3:0] |    |    | FRN1[1:0] |    | DLN1[1:0] |    |    |
| 5Fh         | R/W | N2        | BLN2[3:0] |    |    | FRN2[1:0] |    | DLN2[1:0] |    |    |
| 60h         | R/W | N3        | BLN3[3:0] |    |    | FRN3[1:0] |    | DLN3[1:0] |    |    |
| 61h         | R/W | N4        | BLN4[3:0] |    |    | FRN4[1:0] |    | DLN4[1:0] |    |    |
| 62h         | R/W | N5        | BLN5[3:0] |    |    | FRN5[1:0] |    | DLN5[1:0] |    |    |
| 63h         | R/W | N6        | BLN6[3:0] |    |    | FRN6[1:0] |    | DLN6[1:0] |    |    |
| 64h         | R/W | N7        | BLN7[3:0] |    |    | FRN7[1:0] |    | DLN7[1:0] |    |    |
| 65h         | R/W | O1        | BLO1[3:0] |    |    | FRO1[1:0] |    | DLO1[1:0] |    |    |
| 66h         | R/W | O2        | BLO2[3:0] |    |    | FRO2[1:0] |    | DLO2[1:0] |    |    |
| 67h         | R/W | O3        | BLO3[3:0] |    |    | FRO3[1:0] |    | DLO3[1:0] |    |    |
| 68h         | R/W | O4        | BLO4[3:0] |    |    | FRO4[1:0] |    | DLO4[1:0] |    |    |
| 69h         | R/W | O5        | BLO5[3:0] |    |    | FRO5[1:0] |    | DLO5[1:0] |    |    |
| 6Ah         | R/W | O6        | BLO6[3:0] |    |    | FRO6[1:0] |    | DLO6[1:0] |    |    |
| 6Bh         | R/W | O7        | BLO7[3:0] |    |    | FRO7[1:0] |    | DLO7[1:0] |    |    |

**OPERATION (continued)**

**2. Register Map (2) (continued)**

| Sub Address | R/W | Data name | DATA      |    |    |    |           |    |           |    |
|-------------|-----|-----------|-----------|----|----|----|-----------|----|-----------|----|
|             |     |           | D7        | D6 | D5 | D4 | D3        | D2 | D1        | D0 |
| 6Ch         | R/W | P1        | BLP1[3:0] |    |    |    | FRP1[1:0] |    | DLP1[1:0] |    |
| 6Dh         | R/W | P2        | BLP2[3:0] |    |    |    | FRP2[1:0] |    | DLP2[1:0] |    |
| 6Eh         | R/W | P3        | BLP3[3:0] |    |    |    | FRP3[1:0] |    | DLP3[1:0] |    |
| 6Fh         | R/W | P4        | BLP4[3:0] |    |    |    | FRP4[1:0] |    | DLP4[1:0] |    |
| 70h         | R/W | P5        | BLP5[3:0] |    |    |    | FRP5[1:0] |    | DLP5[1:0] |    |
| 71h         | R/W | P6        | BLP6[3:0] |    |    |    | FRP6[1:0] |    | DLP6[1:0] |    |
| 72h         | R/W | P7        | BLP7[3:0] |    |    |    | FRP7[1:0] |    | DLP7[1:0] |    |
| 73h         | R/W | Q1        | BLQ1[3:0] |    |    |    | FRQ1[1:0] |    | DLQ1[1:0] |    |
| 74h         | R/W | Q2        | BLQ2[3:0] |    |    |    | FRQ2[1:0] |    | DLQ2[1:0] |    |
| 75h         | R/W | Q3        | BLQ3[3:0] |    |    |    | FRQ3[1:0] |    | DLQ3[1:0] |    |
| 76h         | R/W | Q4        | BLQ4[3:0] |    |    |    | FRQ4[1:0] |    | DLQ4[1:0] |    |
| 77h         | R/W | Q5        | BLQ5[3:0] |    |    |    | FRQ5[1:0] |    | DLQ5[1:0] |    |
| 78h         | R/W | Q6        | BLQ6[3:0] |    |    |    | FRQ6[1:0] |    | DLQ6[1:0] |    |
| 79h         | R/W | Q7        | BLQ7[3:0] |    |    |    | FRQ7[1:0] |    | DLQ7[1:0] |    |



**OPERATION (continued)**

**3. Register Map (1) Detail descriptions**

Address 01h to 13h

| Sub address   |           | DATA |     |     |     |     |     |     |        |
|---------------|-----------|------|-----|-----|-----|-----|-----|-----|--------|
|               |           | D7   | D6  | D5  | D4  | D3  | D2  | D1  | D0     |
| 01h<br>MAPCHG | Data name | —    | —   | —   | —   | —   | —   | —   | MAPCHG |
|               | Default   | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 0      |
|               | mode      | W/R  | W/R | W/R | W/R | W/R | W/R | W/R | W/R    |

D0 : MAPCHG Register Map selection bit

[0] : Register selection for matrix default setup control (default)

It is possible to access Address 01h to 13h described in Register Map (1) (Page 20).

[1] : RAM1, RAM2 selection bit, Address selection for RAM1, RAM2 data setup

It is possible to access Address 01h to 79h described in Register Map (2) (Page 21 to Page 24).

| Sub address     |           | DATA |     |     |     |     |     |     |       |
|-----------------|-----------|------|-----|-----|-----|-----|-----|-----|-------|
|                 |           | D7   | D6  | D5  | D4  | D3  | D2  | D1  | D0    |
| 02h<br>POWERCNT | Data name | —    | —   | —   | —   | —   | —   | —   | OSCEN |
|                 | Default   | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 0     |
|                 | mode      | W/R  | W/R | W/R | W/R | W/R | W/R | W/R | W/R   |

D0 : OSCEN ON/OFF bit for internal oscillators

[0] : Internal oscillator is OFF (default)

[1] : Internal oscillator is ON

The variation width of an internal oscillator is set to 0.96 MHz to 1.44 MHz.

The variation width of an internal clock is set to 694.4 ns to 1,042 ns.

When 01hD0 : MAPCHG = "0" is set, this address is effective.

**OPERATION (continued)**

**3. Register Map (1) Detail descriptions (continued)**

Address 01h to 13h (continued)

| Sub address   |           | DATA |     |     |     |     |     |     |       |
|---------------|-----------|------|-----|-----|-----|-----|-----|-----|-------|
|               |           | D7   | D6  | D5  | D4  | D3  | D2  | D1  | D0    |
| 03h<br>LDOCNT | Data name | —    | —   | —   | —   | —   | —   | —   | REG18 |
|               | Default   | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 1     |
|               | mode      | W/R  | W/R | W/R | W/R | W/R | W/R | W/R | W/R   |

D0 : REG18 ON/OFF control for LDO (At LDOCNT pin = Low)

[0] : LDO OFF

[1] : LDO ON (default)

When LDOCNT pin is High, regardless of the state of REG18, LDO will be active.

Set LDOCNT to "0" after setting REG18 to "0" to put into OFF mode.

When 01hD0 : MAPCHG = "0" is set, this address is effective.

| Sub address  |           | DATA  |    |    |    |    |    |    |    |
|--------------|-----------|-------|----|----|----|----|----|----|----|
|              |           | D7    | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 04h<br>TEST0 | Data name | TEST0 |    |    |    |    |    |    |    |
|              | Default   | 0     | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
|              | mode      | R     | R  | R  | R  | R  | R  | R  | R  |

This register is used for the LSI testing.

When 01hD0 : MAPCHG = "0" is set, this address is effective.

**OPERATION (continued)**

**3. Register Map (1) Detail descriptions (continued)**

Address 01h to 13h (continued)

| Sub address |           | DATA |    |    |    |    |    |        |        |
|-------------|-----------|------|----|----|----|----|----|--------|--------|
|             |           | D7   | D6 | D5 | D4 | D3 | D2 | D1     | D0     |
| 05h<br>INT  | Data name | —    | —  | —  | —  | —  | —  | RAMACT | FRMINT |
|             | Default   | 0    | 0  | 0  | 0  | 0  | 0  | 0      | 0      |
|             | mode      | R    | R  | R  | R  | R  | R  | R      | R      |

D1 : RAMACT Internal RAM access judgment

[0] : RAM is not accessed. (default)

[1] : RAM is accessed.

D0 : FRMINT An one-frame display end judging scroll on display

[0] : Under a frame display. (default)

[1] : Frame display end.

RAM access from CPU cannot be performed at RAMACT = [1].

The interval of RAMACT = [1] is the period of internal 1 clock after RAM clear, and then returns [0].

While each address 05h register is [1], the pulse with 4 ms cycle is output from INT.

When the interrupt is generated by the other interrupt factors after INT pulse is generated, INT pulse is generated again at that timing and then the pulse with 4 ms cycle is output from INT again.

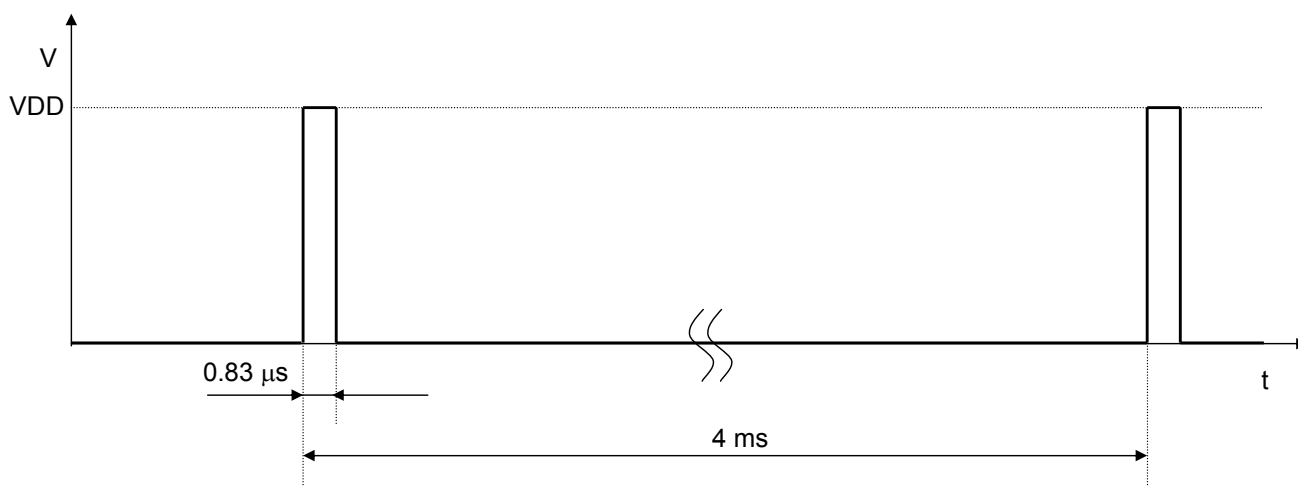
The pulse output from INT continues to output until address 05h is read. (Only FRMINT)

RAMACT generates INT pulse only one time after RAM is cleared. 4 ms after RAM is cleared, pulses will not be generated.

NRST = Low or 0Dh SRST = [1] can reset to stop the INT pulse signal in case of that the serial read function is not used.

The state for RAMACT = [1] is during the time that RAM is cleared.

When 01hD0 : MAPCHG = "0" is set, this address is effective.



**OPERATION (continued)**

**3. Register Map (1) Detail descriptions (continued)**

Address 01h to 13h (continued)

| Sub address   |           | DATA   |        |     |     |     |     |        |        |
|---------------|-----------|--------|--------|-----|-----|-----|-----|--------|--------|
|               |           | D7     | D6     | D5  | D4  | D3  | D2  | D1     | D0     |
| 06h<br>OPTION | Data name | LEDACT | DISMTX | —   | —   | —   | —   | CLKOUT | EXTCLK |
|               | Default   | 0      | 0      | 0   | 0   | 0   | 0   | 0      | 0      |
|               | mode      | W/R    | W/R    | W/R | W/R | W/R | W/R | W/R    | W/R    |

D7 : LEDACT Input signal polarity setting for LED turn-on/off function controlled by LEDCTL pin.

[0] : The light is switched off at LEDCTL = Low (default)

[1] : The light is switched on at LEDCTL = High

D6 : DISMTX LED turn-on/off function for 7 x 17 dots matrix LED controlled by LEDCTL pin.

[0] : LED turn-on/off function is OFF by LEDCTL pin. (default)

[1] : LED turn-on/off function is ON by LEDCTL pin.

D1 : CLKOUT Internal clock output switch setup of this LSI

[0] : The internal clock is not output from CLKOUT. CLKOUT = Low (default)

[1] : The internal clock is output from CLKOUT.

D0 : EXTCLK Reference clock selection used for the LSI operation

[0] : Internal clock is used for the LSI operation (default).

[1] : External clock (EXTCLK) is used for the LSI operation.

When 01hD0 : MAPCHG = "0" is set, this address is effective.

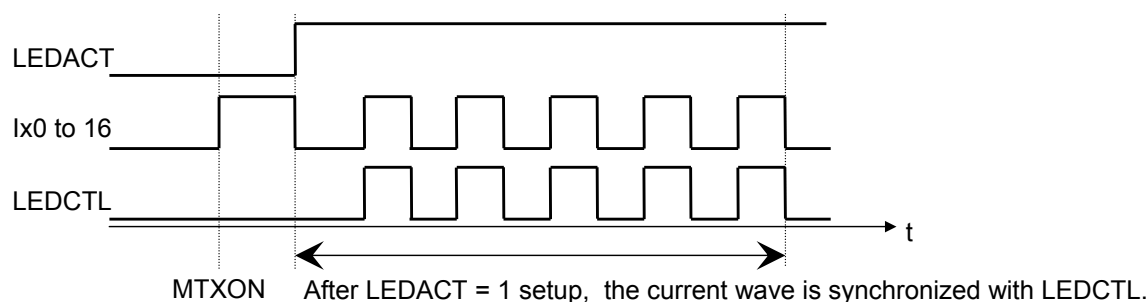
The PWM pulse applied to LEDCTL can control LED turn-on/off.

For example, when music signal is input as the input signal, LED blinking can be synchronized with the music signal. As the internal circuit operates by VDD power supply, please input more than 1.5 V[p-p] amplitude.

As this input is open gate input, please connect the pull-up or pull-down resistors externally if necessary.

The control by LEDCTL can be set by the register 06h.

LED matrix can be set independently. (In default setting, this setting is invalid.)



**OPERATION (continued)**

**3. Register Map (1) Detail descriptions (continued)**

Address 01h to 13h (continued)

| Sub address  |           | DATA |     |     |     |     |     |     |       |
|--------------|-----------|------|-----|-----|-----|-----|-----|-----|-------|
|              |           | D7   | D6  | D5  | D4  | D3  | D2  | D1  | D0    |
| 07h<br>MTXON | Data name | —    | —   | —   | —   | —   | —   | —   | MTXON |
|              | Default   | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 0     |
|              | mode      | W/R  | W/R | W/R | W/R | W/R | W/R | W/R | W/R   |

D0 : MTXON ON/OFF setup of matrix LED  
 [0] : OFF (default)  
 [1] : ON

During MTXON = [1], subsequent RAM and the control contents to a register are sequentially processed and LEDs are lit up.

When EXTCLK (address 06h) is set to [0], set MTXON to [1] in 5 ms after OSCEN (address 02h) is set to [1].

When EXTCLK (address 06h) is set to [1], set MTXON to [1] in 5 ms after the clock is inputted into EXTCLK pin.

Set MTXON to [1], and then set up other addresses to display the matrix part.

When 01hD0 : MAPCHG = "0" is set, this address is effective.

**OPERATION (continued)**

**3. Register Map (1) Detail descriptions (continued)**

Address 01h to 13h (continued)

| Sub address    |           | DATA |     |     |     |     |     |         |     |
|----------------|-----------|------|-----|-----|-----|-----|-----|---------|-----|
|                |           | D7   | D6  | D5  | D4  | D3  | D2  | D1      | D0  |
| 08h<br>MTXDATA | Data name | —    | —   | —   | —   | —   | —   | MTXDATA |     |
|                | Default   | 0    | 0   | 0   | 0   | 0   | 0   | 0       | 0   |
|                | mode      | W/R  | W/R | W/R | W/R | W/R | W/R | W/R     | W/R |

D1-0 : MTXDATA[1:0] Address setup of RAM display

[00] : Display OFF (Set all the data in the buffer for display to "0".)

[01] : RAM1 display (Luminance + Cycle + Delay)

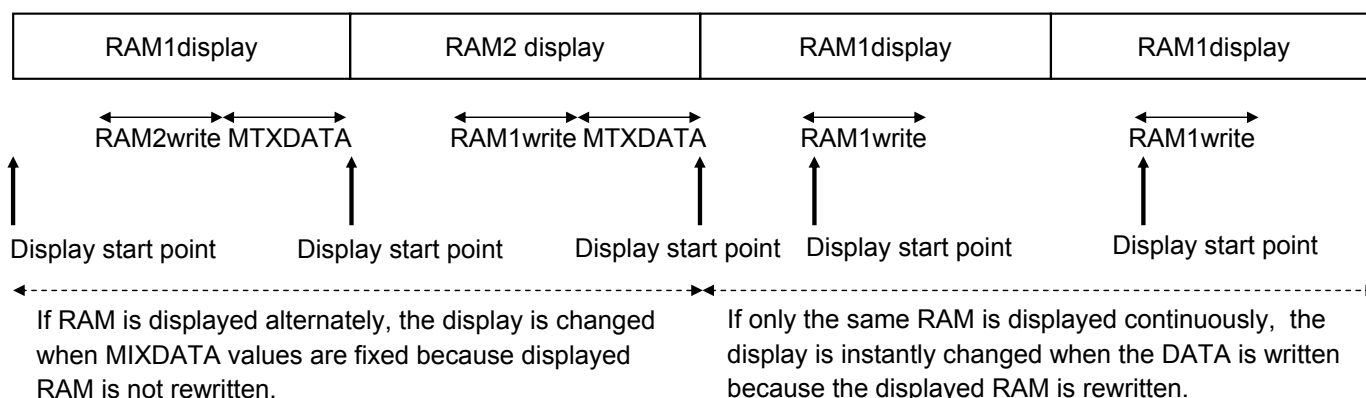
[10] : RAM2 display (Luminance + Cycle + Delay)

[11] : Display OFF (Set all the data in the buffer for display to "0".)

Display OFF setting is to set all the matrix LED data in the buffer for display to "0".

If the values of RAM1(RAM2) are changed during the display of RAM1(RAM2), in each case the values of each LED are instantly updated. Therefore, the data update time in case that the same RAM is used (for example, RAM1 → RAM1 → RAM1) is shorter than in case that RAM1 and RAM2 are used alternately (for example, RAM1 → RAM2 → RAM1). Because the time for writing into RAM and the change of MTXDATA values can be omitted.

When 01hD0 : MAPCHG = "0" is set, this address is effective.



**OPERATION (continued)**

**3. Register Map (1) Detail descriptions (continued)**

Address 01h to 13h (continued)

| Sub address   |           | DATA |     |     |     |     |     |      |      |
|---------------|-----------|------|-----|-----|-----|-----|-----|------|------|
|               |           | D7   | D6  | D5  | D4  | D3  | D2  | D1   | D0   |
| 09h<br>RAMRST | Data name | —    | —   | —   | —   | —   | —   | RAM1 | RAM2 |
|               | Default   | 0    | 0   | 0   | 0   | 0   | 0   | 0    | 0    |
|               | mode      | W/R  | W/R | W/R | W/R | W/R | W/R | W/R  | W/R  |

D1 : RAM1 The data in 7 × 17 RAM1 is cleared.

0 : Overwrite is possible. (default)

1 : The data in 7 × 17 RAM1 is cleared. (It returns back to "0" automatically during the internal 2 clocks.)

D0 : RAM2 The data in 7 × 17 RAM2 is cleared.

0 : Overwrite is possible. (default)

1 : The data in 7 × 17 RAM2 is cleared. (It returns back to "0" automatically during the internal 2 clocks.)

Don't set the RAM-clear operation for RAM1 or RAM2 during the scroll display function (SCLON = [1]).

Data in RAM1, RAM2 is cleared after reset release.

When 01hD0 : MAPCHG = "0" is set, this address is effective.

| Sub address   |           | DATA |     |     |     |     |     |     |       |
|---------------|-----------|------|-----|-----|-----|-----|-----|-----|-------|
|               |           | D7   | D6  | D5  | D4  | D3  | D2  | D1  | D0    |
| 0Ah<br>SCROLL | Data name | —    | —   | —   | —   | —   | —   | —   | SCLON |
|               | Default   | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 0     |
|               | mode      | W/R  | W/R | W/R | W/R | W/R | W/R | W/R | W/R   |

D0 : SCLON ON/OFF setup for scroll display function

0 : OFF (default)

1 : ON

The scroll display function can realize the display scroll one line or row at a time by shifting the data which exists in the RAM1 and 2 of 7 × 17. The scroll direction is specified by 0Bh.

During the display scroll, the data can be written in RAM without specifying RAM number.

(Writing is performed to the RAM which is not displayed at that timing.)

The display scroll starts by MTXON = [1] and SCLON = [1].

During the display scroll (SCLON = [1] ), don't clear the setting of RAM(RAM1, RAM2).

When SCLON = [1] is set with cycle and delay setup for RAM data, only brightness setup is enabled and the scroll display can be set. (Firefly and delay control setting are disabled during the scroll display.)

When the scroll display is set to OFF (SCLON = [0]) and the display returns the normal display, the display setting follows MTXDATA setup values at the time.

During the scroll display, it is possible to access (Read/Write) to MTXDATA existing Address 08h. However, the setting is reflected only after scroll OFF setting (SCLON = [0]).

When 01hD0 : MAPCHG = "0" is set, this address is effective.

**OPERATION (continued)**

**3. Register Map (1) Detail descriptions (continued)**

Address 01h to 13h (continued)

| Sub address    |           | DATA |     |      |       |      |              |     |     |
|----------------|-----------|------|-----|------|-------|------|--------------|-----|-----|
|                |           | D7   | D6  | D5   | D4    | D3   | D2           | D1  | D0  |
| 0Bh<br>SCLMODE | Data name | —    | UP  | DOWN | RIGHT | LEFT | SCLTIME[2:0] |     |     |
|                | Default   | 0    | 0   | 0    | 0     | 1    | 0            | 0   | 0   |
|                | mode      | W/R  | W/R | W/R  | W/R   | W/R  | W/R          | W/R | W/R |

D6 : UP Scroll direction setup “from downside to upside”

0 : Normal display (default)

1 : Setting the scroll direction from downside to upside

D5 : DOWN Scroll direction setup “from upside to downside”

0 : Normal display (default)

1 : Setting the scroll direction from upside to downside

D4 : RIGHT Scroll direction setup “from left side to right side”

0 : Normal display (default)

1 : Setting the scroll direction from left side to right side

D3 : LEFT Scroll direction setup “from right side to left side”

0 : Normal display

1 : Setting the scroll direction from right side to left side (default)

D2-0 : One display frame time setup for scroll display

[000] : 0.1 s (default)                      [100] : 0.5 s

[001] : 0.2 s                                      [101] : 0.6 s

[010] : 0.3 s                                      [110] : 0.7 s

[011] : 0.4 s                                      [111] : 0.8 s

The scroll function is disabled when any two or more bits of D3 to D6 are simultaneously set to [1] or when all of them is set to [0]. (The display is set to RAM display according to MTXDATA at normal mode.)

The normal display continues if two or more commands for the scroll direction are set before the scroll display.

When two or more commands for the scroll direction are set during the scroll display, the scroll display stops at that timing. The display follows the MTXDATA setting.

All the 7 × 17 data written in RAM1, RAM2 are called the frame.

When the scroll direction is changed during the scroll display, the scroll display before that change continues until the present frame display finishes. The frame at the timing when the setting is changed ends, the new scroll direction is reflected from the next frame.

When the scroll direction is set to RIGHT or LEFT, the display shifting time of a row is the setting value of SCLTIME.

When the scroll direction is set to UP or DOWN, the display shifting time of a line is the setting value of SCLTIME.

When 01hD0 : MAPCHG = "0" is set, this address is effective.





**OPERATION (continued)**

**3. Register Map (1) Detail descriptions (continued)**

Address 01h to 13h (continued)

| Sub address  |           | DATA |     |     |     |     |     |     |      |
|--------------|-----------|------|-----|-----|-----|-----|-----|-----|------|
|              |           | D7   | D6  | D5  | D4  | D3  | D2  | D1  | D0   |
| 0Dh<br>RESET | Data name | —    | —   | —   | —   | —   | —   | —   | SRST |
|              | Default   | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 0    |
|              | mode      | W/R  | W/R | W/R | W/R | W/R | W/R | W/R | W/R  |

D0 : SRST Soft reset control bit

[0] : Reset release state (default)

[1] : Reset state (It returns back to [0] automatically by the internal or external 2 clocks)

It returns back to [0] automatically by the internal 2 clocks during the internal clock operation and by the external 2 clocks during the external clock operation. In case of no clock, it can not return to [0] automatically.

| Sub address    |           | DATA |     |     |     |     |     |     |     |
|----------------|-----------|------|-----|-----|-----|-----|-----|-----|-----|
|                |           | D7   | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
| 10h<br>XCONST1 | Data name | X16  | X15 | X14 | X13 | X12 | X11 | X10 | X9  |
|                | Default   | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
|                | mode      | W/R  | W/R | W/R | W/R | W/R | W/R | W/R | W/R |

D7 : X16 Constant current mode setup selection bit of X16

0 : Matrix operation (default)

1 : Constant current operation

D6 : X15 Constant current mode setup selection bit of X15

0 : Matrix operation (default)

1 : Constant current operation

D5 : X14 Constant current mode setup selection bit of X14

0 : Matrix operation (default)

1 : Constant current operation

D4 : X13 Constant current mode setup selection bit of X13

0 : Matrix operation (default)

1 : Constant current operation

D3 : X12 Constant current mode setup selection bit of X12

0 : Matrix operation (default)

1 : Constant current operation

D2 : X11 Constant current mode setup selection bit of X11

0 : Matrix operation (default)

1 : Constant current operation

D1 : X10 Constant current mode setup selection bit of X10

0 : Matrix operation (default)

1 : Constant current operation

D0 : X9 Constant current mode setup selection bit of X9

0 : Matrix operation (default)

1 : Constant current operation

When these bits are set to "1", Xx pin becomes the constant current mode. And the brightness for each Xx pin is controlled by the setting of LED which is connected between Xx pin and Y0 pin.

When 01hD0 : MAPCHG = "0" is set, this address is effective.

**OPERATION (continued)**

**3. Register Map (1) Detail descriptions (continued)**

Address 01h to 13h (continued)

| Sub address    |           | DATA |     |     |     |     |     |     |     |
|----------------|-----------|------|-----|-----|-----|-----|-----|-----|-----|
|                |           | D7   | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
| 11h<br>XCONST2 | Data name | X8   | X7  | X6  | X5  | X4  | X3  | X2  | X1  |
|                | Default   | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
|                | mode      | W/R  | W/R | W/R | W/R | W/R | W/R | W/R | W/R |

D7 : X8 Constant current mode setup selection bit of X8

- 0 : Matrix operation (default)
- 1 : Constant current operation

D6 : X7 Constant current mode setup selection bit of X7

- 0 : Matrix operation (default)
- 1 : Constant current operation

D5 : X6 Constant current mode setup selection bit of X6

- 0 : Matrix operation (default)
- 1 : Constant current operation

D4 : X5 Constant current mode setup selection bit of X5

- 0 : Matrix operation (default)
- 1 : Constant current operation

D3 : X4 Constant current mode setup selection bit of X4

- 0 : Matrix operation (default)
- 1 : Constant current operation

D2 : X3 Constant current mode setup selection bit of X3

- 0 : Matrix operation (default)
- 1 : Constant current operation

D1 : X2 Constant current mode setup selection bit of X2

- 0 : Matrix operation (default)
- 1 : Constant current operation

D0 : X1 Constant current mode setup selection bit of X1

- 0 : Matrix operation (default)
- 1 : Constant current operation

When these bits are set to "1", Xx pin becomes the constant current mode. And the brightness for each Xx pin is controlled by the setting of LED which is connected between Xx pin and Y0 pin.

When 01hD0 : MAPCHG = "0" is set, this address is effective.

| Sub address    |           | DATA |     |     |     |     |     |     |     |
|----------------|-----------|------|-----|-----|-----|-----|-----|-----|-----|
|                |           | D7   | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
| 12h<br>XCONST3 | Data name | —    | —   | —   | —   | —   | —   | —   | X0  |
|                | Default   | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
|                | mode      | W/R  | W/R | W/R | W/R | W/R | W/R | W/R | W/R |

D0 : X0 Constant current mode setup selection bit of X0

- 0 : Matrix operation (default)
- 1 : Constant current operation

When these bits are set to "1", Xx pin becomes the constant current mode. And the brightness for each Xx pin is controlled by the setting of LED which is connected between Xx pin and Y0 pin.

When 01hD0 : MAPCHG = "0" is set, this address is effective.

**OPERATION (continued)**

**3. Register Map (1) Detail descriptions (continued)**

Address 01h to 13h (continued)

| Sub address |           | DATA |     |     |     |     |     |           |     |
|-------------|-----------|------|-----|-----|-----|-----|-----|-----------|-----|
|             |           | D7   | D6  | D5  | D4  | D3  | D2  | D1        | D0  |
| 13h<br>IMAX | Data name | —    | —   | —   | —   | —   | —   | IMAX[1:0] |     |
|             | Default   | 0    | 0   | 0   | 0   | 0   | 0   | 0         | 1   |
|             | mode      | W/R  | W/R | W/R | W/R | W/R | W/R | W/R       | W/R |

D1-0 : IMAX[1:0] Maximum value selection bit for current setup

[00] : 15 mA

[01] : 20 mA (default)

[10] : 25 mA

[11] : 30 mA

The constant current operation follows the maximum value selection bit set by this register.

The each current step is set by 1/15 of maximum value.

When 01hD0 : MAPCHG = "0" is set, this address is effective.

**OPERATION (continued)**

**3. Register Map (2) Detail descriptions**

Address 02h to 79h

| Sub address   |           | DATA |     |     |     |     |     |     |        |
|---------------|-----------|------|-----|-----|-----|-----|-----|-----|--------|
|               |           | D7   | D6  | D5  | D4  | D3  | D2  | D1  | D0     |
| 02h<br>RAMNUM | Data name | —    | —   | —   | —   | —   | —   | —   | RAMNUM |
|               | Default   | 0    | 0   | 0   | 0   | 0   | 0   | 0   | 0      |
|               | mode      | W/R  | W/R | W/R | W/R | W/R | W/R | W/R | W/R    |

D0 : RAMNUM RAM number setup for the CPU access (Read, Write).

[0] : RAM number 1

[1] : RAM number 2

Accessing to 02h is disabled during the scroll display function (0Ah SCLON = [1]).

When RAM data are written during the scroll display function, the data is written to the RAM which is not used for the display.

(Ex.)When the data is written while RAM1 is displayed during the scroll display function (0Ah SCLON = [1]), the data is written to RAM2 regardless of RAMNUM.

When 01hD0 : MAPCHG = "1" is set, this address is effective.

**OPERATION (continued)**

**3. Register Map (2) Detail descriptions (continued)**

Address 02h to 79h (continued)

| Sub address |           | DATA      |     |     |     |           |     |           |     |
|-------------|-----------|-----------|-----|-----|-----|-----------|-----|-----------|-----|
|             |           | D7        | D6  | D5  | D4  | D3        | D2  | D1        | D0  |
| 03h<br>A1   | Data name | BLA1[3:0] |     |     |     | FRA1[1:0] |     | DLA1[1:0] |     |
|             | Default   | 0         | 0   | 0   | 0   | 0         | 0   | 0         | 0   |
|             | mode      | W/R       | W/R | W/R | W/R | W/R       | W/R | W/R       | W/R |

D7-4 : BLA1[3:0] Brightness setup of LED No.A1

In case of address13h IMAX=[01] (default)

|                         |                   |
|-------------------------|-------------------|
| [0000] : 0 mA (default) | [1000] : 10.66 mA |
| [0001] : 1.33 mA        | [1001] : 12.00 mA |
| [0010] : 2.66 mA        | [1010] : 13.33 mA |
| [0011] : 4.00 mA        | [1011] : 14.66 mA |
| [0100] : 5.33 mA        | [1100] : 16.00 mA |
| [0101] : 6.67 mA        | [1101] : 17.33 mA |
| [0110] : 8.00 mA        | [1110] : 18.66 mA |
| [0111] : 9.33 mA        | [1111] : 20.00 mA |

D3-2 : FRA1[1:0] Firefly operation and cycle setup of the LED No.A1

- [00] : Normal lighting mode (default)
- [01] : Firefly lighting cycle 1 s
- [10] : Firefly lighting cycle 2 s
- [11] : Firefly lighting cycle 3 s

D1-0 : DLA1[1:0] Firefly operation delay setup of the LED No.A1

- [00] : No delay (default)
- [01] : Delay 25%
- [10] : Delay 50%
- [11] : Delay 75%

Brightness setup values (each step) of [D7-4] are changeable in address 13h of IMAX[1:0].

(example) [0000] : 0 mA (default)

|                               |
|-------------------------------|
| [0001] : 1.00 mA              |
| [0010] : 2.00 mA              |
| :                             |
| [1111] : 15.00 mA * 1 mA/STEP |

The operation is the same above for the addresses to 79h corresponding to each LED number.

The waiting time for 2 or more internal clocks (2 μs or more) is required after the data from address 03h to 79h is written in. Please input other serial commands after that.

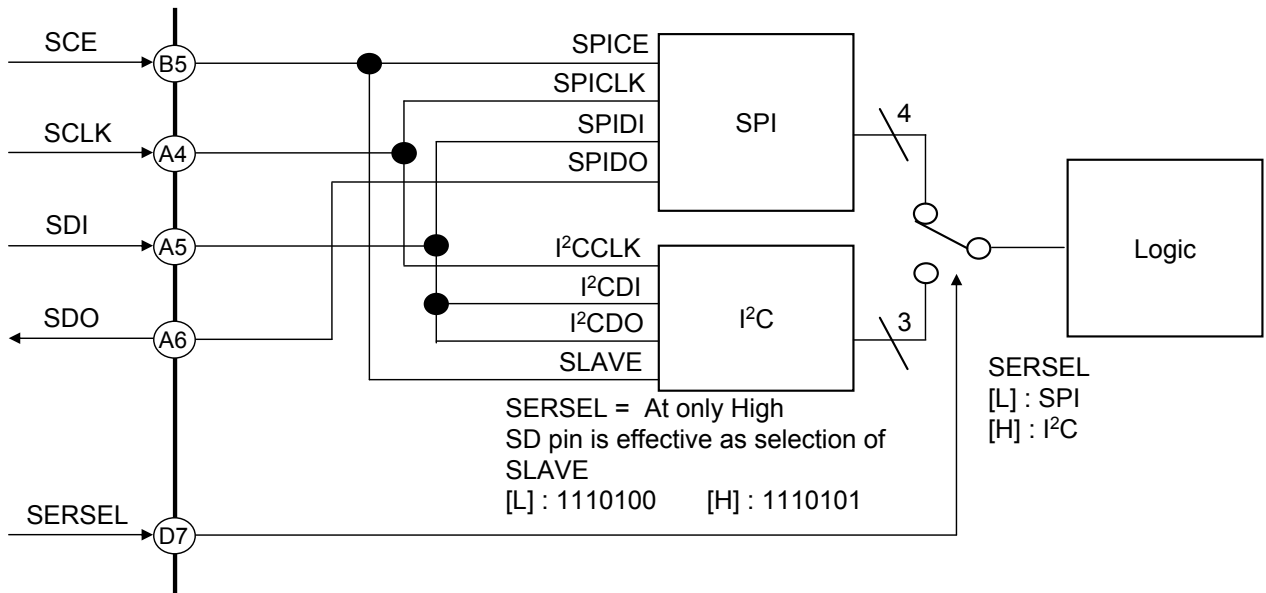
For the data in Address 03h to79h during scroll operation, only Luminance setup[D7-4] is enabled, Delay setup [D1-0] and Firefly lighting setup[D3-2] are disabled.

Address 03h to 79h are the same setting as the above description.

At 01hD0 : MAPCHG = "1" setup, this address is effective.

**OPERATION (continued)**

**4. Interface configuration**



**OPERATION (continued)**

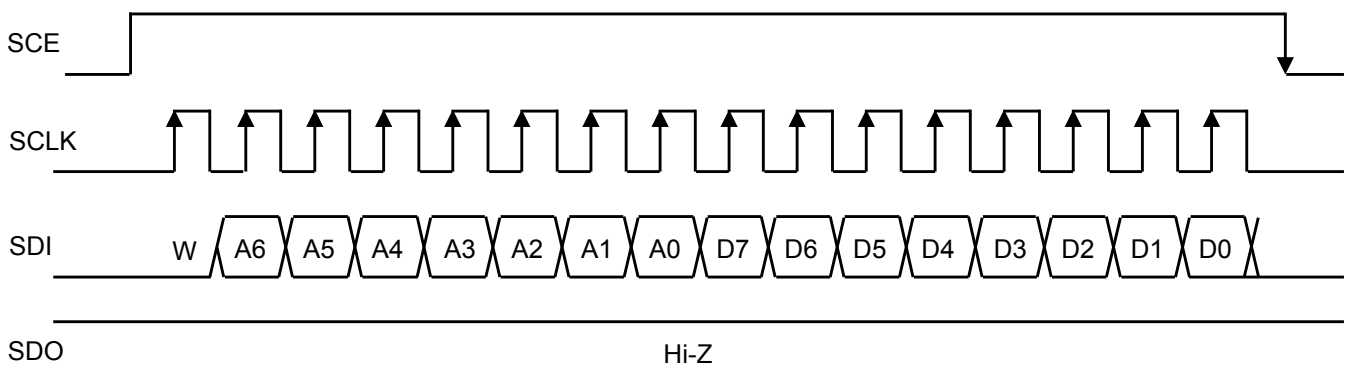
**5. SPI interface**

The interface with microcomputer consists of 16 bit-serial register (8-bit of command, 8-bit of address), and address decoder and transmitting register (8-bit).  
Serial interface consists of four terminals of serial clock pin (SCLK), serial-data input pin (SDI), serial-data output pin (SDO), and chip enable input pin (SCE).

(1) Write operation

At MSB first and the first clk of SCLK, Write is recognized by SDI = Low  
Data is taken into internal shift register by the rising edge of SCLK. (Maximum 13 MHz of frequency of CLK can be used)  
In High interval of SCE, reception of data becomes ENABLE. (active : High)  
Data is transmitted at MSB first in order of a control register address (8-bit) and control command (8-bit).

Write access timing





**OPERATION (continued)**

**5. SPI interface (continued)**

(2) Transmission operation

At MSB first and the first clk of SCLK, Read is recognized by SDI = High.

Data is taken into internal shift register by the rising edge of CLK.

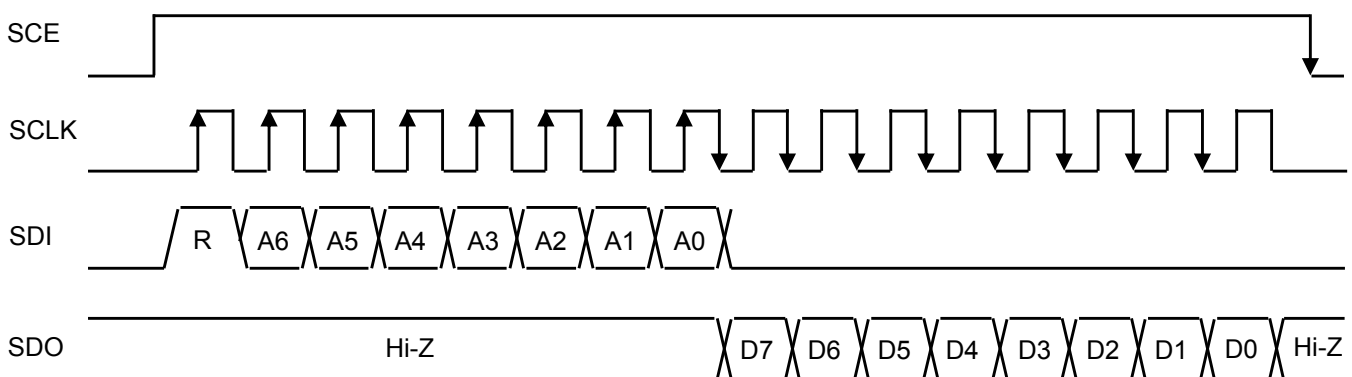
(A maximum of 6 MHz of frequency of CLK can be used)

In High interval of SCE, reception of data becomes ENABLE. (active : High)

Data is transmitted at MSB first in order of a control register address (8-bit) and control command (max 8-bit).

It is not possible to Read RAM data.

Read access timing



## OPERATION (continued)

### 6. I<sup>2</sup>C interface

#### 6.1 Basic Rules

This LSI, I<sup>2</sup>C-bus, is designed to correspond to the Standard-mode (100 kbps) and Fast-mode(400 kbps) devices in the version 2.1 of NXP's specification. However, it does not correspond to the HS-mode (to 3.4 Mbps).

This LSI will be operated as a slave device in the I<sup>2</sup>C-bus system.

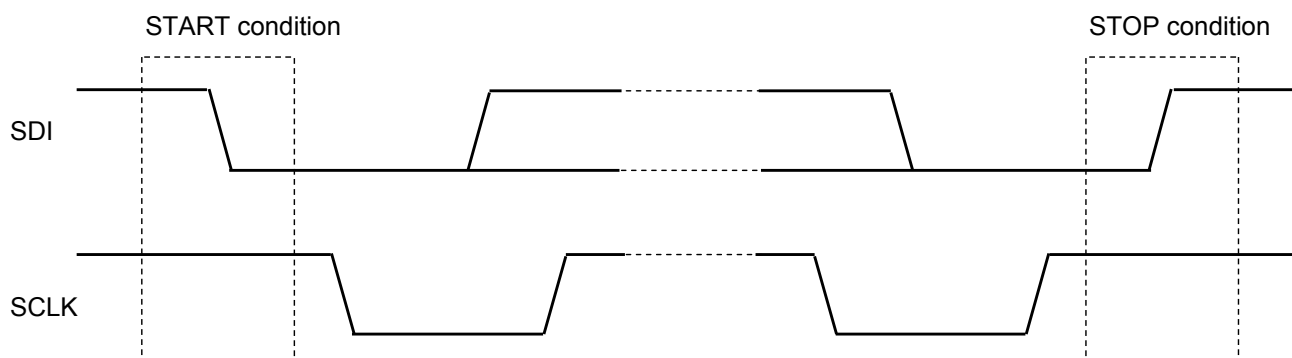
The program operation check of this LSI has not been conducted on the multi-master bus system and the mix-speed bus system, yet. The connected confirmation of this LSI to the CBUS receiver also has not been checked. Please confirm with our company if it will be used in these mode systems.

Purchase of Panasonic I<sup>2</sup>C Components conveys a license under the NXP I<sup>2</sup>C patent right to use these components in an I<sup>2</sup>C systems, provided that the system conforms to the I<sup>2</sup>C standard specifications as defined by NXP.

#### 6.2 START and STOP conditions

A High to Low transition on the SDA line while SCLK is High is one such unique case. This situation indicates a START condition. A Low to High transition on the SDA line while SCLK is High defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is busy after the START condition is generated. The bus is considered to be free again a certain time after the STOP condition.



**OPERATION (continued)**

**6. I<sup>2</sup>C interface (continued)**

6.3 Transferring Data

Every byte put on the SDA line must be 8-bit long.

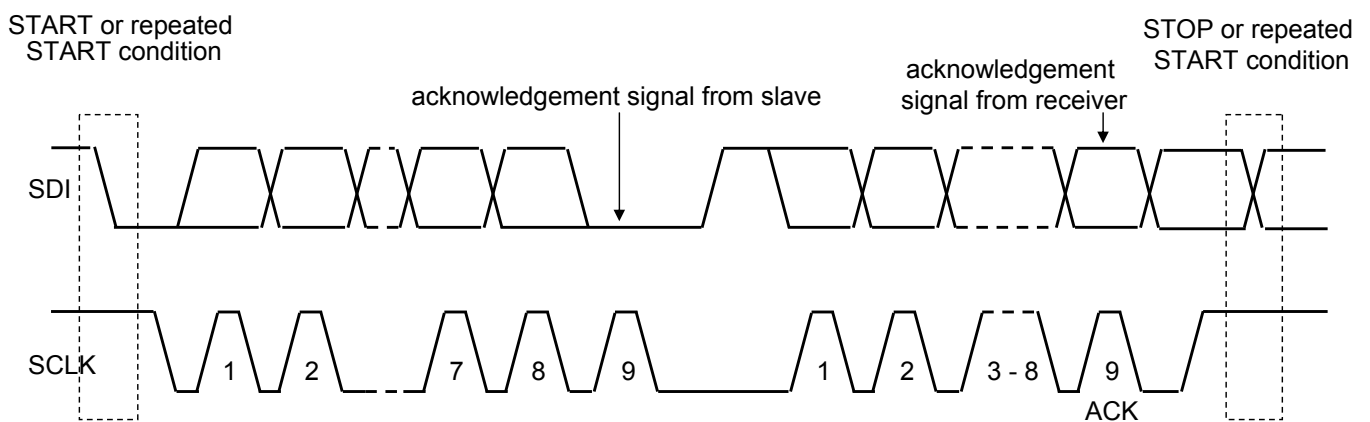
The number of bytes that can be transmitted per transfer is unrestricted.

Each byte has to be followed by an acknowledge bit.

Data is transferred with the most significant bit (MSB) first.

If a slave can't receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCLK Low to force the master into a wait state.

Data transfer then continues when the slave is ready for another byte of data and releases clock line SCLK.



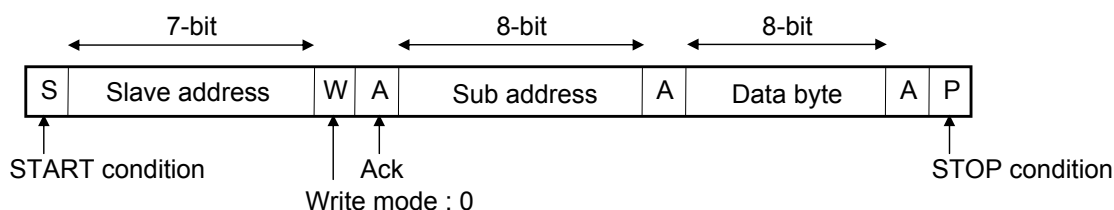
**OPERATION (continued)**

**6. I<sup>2</sup>C interface (continued)**

6.4 DATA format

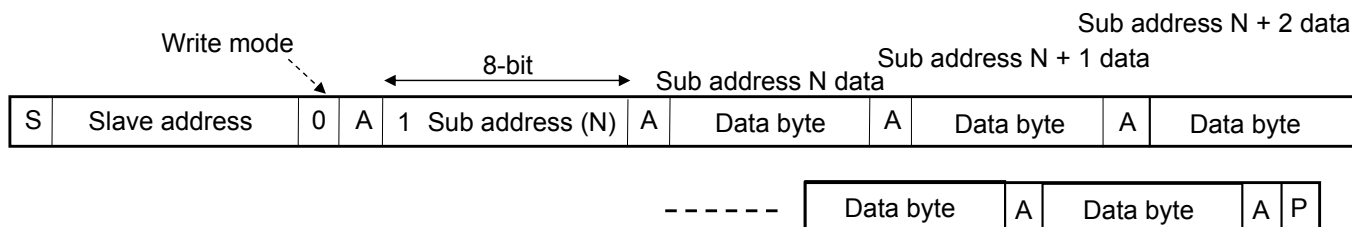
When I<sup>2</sup>C format is used in this LSI, use it while SERSEL pin is fixed to High level.  
 Slave address can be selected by switching SCE pin Low and High-level.  
 Slave address of this LSI is set to 74h when SCE pin is Low-level, is set to 75h when SCE pin is High-level.

Write mode



The mode becomes Auto increment mode when MSB of Sub address is "1".  
 The next data byte is Written in the next Sub address by transmitting data byte continuously.  
 Sub address is performed increment automatically.  
 The mode becomes Data update mode when the MSB of Sub address is "0".  
 The next data byte is Written in the same Sub address by transmitting data byte continuously.

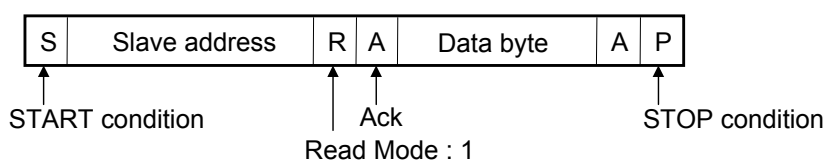
Auto increment mode (Write mode)



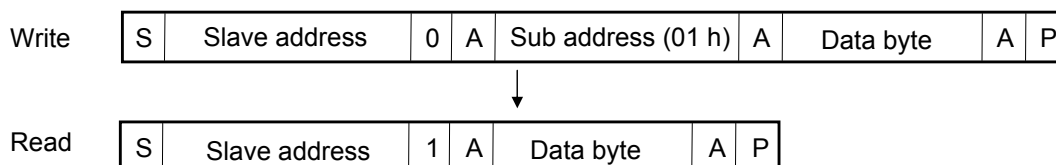
Read mode

A) In case Sub address is not specified

When Sub address is not specified and data is read, this LSI allows to read the value of adjacent Sub address specified in the last Write mode.



Ex.) In case data is written to Address 01h and read from Address 01h.



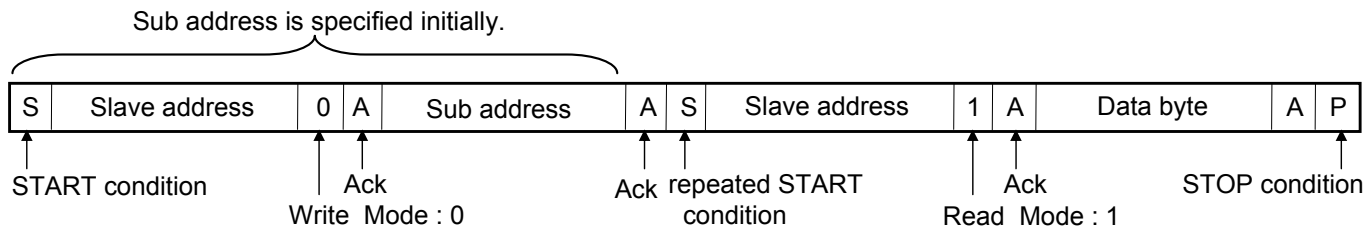
**OPERATION (continued)**

**6. I<sup>2</sup>C interface (continued)**

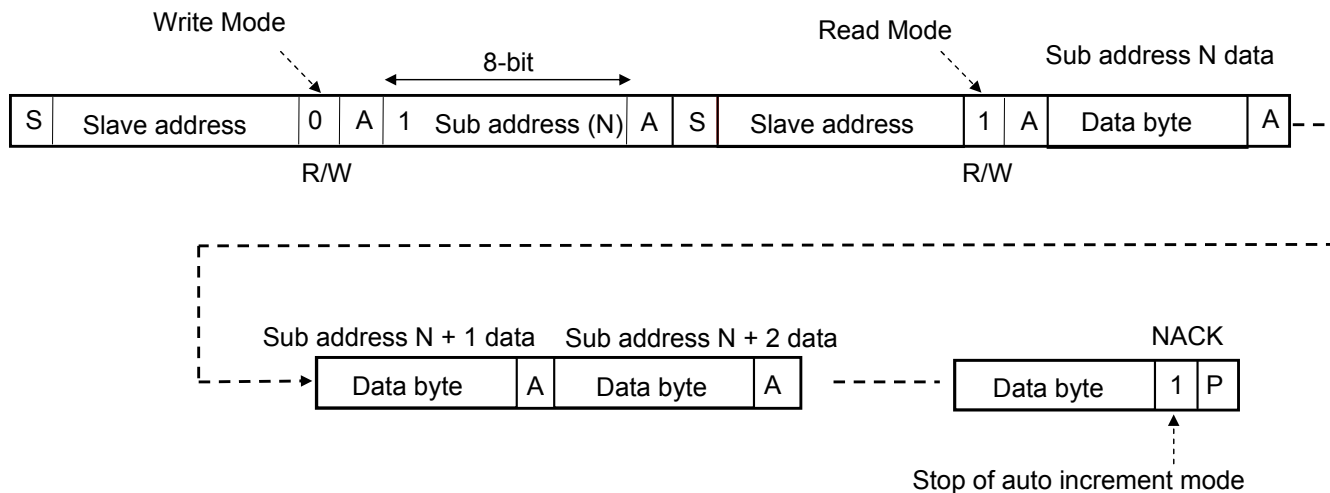
6.4 DATA format (continued)

Read mode (continued)

B) In case Sub address if specified



Auto increment mode (Read mode)



**OPERATION (continued)**

**7. Functions and sequences of each block**

7.1 LED matrix driver

LED matrix driver block (LED 0 to 16, Y0 to 6) can control each driver independently.

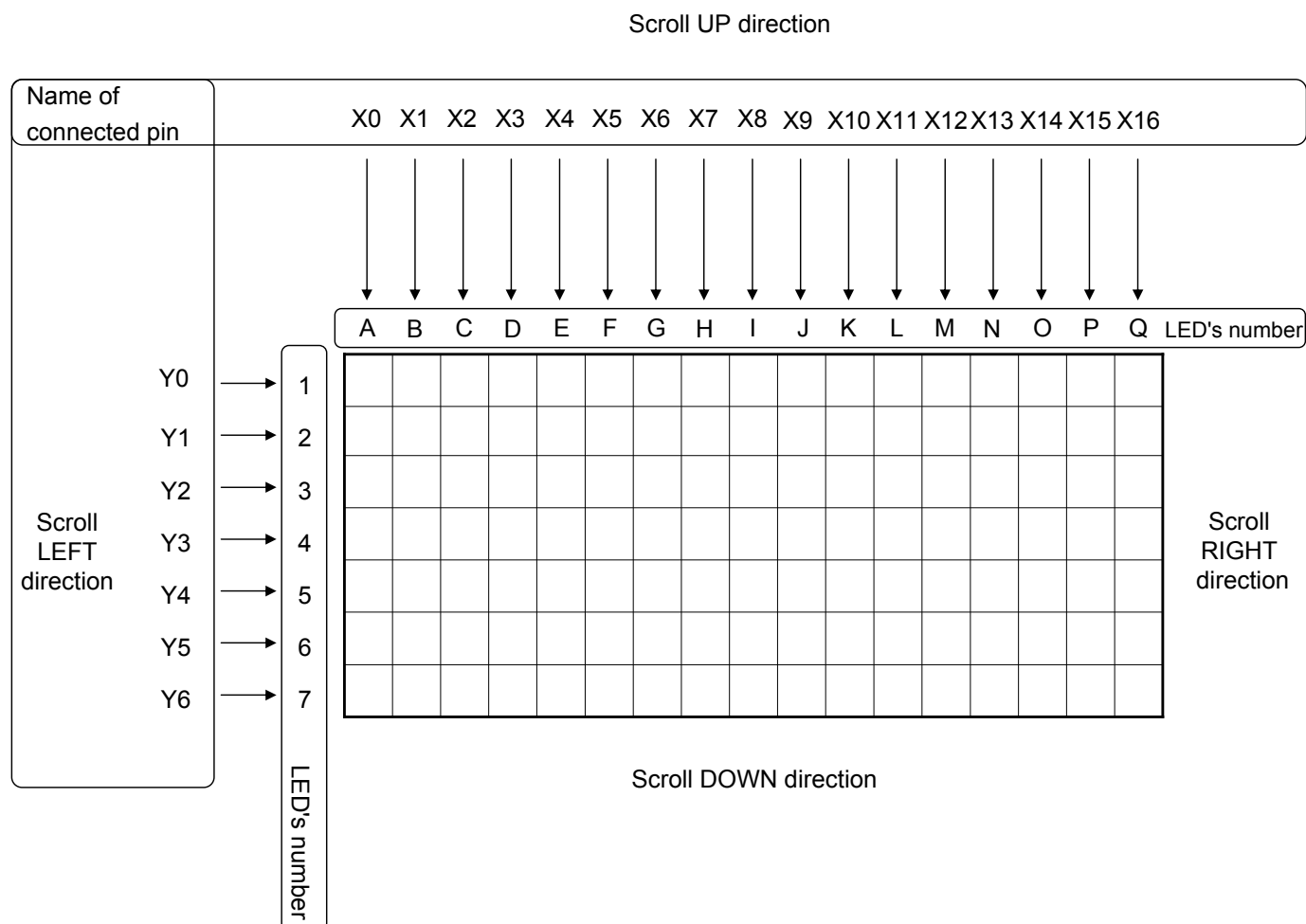
LED matrix driver can perform current value settings and firefly settings to 119 LEDs respectively.

LED matrix driver circuit can display characters and patterns by controlling the 7 × 17 matrix LED individually.

In this specification, LED's number controlled by each terminal can be matched off against the following figure.

Internal logic circuit is operated by the internal clock or the external clock which is input to EXTCLK (Pad No.43).

Maximum frequency of EXTCLK terminal is 1.44 MHz.



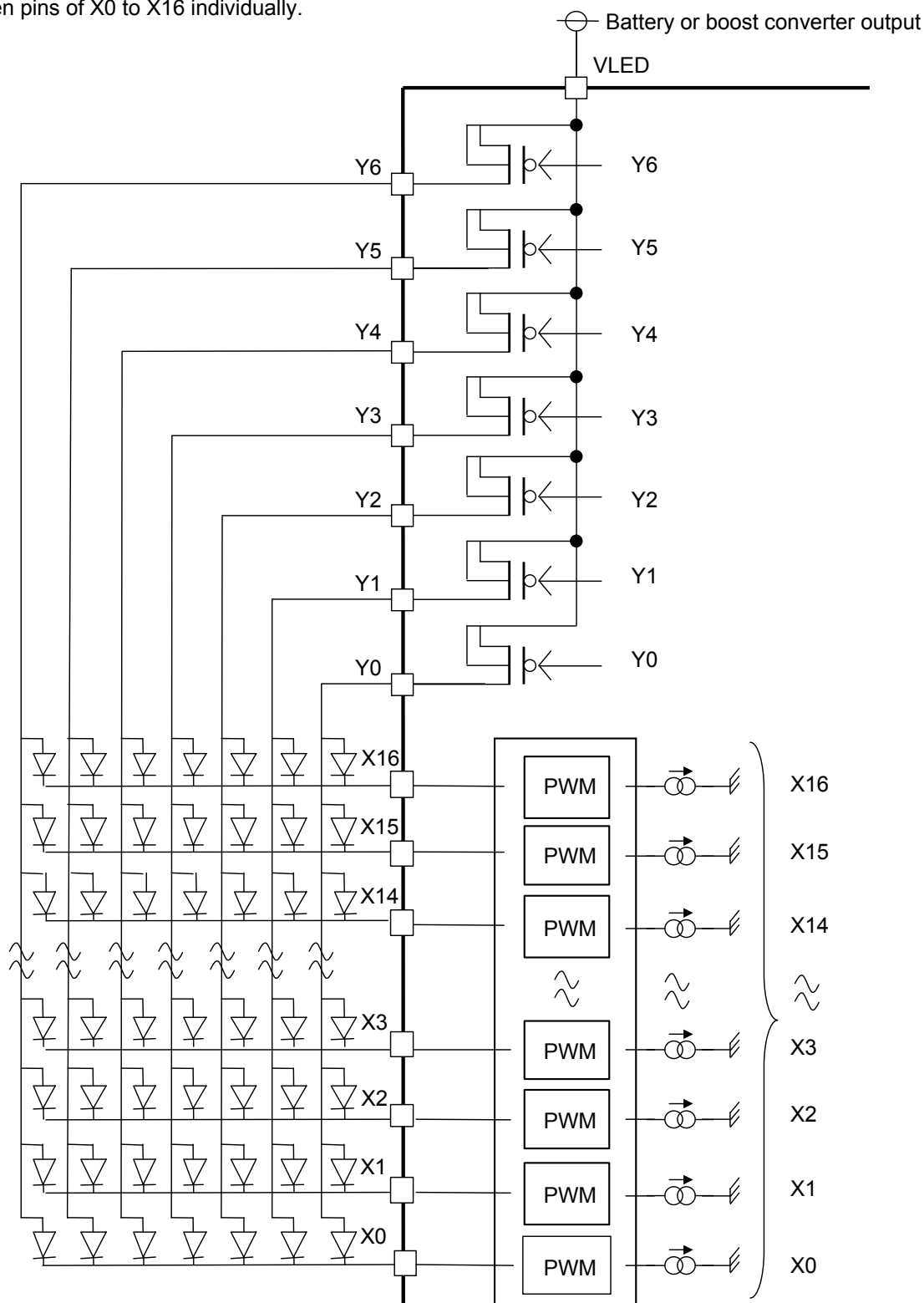
**OPERATION (continued)**

**7. Functions and sequences of each block (continued)**

7.1 LED matrix driver (continued)

Actual driver composition is shown in the following figure.

The anode of 17 LEDs is connected to seven pins of Y0 to Y6 respectively, and the cathode of 7 LEDs is connected to seven pins of X0 to X16 individually.



**OPERATION (continued)**

**7. Functions and sequences of each block (continued)**

7.1 LED matrix driver (continued)

The figure below shows a specific circuit configuration about Y0 to Y6 and X0.

(The actual LSI has 17 internal circuits of the same configuration as the figure below. See the previous page.)

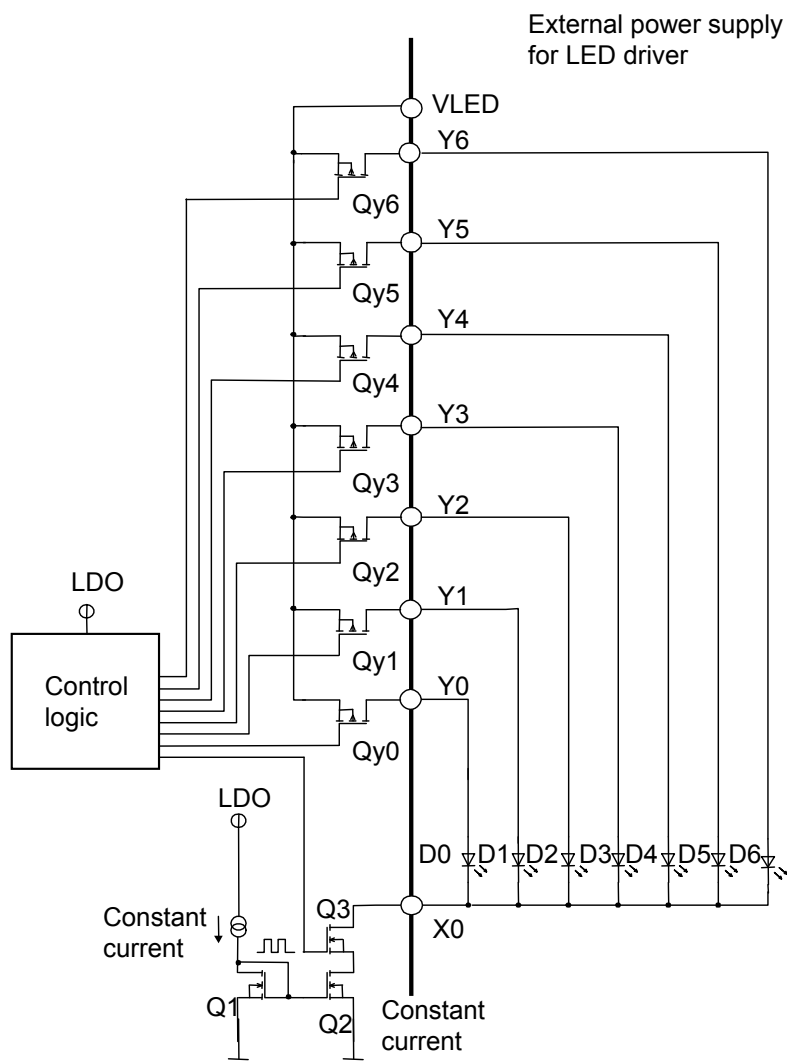
VLED1, 2 is the external power supply for LED driver in this circuit.

2 pins are used because impedance of the power supply line is lowered. Connect the power supply to both pins when the circuit pattern is designed actually.

In the side from Y0 to Y6, the gate voltage in the internal control logic circuit is controlled and the P-ch MOS switch (Qy0 to Qy6) is turned ON/OFF.

In the X0 side, Q1, Q2 compose the constant current. Q3 operates as a SW and controls ON/OFF of the gate voltage with the control logic. Moreover, it is possible to change luminance by variable current value with the serial control. For example, when Qy0 is ON (gate voltage : Low) and Q3 is ON (gate voltage : High), a current flows into D0, and then the LED will light up.

Internal LDO (1.85 V) is used for power supply of the internal logic circuit.





**OPERATION (continued)**

**7. Functions and sequences of each block (continued)**

7.1 LED matrix driver (continued)

Y0 to Y6 operating description

The timing chart at operating is shown in below figure.

External clock frequency from EXTCLK pin (Pad. No. 43) is a timing controller.

It is controlled by the internal 1.2 MHz clock in default condition.

It is possible to switch as follows by setting of register 06h : D0.

0 : Internal clock 1 : EXTCLK input

In the case of different input frequency, calculate the time on the basis of the number of clocks written together.

Y side switches from Y0 to Y6 by turns.

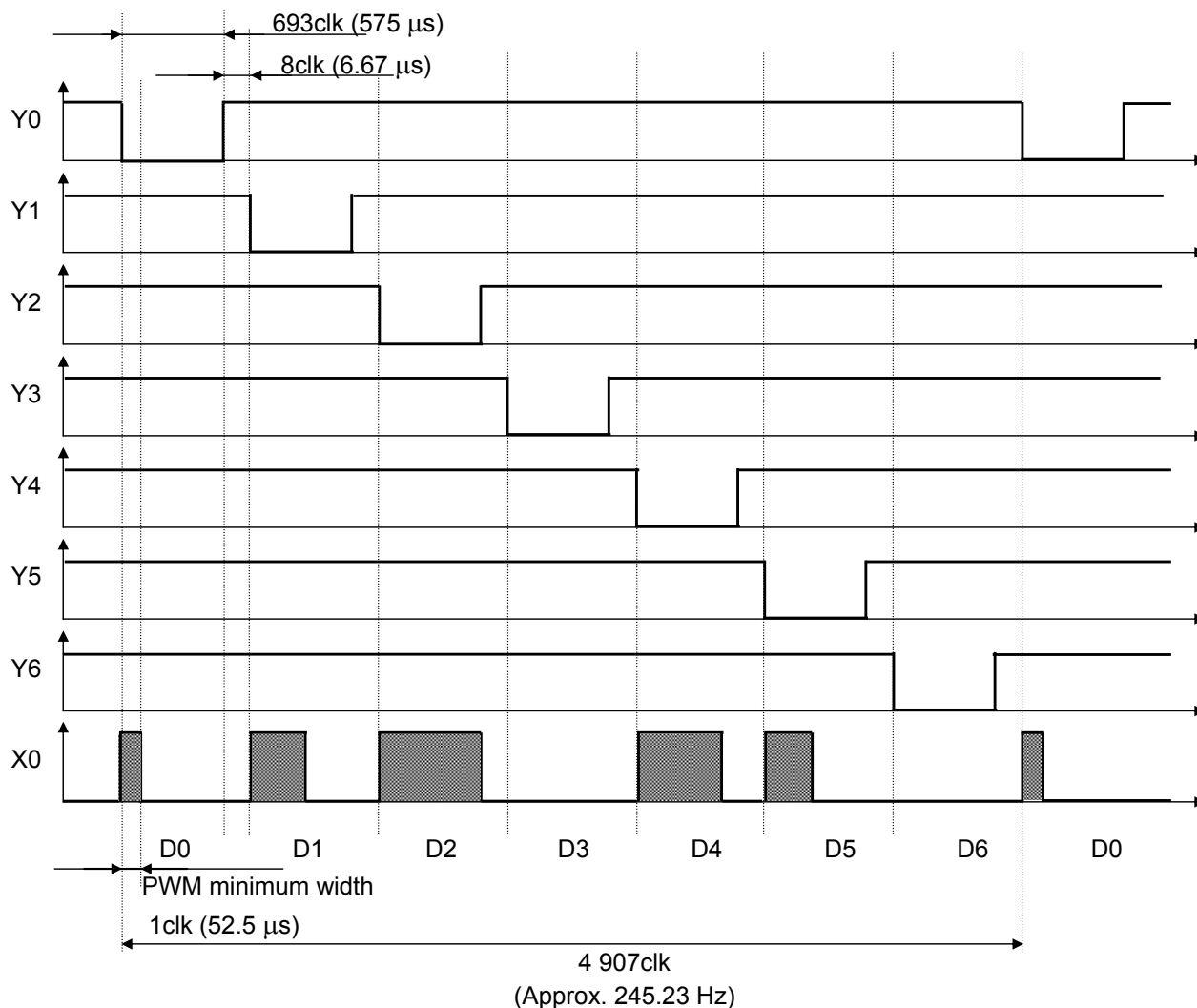
The turning on term of each pin is constant 693clk (575 μs) and each turning on term includes 8CLK(6.67 μs) interval.

Black squares show the turning on term and D3 and D6 are the turning off term in below figure.

7 × 17 matrix display is controlled by X1 to X 16 with line control.

The following waveform is an internal signal.

At Yx = Xx = Low, the waveform of actual Yx terminal is set to Hi-Z.



**OPERATION (continued)**

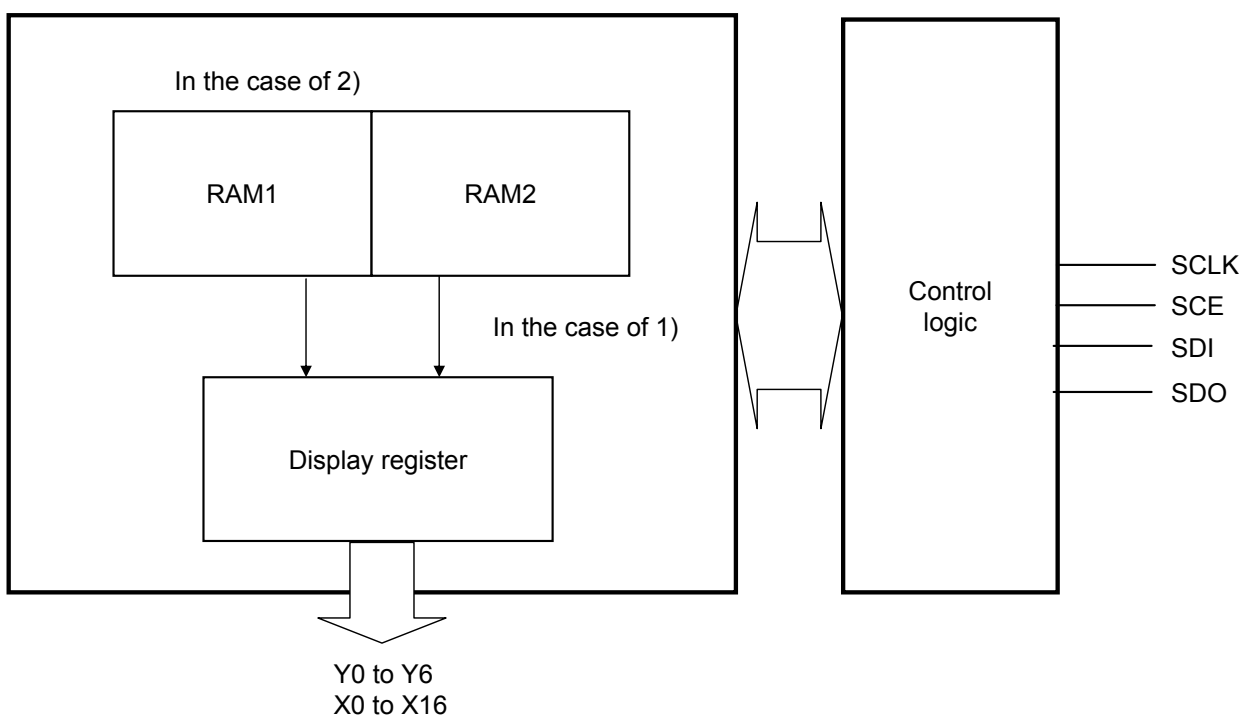
**7. Functions and sequences of each block (continued)**

7.2 Display method of RAM1, RAM2

This LSI has RAM 238 byte (7 × 17 matrix 2-side) for display.  
 There are the two following patterns as the dot matrix display.

- 1) RAM write data display
- 2) Scroll display

In the case of 1), RAM data is directly transmitted to a display register, and the dot matrix is displayed.  
 In the case of 2), scroll processing is performed on RAM and the contents are transmitted to a display register.  
 Block diagram is shown below.



Internal memory address 08h map

| Memory address | Function     |
|----------------|--------------|
| 00             | All "0" data |
| 01             | RAM1         |
| 10             | RAM2         |
| 11             | All "0" data |

## OPERATION (continued)

### 7. Functions and sequences of each block (continued)

#### 7.2 Display method of RAM1, RAM2 (continued)

There are the three following items in the parameter of display change.

1) Luminance

Current value can be set as 16 steps from 0 mA to 20 mA.

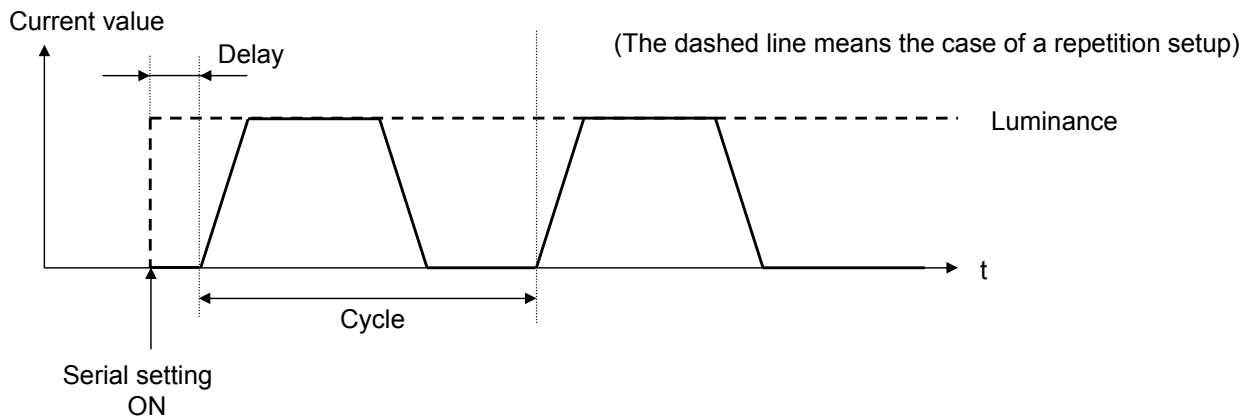
2) Cycle

A luminance variation is periodically repeated like fluorescence at always lit or the cycle of 1 s /2 s /3 s.

3) Delay

It can change the time (no delay or 25%, 50%, 75% of the cycle) from the timing of serial setup ON to the timing of which current starts to flow into the LED driver.

Change parameter image



## OPERATION (continued)

### 7. Functions and sequences of each block (continued)

#### 7.3 Setting for PWM lighting

##### (1) Display the contents of RAM

In the case of the contents of RAM, it is necessary to perform the display setup by the  $7 \times 17$  matrix for every LED to display.

In the case of RAM display, the setup of luminosity, cycle, and delay is possible.

Ex.) LED of A1 to made to lit up

##### 1-1) When using internal CLK

02h Write 00000001 When 02h : D0 is set to 1, internal oscillator is ON.

##### 1-2) When using external CLK (1.44 MHz<sub>max</sub>)

06h Write 00000001 When 06h : D0 is set to 1, please input from the exterior after setting it as EXTCLK operation.

Note) Be sure to set 1-1) or 1-2) first.

- 2) 01h Write 00000001 Change the register map
- 3) 03h Write 01010000 A1 display specification : 5 mA, the always lighting, no delay
- 4) 01h Write 00000000 Change the register map
- 5) 08h Write 00000001 RAM1 display specification
- 6) 07h Write 00000001 Matrix display ON setup

Note) Be sure to set 6) finally.

By the above command instructions, the continuation display of the contents of RAM corresponding to RAM1 can be performed.

When making all the LED of  $7 \times 17$  lit up, it is necessary to perform instructions of 3) to all the LED (from 03h to 79h) of A1to Q7.

The setup of luminosity , cycle, and delay by the setup of 03h to 79h is shown in the following page.

**OPERATION (continued)**

**7. Functions and sequences of each block (continued)**

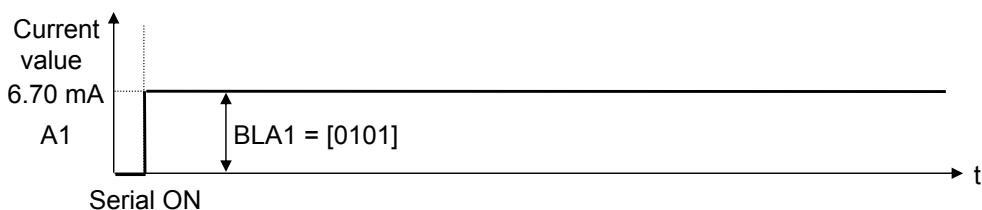
7.3 Setting for PWM lighting (continued)

(1) Display the contents of RAM (continued)

Setting for lighting Ex.

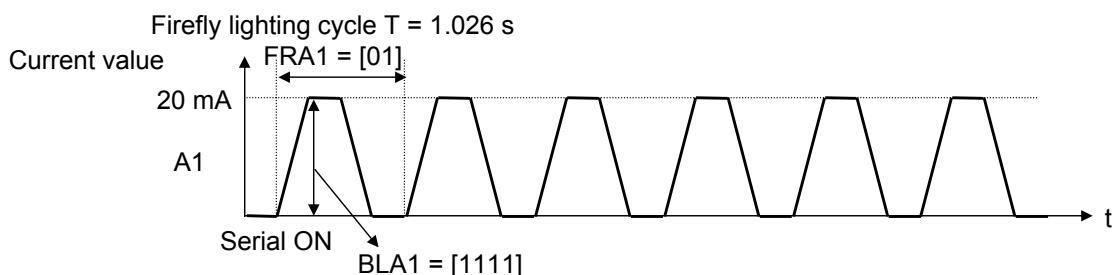
1) Example of initial setting for lighting always lighting

|           |   |   |   |           |   |           |   |
|-----------|---|---|---|-----------|---|-----------|---|
| BLA1[3:0] |   |   |   | FRA1[1:0] |   | DLA1[1:0] |   |
| 0         | 1 | 0 | 1 | 0         | 0 | 0         | 0 |



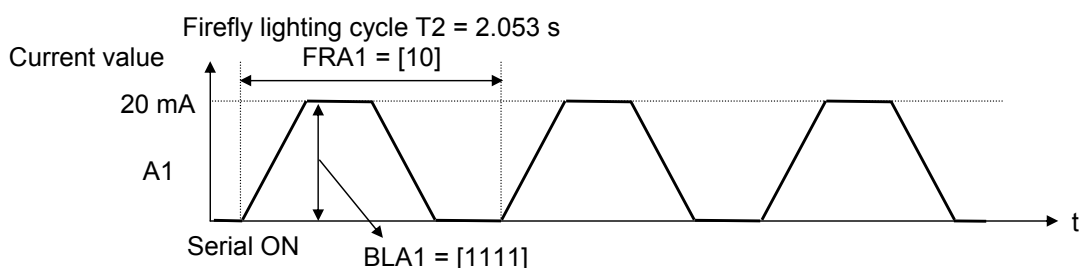
2) Firefly lighting 1 s

|           |   |   |   |           |   |           |   |
|-----------|---|---|---|-----------|---|-----------|---|
| BLA1[3:0] |   |   |   | FRA1[1:0] |   | DLA1[1:0] |   |
| 1         | 1 | 1 | 1 | 0         | 1 | 0         | 0 |



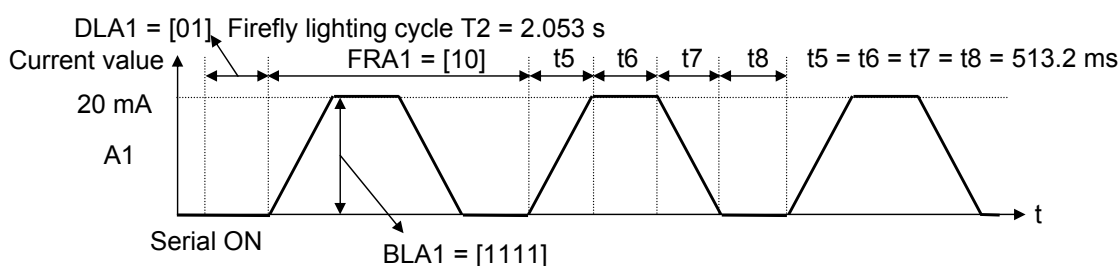
• Cycle change 1 s → 2 s

|           |   |   |   |           |   |           |   |
|-----------|---|---|---|-----------|---|-----------|---|
| BLA1[3:0] |   |   |   | FRA1[1:0] |   | DLA1[1:0] |   |
| 1         | 1 | 1 | 1 | 1         | 0 | 0         | 0 |



• Delay change 0 → 25%

|           |   |   |   |           |   |           |   |
|-----------|---|---|---|-----------|---|-----------|---|
| BLA1[3:0] |   |   |   | FRA1[1:0] |   | DLA1[1:0] |   |
| 1         | 1 | 1 | 1 | 1         | 0 | 0         | 1 |



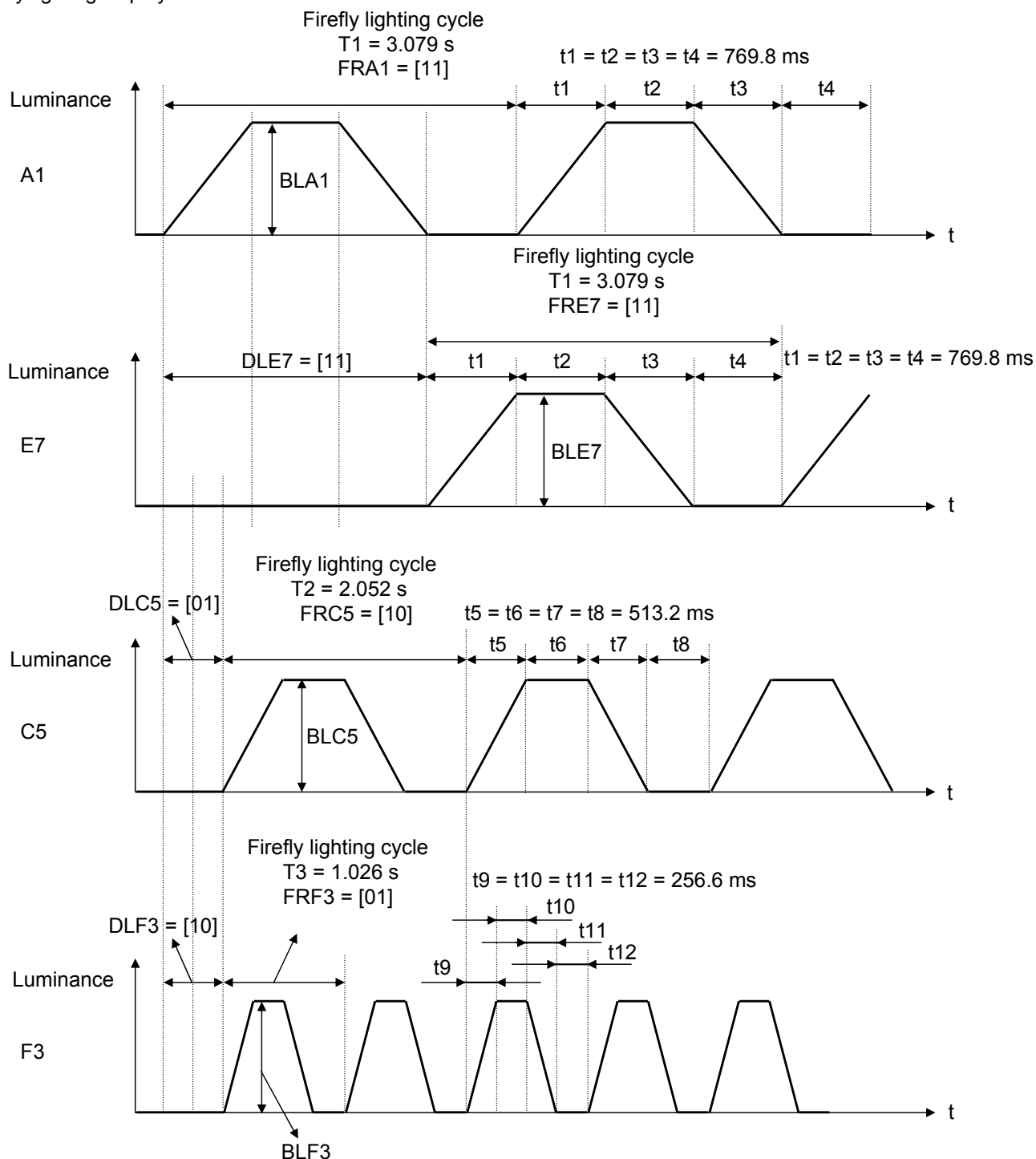
**OPERATION (continued)**

**7. Functions and sequences of each block (continued)**

7.3 Setting for PWM lighting (continued)

(1) Display the contents of RAM (continued)

Firefly lighting display



**OPERATION (continued)**

**7. Functions and sequences of each block (continued)**

7.3 Setting for PWM lighting (continued)

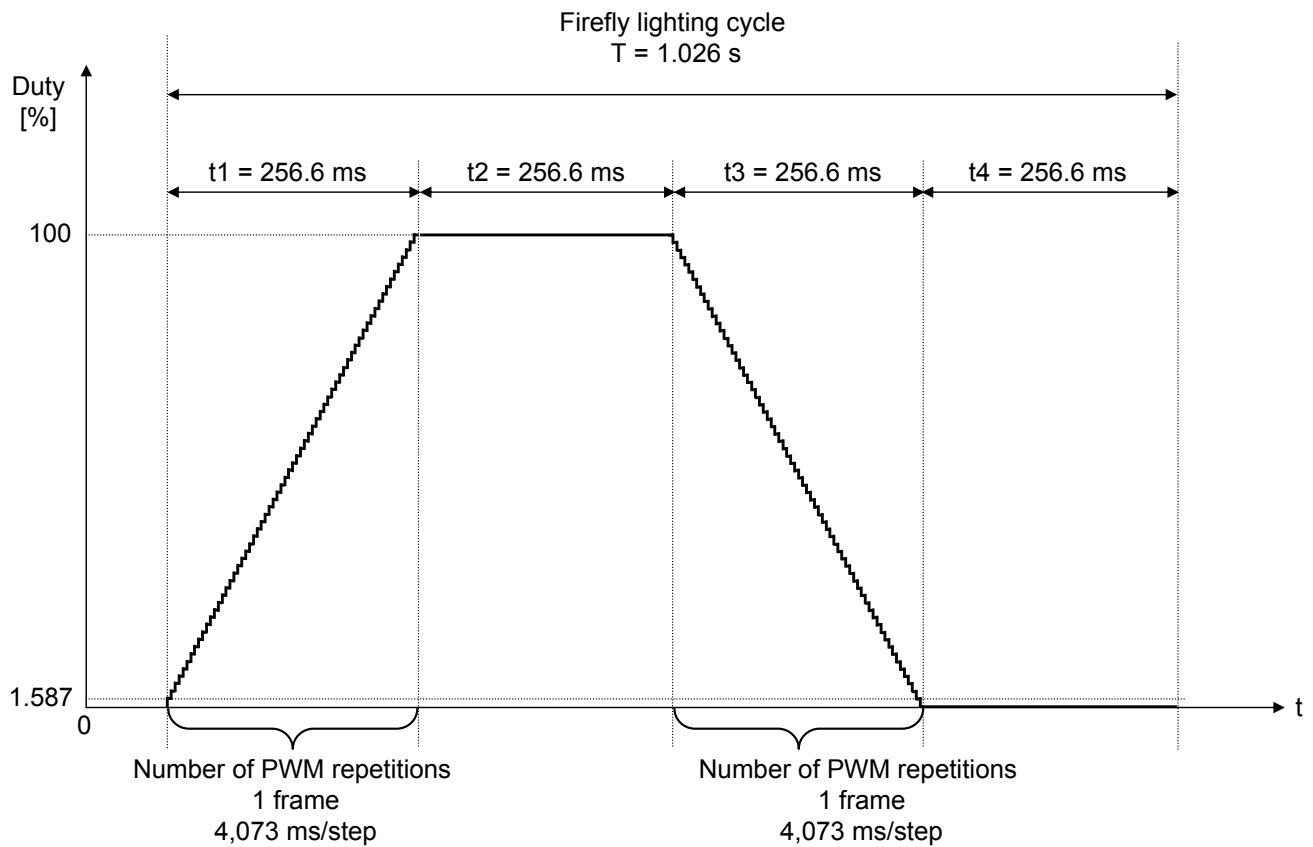
(1) Display the contents of RAM (continued)

Firefly lighting display (continued)

The following time is the time that an internal clock is the typical value (1.2 MHz).

And it is an example when setting a lighting cycle to 1s.

(When setting to 2 s or 3 s, each time becomes twice or 3 times.)



## OPERATION (continued)

### 7. Functions and sequences of each block (continued)

#### 7.3 Setting for PWM lighting (continued)

##### (2) Scroll display

By inputting 0Ah 00000001, the specified character can be scrolled for display from the left to the right.

(The scroll direction can be changed by the setup of 0Bh.)

The display moves every one row in specified scroll time.

(The scroll time can be changed by the setup of 0Bh.)

Ex.) The arbitrary display data is scrolled for display.

##### 1-1) When using the internal CLK

02h Write 00000001 When 02h : D0 is set to 1, the internal oscillator is ON.

##### 1-2) When using the external CLK (1.44 MHz<sub>max</sub>)

06h Write 00000001 When 06h : D0 is set to 1, please input CLK from the exterior after setting as EXTCL operation.

Note) Be sure to set 1-1) or 1-2) first.

- 2) 01h Write 00000001 The register map is switched.
- 3) 02h Write 00000000 RAM1 selection
- 4) 03h ~ 79h Write The lighting data of A1 to Q7 is set.
- 5) 02h Write 00000001 RAM2 selection
- 6) 03h ~ 79h Write The lighting data of A1 to Q7 is set.
- 7) 01h Write 00000000 The register map is switched.
- 8) 0Bh Write 00001000 The scroll time and the scroll direction are set.
- 9) 0Ah Write 00000001 SCLON
- 10) 07h Write 00000001 MTXON
- 11) After the output of INT (Pin B7) changes to High, 05h Read D1[1] is confirmed.
- 12) 01h Write 00000001 The register map is switched.
- 13) 03h ~ 79h Write The lighting data of A1 to Q7 is set. (Write to the empty RAM.)
- 14) 01h Write 00000000 The register map is switched.
- 15) After the output of INT (Pin B7) changes to High, 05h Read D1[1] is confirmed.
- 16) 01h Write 00000001 The register map is switched.
- 17) 03h ~ 79h Write The lighting data of A1 to Q7 is set. (Write to the empty RAM.)
- 18) 01h Write 00000000 The register map is switched.
- 19) After the output of INT(Pin B7) changes to High, 05h Read D1[1] is confirmed.
- 20) The step of 16) to 19) is repeated in the request times.



**OPERATION (continued)**

**7. Functions and sequences of each block (continued)**

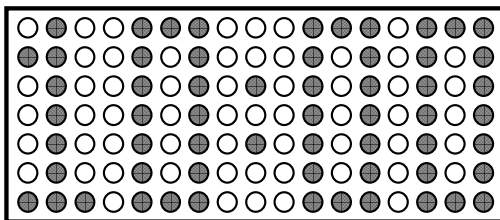
7.3 Setting for PWM lighting (continued)

(2) Scroll display (continued)

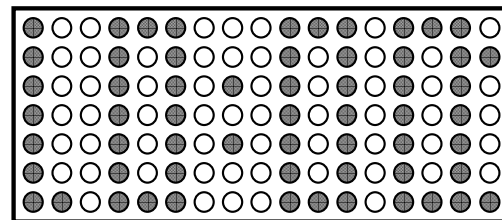
The scroll time and the scroll direction can be changed by the setting of 0Bh register.

The scroll time means the time that the display changes the (a) state to the (b) state in the following figure, that is the display shifts one row in case the scroll direction is the left (0Bh setup is LEFT). The initial setting is 0.1 s.

During scroll operation, only the setup of the luminance [D7-4] is enabled, the setups of Delay [D1-0] and the firefly [D3-2] are disabled on the data of Address 03h to 79h.



(a)



(b)

**OPERATION (continued)**

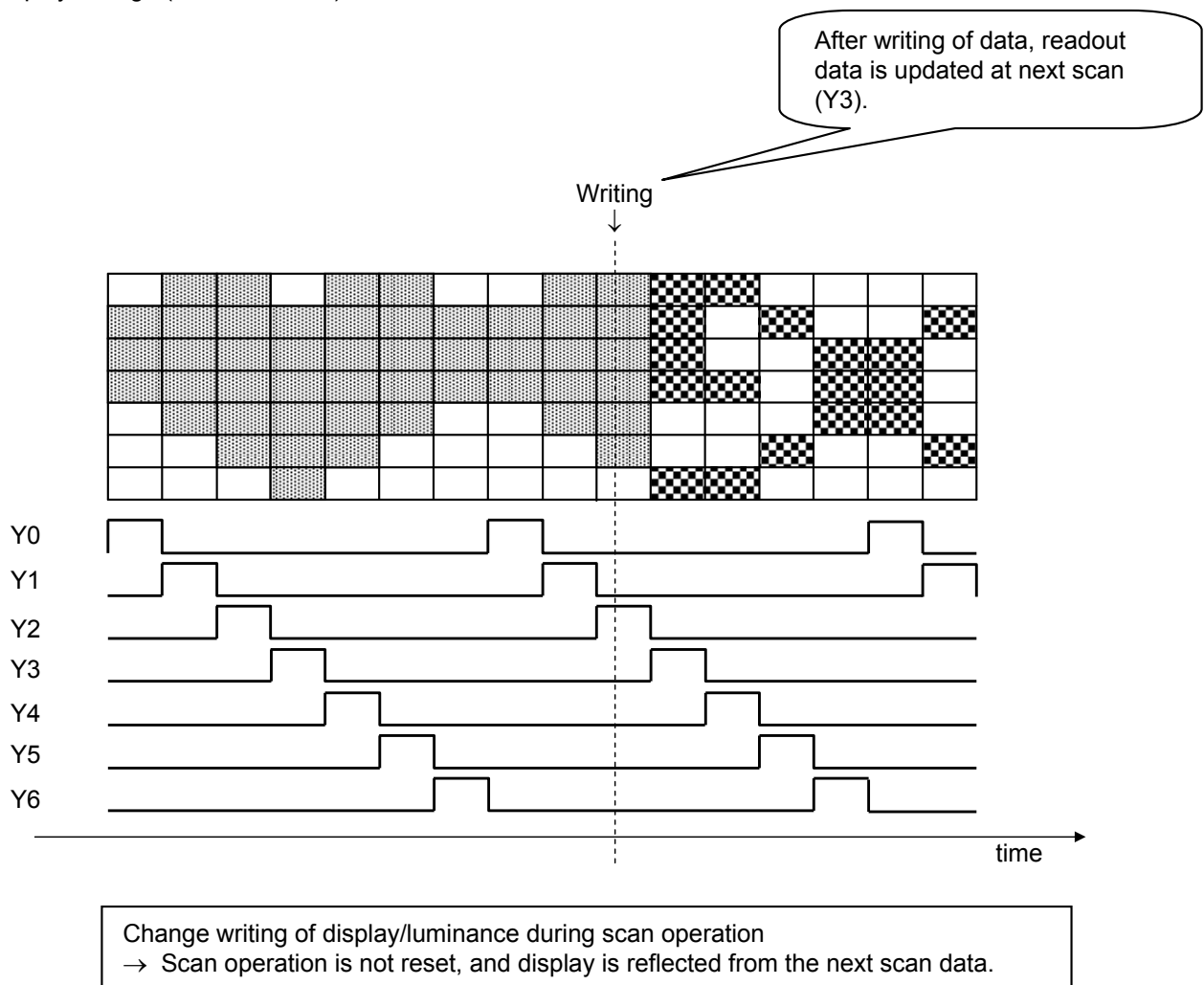
**7. Functions and sequences of each block (continued)**

7.4 Operation at Matrix block RAM data change (1)

Matrix LED display / Luminance change

1. Display / Luminance change Writing  
↓
2. Scan maintains the present state. ( No Reset)  
↓
3. Data is updated from next scan

Ex.) Display change (Heart → Clock)



**OPERATION (continued)**

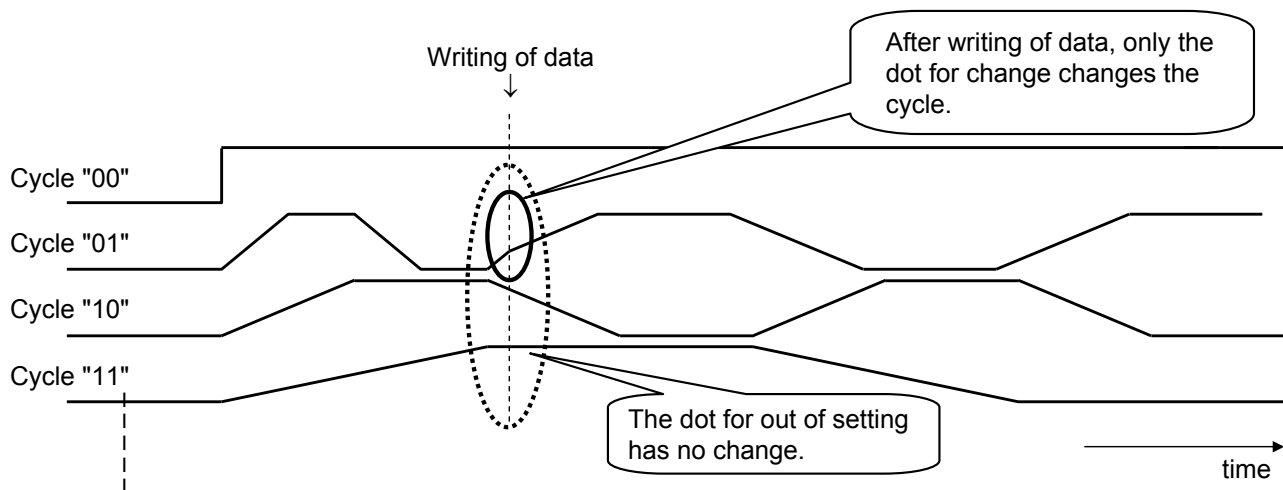
**7. Functions and sequences of each block (continued)**

7.4 Operation at Matrix block RAM data change (2)

Matrix LED Firefly Cycle change

1. Cycle change Writing  
↓
2. Only cycle change dot changes cycle (No Reset)

Ex.) Cycle change ("01" → "10")



Change writing of cycle  
→ Only the dot for change of cycle is not reset, cycle change is reflected.

**OPERATION (continued)**

**7. Functions and sequences of each block (continued)**

7.4 Operation at Matrix block RAM data change (3)

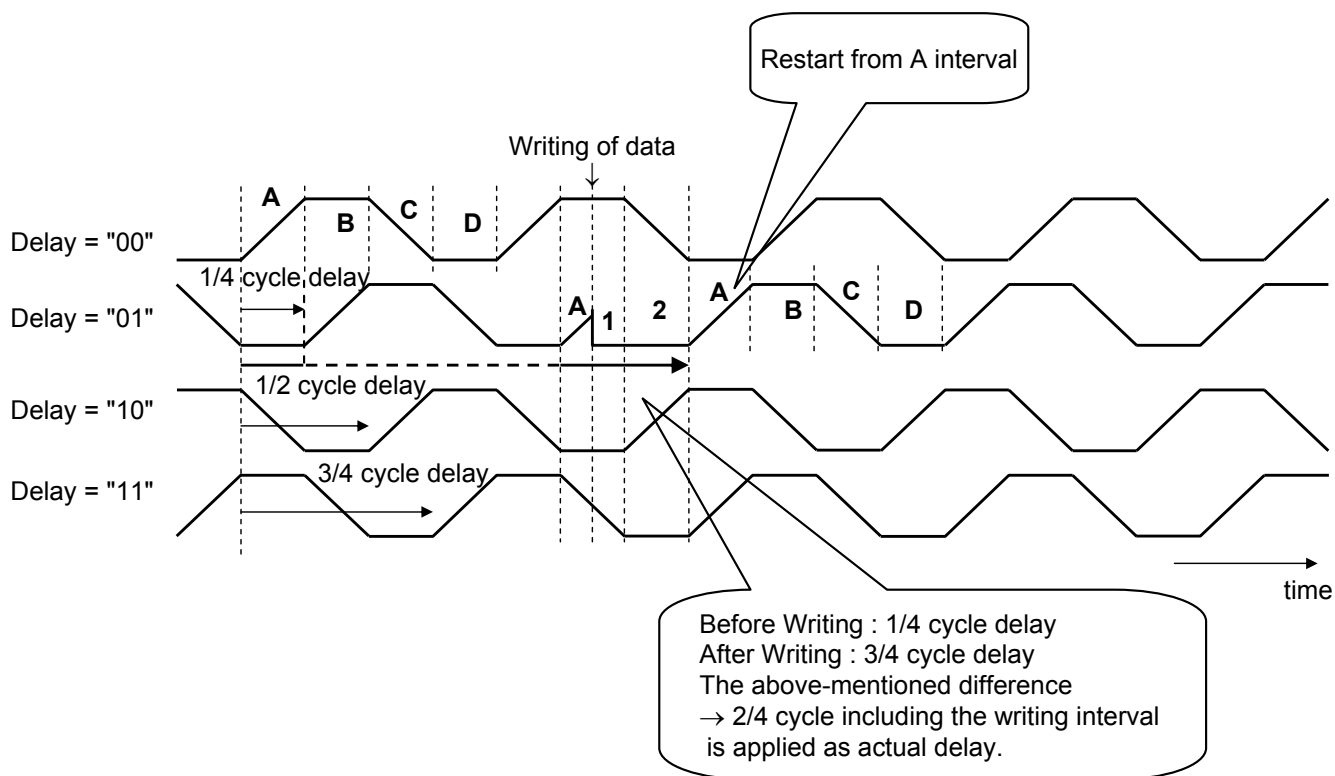
Matrix LED Firefly Cycle Delay change

(1) Delay change at A interval

1. Delay change Writing
- ↓
2. Reset / Only the dot for change is RESET
- ↓
3. The difference of a Delay setup before and after writing is applied as actual Delay.
- ↓
4. The dot for change restart from A interval.

Ex.) Delay change ("01" → "11")

(1) Delay change at A interval (at the increase of Duty)



**OPERATION (continued)**

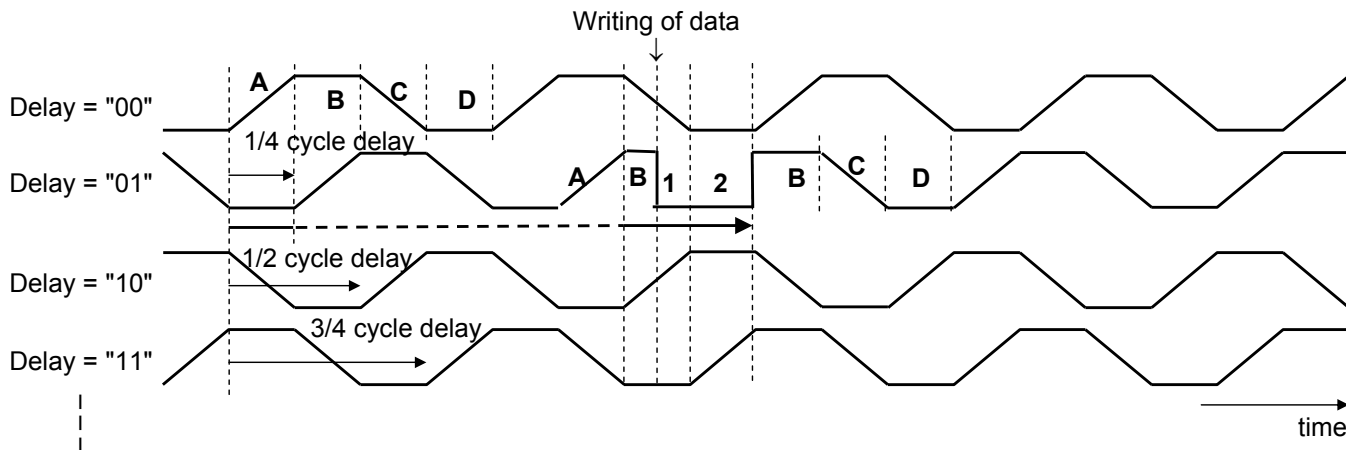
**7. Functions and sequences of each block (continued)**

7.4 Operation at Matrix block RAM data change (4)

Matrix LED Firefly Cycle Delay change (continued)

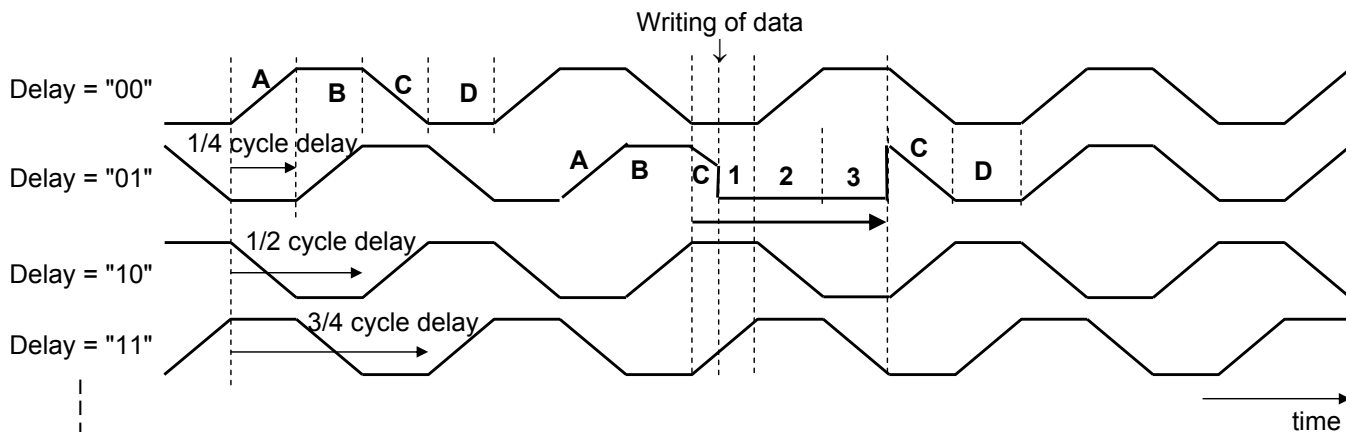
Ex.) Delay change ("01" → "11")

(2) Delay change at B interval (at Duty 100%)



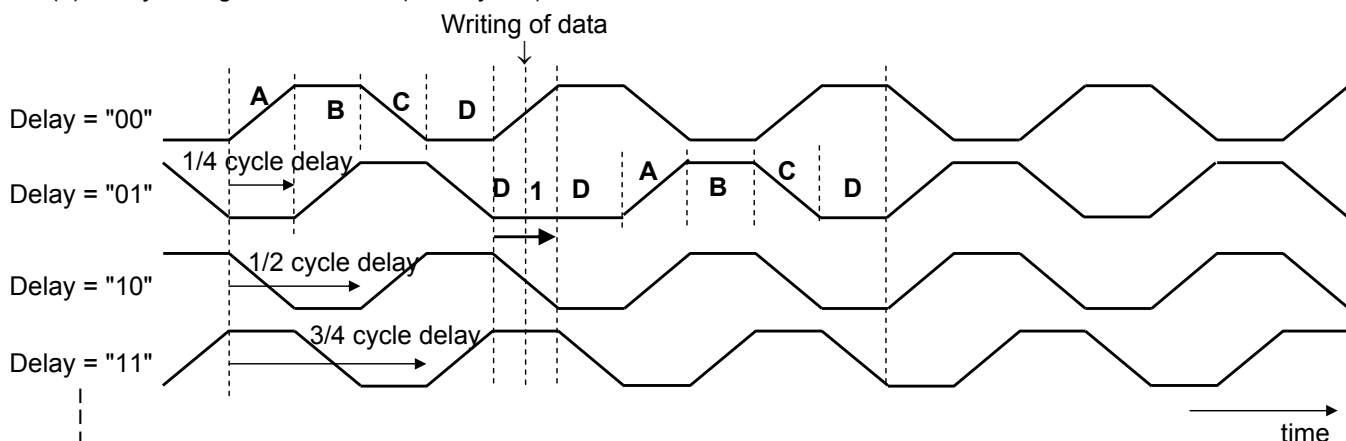
Ex.) Delay change ("01" → "00")

(3) Delay change at C interval (at the decrease of Duty)



Ex.) Delay change ("01" → "10")

(4) Delay change at D interval (at Duty 0%)



## OPERATION (continued)

### 7. Functions and sequences of each block (continued)

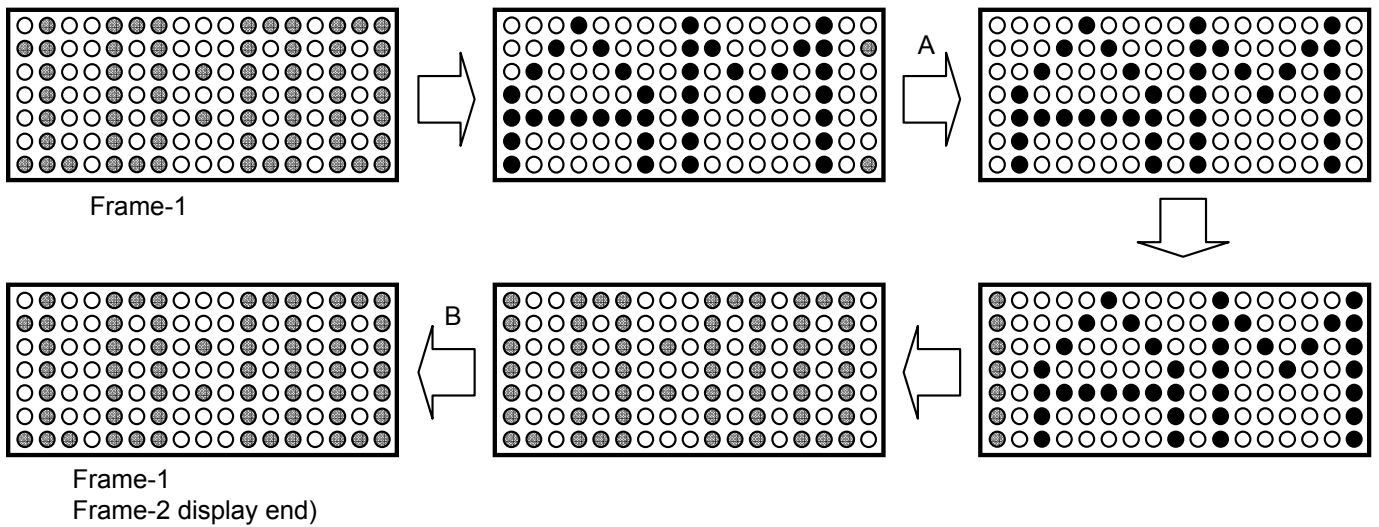
#### 7.5 FRMINT generation timing

operating description example

Write "10:00" to RAM1

Write "A M" to RAM2

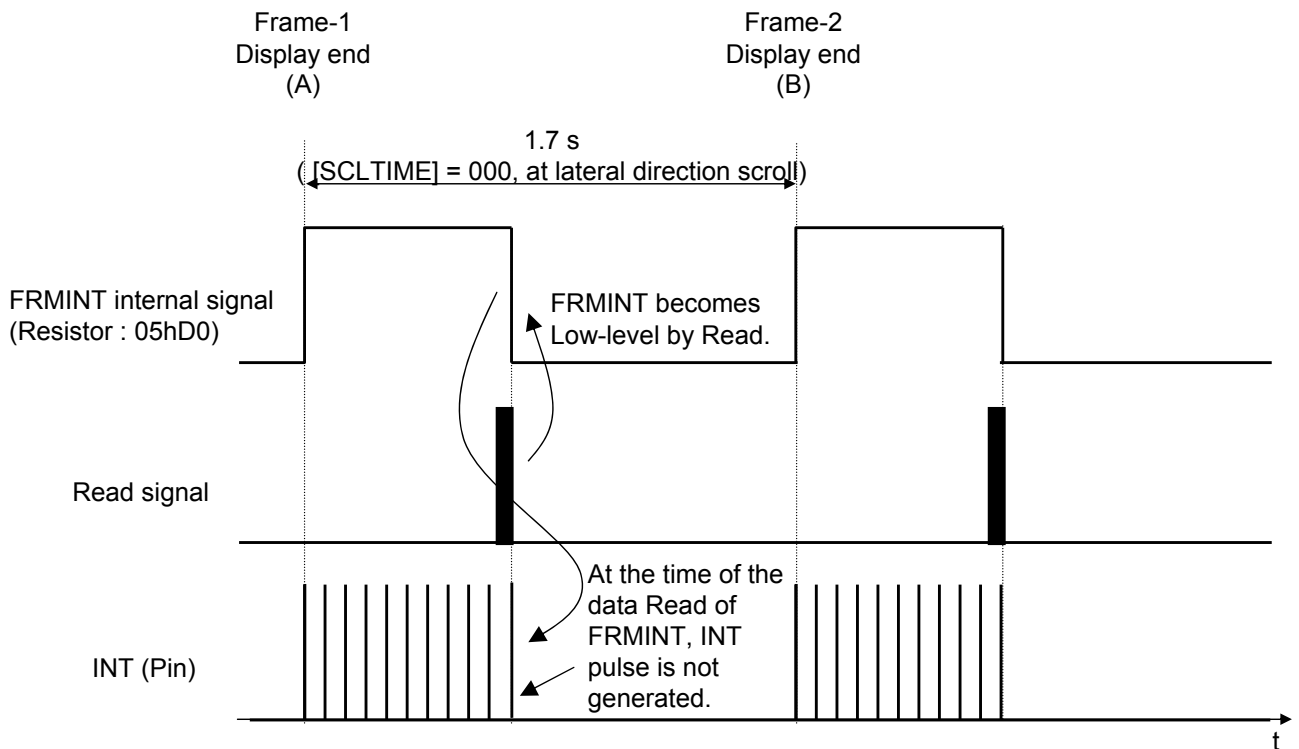
At setup of [SCLTIME] = [000] (0.1 s)



## OPERATION (continued)

### 7. Functions and sequences of each block (continued)

#### 7.5 FRMINT generation timing (continued)



FRMINT signal is generated when 1 frame display during scroll display ends. (Ex. Refer to A)

For example, in case that the setting value is set to [SCLTIME] = 000 (0.1 s), the scroll direction is lateral direction (right → left, left → right), FRMINT signal is generated every 1.7 s (SCLTIME 0.1 s × 17rows).

In case of longitudinal scroll direction (up → down, down → up), FRMINT signal is generated every 0.7 s (SCLTIME 0.1 s × 7 lines).

FRMINT signal changes Low-level at data read, INT pulse waveform is not generated. (Ex. Refer to B)

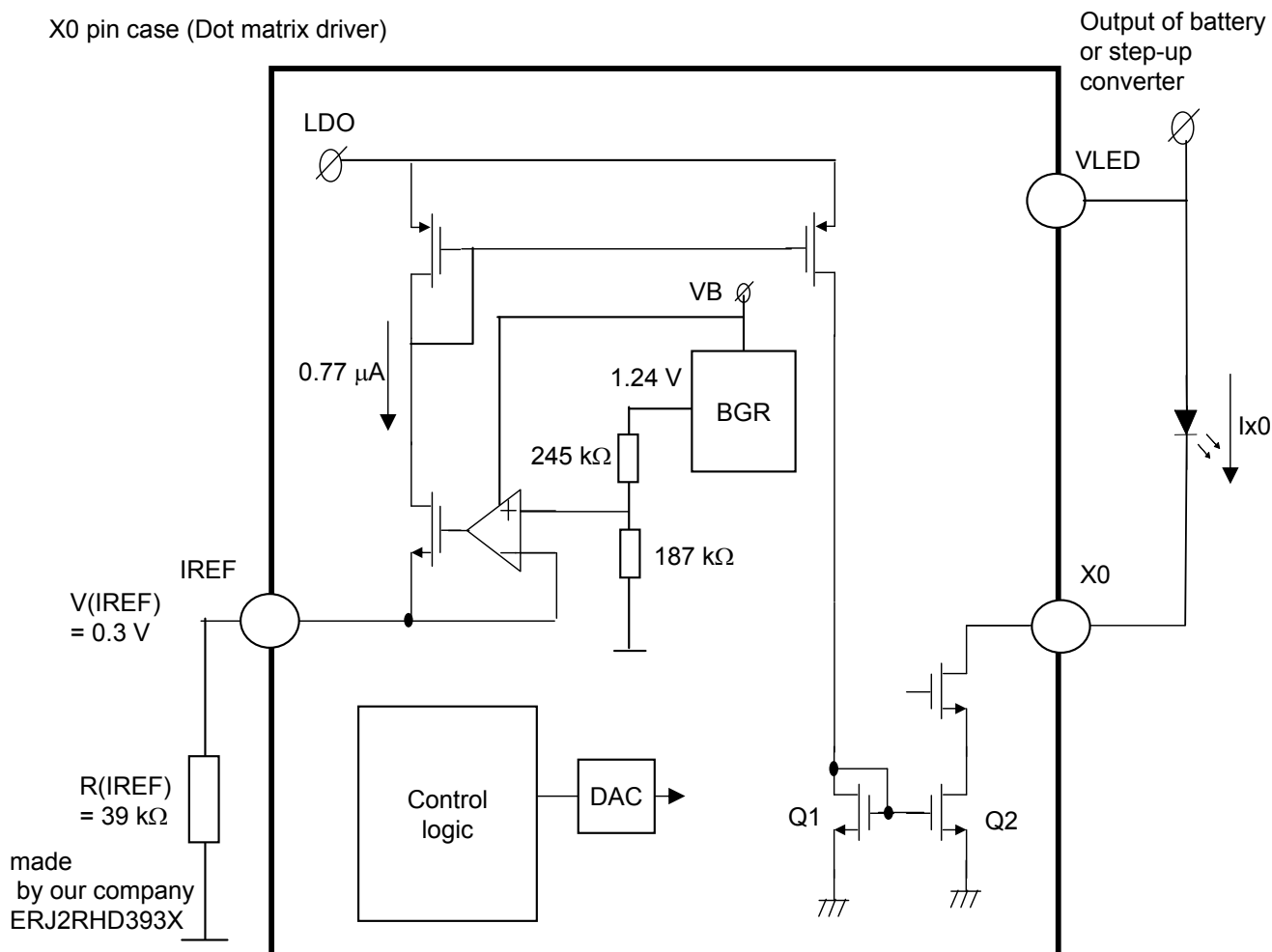
(FRMINT signal is always High-level during scroll if it is not performed data read.)

**OPERATION (continued)**

**7. Functions and sequences of each block (continued)**

7.6 Equivalent circuit example of constant current driver block

X0 pin case (Dot matrix driver)



The example of the constant current driver of matrix LED driver ( X0 pin ) is shown in the above figure.

The reference current for constant current driver is calculated by the following formula.

$$V ( IREF ) / R ( IREF ) = 0.3 \text{ V} / 39 \text{ k}\Omega = 0.77 \text{ }\mu\text{A}$$

The LED driver current (Ix0) can be set from 0 mA to 20 mA by adjusting the mirror ratio of Q1 and Q2 via serial interface at DAC (Refer to Page 38 for details).

When R ( IREF ) is changed into 78 kΩ twice as many as this as an example of change, a constant current value is set to 1/2 of each address setting values of Page 38.

( However, the accuracy of each current value in the case cannot be guaranteed.)

Moreover, keep in mind that the constant current value of all LED drivers is also set to 1/2 setting values.

V ( IREF ) precision is  $0.3 \pm 0.1 \text{ V}$ .

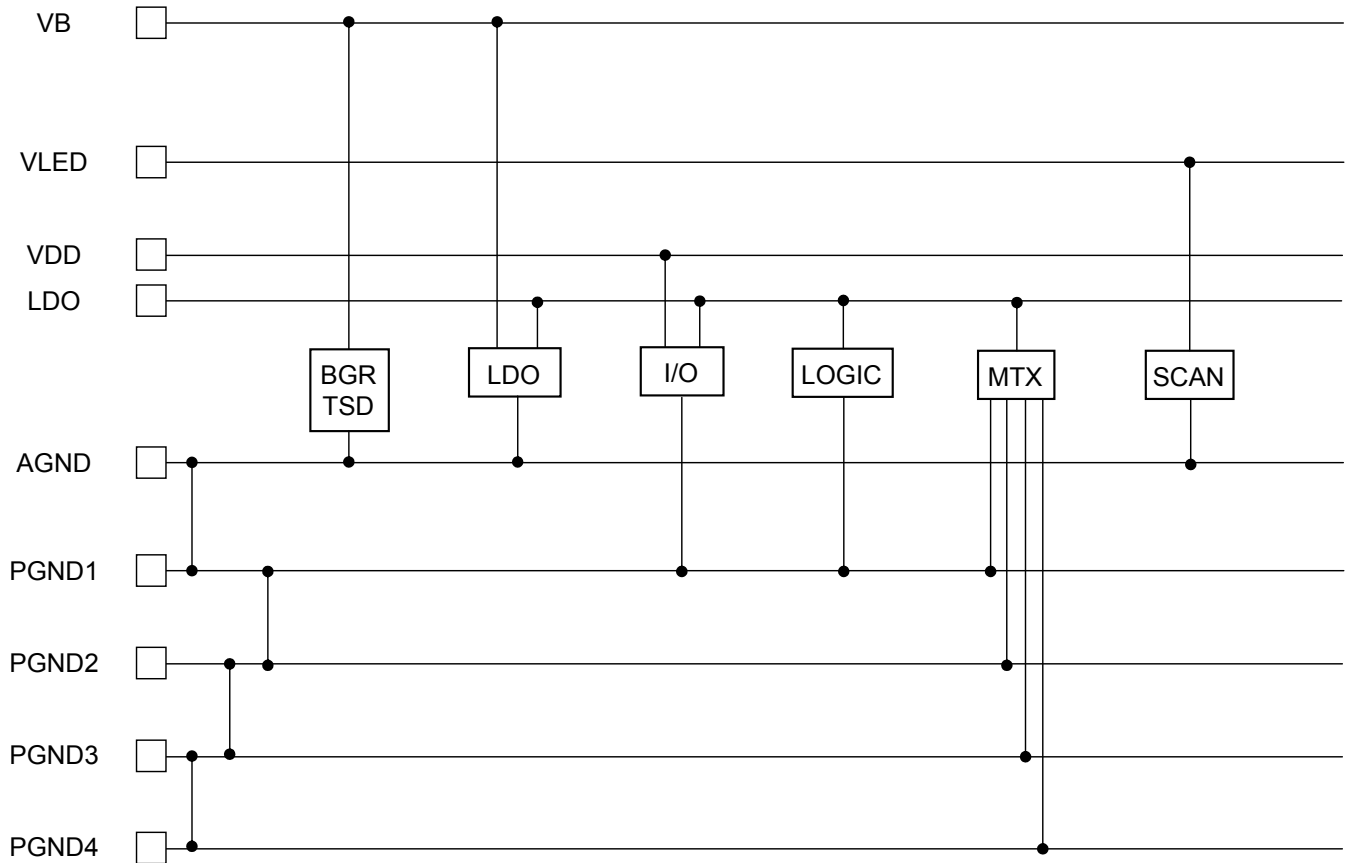
ERJ2RHD393X ( $\pm 0.5 \%$ ) is recommended for R ( IREF ) to keep the accuracy of constant current value for LED.





**OPERATION (continued)**

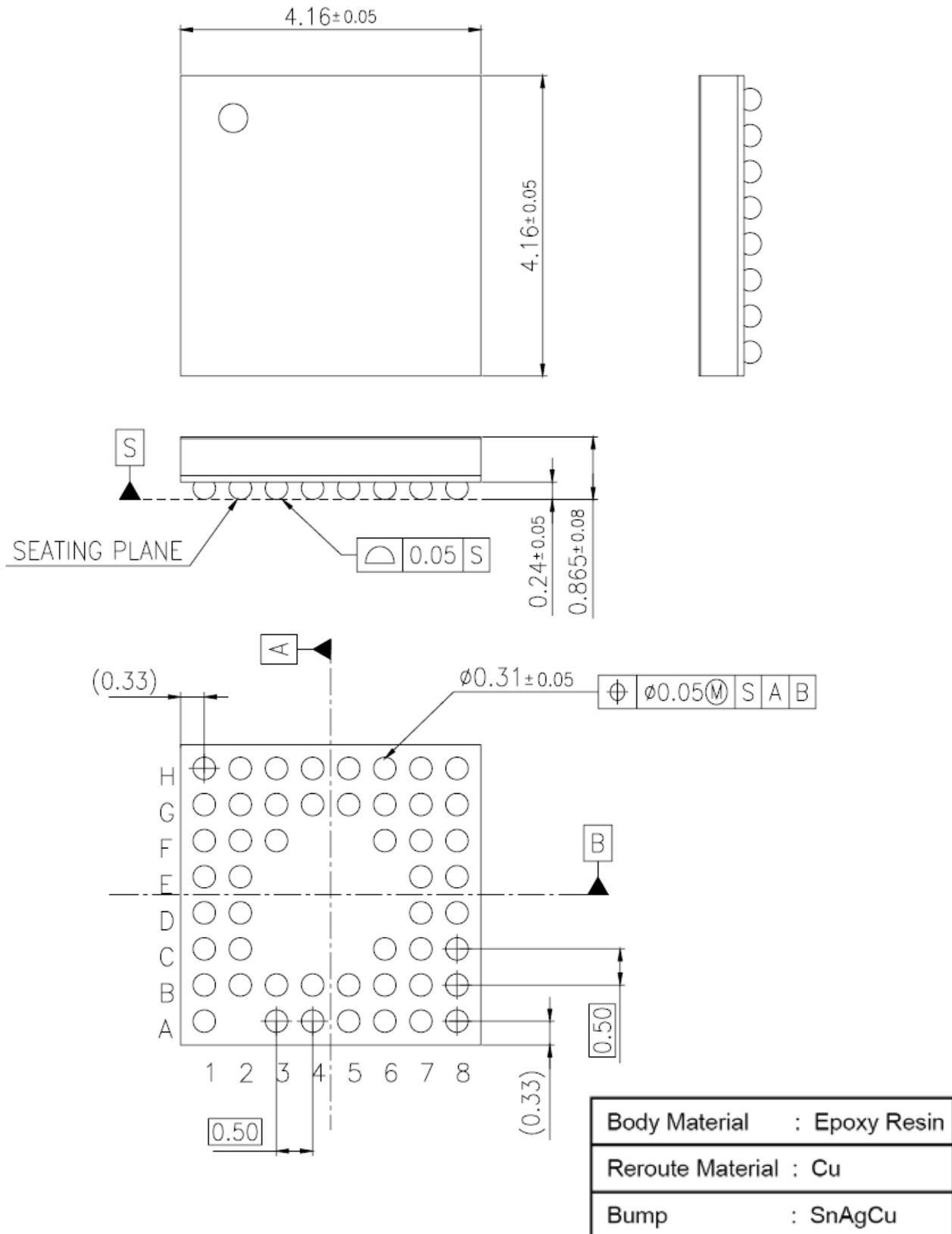
**8. Connections between power supplies**



**PACKAGE INFORMATION ( Reference Data )**

UBGA050-W-4242AEL

Unit:mm



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1. When using the LSI for new models, verify the safety including the long-term reliability for each product.
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Please read the notes to descriptions and the usage notes in the book.
3. This LSI is intended to be used for general electronic equipment.  
Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this LSI may directly jeopardize life or harm the human body.  
Any applications other than the standard applications intended.
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  - (4) Submarine transponder
  - (5) Control equipment for power plant
  - (6) Disaster prevention and security device
  - (7) Weapon
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6. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might emit smoke or ignite.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the semiconductor device. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
9. Take notice in the use of this product that it might be damaged or occasionally emit smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.  
Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.
11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
12. Verify the risks which might be caused by the malfunctions of external components.
13. Due to the unshielded structure of this LSI, functions and characteristics of the product cannot be guaranteed under the exposure of light. During normal operation or even under testing condition, please ensure that the LSI is not exposed to light.
14. Please ensure that your design does not have metal shield parts touching the chip surface as the surface potential is GND voltage.
15. Pay attention to the breakdown voltage of this LSI when using.  
More than + 1500 V or less than - 1500 V electrostatic discharge to all the pins might damage this product.

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