

# RF Power LDMOS Transistor

## N-Channel Enhancement-Mode Lateral MOSFET

This 30 W symmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 716 to 960 MHz.

### 780 MHz

- Typical Doherty Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Vdc,  $I_{DQA} = 450$  mA,  $V_{GSB} = 1.2$  Vdc,  $P_{out} = 30$  W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)
758 MHz	22.2	47.7	7.3	-29.3
780 MHz	22.1	47.9	7.3	-30.1
803 MHz	21.5	48.5	7.2	-31.4

### 880 MHz

- Typical Doherty Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Vdc,  $I_{DQA} = 450$  mA,  $V_{GSB} = 1.3$  Vdc,  $P_{out} = 30$  W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

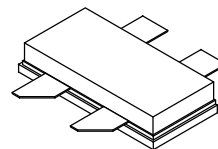
Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)
865 MHz	20.5	48.4	7.4	-31.5
880 MHz	20.5	48.6	7.4	-31.6
895 MHz	20.3	49.2	7.3	-31.6

### Features

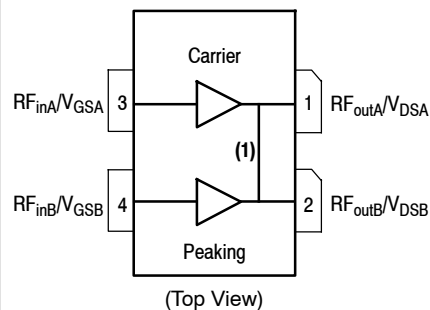
- Designed for Wide Instantaneous Bandwidth Applications
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Able to Withstand Extremely High Output VSWR and Broadband Operating Conditions
- Designed for Digital Predistortion Error Correction Systems
- In Tape and Reel. R3 Suffix = 250 Units, 32 mm Tape Width, 13-inch Reel.

**A2T07D160W04SR3**

**716–960 MHz, 30 W AVG., 28 V  
AIRFAST RF POWER LDMOS  
TRANSISTOR**



NI-780S-4L



**Figure 1. Pin Connections**

- Pin connections 1 and 2 are DC coupled and RF independent.

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +70	Vdc
Gate-Source Voltage	$V_{GS}$	-6.0, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature Range	$T_C$	-40 to +125	°C
Operating Junction Temperature Range (1,2)	$T_J$	-40 to +225	°C
CW Operation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	CW	94 0.87	W W/°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature $77^\circ\text{C}$ , 30 W W-CDMA, 28 Vdc, $I_{DQA} = 450\text{ mA}$ , $V_{GSB} = 1.2\text{ Vdc}$ , 780 MHz	$R_{\theta JC}$	0.63	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	IV

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics (4,5)**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 70\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 32\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	5	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics - Side A (4,6) (Carrier)**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 112\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.0	1.5	2.0	Vdc
Gate Quiescent Voltage ( $V_{DD} = 28\text{ Vdc}$ , $I_{DA} = 450\text{ mAdc}$ , Measured in Functional Test)	$V_{GS(Q)}$	1.7	2.2	2.7	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 1.12\text{ Adc}$ )	$V_{DS(on)}$	0.05	0.14	0.3	Vdc

**On Characteristics - Side B (4,6) (Peaking)**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 112\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.0	1.5	2.0	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 1.12\text{ Adc}$ )	$V_{DS(on)}$	0.05	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rtf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rtf>. Select Documentation/Application Notes - AN1955.
4.  $V_{DDA}$  and  $V_{ddb}$  must be tied together and powered by a single DC power supply.
5. Side A and Side B are tied together for these measurements.
6. Each side of device measured separately.

(continued)

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Functional Tests</b> <sup>(1,2,3)</sup> (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$ , $I_{DQA} = 450\text{ mA}$ , $V_{GSB} = 1.2\text{ Vdc}$ , $P_{out} = 30\text{ W Avg.}$ , $f = 803\text{ MHz}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	$G_{ps}$	20.2	21.5	23.2	dB
Drain Efficiency	$\eta_D$	46.0	48.5	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.8	7.2	—	dB
Adjacent Channel Power Ratio	ACPR	—	-31.4	-28.0	dBc

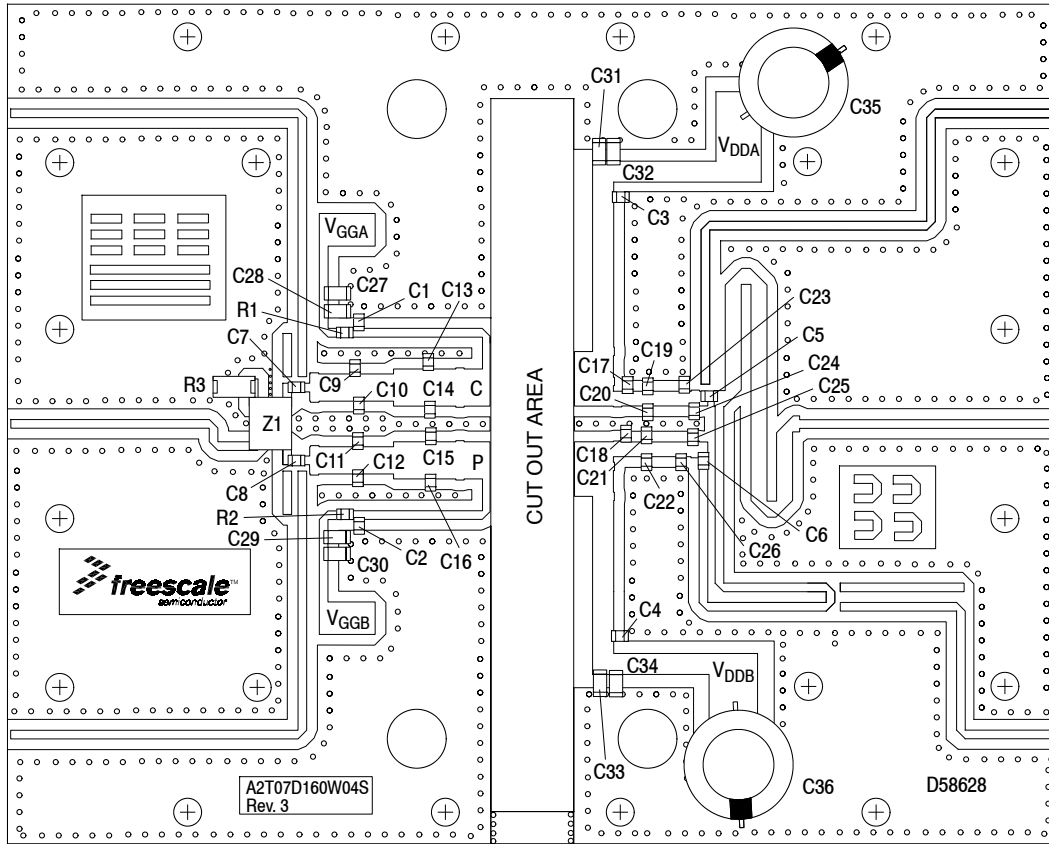
**Load Mismatch** <sup>(3)</sup> (In Freescale Doherty Test Fixture, 50 ohm system)  $I_{DQA} = 450\text{ mA}$ ,  $V_{GSB} = 1.2\text{ Vdc}$ ,  $f = 780\text{ MHz}$ 

VSWR 10:1 at 32 Vdc, 132 W Pulse Output Power (3 dB Input Overdrive from 85 W Pulse Rated Power)	No Device Degradation
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**Typical Performance** <sup>(3)</sup> (In Freescale Doherty Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQA} = 450\text{ mA}$ ,  $V_{GSB} = 1.2\text{ Vdc}$ , 758 to 803 MHz Bandwidth

$P_{out}$ @ 1 dB Compression Point, CW	P1dB	—	79	—	W
$P_{out}$ @ 3 dB Compression Point <sup>(4)</sup>	P3dB	—	186	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 758–803 MHz frequency range)	$\Phi$	—	-18	—	$^\circ$
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	$VBW_{res}$	—	120	—	MHz
Gain Flatness in 45 MHz Bandwidth @ $P_{out} = 30\text{ W Avg.}$	$G_F$	—	0.4	—	dB
Gain Variation over Temperature ( $-30^\circ\text{C}$ to $+85^\circ\text{C}$ )	$\Delta G$	—	0.01	—	dB/ $^\circ\text{C}$
Output Power Variation over Temperature ( $-30^\circ\text{C}$ to $+85^\circ\text{C}$ ) <sup>(5)</sup>	$\Delta P1dB$	—	0.3	—	dB/ $^\circ\text{C}$

1.  $V_{DDA}$  and  $V_{ddb}$  must be tied together and powered by a single DC power supply.
2. Part internally matched both on input and output.
3. Measurement made with device in a symmetrical Doherty configuration.
4.  $P3dB = P_{avg} + 7.0\text{ dB}$  where  $P_{avg}$  is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
5. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.



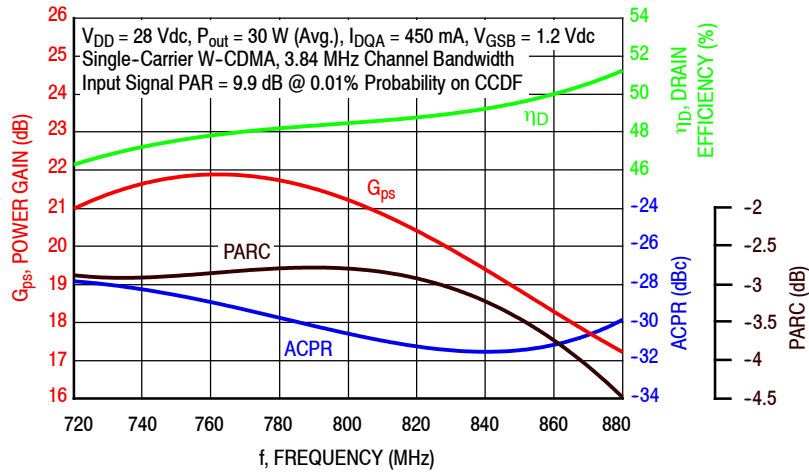
Note: VDDA and VDDB must be tied together and powered by a single DC power supply.

**Figure 2. A2T07D160W04SR3 Test Circuit Component Layout — 758–803 MHz**

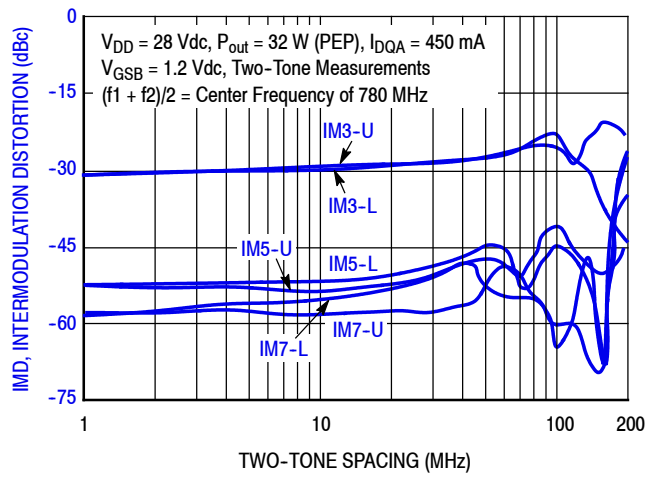
**Table 5. A2T07D160W04SR3 Test Circuit Component Designations and Values — 758–803 MHz**

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6	100 pF Chip Capacitors	ATC600F101JT250XT	ATC
C7, C8	30 pF Chip Capacitors	ATC600F300JT250XT	ATC
C9, C10, C11, C12	3.3 pF Chip Capacitors	ATC600F3R3BT250XT	ATC
C13, C15	4.7 pF Chip Capacitors	ATC600F4R7BT250XT	ATC
C14, C16	6.8 pF Chip Capacitors	ATC600F6R8BT250XT	ATC
C17, C18	5.6 pF Chip Capacitors	ATC600F5R6BT250XT	ATC
C19, C20, C21, C22	3.9 pF Chip Capacitors	ATC600F3R9BT250XT	ATC
C23, C24, C25, C26	2.7 pF Chip Capacitors	ATC600F2R7BT250XT	ATC
C27, C30	10 $\mu$ F Chip Capacitors	GRM31CR61H106KA12	Murata
C28, C29, C31, C33	1 $\mu$ F Chip Capacitors	GRM31CR72A105KA01L	Murata
C32, C34	10 $\mu$ F Chip Capacitors	C5750X7S2A106M230KB	TDK
C35, C36	330 $\mu$ F, 63 V Electrolytic Capacitors	MCRH63V337M13X21-RH	Multicomp
R1, R2	2.2 $\Omega$ , 1/4 W Chip Resistors	CRCW12062R20JNEA	Vishay
R3	50 $\Omega$ , 10 W Termination	81A7031-50-5F	Florida RF Labs
Z1	620–900 MHz Band, 90°, 3 dB Hybrid Coupler	CMX07Q03	RN2 Technologies
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D58628	MTL

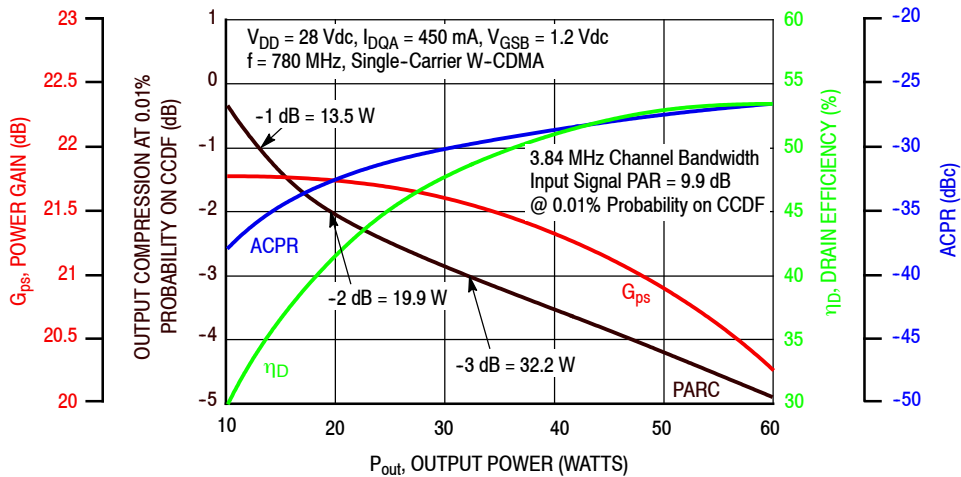
### TYPICAL CHARACTERISTICS — 758–803 MHz



**Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 30$  Watts Avg.**

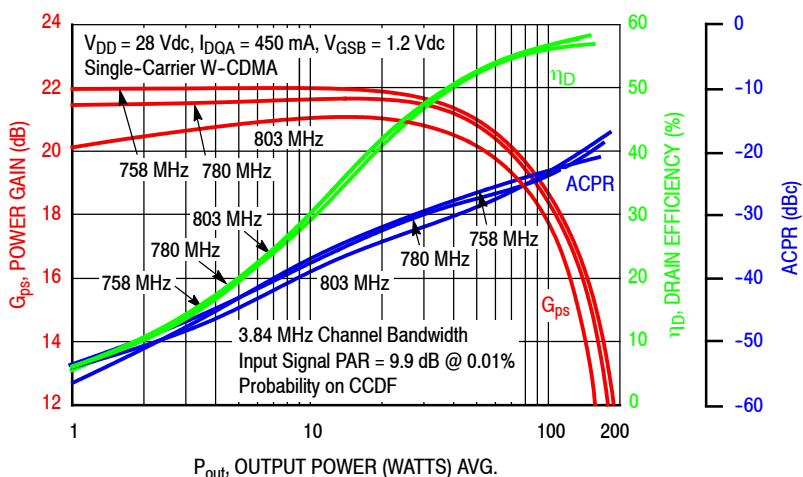


**Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing**

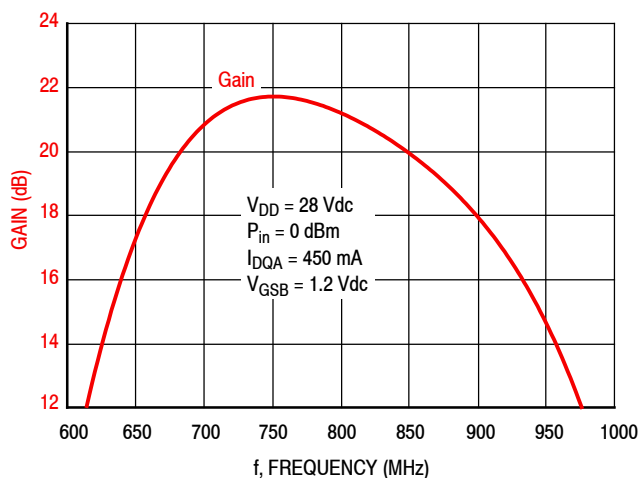


**Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power**

### TYPICAL CHARACTERISTICS — 758–803 MHz



**Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**



**Figure 7. Broadband Frequency Response**

**Table 6. Carrier Side Load Pull Performance — Maximum Power Tuning**
 $V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQA} = 438 \text{ mA}$ , Pulsed CW, 10  $\mu\text{sec}$ (on), 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
748	2.46 – j4.48	2.43 + j4.57	2.31 – j4.78	21.1	50.1	102	51.5	–8
790	3.06 – j5.44	3.03 + j5.57	2.02 – j4.88	20.6	50.5	112	53.2	–8
806	3.32 – j5.90	3.30 + j6.00	1.92 – j5.08	20.2	50.1	103	50.0	–8

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
748	2.46 – j4.48	2.42 + j4.80	2.08 – j5.25	18.7	51.3	134	53.8	–12
790	3.06 – j5.44	3.04 + j5.81	1.94 – j5.25	18.4	51.6	145	56.8	–12
806	3.32 – j5.90	3.33 + j6.24	1.81 – j5.44	17.9	51.4	137	53.3	–12

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

$Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

$Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.

**Table 7. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning**
 $V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQA} = 438 \text{ mA}$ , Pulsed CW, 10  $\mu\text{sec}$ (on), 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
748	2.46 – j4.48	2.35 + j4.51	8.41 – j2.61	24.9	47.4	55	68.0	–13
790	3.06 – j5.44	2.96 + j5.51	6.20 – j2.16	24.2	47.9	61	69.9	–15
806	3.32 – j5.90	3.25 + j5.90	6.00 – j2.35	23.9	47.6	58	66.9	–14

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
748	2.46 – j4.48	2.40 + j4.77	7.65 – j4.43	22.5	48.9	78	71.9	–18
790	3.06 – j5.44	3.04 + j5.78	7.12 – j2.62	22.4	48.4	70	72.7	–21
806	3.32 – j5.90	3.32 + j6.18	6.10 – j3.14	21.8	48.8	76	70.5	–19

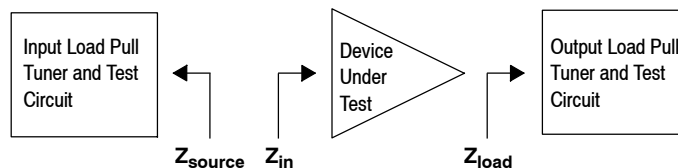
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

$Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

$Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.



**Table 8. Peaking Side Load Pull Performance — Maximum Power Tuning**
 $V_{DD} = 28 \text{ Vdc}$ ,  $V_{GSB} = 1.2 \text{ Vdc}$ , Pulsed CW, 10  $\mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{in}}$ ( $\Omega$ )	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
748	2.58 – j4.22	2.49 + j4.51	2.39 – j5.81	16.9	50.0	99	51.7	–14
790	3.29 – j5.33	3.04 + j5.49	1.84 – j5.81	16.6	50.5	111	50.6	–14
806	3.44 – j5.61	3.33 + j5.94	1.88 – j5.93	16.4	50.3	107	50.5	–14

f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{in}}$ ( $\Omega$ )	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
748	2.58 – j4.22	2.51 + j4.76	2.09 – j6.19	14.4	51.2	131	53.5	–18
790	3.29 – j5.33	3.10 + j5.74	1.73 – j6.07	14.3	51.5	142	52.4	–17
806	3.44 – j5.61	3.40 + j6.19	1.81 – j6.16	14.2	51.4	139	53.3	–17

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

 $Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

 $Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

 $Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.

**Table 9. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning**
 $V_{DD} = 28 \text{ Vdc}$ ,  $V_{GSB} = 1.2 \text{ Vdc}$ , Pulsed CW, 10  $\mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{in}}$ ( $\Omega$ )	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
748	2.58 – j4.22	2.28 + j4.33	9.57 – j3.66	18.8	47.3	54	71.6	–21
790	3.29 – j5.33	2.80 + j5.22	7.77 – j1.84	18.6	47.2	52	72.4	–20
806	3.44 – j5.61	3.09 + j5.65	7.33 – j2.01	18.4	47.2	53	71.4	–18

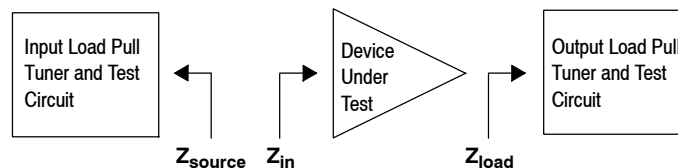
f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{in}}$ ( $\Omega$ )	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
748	2.58 – j4.22	2.33 + j4.59	8.90 – j5.28	16.6	48.4	69	72.6	–24
790	3.29 – j5.33	2.92 + j5.54	6.52 – j4.24	16.6	49.0	80	73.8	–22
806	3.44 – j5.61	3.22 + j5.98	6.58 – j4.08	16.3	48.9	77	72.8	–21

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

 $Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

 $Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

 $Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.




### P1dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 790 MHz

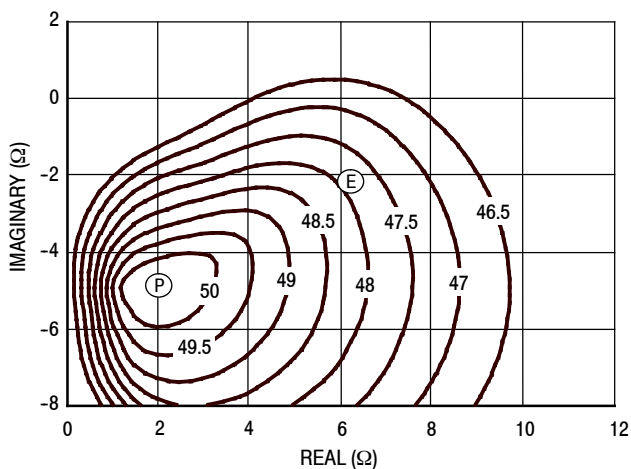


Figure 8. P1dB Load Pull Output Power Contours (dB)

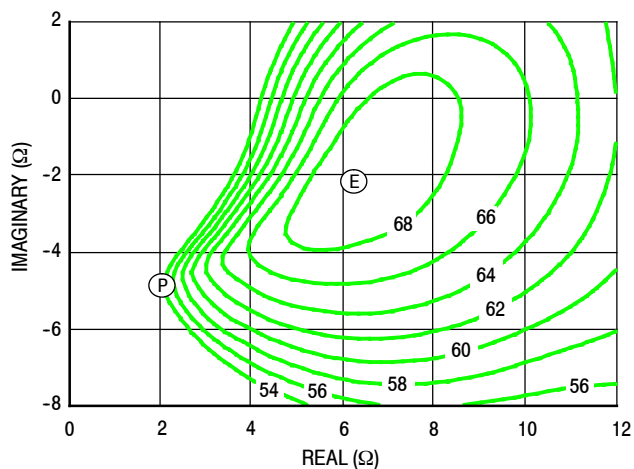


Figure 9. P1dB Load Pull Efficiency Contours (%)

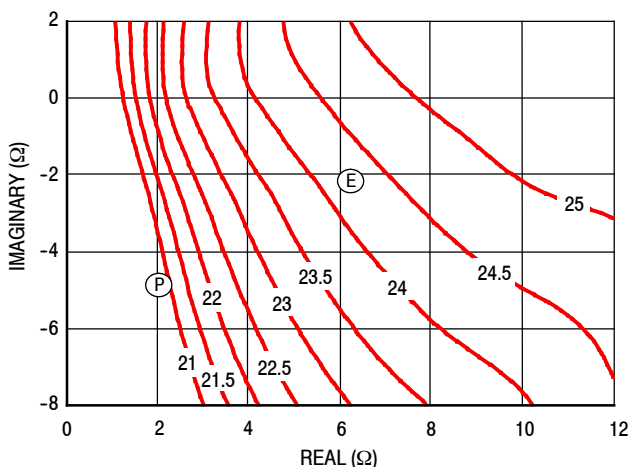


Figure 10. P1dB Load Pull Gain Contours (dB)

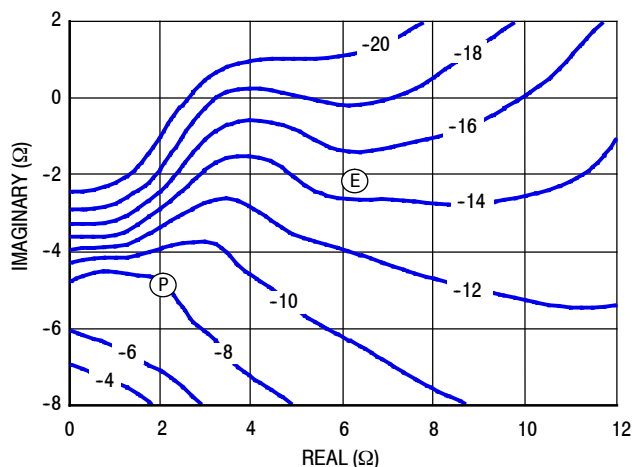


Figure 11. P1dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

### P3dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 790 MHz

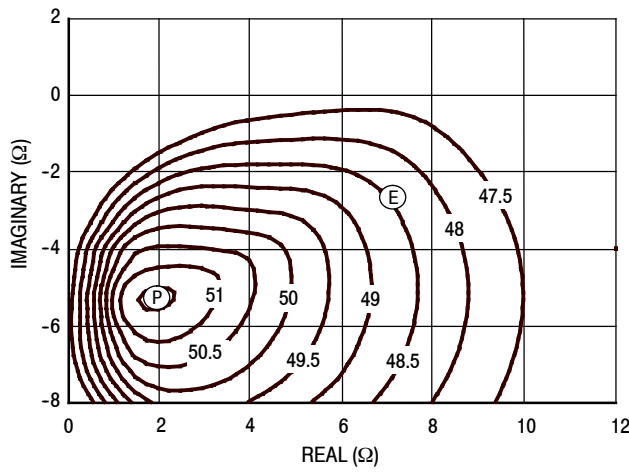


Figure 12. P3dB Load Pull Output Power Contours (dBm)

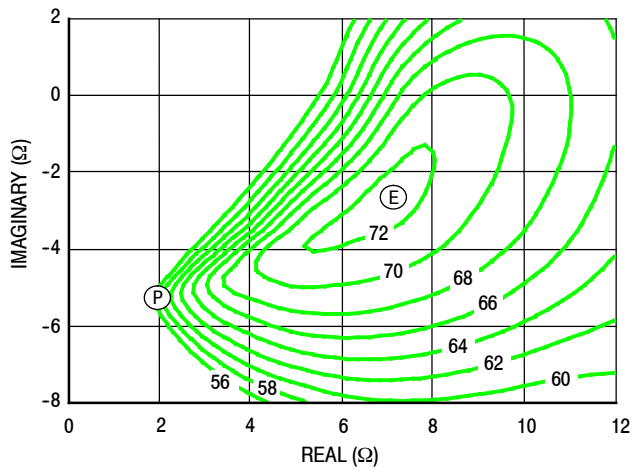


Figure 13. P3dB Load Pull Efficiency Contours (%)

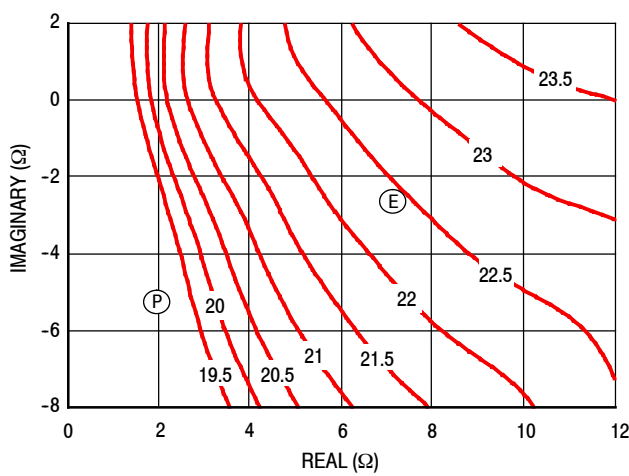


Figure 14. P3dB Load Pull Gain Contours (dB)

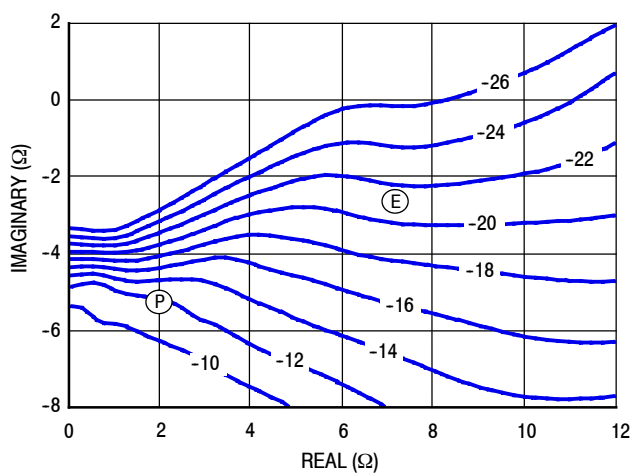


Figure 15. P3dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

### P1dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 790 MHz

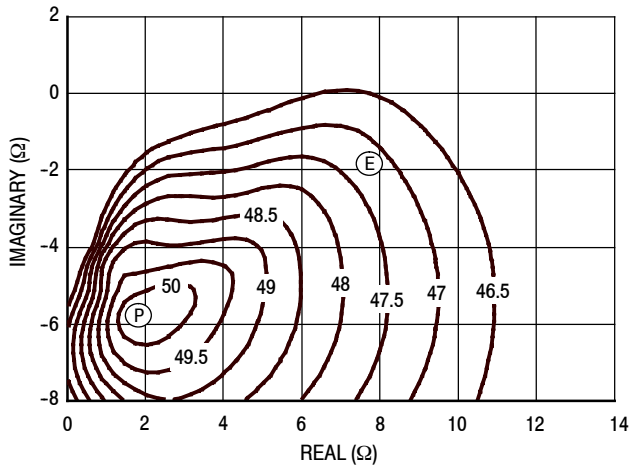


Figure 16. P1dB Load Pull Output Power Contours (dBm)

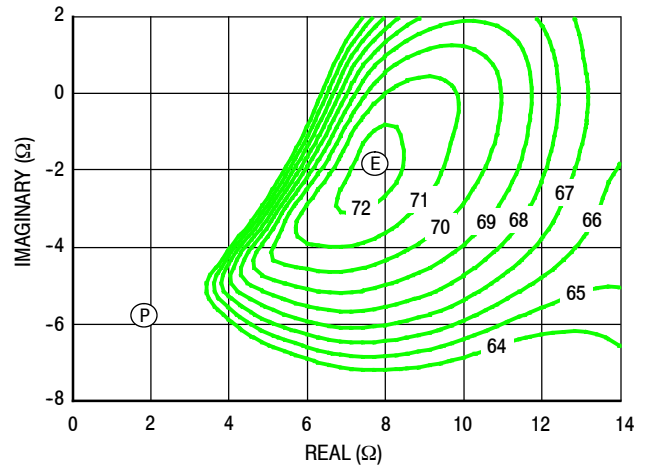


Figure 17. P1dB Load Pull Efficiency Contours (%)

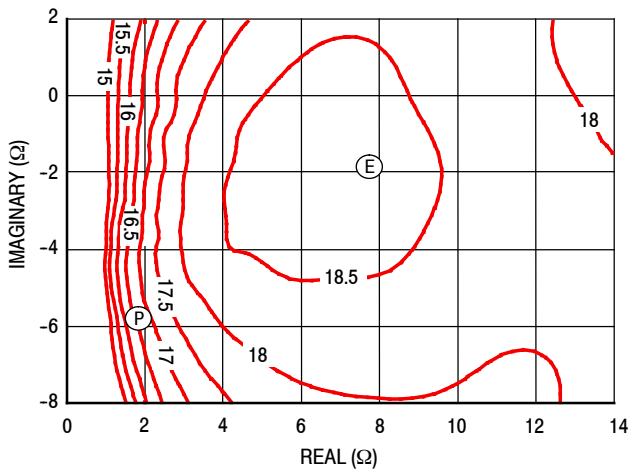


Figure 18. P1dB Load Pull Gain Contours (dB)

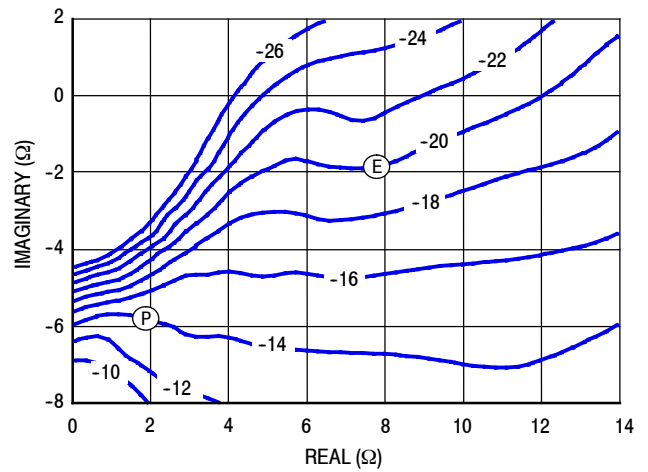


Figure 19. P1dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

### P3dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 790 MHz

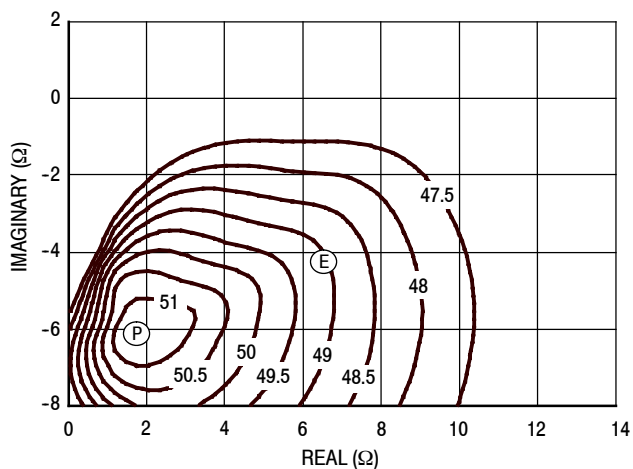


Figure 20. P3dB Load Pull Output Power Contours (dBm)

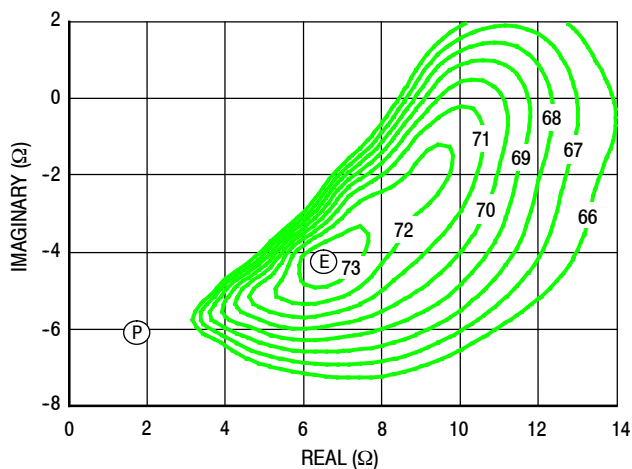


Figure 21. P3dB Load Pull Efficiency Contours (%)

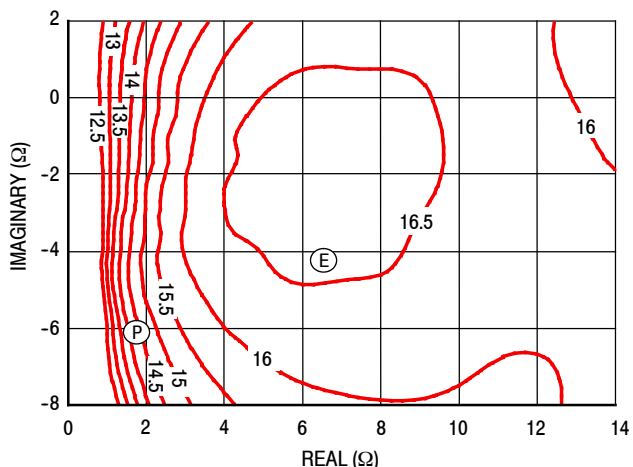


Figure 22. P3dB Load Pull Gain Contours (dB)

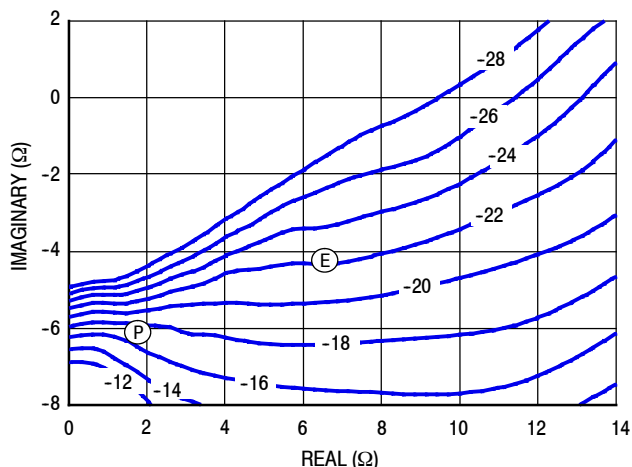
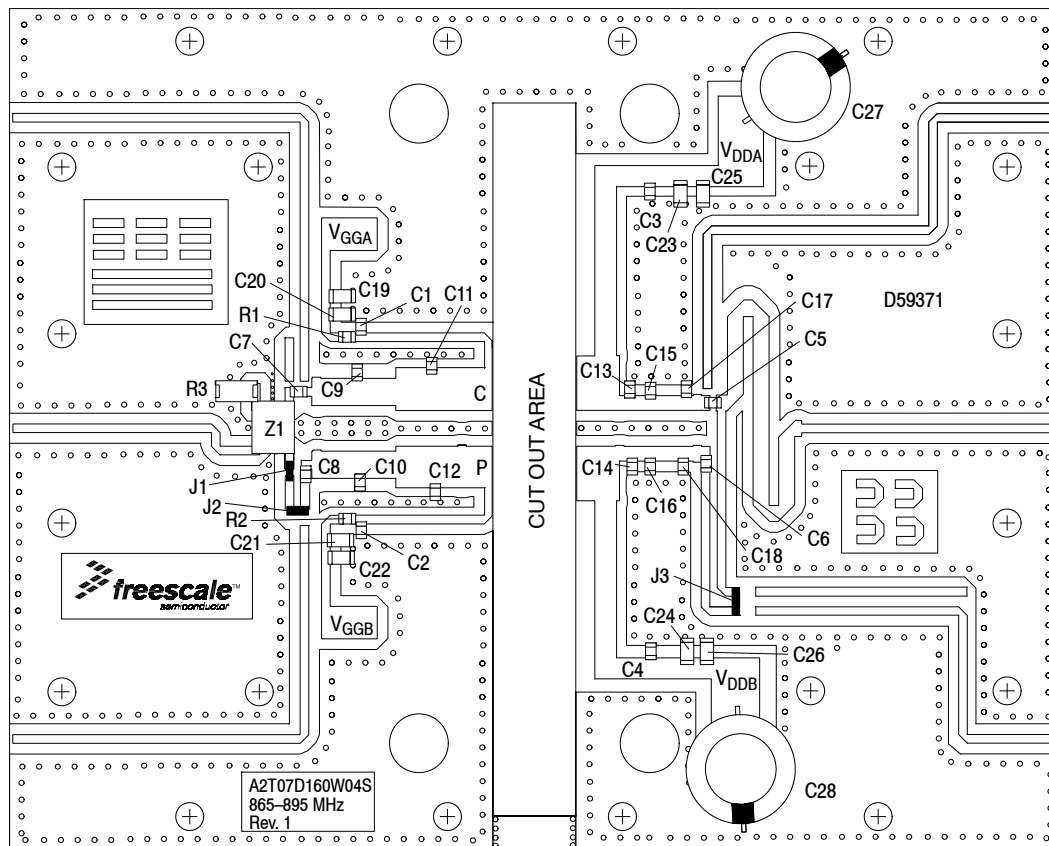


Figure 23. P3dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

## 865–895 MHz CHARACTERISTICS



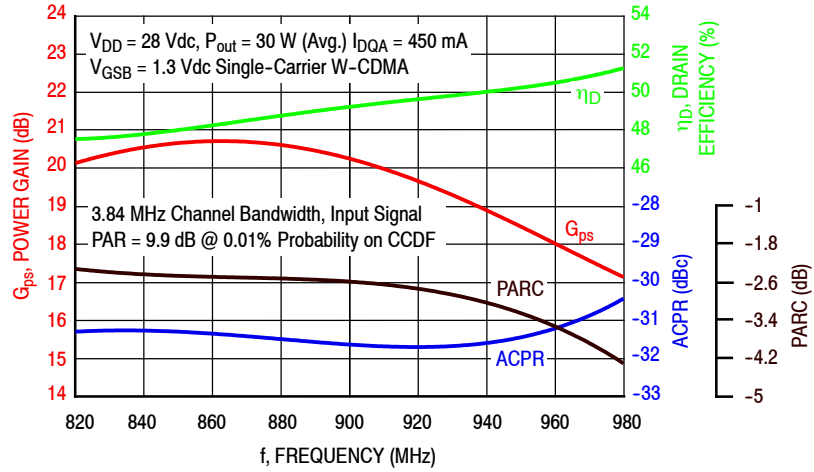
Note:  $V_{DDA}$  and  $V_{DDB}$  must be tied together and powered by a single DC power supply.

**Figure 24. A2T07D160W04SR3 Test Circuit Component Layout — 865–895 MHz**

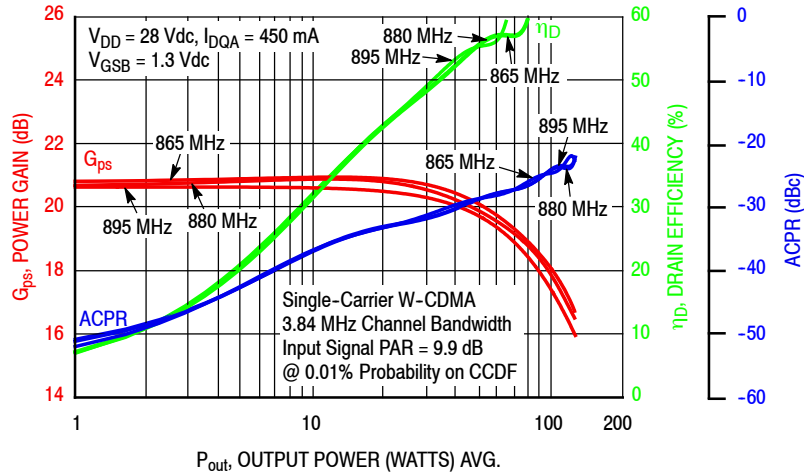
**Table 10. A2T07D160W04SR3 Test Circuit Component Designations and Values — 865–895 MHz**

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6	100 pF Chip Capacitors	ATC600F101JT250XT	ATC
C7, C8	30 pF Chip Capacitors	ATC600F300JT250XT	ATC
C9, C10	3.3 pF Chip Capacitors	ATC600F3R3BT250XT	ATC
C11, C12	4.7 pF Chip Capacitors	ATC600F4R7BT250XT	ATC
C13, C14, C15, C16	5.6 pF Chip Capacitors	ATC600F5R6BT250XT	ATC
C17, C18	2.7 pF Chip Capacitors	ATC600F2R7BT250XT	ATC
C19, C22	10 $\mu$ F Chip Capacitors	GRM31CR61H106KA12	Murata
C20, C21, C23, C24	1 $\mu$ F Chip Capacitors	GRM31CR72A105KA01L	Murata
C25, C26	10 $\mu$ F Chip Capacitors	C5750X7S2A106M230KB	TDK
C27, C28	330 $\mu$ F, 63 V Electrolytic Capacitors	MCRH63V337M13X21-RH	Multicomp
J1, J2, J3	Copper Foil		
R1, R2	2.2 $\Omega$ , 1/4 W Chip Resistors	CRCW12062R20JNEA	Vishay
R3	50 $\Omega$ , 10 W Termination	81A7031-50-5F	Florida RF Labs
Z1	620–900 MHz Band, 90°, 3 dB Hybrid Coupler	CMX07Q03	RN2 Technologies
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D59371	MTL

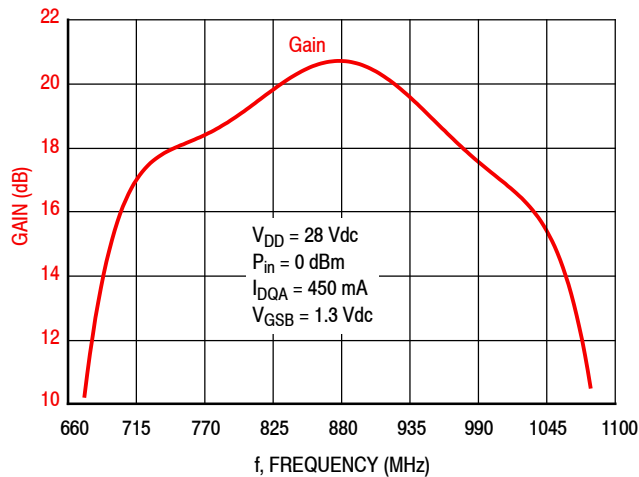
### TYPICAL CHARACTERISTICS — 865–895 MHz



**Figure 25. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 30$  Watts Avg.**



**Figure 26. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**



**Figure 27. Broadband Frequency Response**

**Table 11. Carrier Side Load Pull Performance — Maximum Power Tuning**
 $V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQA} = 434 \text{ mA}$ , Pulsed CW, 10  $\mu\text{sec}$ (on), 10% Duty Cycle

f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{in}}$ ( $\Omega$ )	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
865	4.65 – j7.47	5.05 + j7.41	1.80 – j5.49	19.8	50.8	121	55.0	–7
880	5.83 – j8.00	5.80 + j7.75	1.80 – j5.61	19.7	50.9	122	55.6	–8
895	7.11 – j8.39	6.76 + j8.03	1.73 – j5.70	19.5	50.9	123	55.3	–8

f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{in}}$ ( $\Omega$ )	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
865	4.65 – j7.47	5.18 + j7.65	1.74 – j5.86	17.5	51.8	152	57.1	–11
880	5.83 – j8.00	5.97 + j7.98	1.75 – j5.96	17.4	51.8	153	58.1	–11
895	7.11 – j8.39	6.99 + j8.24	1.68 – j6.06	17.1	51.8	153	57.4	–11

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

 $Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

 $Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

 $Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.

**Table 12. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning**
 $V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQA} = 434 \text{ mA}$ , Pulsed CW, 10  $\mu\text{sec}$ (on), 10% Duty Cycle

f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{in}}$ ( $\Omega$ )	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
865	4.65 – j7.47	5.06 + j7.28	4.56 – j2.53	23.4	48.0	64	71.5	–17
880	5.83 – j8.00	5.83 + j7.61	4.21 – j2.63	23.2	48.0	63	70.8	–17
895	7.11 – j8.39	6.78 + j7.77	4.30 – j3.29	22.9	48.2	65	69.3	–15

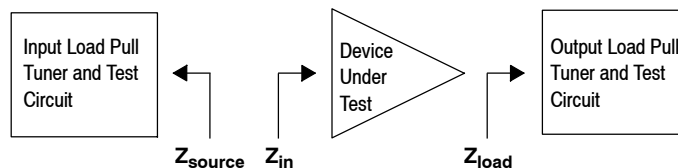
f (MHz)	$Z_{\text{source}}$ ( $\Omega$ )	$Z_{\text{in}}$ ( $\Omega$ )	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
865	4.65 – j7.47	5.27 + j7.55	4.99 – j2.61	21.5	48.7	74	74.3	–23
880	5.83 – j8.00	6.03 + j7.85	4.42 – j3.17	21.0	49.1	81	74.2	–22
895	7.11 – j8.39	7.02 + j8.06	3.97 – j3.55	20.7	49.3	84	72.2	–22

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

 $Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

 $Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

 $Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.


**Table 13. Peaking Side Load Pull Performance — Maximum Power Tuning**
 $V_{DD} = 28 \text{ Vdc}$ ,  $V_{GSB} = 1.2 \text{ Vdc}$ , Pulsed CW, 10  $\mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
865	5.24 – j6.88	5.26 + j7.37	1.82 – j6.25	16.2	50.8	120	54.9	–12
880	6.04 – j7.55	6.11 + j7.76	1.64 – j6.44	15.9	51.0	125	53.7	–12
895	6.85 – j7.68	7.15 + j8.00	1.69 – j6.53	15.9	51.0	127	55.6	–12

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
865	5.24 – j6.88	5.49 + j7.64	1.73 – j6.60	13.9	51.8	151	56.6	–15
880	6.04 – j7.55	6.38 + j8.00	1.68 – j6.73	13.8	51.9	154	56.5	–15
895	6.85 – j7.68	7.52 + j8.23	1.62 – j6.79	13.7	52.0	158	57.1	–16

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

 $Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

 $Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

 $Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.

**Table 14. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning**
 $V_{DD} = 28 \text{ Vdc}$ ,  $V_{GSB} = 1.2 \text{ Vdc}$ , Pulsed CW, 10  $\mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
865	5.24 – j6.88	4.85 + j7.03	5.19 – j1.71	18.0	47.2	52	75.0	–23
880	6.04 – j7.55	5.64 + j7.43	4.50 – j2.89	17.9	47.9	62	74.3	–21
895	6.85 – j7.68	6.63 + j7.71	4.17 – j3.30	17.6	48.1	64	73.3	–21

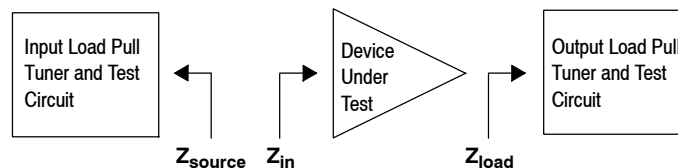
f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
865	5.24 – j6.88	5.14 + j7.35	5.55 – j3.10	15.9	48.6	72	76.0	–25
880	6.04 – j7.55	5.96 + j7.71	4.88 – j3.27	15.8	48.7	74	75.6	–26
895	6.85 – j7.68	7.09 + j8.01	3.95 – j4.44	15.6	49.6	91	74.6	–24

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

 $Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

 $Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

 $Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.




### P1dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 880 MHz

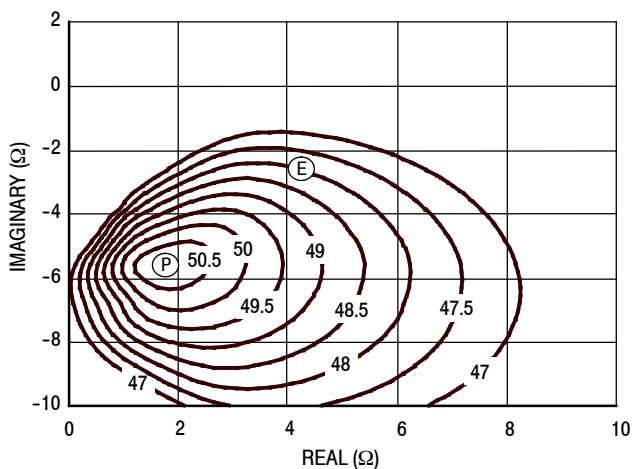


Figure 28. P1dB Load Pull Output Power Contours (dBm)

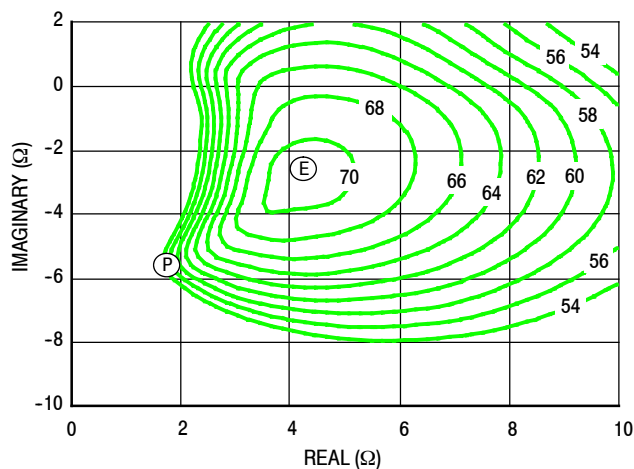


Figure 29. P1dB Load Pull Efficiency Contours (%)

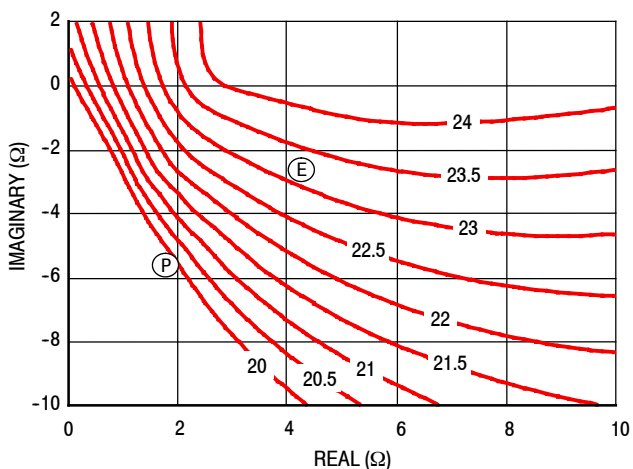


Figure 30. P1dB Load Pull Gain Contours (dB)

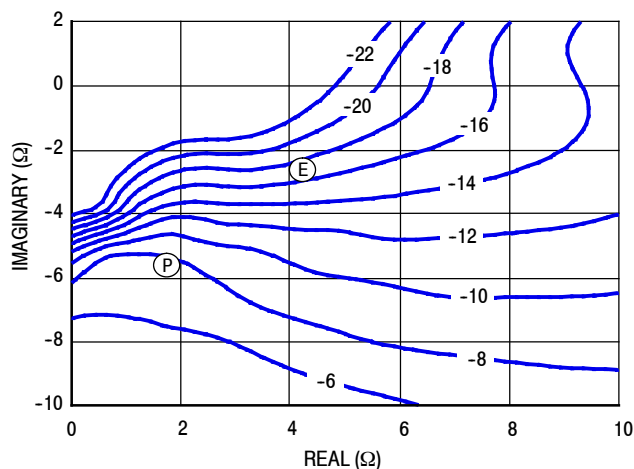


Figure 31. P1dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

### P3dB - TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 880 MHz

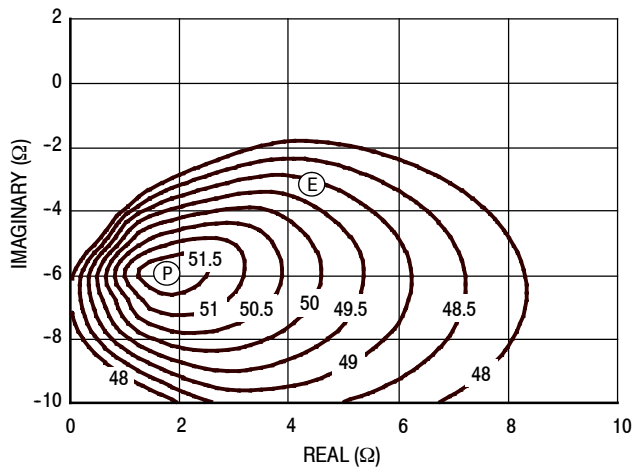


Figure 32. P3dB Load Pull Output Power Contours (dBm)

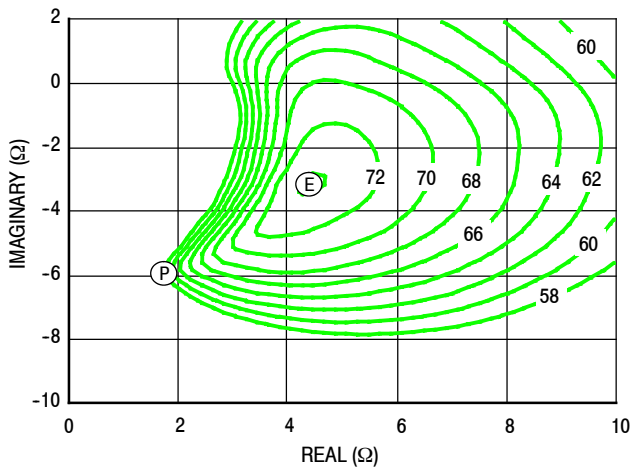


Figure 33. P3dB Load Pull Efficiency Contours (%)

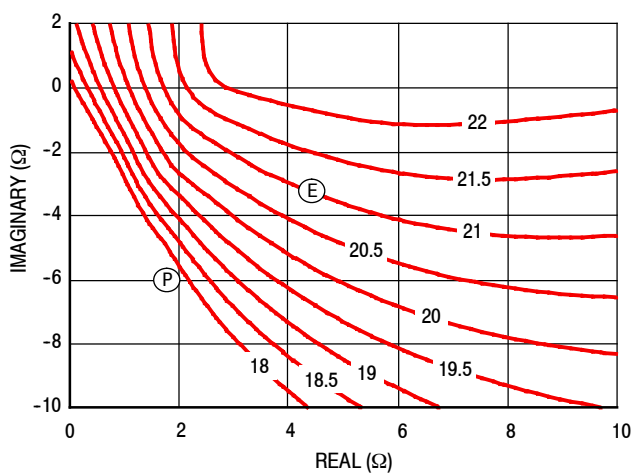


Figure 34. P3dB Load Pull Gain Contours (dB)

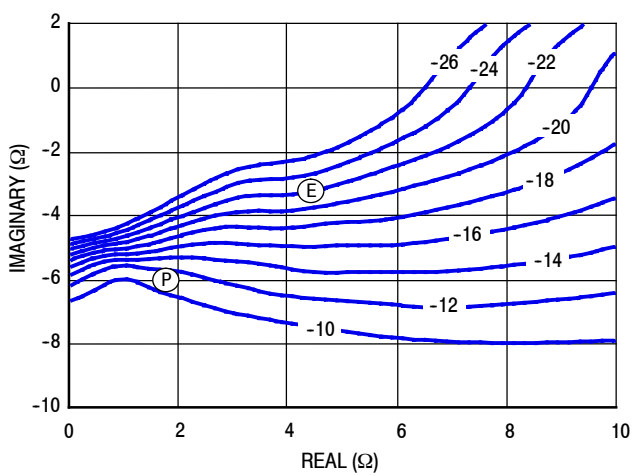
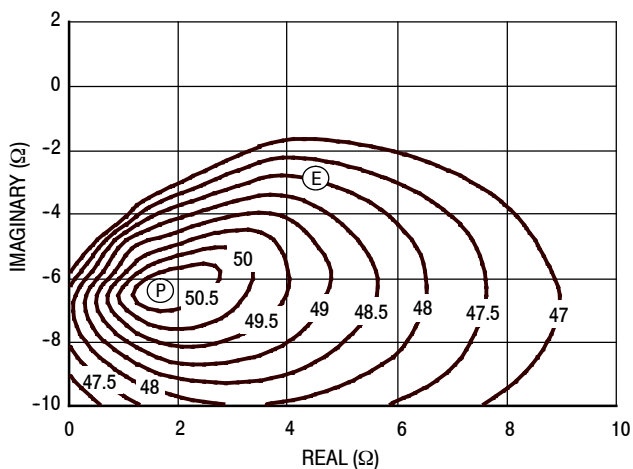


Figure 35. P3dB Load Pull AM/PM Contours (°)

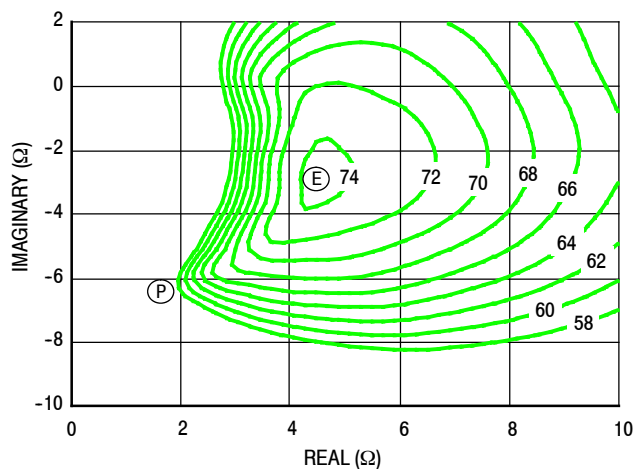
**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

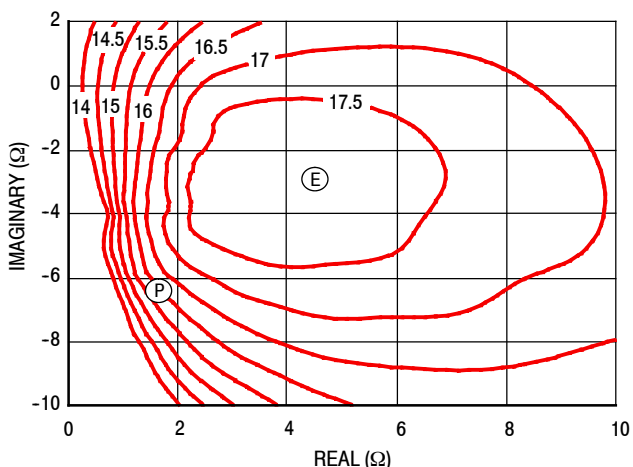
**P1dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 880 MHz**



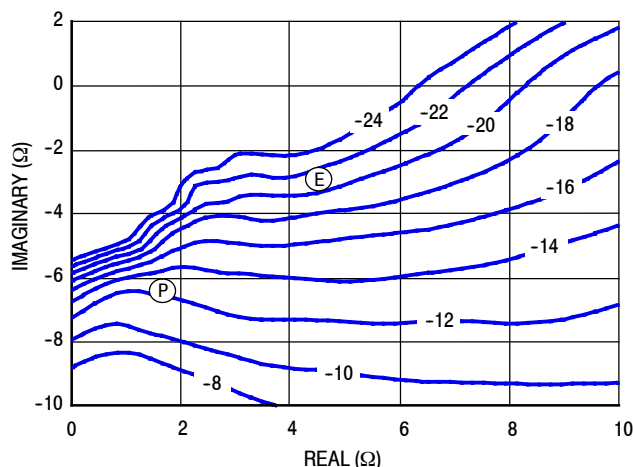
**Figure 36. P1dB Load Pull Output Power Contours (dBm)**



**Figure 37. P1dB Load Pull Efficiency Contours (%)**



**Figure 38. P1dB Load Pull Gain Contours (dB)**



**Figure 39. P1dB Load Pull AM/PM Contours (°)**

**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

### P3dB - TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 880 MHz

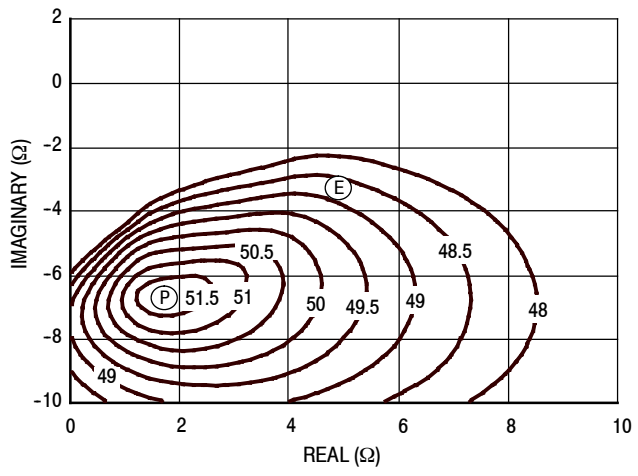


Figure 40. P3dB Load Pull Output Power Contours (dBm)

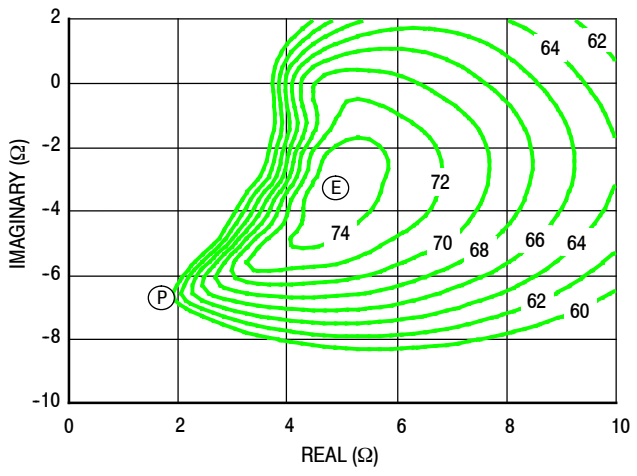


Figure 41. P3dB Load Pull Efficiency Contours (%)

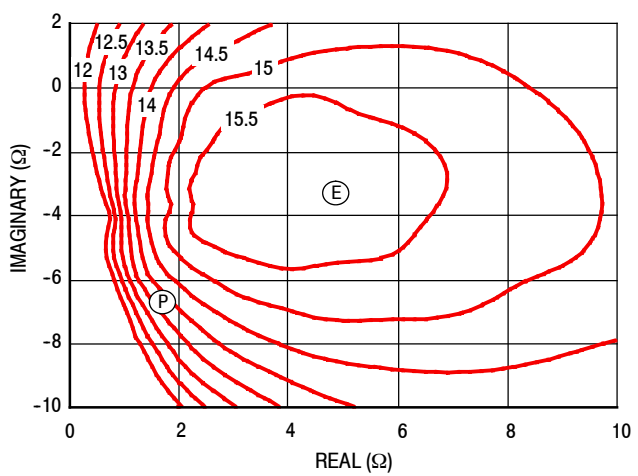


Figure 42. P3dB Load Pull Gain Contours (dB)

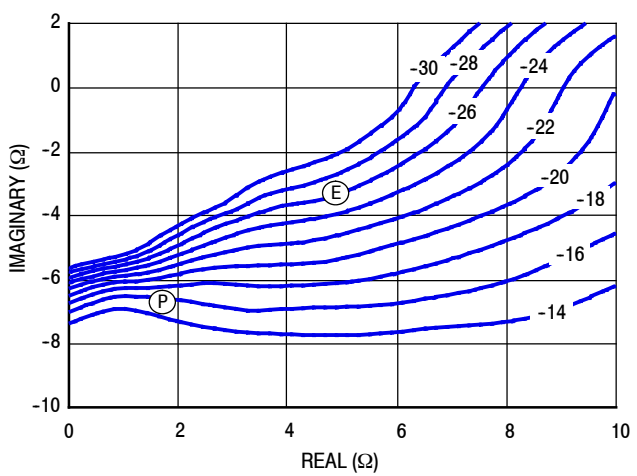
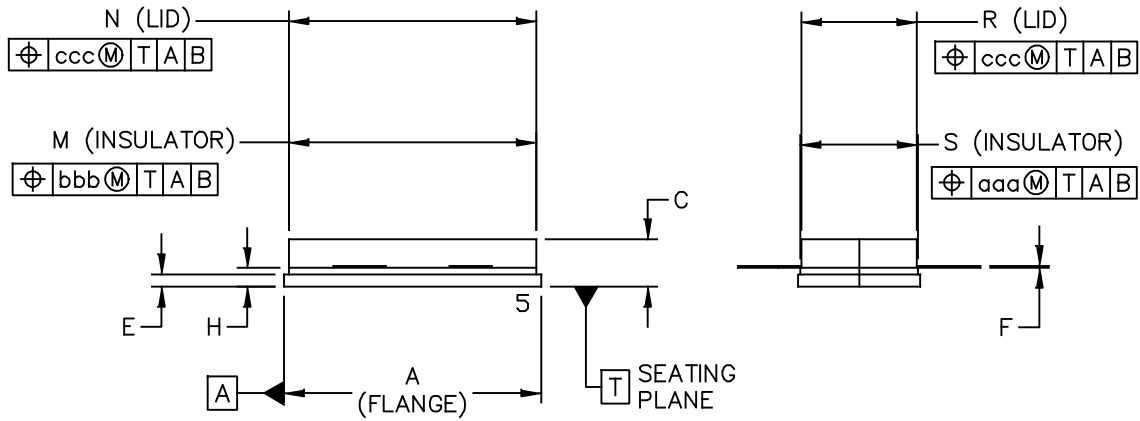
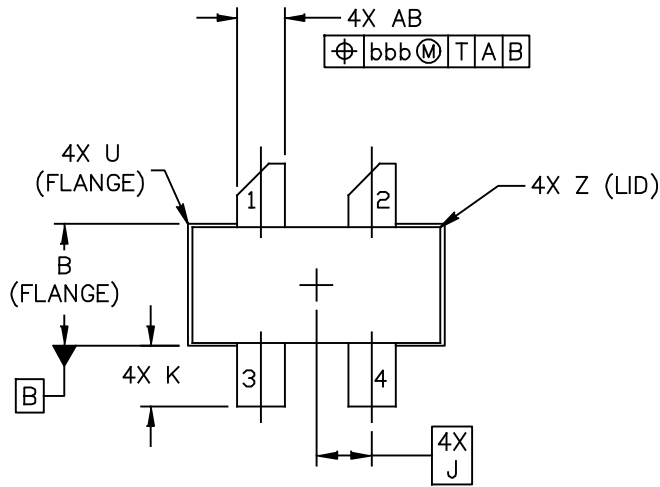


Figure 43. P3dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

### PACKAGE DIMENSIONS



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	CASE NUMBER: 465H-02		27 MAR 2007
	STANDARD: NON-JEDEC		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:

- PIN 1. DRAIN
- 2. DRAIN
- 3. GATE
- 4. GATE
- 5. SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.805	.815	20.45	20.7	U		.040		1.02
B	.380	.390	9.65	9.91	Z		.030		0.76
C	.125	.170	3.18	4.32	AB	.145	.155	3.68	- 3.94
E	.035	.045	0.89	1.14					
F	.003	.006	0.08	0.15	aaa		.005		0.127
H	.057	.067	1.45	1.7	bbb		.010		0.254
J	.175 BSC		4.44 BSC		ccc		.015		0.381
K	.170	.210	4.32	5.33					
M	.774	.786	19.61	20.02					
N	.772	.788	19.61	20.02					
R	.365	.375	9.27	9.53					
S	.365	.375	9.27	9.52					
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TITLE:  NI 780S-4					DOCUMENT NO: 98ASA10718D			REV: A	
					CASE NUMBER: 465H-02			27 MAR 2007	
					STANDARD: NON-JEDEC				

## PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

### Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Aug. 2014	• Initial Release of Data Sheet

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- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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