



# CPH5905

## N-Channel JFET and NPN Bipolar Transistor 15V, 10 to 32mA, 50V, 150mA, Composite type, CPH5

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### Features

- Composite type with J-FET and NPN transistors contained in the CPH5 package, improving the mounting efficiency greatly
- The CPH5905 contains a 2SK3357-equivalent chip and a 2SC4639-equivalent chip in one package
- Drain and emitter are shared

### Specifications

#### Absolute Maximum Ratings at Ta=25°C

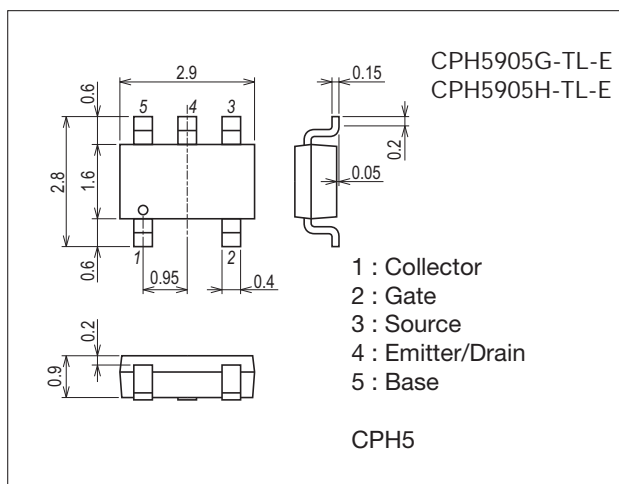
Parameter	Symbol	Conditions	Ratings	Unit
[FET]				
Drain-to-Source Voltage	V <sub>DSX</sub>		15	V
Gate-to-Drain Voltage	V <sub>GD</sub>		-15	V
Gate Current	I <sub>G</sub>		10	mA
Drain Current	I <sub>D</sub>		50	mA
Allowable Power Dissipation	P <sub>D</sub>	Mounted on a ceramic board (600mm <sup>2</sup> ×0.8mm)	350	mW
[TR]				
Collector-to-Base Voltage	V <sub>CBO</sub>		55	V
Collector-to-Emitter Voltage	V <sub>CEO</sub>		50	V
Emitter-to-Base Voltage	V <sub>EBO</sub>		6	V
Collector Current	I <sub>C</sub>		150	mA
Collector Current (Pulse)	I <sub>CP</sub>		300	mA
Base Current	I <sub>B</sub>		30	mA
Collector Dissipation	P <sub>C</sub>	Mounted on a ceramic board (600mm <sup>2</sup> ×0.8mm)	350	mW
[TR]				
Total Power Dissipation	P <sub>T</sub>	Mounted on a ceramic board (600mm <sup>2</sup> ×0.8mm)	500	mW
Junction Temperature	T <sub>j</sub>		150	°C
Storage Temperature	T <sub>stg</sub>		-55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

### Package Dimensions

unit : mm (typ)

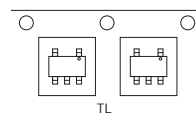
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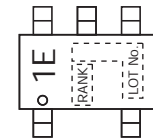
### Product & Package Information

- Package : CPH5
- JEITA, JEDEC : SC-74A, SOT-25
- Minimum Packing Quantity : 3,000 pcs./reel

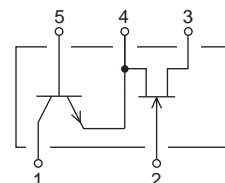
### Packing Type : TL



### Marking



### Electrical Connection



# CPH5905

## Electrical Characteristics at Ta=25°C

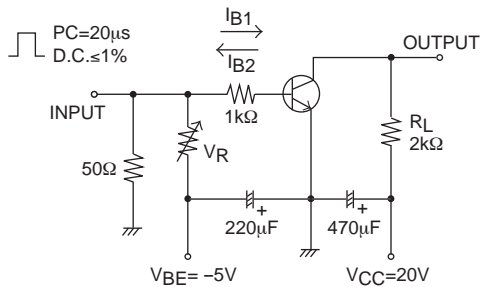
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[FET]						
Gate-to-Drain Breakdown Voltage	V(BR)GDS	I <sub>G</sub> =-10μA, V <sub>GS</sub> =0V	-15			V
Gate Cutoff Current	I <sub>GSS</sub>	V <sub>GS</sub> =-10V, V <sub>DS</sub> =0V			-1.0	nA
Cutoff Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =100μA	-0.4	-0.7	-1.5	V
Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =5V, V <sub>GS</sub> =0V	10.0*		32.0*	mA
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> =5V, V <sub>GS</sub> =0V, f=1kHz	24	35		mS
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =5V, V <sub>GS</sub> =0V, f=1kHz		10.0		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	V <sub>DS</sub> =5V, V <sub>GS</sub> =0V, f=1kHz		2.9		pF
Noise Figure	NF	V <sub>DS</sub> =5V, R <sub>g</sub> =1kΩ, I <sub>D</sub> =1mA, f=1kHz		1.0		dB
[TR]						
Collector Cutoff Current	I <sub>CBO</sub>	V <sub>CB</sub> =35V, I <sub>E</sub> =0A			0.1	μA
Emitter Cutoff Current	I <sub>EBO</sub>	V <sub>EB</sub> =4V, I <sub>C</sub> =0A			0.1	μA
DC Current Gain	h <sub>FE</sub>	V <sub>CE</sub> =6V, I <sub>C</sub> =1mA	135		400	
Gain-Bandwidth Product	f <sub>T</sub>	V <sub>CE</sub> =6V, I <sub>C</sub> =10mA		200		MHz
Output Capacitance	C <sub>ob</sub>	V <sub>CB</sub> =6V, f=1MHz		1.7		pF
Collector-to-Emitter Saturation Voltage	V <sub>CE(sat)</sub>	I <sub>C</sub> =50mA, I <sub>B</sub> =5mA		0.08	0.4	mV
Base-to-Emitter Saturation Voltage	V <sub>BE(sat)</sub>	I <sub>C</sub> =50mA, I <sub>B</sub> =5mA		0.8	1.0	V
Collector-to-Base Breakdown Voltage	V(BR)CBO	I <sub>C</sub> =10μA, I <sub>E</sub> =0A	55			V
Collector-to-Emitter Breakdown Voltage	V(BR)CEO	I <sub>C</sub> =1mA, R <sub>BE</sub> =∞	50			V
Emitter-to-Base Breakdown Voltage	V(BR)EBO	I <sub>E</sub> =10μA, I <sub>C</sub> =0A	6			V
Turn-On Time	t <sub>on</sub>	See specified Test Circuit.		0.15		ns
Storage Time	t <sub>stg</sub>			0.75		ns
Fall Time	t <sub>f</sub>			0.20		ns

\* : The CPH5905 is classified by I<sub>DSS</sub> as follows : (unit : mA)

Rank	G	H
I <sub>DSS</sub>	10.0 to 20.0	16.0 to 32.0

The specifications shown above are for each individual FET or transistor.

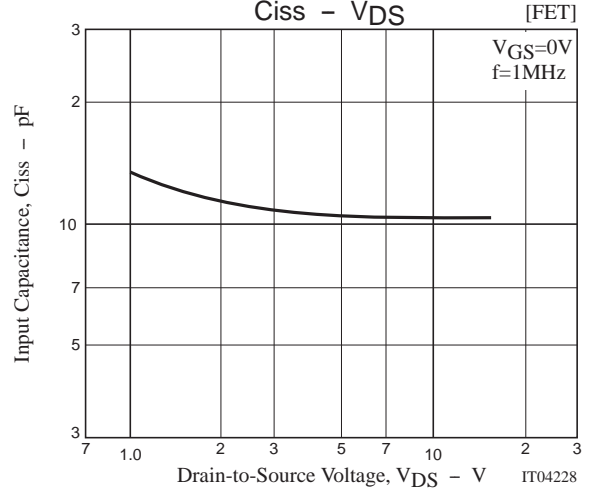
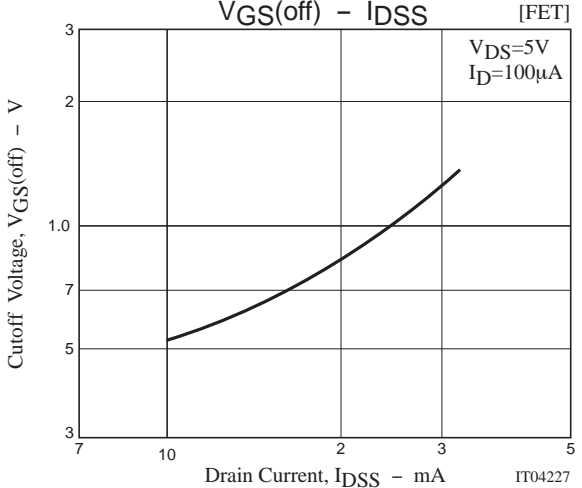
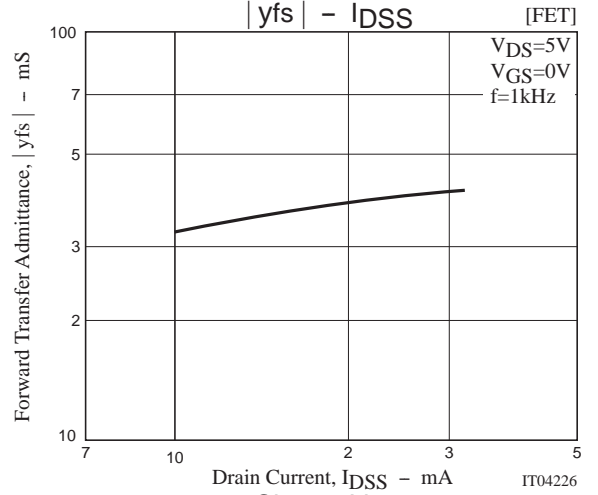
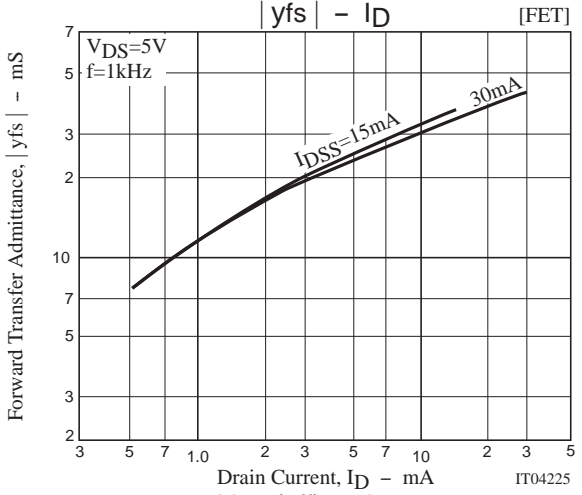
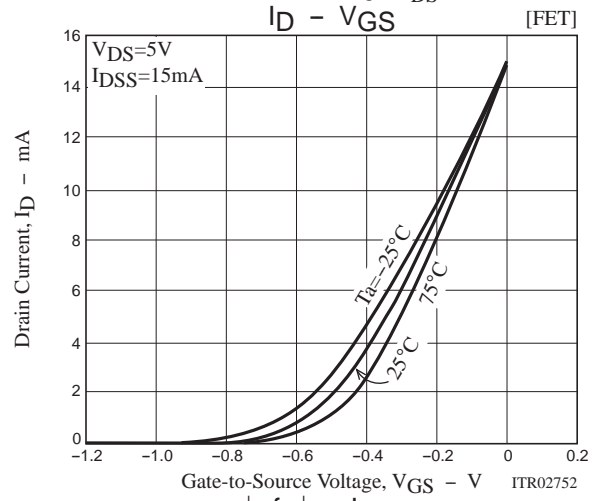
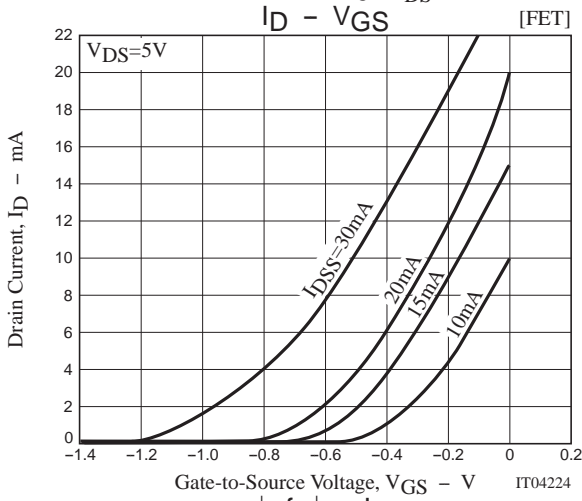
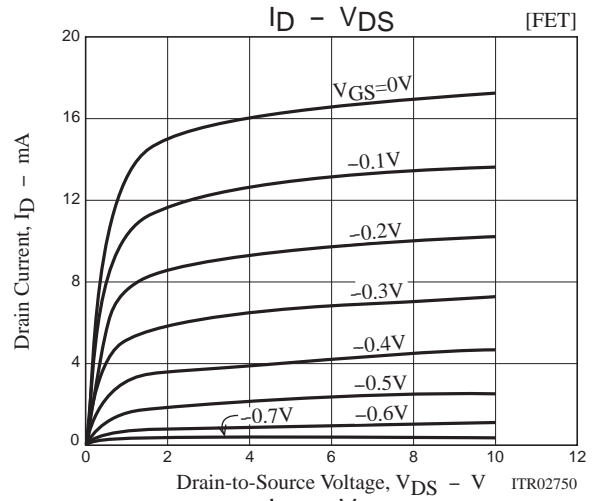
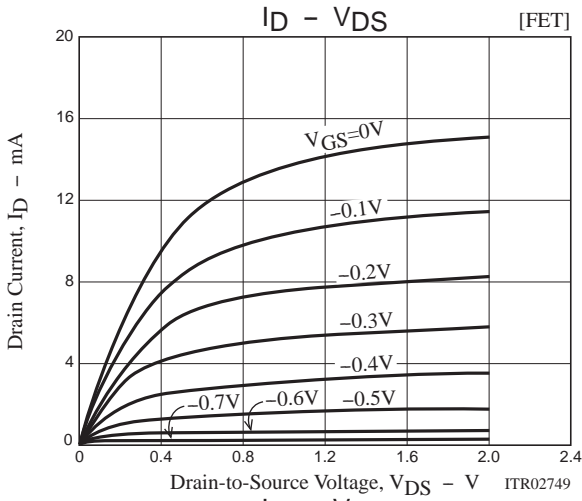
### Switching Time Test Circuit

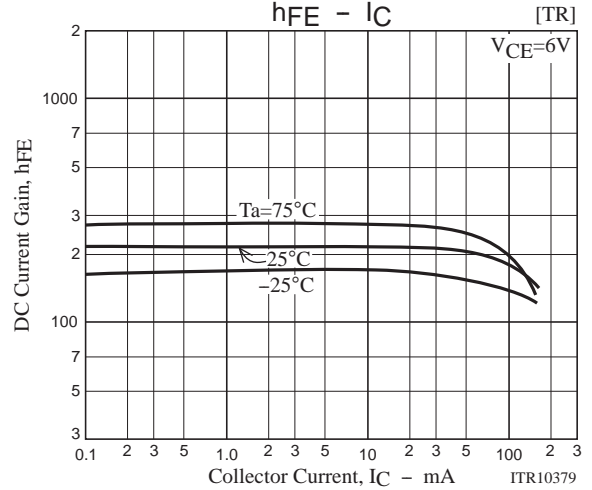
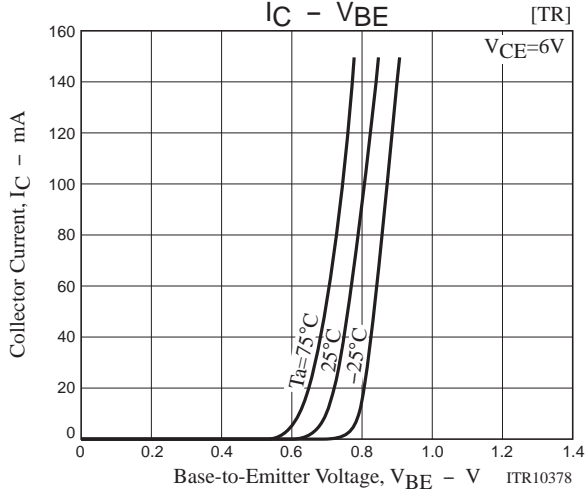
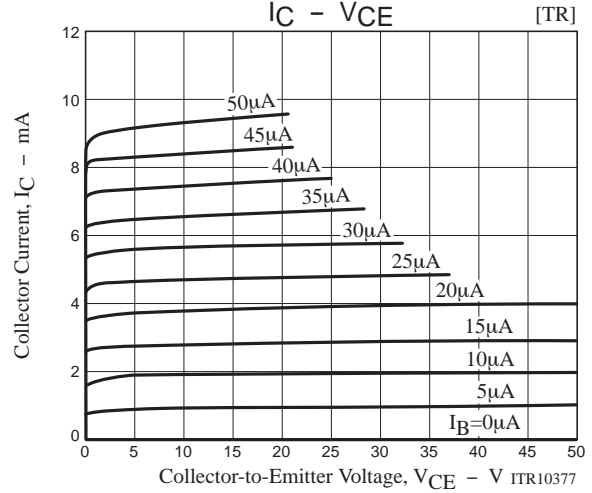
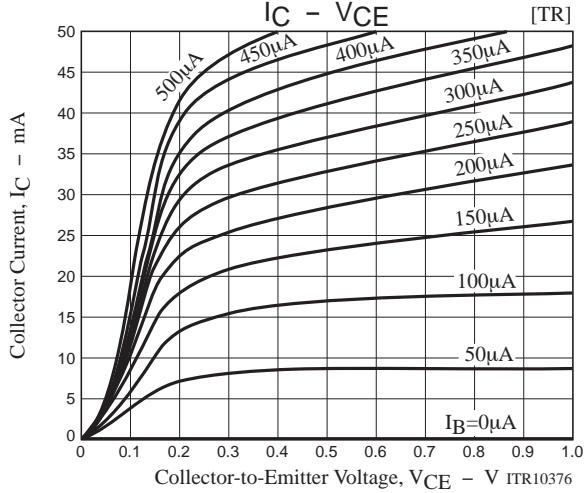
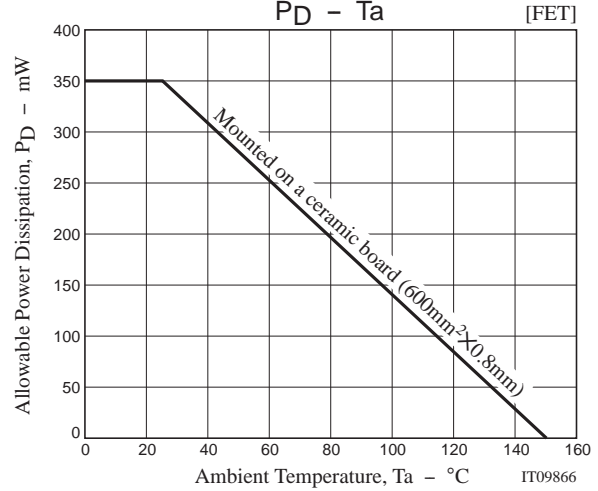
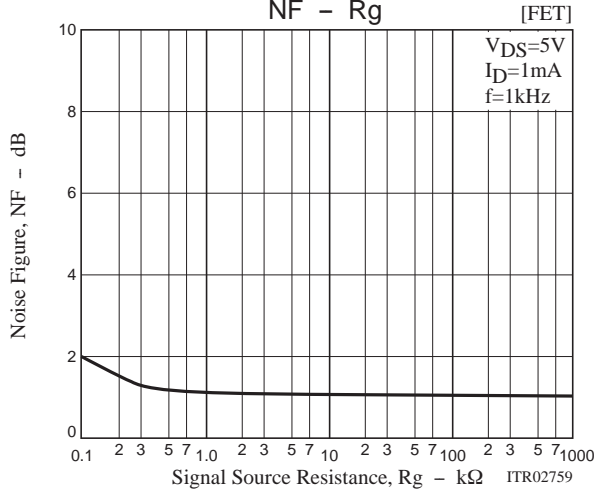
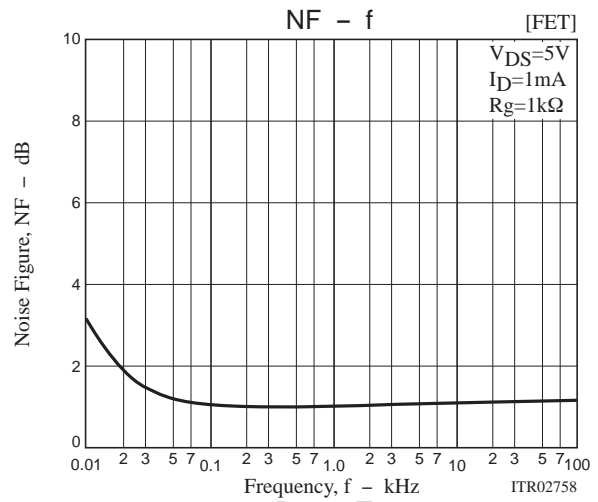
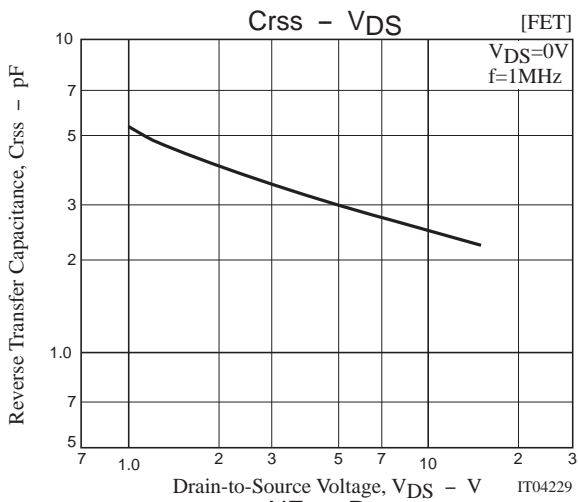


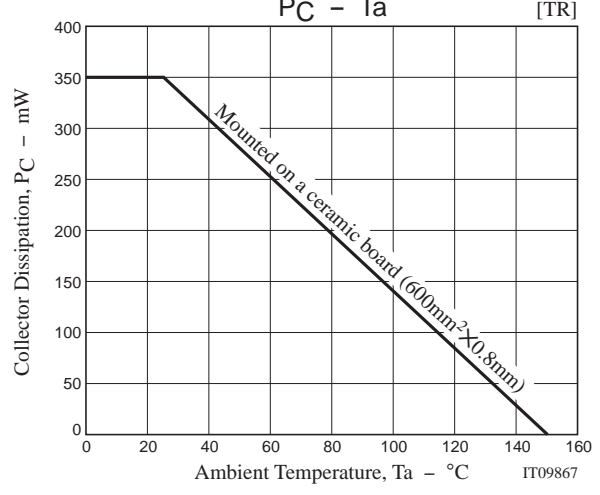
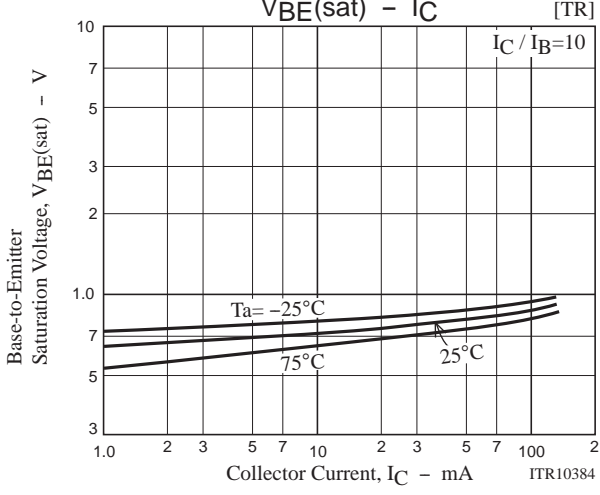
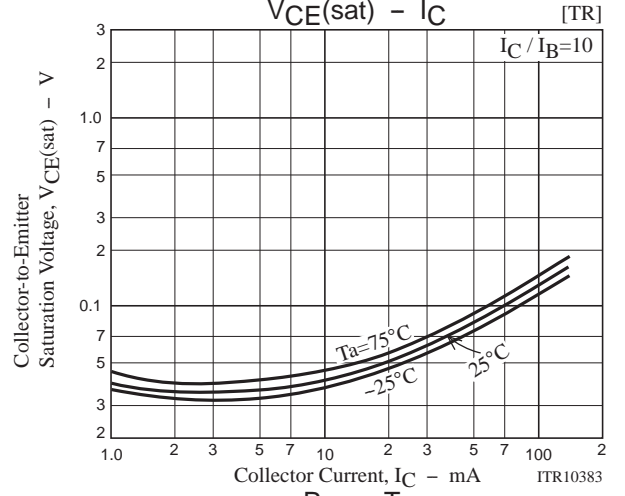
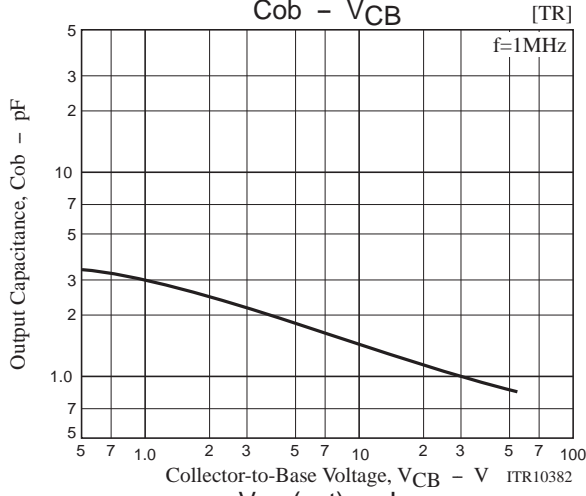
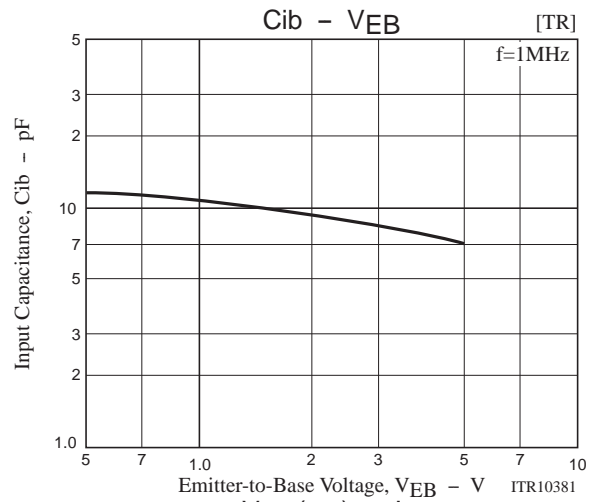
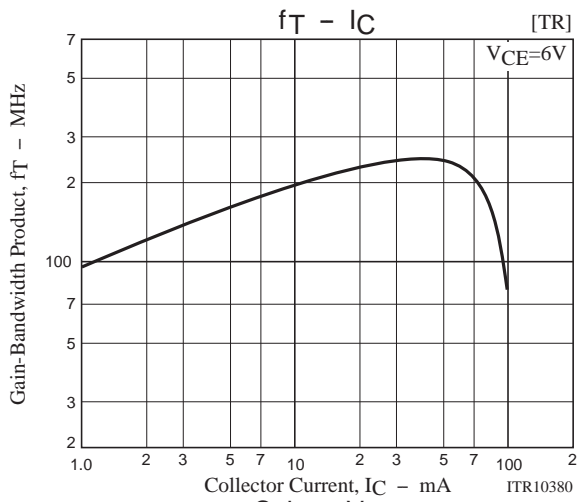
$$10I_{B1} = -10I_{B2} = I_C = 10\text{mA}$$

### Ordering Information

Device	Package	Shipping	memo
CPH5905G-TL-E	CPH5	3,000pcs./reel	Pb Free
CPH5905H-TL-E	CPH5	3,000pcs./reel	







Embossed Taping Specification

CPH5905G-TL-E, CPH5905H-TL-E

1. Packing Format

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	Inner BOX (C-1)	Outer BOX (A-7)
CPH5	CPH6	3,000	15,000	90,000	5 reels contained Dimensions:mm (external) 183×72×185	6 inner boxes contained Dimensions:mm (external) 440×195×210

Reel label, Inner box label  
(unit:mm)

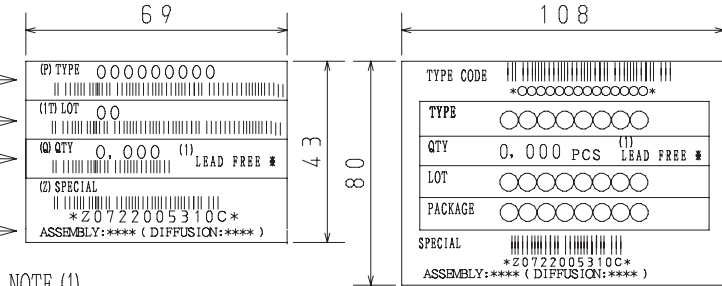
Outer box label  
It is a label at the time of factory shipments.  
The form of a label may change in physical distribution process.

Packing method



Reel label

Type No.  
LOT No.  
Quantity  
Origin



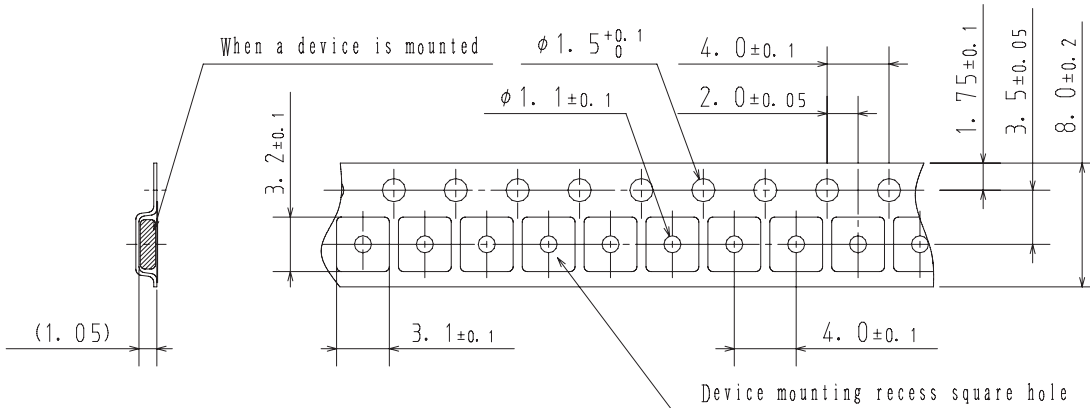
NOTE (1)

The LEAD FREE \* description shows that the surface treatment of the terminal is lead free.

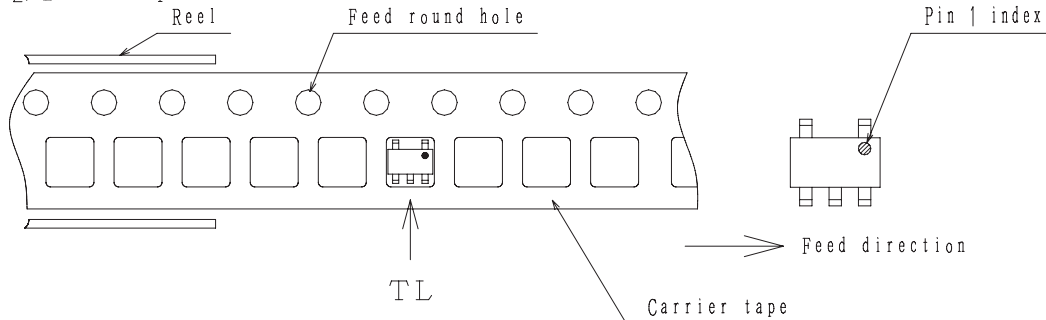
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



2-2. Device placement direction



Those with pin 1 index on the feed hole side.....TL

# CPH5905

## Outline Drawing

CPH5905G-TL-E, CPH5905H-TL-E



## Land Pattern Example



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Тел: +7 (812) 336 43 04 (многоканальный)  
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