MLX75024 Time-of-Flight Sensor Array

Datasheet

Features & Benefits

- 1/3” optical Time-of-Flight sensor (optical area = 4.8 x 3.6 mm^2)
- QVGA resolution, 320 x 240 pixels
- 15 x 15 µm DepthSense™ pixels
- Demodulation frequency up to 40 MHz
- Two dual channel analog outputs
- Pixel rate up to 80 MSPS
- 960 us minimum image acquisition and readout time
- Gain modes for amplified signal
- 22% external quantum efficiency (850 nm wavelength)
- 13% external quantum efficiency (940 nm wavelength)
- Over 87% AC contrast (20 MHz modulation frequency)
- Over 85% AC contrast (40 MHz modulation frequency)
- Built-in temperature sensor
- Wafer level glass BGA package (Dimensions : 6.6 x 5.5 x 0.6 mm)
- AEC-Q100 qualified (grade 2)
- Ambient operating temperature ranges of -20 +85°C to -40 to +105°C

Description

MLX75024 is an optical time-of-flight (TOF) image sensor. Potential use cases include gesture recognition, automotive in-cabin monitoring, surveillance, people counting and robot vision. The sensor features 320 x 240 (QVGA) time-of-flight pixels based on DepthSense® pixel technology. MLX75024 is the successor of MLX75023, with enhanced sensitivity and reduced power consumption. In combination with MLX75123BA, Melexis’s dedicated ToF companion chip, the chipset provides a complete ToF sensor solution. The sensor is available in automotive and industrial grades, both in a small glass BGA wafer level package form factor which offers many integration possibilities.

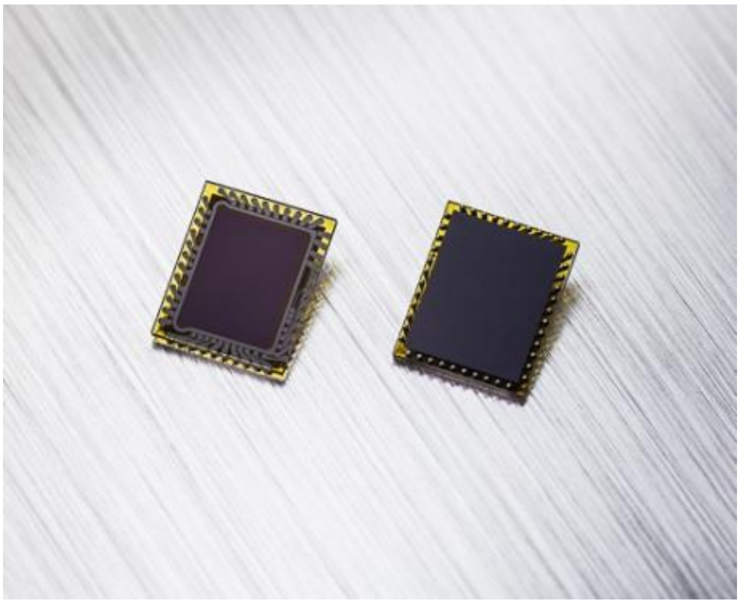

Figure 1: MLX75024 top (left) and bottom (right)

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1. Datasheet Changelog

Version	Date	Changes
0.10.6	13/Dec/2018	Preliminary release version.
0.10.7	03/Jan/2019	Addition of PDNU and PNNU formulas.
1.0	09/Apr/2019	ROI drawback related to gain mode updated. MLX75123BA FLIP_MIRROR mode & temperature readout limitation added.
1.1	18/Apr/2019	Change of the ARRAYBIAS current value without serial resistor. Addition of Dem. Contrast VS ARRAYBIAS voltage & MIXH voltage graphs.
1.2	02/Jan/2020	Modification of chapter 10 with details on timings and updated description of the different timing periods. Several grammar corrections. Addition of the DepthSense trademark disclaimer. Updated shelf life duration for samples with covertape.

Table 1: Changelog

2. Glossary of terms

Term	Definition
CAPD	Current Assisted Photonic Demodulator.
DC contrast	Capability of the sensor to demodulate signals under a constant light source.
AC contrast	Capability of the sensor to demodulate signals under a modulated light source.
Full well capacity	Maximum number of electrons which can be collected on a single tap of the pixel.
T_{INT}	Integration time. Period of time when DMIX signals are toggling, illumination is activated and electrons are captured in the pixels.
$T_{COOLDOWN}$	Period of time after integration when illumination is off.
T_{READ}	Period of time required to readout the values of all the pixels of the array.
PDNU	Pixel depth non uniformity. This metric is calculated on a depth map generated from the sensor's output data. It defines how much deviation is present between pixels (in distance) for a flat field measurement. PDNU is expressed in [m].
PNNU	Pixel norm non uniformity. This metric is calculated on a norm/confidence map generated from the sensor's output data. It defines how much contrast difference is present between pixels for a flat field measurement. PNNU is expressed in %.

Table 2: Glossary of terms

3. Ordering Information

Ordering example: MLX75024RTF-GAA-001-TR

Product	Temperature Code	Package	Option Code	Packing Form
MLX75024	R	TF	GAA-000	TR
MLX75024	S	TF	GAA-000	TR
MLX75024	R	TF	GAA-001	TR
MLX75024	S	TF	GAA-001	TR

Table 3: Product ordering code(s)

Legend:

Temperature Code	R : -40°C to 105°C S : -20°C to 85°C
Package Code	TF : Glass BGA Package, 44pins
Option Code	GAA-000 : without cover tape GAA-001 : with cover tape[1]
Packing Form	TR : Tray

Table 4: Option code(s)

[1] The properties of the covertape are guaranteed for 1 year after shipping date considering the devices are stored in appropriate conditions according the device MSL rating.

4. Application System Architecture

A complete TOF system or camera module typically includes the following main components:

- MLX75123 + MLX75024 TOF chipset
- An infrared (NIR) illumination source (LED or laser) with fast response and relaxation time.
- Beam shaping optics for the light distribution
- A receiving sensor lens, optimized for maximum NIR transmittance
- A microcontroller or DSP to calculate and process the data

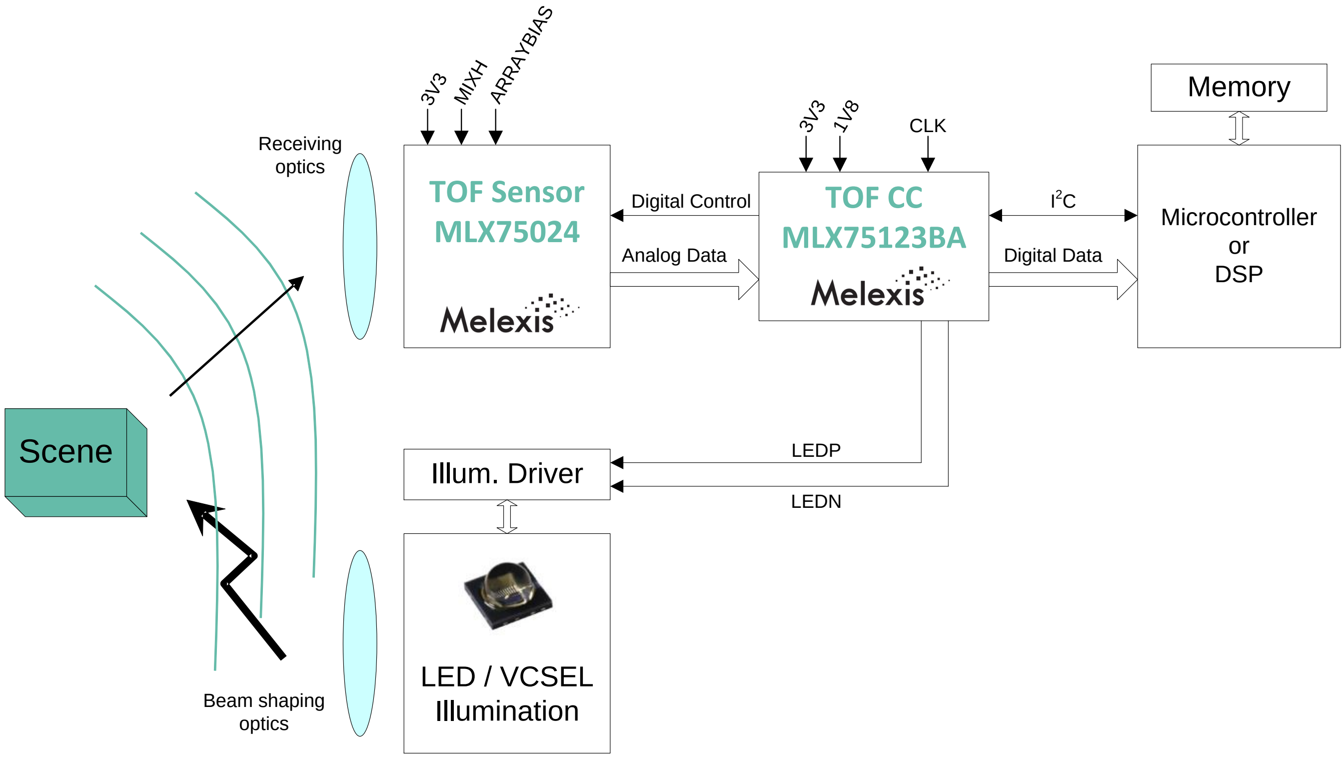

Figure 2: System architecture

5. Pinout Description

Designator	Pin #	Function	Description
ROW[7] ROW[6] ROW[5] ROW[4] ROW[3] ROW[2] ROW[1] ROW[0]	1 2 3 4 5 6 7 8	Digital Input	These inputs are used to apply the pixel row address of the pixel array controlled by the MLX75123BA.
ARRAYBIAS	9	Voltage Bias	Negative bias voltage.
PIXELVDD	10	Pixel voltage pin	Internally regulated pixel supply voltage pin.
VDDA	11	Analog Supply	
AGND	12	Ground	
OUT3	13	Analog Output	
OUT2	14	Analog Output	
OUT0	15	Analog Output	
OUT1	16	Analog Output	
LATCH_ENABLE	17	Digital Input	Enables the configuration of the sensor. Active high.
PIXELFLUSH	18	Digital Input	Control to clear charges in pixels. Active low.
CORE_RESET	19	Digital Input	Detector reset signal.
SHUTTER	20	Digital Input	Enable global shutter.
CS	21	Digital Input	Chip select. Active High.
DGND	22	Ground	
VDDD	23	Digital Supply	
COLUMN[0] COLUMN[1] COLUMN[2] COLUMN[3] COLUMN[4] COLUMN[5] COLUMN[6] COLUMN[7]	24 25 26 27 28 29 30 31	Digital Input	These inputs are used to apply the pixel column address of the pixel array controlled by the MLX75123BA.
DGND	32	Ground	
VDDD	33	Digital Supply	
DMIX[1] DMIX[0]	34 35	Digital Input	Modulation signals. Active High. Pulled-down internally.
DGND	36	Ground	
MIXH	37	Supply	Supply voltage for the demodulator
MIXH	38	Supply	Supply voltage for the demodulator
DGND	39	Ground	
DGND	40	Ground	
MIXH	41	Supply	Supply voltage for the demodulator
MIXH	42	Supply	Supply voltage for the demodulator
DGND	43	Ground	
VDDD	44	Digital Supply	

Table 5: MLX75024 Pinout

6. Typical Connection Diagram

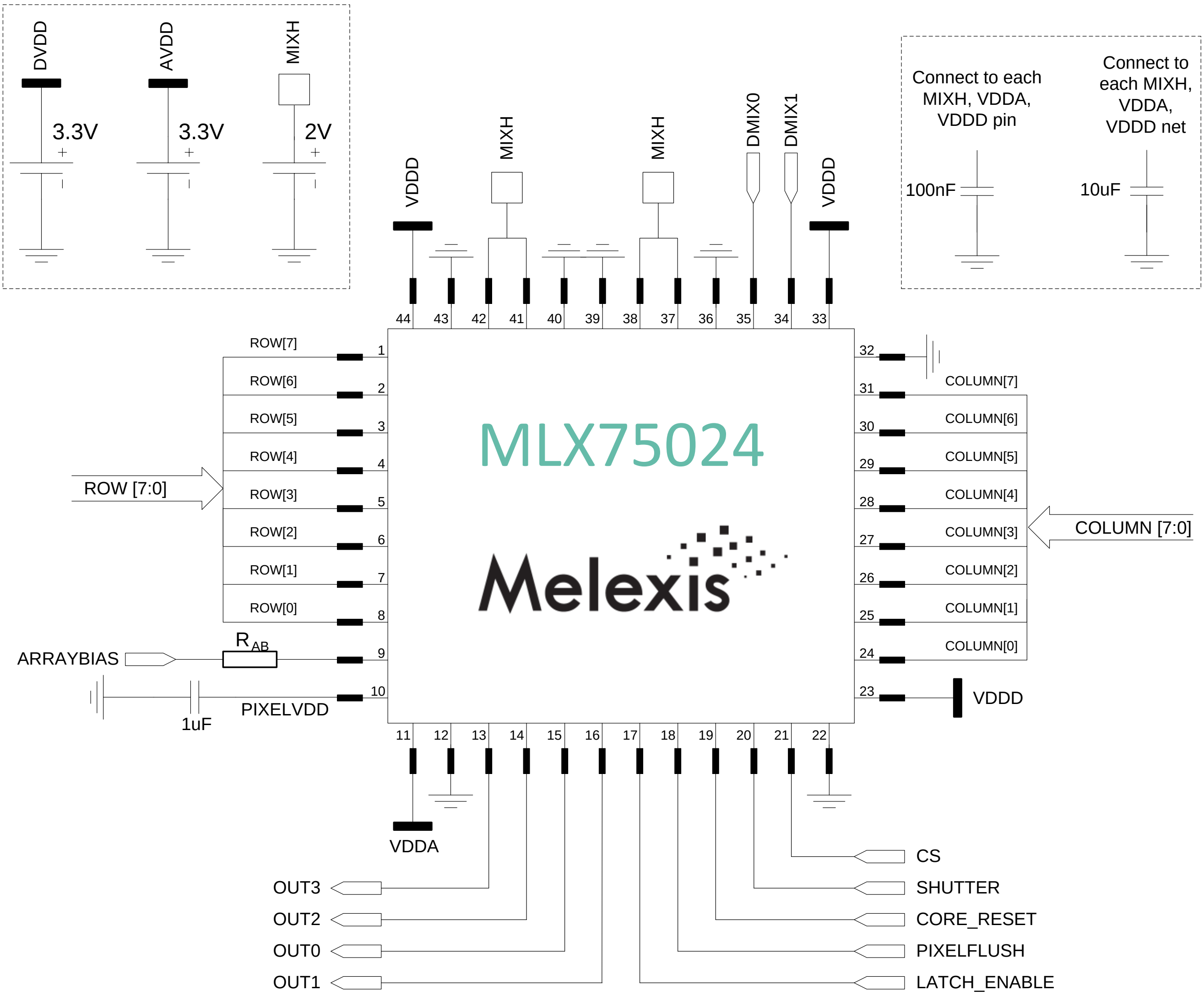

Figure 3: Typical connection diagram[2]

[2] R_{AB} value will influence the demodulation contrast of the sensor. Please refer to chapters 8.7.3, 8.7.4 and 8.7.5 for additional information. The performance of the MLX75024 has been tested with 68 Ω resistor for R_{AB} and -3.3V for the ARRAYBIAS voltage.

7. Block diagram

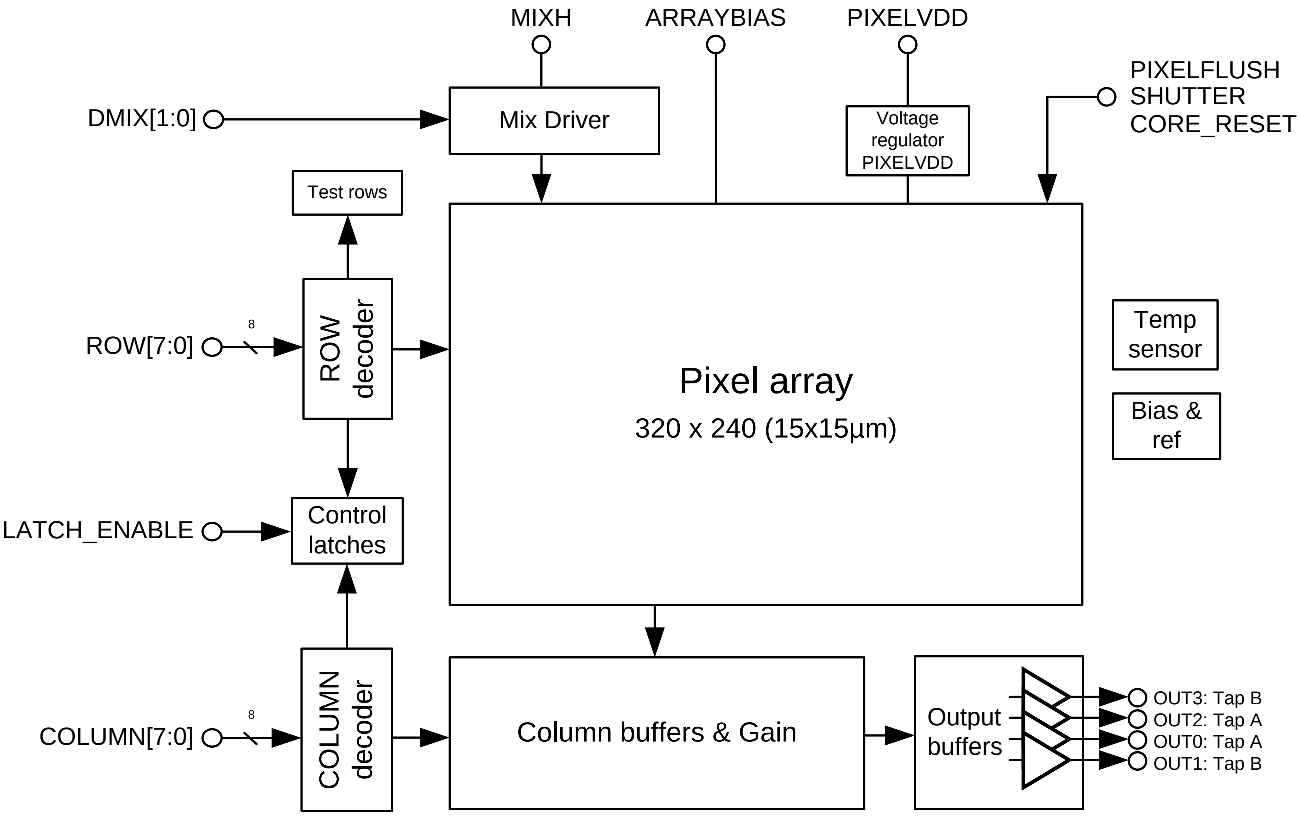

Figure 4: MLX75024 block diagram

8. Electrical Characteristics

8.1. Absolute Maximum Ratings

Absolute maximum ratings must not be exceeded to prevent permanent damage to the device. The device is not guaranteed to be functional while applying the absolute maximum stress.

Parameter	Symbol	Min.	Max.	Unit
3V3 DC input voltages	V_{DDX}	-0.3	4.5	V
MIXH input voltage	V_{MIXH}		2.5	V
Storage temperature	T_{stg}	-50	125	°C
Junction temperature	T_J		125	°C

Table 6: Absolute maximum ratings

8.2. ESD Ratings

Parameter	Symbol	Max.	Unit
Electrostatic discharge, human-body model (HBM) according to AEC-Q100-002	V_{ESD_HBM}	± 2000	V
Electrostatic discharge, charged-device model (CDM), according to ANSI/ESDA/JEDEC JS-002	V_{ESD_CDM}	±500	V

Table 7: ESD ratings

8.3. Digital IO Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital input threshold level high	V_{IH}	0.7* V_{DDD}			V
Digital input threshold level low	V_{IL}			0.3* V_{DDD}	V
Input hysteresis	V_{HYST}	0.5			V
Digital input leakage current	I_{DIN}			1	µA
Digital input pin capacitance	C_{DIN}			10	pF
Pull down resistor at DMIX	R_{PD_MIX}		50		kΩ

Table 8: Digital IO characteristics

8.4. Current consumption in operating conditions

If not mentioned, typical conditions for measurement of the following values are: V_{DDA} = 3.3V, V_{DDD} = 3.3V, ambient temperature = 27°C.

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
VDDA supply voltage		V_{DDA}	3.0	3.3	3.6	V
VDDA supply current	Integration	$I\_VDDA_{INTEGRATION\_CS\_H}$		38		mA
VDDA supply current	Readout, OUT_SR_2X = 0[3]	$I\_VDDA_{READOUT\_SR\_L}$		47		mA
VDDA supply current	Readout, OUT_SR_2X = 1[3]	$I\_VDDA_{READOUT\_SR\_H}$		70		mA
VDDA supply current	Readout, CS low	$I\_VDDA_{READOUT\_CS\_L}$		22		mA
VDDA supply current	POWER_DOWN	$I\_VDDA_{POWER\_DOWN}$		15		uA
VDDD supply voltage		V_{DDD}	3.0	3.3	3.6	V
VDDD supply current	During Idle time, before or after readout	I_VDDD_{IDLE}		2		µA
VDDD supply current	Integration, f_{MIX} = 20 MHz	$I\_VDDD_{INTEGRATION\_20MHZ}$		8	10	mA
VDDD supply current	Integration, f_{MIX} = 40 MHz	$I\_VDDD_{INTEGRATION\_40MHZ}$		16	20	mA
VDDD supply current	Readout	$I\_VDDD_{READOUT}$		300		uA
ARRAYBIAS supply voltage		$V_{ArrayBias}$	-5	-3.3	0	V
ARRAYBIAS supply current	V_{MIXH} = 2V, $V_{ArrayBias}$ = -3.3V 68Ω R_{AB}	$I_{ArrayBias}$		17		mA
MIXH supply voltage		V_{MIXH}	1.5	2	2.5	V
MIXH supply current	Integration, V_{MIXH} = 1.5V	$I_{MIXH\_1.5V}$		480	900	mA
MIXH supply current	Integration, V_{MIXH} = 2V	$I_{MIXH\_2.0V}$		720	1000	mA
MIXH supply current	Integration, V_{MIXH} = 2.5V	$I_{MIXH\_2.5V}$		760	1100	mA
PIXELVDD voltage[4]	GAIN_CTRL = 00b	PIX_{VDD_GAIN1}		2.85		V
PIXELVDD voltage[4]	GAIN_CTRL = 11b	$PIX_{VDD\_GAIN\_bypass}$		2.7		V

Table 9: Current consumption table in operation conditions

[3] See 9.1 for additional information about the slew rate parameter.

[4] PIXELVDD is non usable as a voltage output pin.

8.5. Dynamic Characteristics

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Column addressing frequency	OUT_SR_2X = 0[5]	f_{COLUMN}			25[6]	MSPS
Column addressing frequency	OUT_SR_2X = 1[6]	f_{COLUMN}			40	MSPS
Row addressing frequency		f_{ROW}			0.5	MSPS
DMIX frequency		f_{MIX}		20	40	MHz
Delay row/column to analog output settled	OUT_SR_2X = 0[5]	t_{VAL}		26	30	ns
Delay row/column to analog output settled	OUT_SR_2X = 1[6]	t_{VAL}		18.2	25	ns
Output ready after CS high		T_{SETTLE_CS}			60	ns
OUTx output swing		$RANGE_{OUT}$		1.55		V
OUTx output voltage		V_{OUT}	0		1.9	V
OUTx load capacitance	OUT_DRIVE_2X = 0[7]	C_{OUT}			20	pF
OUTx load capacitance	OUT_DRIVE_2X = 1[7]	C_{OUT}			40	pF

Table 10: Dynamic characteristics

8.6. Temperature sensor characteristics

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Gain of temperature sensor		K_{PTAT}	1.74	1.79	1.85	mV/K
Differential PTAT output voltage	Calibrated at 35°C	V_{PTAT}		563.5		mV
Temperature error with 35°C calibration	$T_{JUNCTION}$ = 35°C	$ERROR_{TEMP\_35}$	-3.00		3.00	K
Temperature error with 35°C calibration	$T_{JUNCTION}$ = 85°C	$ERROR_{TEMP\_85}$	-4.80		4.80	K
Temperature error with 35°C calibration	$T_{JUNCTION}$ = 105°C	$ERROR_{TEMP\_105}$	-5.50		5.50	K
Temperature error with 35°C calibration	$T_{JUNCTION}$ = 0°C	$ERROR_{TEMP\_0}$	-4.10		4.10	K
Temperature error with 35°C calibration	$T_{JUNCTION}$ = -40°C	$ERROR_{TEMP\_-40}$	-5.50		5.50	K

Table 11: Temperature sensor characteristics

[5] See chapter 9.1 for additional information about the slew rate.

[6] High slew rate (OUT_SR_2X) must be used in case of 25 MSPS < f_{COL} < 40 MSPS. This will increase the power consumption of the sensor. See Table 9 for power consumption values. Setting OUT_DRIVE_2X = 1 and OUT_SR_2X = 1 at the same time will only enable high slew rate mode without affecting the driving capability of the output buffer. OUT_DRIVE_2X should be set to zero when enabling high slew rate mode to reduce the power consumption of the sensor.

[7] See chapter 9.1 for additional information about the driving capability of the output buffer.

8.7. Sensor Optical and Physical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External quantum efficiency	EQE_{850}	850 nm		23		%
External quantum efficiency	EQE_{940}	940 nm		13		%
DC contrast	C_{DC_850}	850 nm		95		%
AC contrast	$C_{AC\_850\_20MHz}$	850 nm, f_{MIX} = 20 MHz		87		%
AC contrast	$C_{AC\_850\_40MHz}$	850 nm, f_{MIX} = 40 MHz		85		%
DC contrast	C_{DC_940}	940 nm		95		%
AC contrast	$C_{AC\_940\_20MHz}$	940 nm, f_{MIX} = 20 MHz		87		%
AC contrast	$C_{AC\_940\_40MHz}$	940 nm, f_{MIX} = 40 MHz		85		%
Full well capacity	FWC_{GAIN_bypass}	GAIN_CTRL = 11b		458		ke-
Full well capacity	FWC_{GAIN_1}	GAIN_CTRL = 00b		483		ke-
Full well capacity	FWC_{GAIN_2}	GAIN_CTRL = 01b		246		ke-
Full well capacity	FWC_{GAIN_3}	GAIN_CTRL = 10b		137		ke-
PDNU local	$PDNU_{LOCAL\_20MHZ}$	20 MHz		0.38		cm
PDNU global	$PDNU_{GLOBAL\_20MHZ}$	20 MHz		7.41[8]		cm
PDNU local	$PDNU_{LOCAL\_40MHZ}$	40 MHz		0.34		cm
PDNU global	$PDNU_{GLOBAL\_40MHZ}$	40 MHz		9.58[8]		cm
PNNU local	$PNNU_{LOCAL\_20MHZ}$	20 MHz		1.2		%
PNNU global	$PNNU_{GLOBAL\_20MHZ}$	20 MHz		7		%
PNNU local	$PNNU_{LOCAL\_40MHZ}$	40 MHz		1.05		%
PNNU global	$PNNU_{GLOBAL\_40MHZ}$	40 MHz		11.9		%

Table 12: Optical & physical characteristics

8.7.1. PDNU and PNNU global calculation

PDNU global and PNNU global are metrics calculated by dividing the image in blocks of 10 by 10 pixels and calculating the mean distance and mean norm values of these blocks.

PDNU will be the difference of the maximum and the minimum mean value of the distance of the blocks. It is expressed in centimetres.

PNNU will be the difference of the maximum and the minimum mean value of the amplitude of the blocks, divided by the mean of the complete image. It is expressed in percent.

[8] This value is for uncalibrated distance map. This non uniformity is constant for each device and can be calibrated.

8.7.2. PDNU and PNNU local calculation

PDNU local and PNNU local are using 3 by 3 pixels cells, a pixel and its neighbours. For every 3 by 3 pixels cluster (there are 8480 clusters of 3 by 3 pixels on a QVGA image) two factors are calculated:

$$Dn = \frac{\sum_{i=1}^{9}(CONFIDENCE_i - AVERAGE(CONFIDENCE[3\times 3]))^2}{9}$$

$$Dp = \frac{\sum_{i=1}^{9}(Phase_i - AVERAGE(Phase[3\times 3]))^2}{9}$$

Then: $PDNU_{LOCAL} = \sqrt{\frac{\sum_{j=1}^{8480} Dp_j}{8480}}$ and $PNNU_{LOCAL} = \sqrt{\frac{\sum_{j=1}^{8480} Dn_j}{8480}}$

8.7.3. Demodulation contrast & ARRAYBIAS voltage

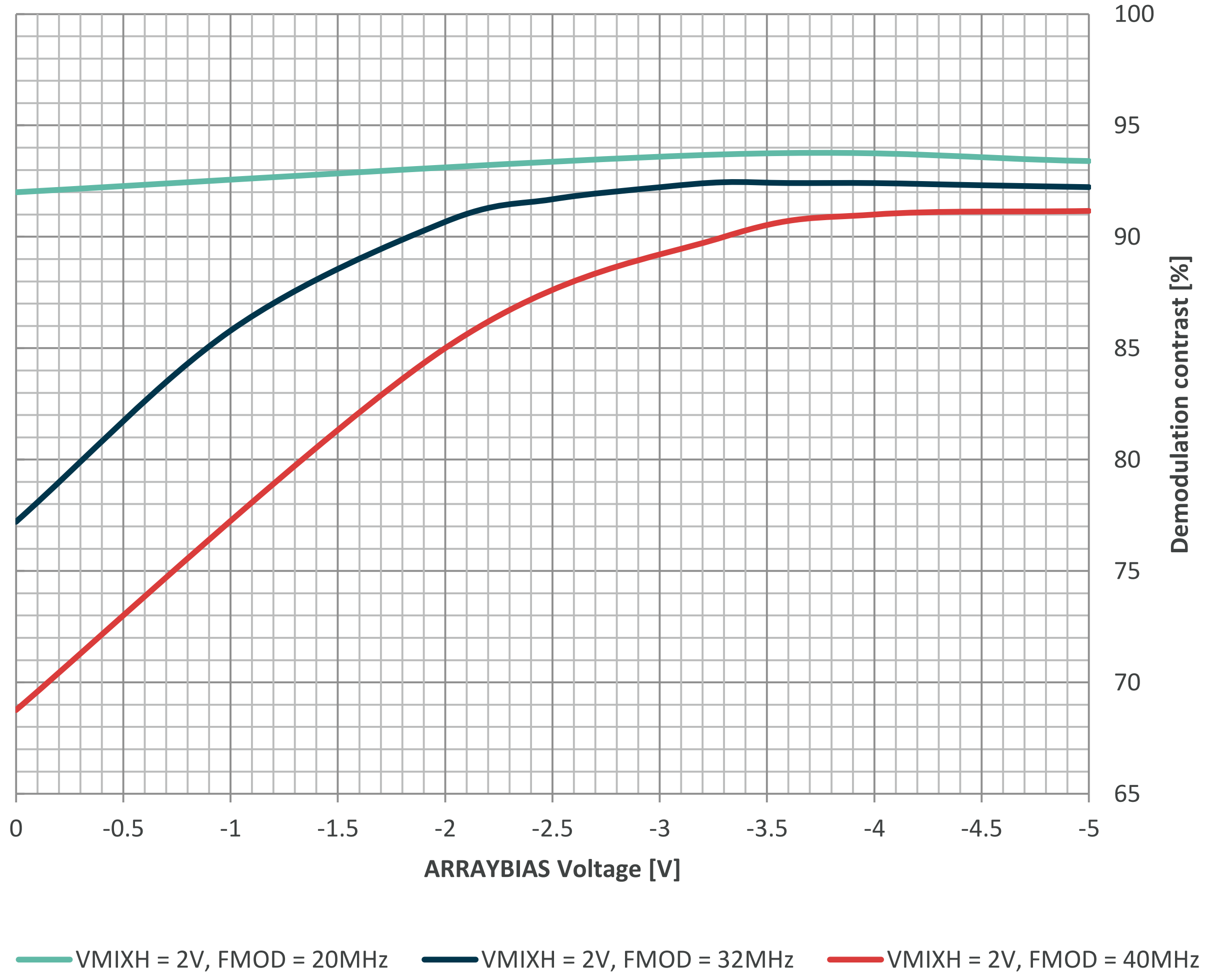

Figure 5: Typical demodulation contrast versus $V_{ArrayBias}$ at 25°C, 2V V_{MIXH} and 68 Ohm R_{AB} with three different modulation frequencies.

8.7.4. Demodulation contrast & R_{AB}

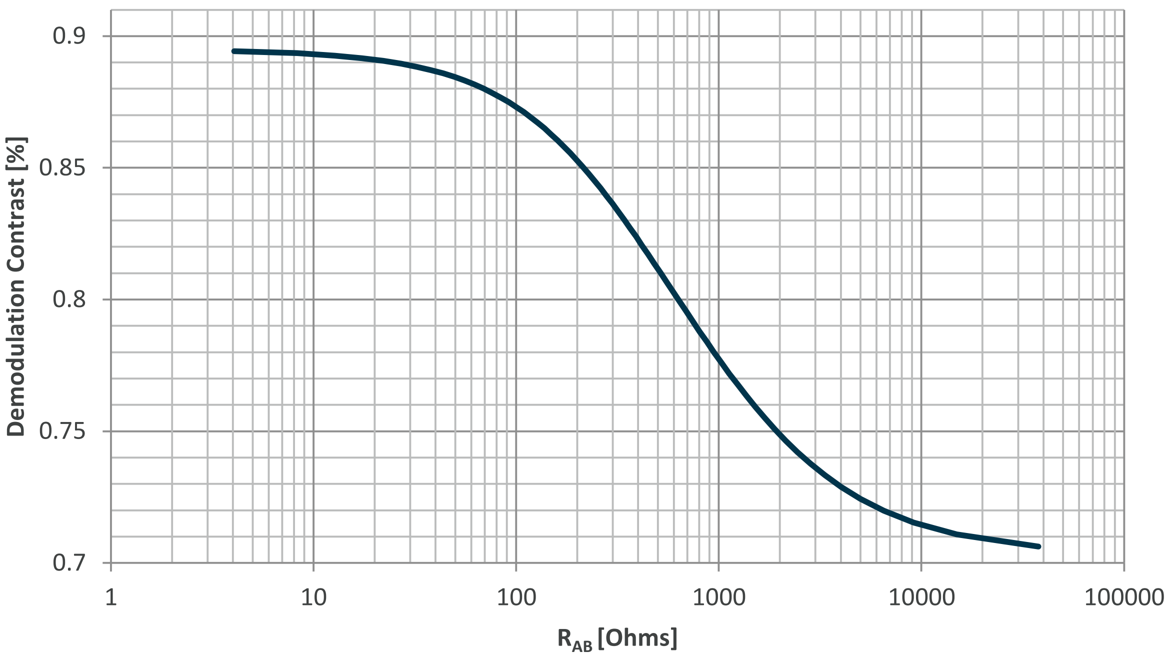

Figure 6: Typical demodulation contrast versus R_{AB} resistor at 25°C, 2V $V_{MIXH,}$ 40 MHz modulation frequency and -3.3 ARRAYBIAS voltage.

8.7.5. Demodulation contrast & ARRAYBIAS current

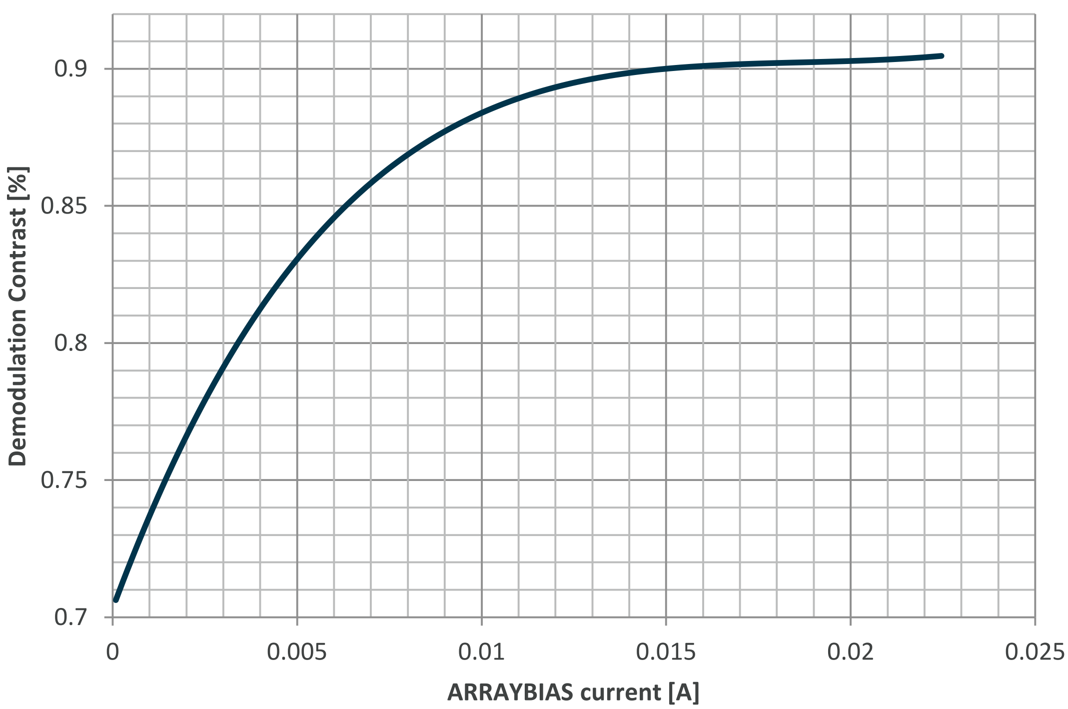

Figure 7: Typical demodulation contrast versus ARRAYBIAS current at 25°C, 2V V_{MIXH} and 68 Ohm $R_{AB,}$ 40 MHz modulation frequency and -3.3 ARRAYBIAS voltage.

8.7.6. Demodulation contrast & MIXH voltage

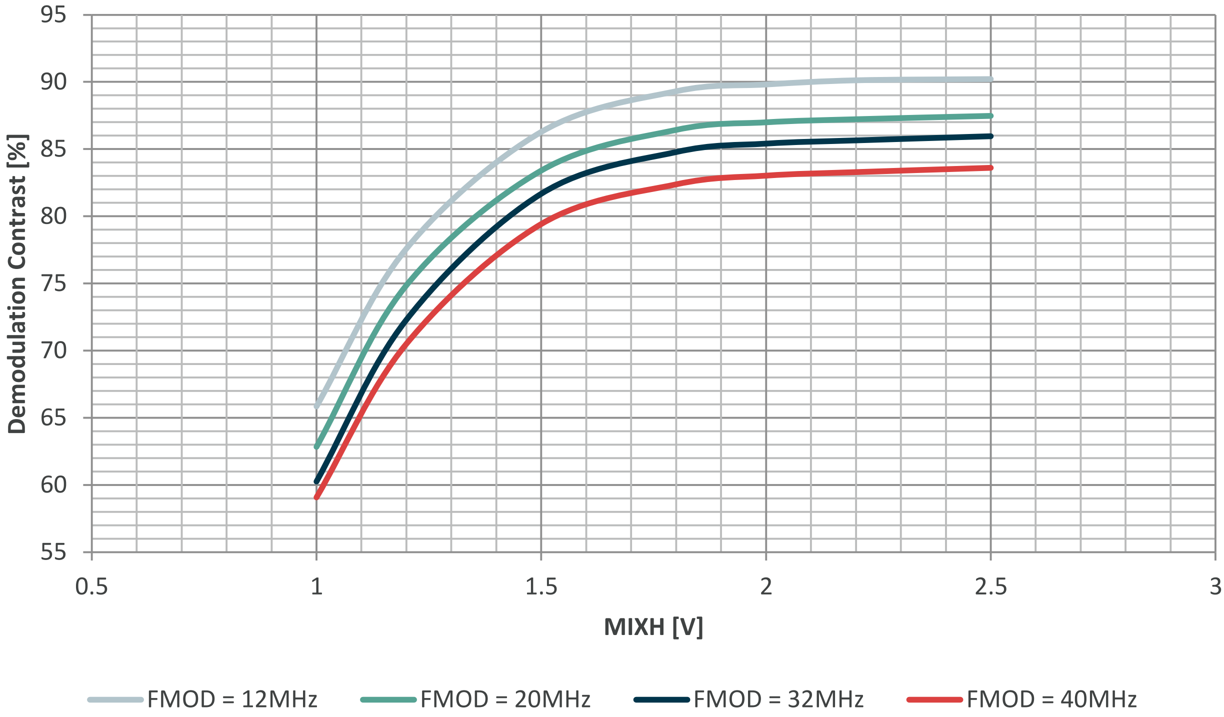

Figure 8: Typical demodulation contrast versus V_{MIXH} at 25°C, -3V3 $V_{ArrayBias}$ and 68 Ohm R_{AB} with 4 different modulation frequencies.

8.7.7. ARRAYBIAS voltage and current consumption

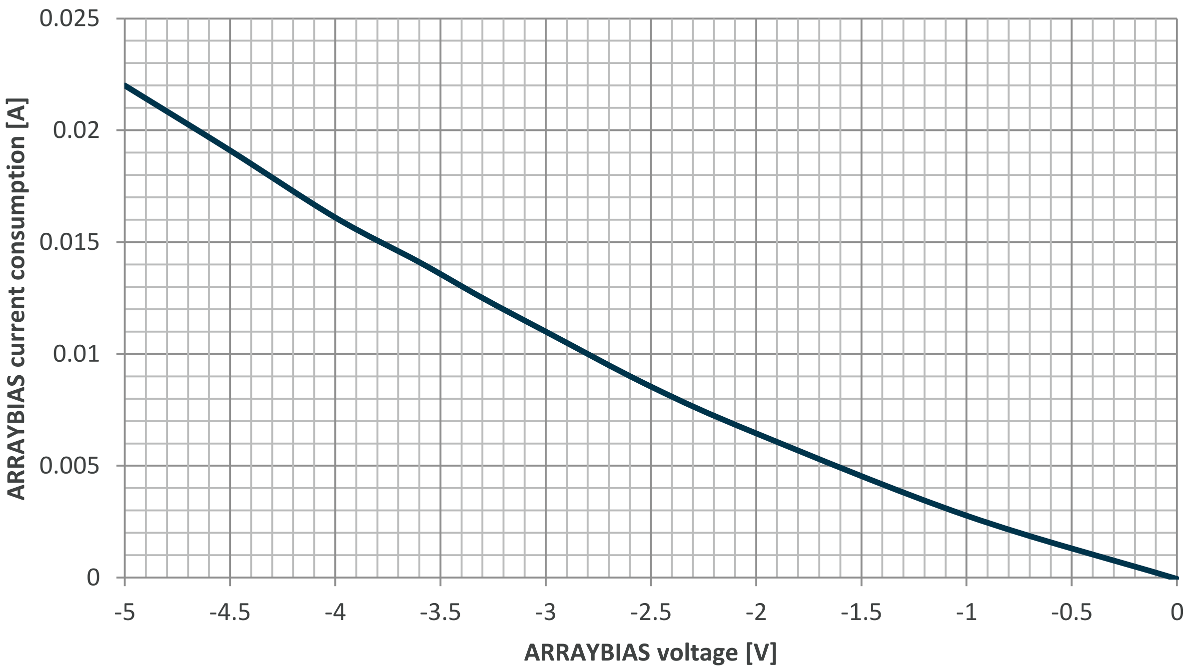

Figure 9: Typical current consumption on the ARRAYBIAS pin depending on the ARRAYBIAS voltage applied.

8.8. Signal Chain, Noise and Gain Modes Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Camera gain	$C\_GAIN_{GAIN\_bypass}$	GAIN_CTRL = 11b		3.47		uV/e-
Camera gain	$C\_GAIN_{GAIN\_1}$	GAIN_CTRL = 00b		3.2		uV/e-
Camera gain	$C\_GAIN_{GAIN\_2}$	GAIN _CTRL = 01b		5.9		uV/e-
Camera gain	$C\_GAIN_{GAIN\_3}$	GAIN _CTRL = 10b		10.3		uV/e-
Dark voltage	$V\_DARK_{GAIN\_bypass}$	GAIN _CTRL = 11b		1.75		V
Dark voltage	$V\_DARK_{GAIN\_1}$	GAIN _CTRL = 00b		1.7		V
Dark voltage	$V\_DARK_{GAIN\_2}$	GAIN _CTRL = 01b		1.65		V
Dark voltage	$V\_DARK_{GAIN\_3}$	GAIN _CTRL = 10b		1.55		V
Bright voltage	$V\_BRIGHT_{GAIN\_bypass}$	GAIN _CTRL = 11b		0.2		V
Bright voltage	$V\_BRIGHT_{GAIN\_1}$	GAIN _CTRL = 00b		0.2		V
Bright voltage	$V\_BRIGHT_{GAIN\_2}$	GAIN _CTRL = 01b		0.2		V
Bright voltage	$V\_BRIGHT_{GAIN\_3}$	GAIN _CTRL = 10b		0.2		V
Analog output swing	$SWING_{GAIN\_bypass}$	GAIN _CTRL = 11b		1.55		V
Analog output swing	$SWING_{GAIN\_1}$	GAIN _CTRL = 00b		1.5		V
Analog output swing	$SWING_{GAIN\_2}$	GAIN _CTRL = 01b		1.45		V
Analog output swing	$SWING_{GAIN\_3}$	GAIN _CTRL = 10b		1.35		V
Dark noise	DN_{GAIN_bypass}	GAIN _CTRL = 11b		130		e-
Dark noise	DN_{GAIN_1}	GAIN _CTRL = 00b		156		e-
Dark noise	DN_{GAIN_2}	GAIN _CTRL = 01b		135		e-
Dark noise	DN_{GAIN_3}	GAIN _CTRL = 10b		128		e-

Table 13 : Signal chain, noise and gain modes characteristics.

9. Device programming interface

9.1. Configuration latches

LATCH_ENABLE allows to program latches which control the general behaviour of the circuitry.

When LATCH_ENABLE is set to high, the ROW[7:0] and COLUMN[7:0] inputs are the latch inputs.

There exist 16 latches (8 on the row address lines and 8 on the column lines) which generally configure some functions of the device. The definition of the latches inputs are described in the following tables:

Latch input	Function	Function name
ROW[0]	Power down mode of the image sensor	POWER_DOWN
ROW[1]	Columns 0 to 3 and 316 to 319 will be replaced by the test pixels	TEST_COLUMN_OUT
ROW[2]	GAIN control bit 0	GAIN_CTRL<0>
ROW[3]	GAIN control bit 1	GAIN_CTRL<1>
ROW[4]	High power mode of analog output buffer[9]	OUT_DRIVE_2X
ROW[5]	High slew rate mode of analog output buffer[10]	OUT_SR_2X
ROW[6]	Reserved – Set to zero	Reserved
ROW[7]	Power down mode of the image sensor	POWER_DOWN

Table 14: Column Latch definition table

Latch input	Function	Function name
COLUMN[0]	Reserved – Set to zero	Reserved
COLUMN[1]	Reserved – Set to zero	Reserved
COLUMN[2]	Reserved – Set to zero	Reserved
COLUMN[3]	Reserved – Set to zero	Reserved
COLUMN[4]	Reserved – Set to zero	Reserved
COLUMN[5]	Shall be set to 1 when reading rows backward.	REVERSE_ROW
COLUMN[6]	Reset and initialization	INIT
COLUMN[7]	Shall be set to 1 when reading columns backward.	REVERSE_COLUMN

Table 15: Row Latch definition table

[9] OUT_DRIVE_2X is used to double the driving capability of the output buffer in order to be able to drive 40 pF load compared to standard 20 pF load. It is necessary in situations where one MLX75123 companion chip is driving 2 MLX75024 sensors where PCB trace load is expected to be higher than in standard mode.

[10] High slew rate (OUT_SR_2X) must be used in case of 25 MSPS < f_{COL} < 40 MSPS. This will increase the power consumption of the sensor. See Table 9 for power consumption values. Setting OUT_DRIVE_2X = 1 and OUT_SR_2X = 1 at the same time will only enable high slew rate mode without affecting the driving capability of the output buffer. OUT_DRIVE_2X should be set to zero when enabling high slew rate mode to reduce the power consumption of the sensor.

9.2. Signal Gain function

The MLX75024 features an active gain of the pixel output signal. ROW[3:2] = GAIN_CTRL[1:0] enables the gain settings:

- GAIN_CTRL[1:0] = 00b: GAIN_Mode = 1
- GAIN_CTRL[1:0] = 01b: GAIN_Mode = 2
- GAIN_CTRL[1:0] = 10b: GAIN_Mode = 3
- GAIN_CTRL[1:0] = 11b: Gain function is bypassed or GAIN_Bypass = 1

Changing the gain setting of the signal path will change the camera gain and dynamic range of the sensor. The affected performance parameters of the GAIN_CTRL setting are listed in Table 12 and Table 13.

Based on application conditions the following setting can be applied:

- GAIN_Bypass = 1 bypasses the active gain signal path. The mode has the best performance in regards to noise and signal range but the fixed pixel to pixel variance of the dark voltage is higher than for GAIN_MODE =1.
- GAIN_Mode = 1 sets the active gain of the pixel signal to one. The fixed pixel to pixel variance of the dark voltage is lower but the noise is slightly higher than for GAIN_Bypass = 1 (refer to Table 12 and Table 13). The GAIN_Mode = 1 is the preferred operating mode.
- GAIN_MODE = 2 and GAIN_MODE = 3 increases the camera gain but decreases the dynamic range. Due to the increased camera gain the impact of disturbances and noise in the signal path including ADC is lowered. The system is more perceptive to dark objects but less robust in regards to sunlight.

9.3. Image flip & mirror modes

The MLX75024 has specific features to cope with the flip and mirror modes of the MLX7513BA companion chip. COLUMN[5] and COLUMN[7] enables the REVERSE_ROW and REVERSE_COLUMN functions. Correct settings of the MLX75024 & MLX75123BA are explained in the table below:

MLX75123BA function	MLX75123BA Tx_FLIP_MIRROR value	MLX75024 corresponding function	MLX75123BA corresponding Tx_Bx_LATCH value
FLIP (along horizontal axis)	2’b01	REVERSE_ROW	0x2000
MIRROR (along vertical axis)	2’b10	REVERSE_COLUMN	0x8000
FLIP & MIRROR	2’b11	REVERSE_ROW & REVERSE_COLUMN	0xA000

When using FLIP & MIRROR mode, there is no possibility of reading out the MLX75024 temperature data using the MetaData.

10. Interface

10.1. Timing Diagrams

This timing diagram is a typical communication and timing flow to control the MLX75024. The MLX75123BA is managing all these timings and durations automatically by the use of programmable registers.

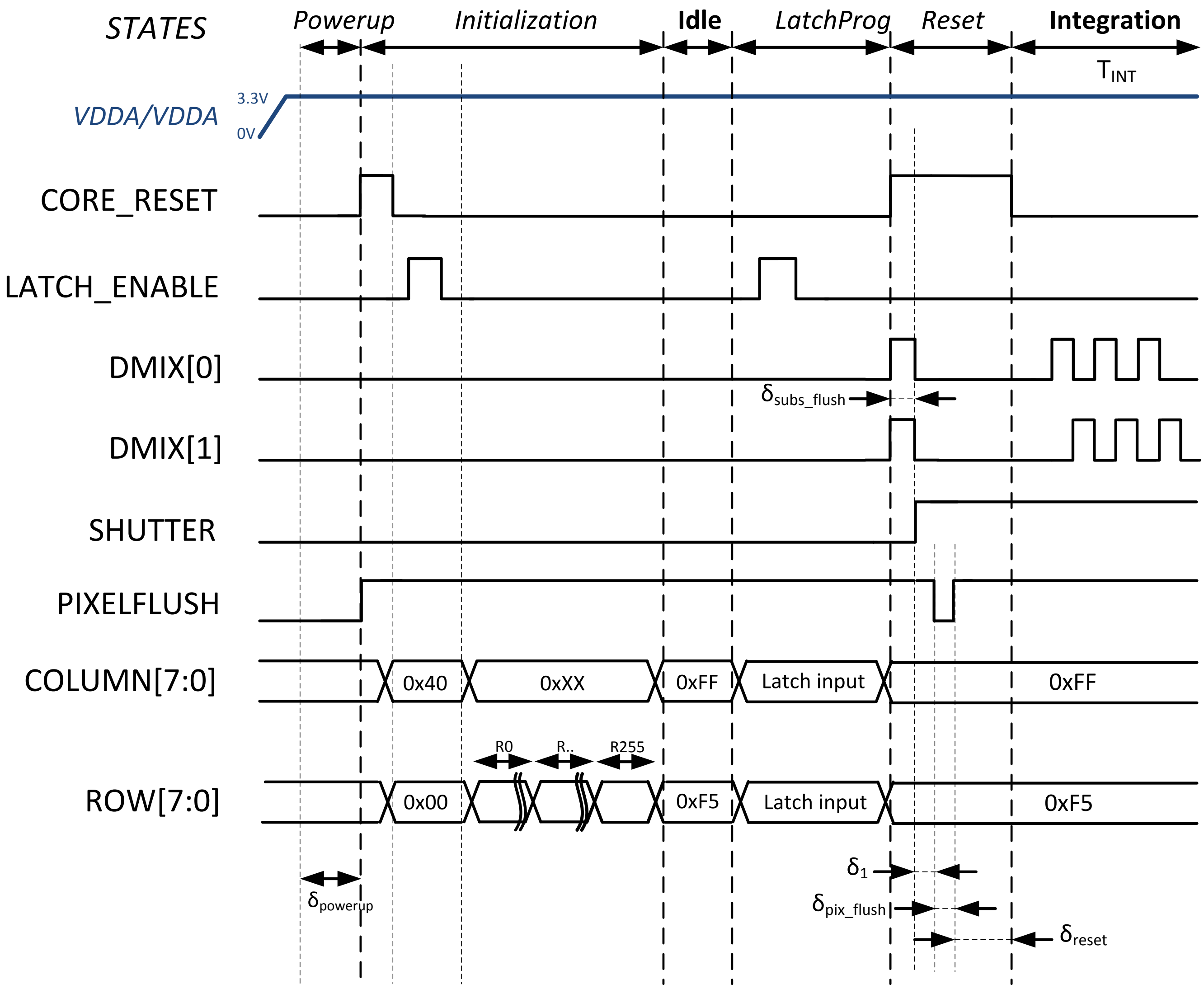

Figure 10: Global timing diagram from power up to integration. Each phase consists of a reset period, an integration period and a read-out period.

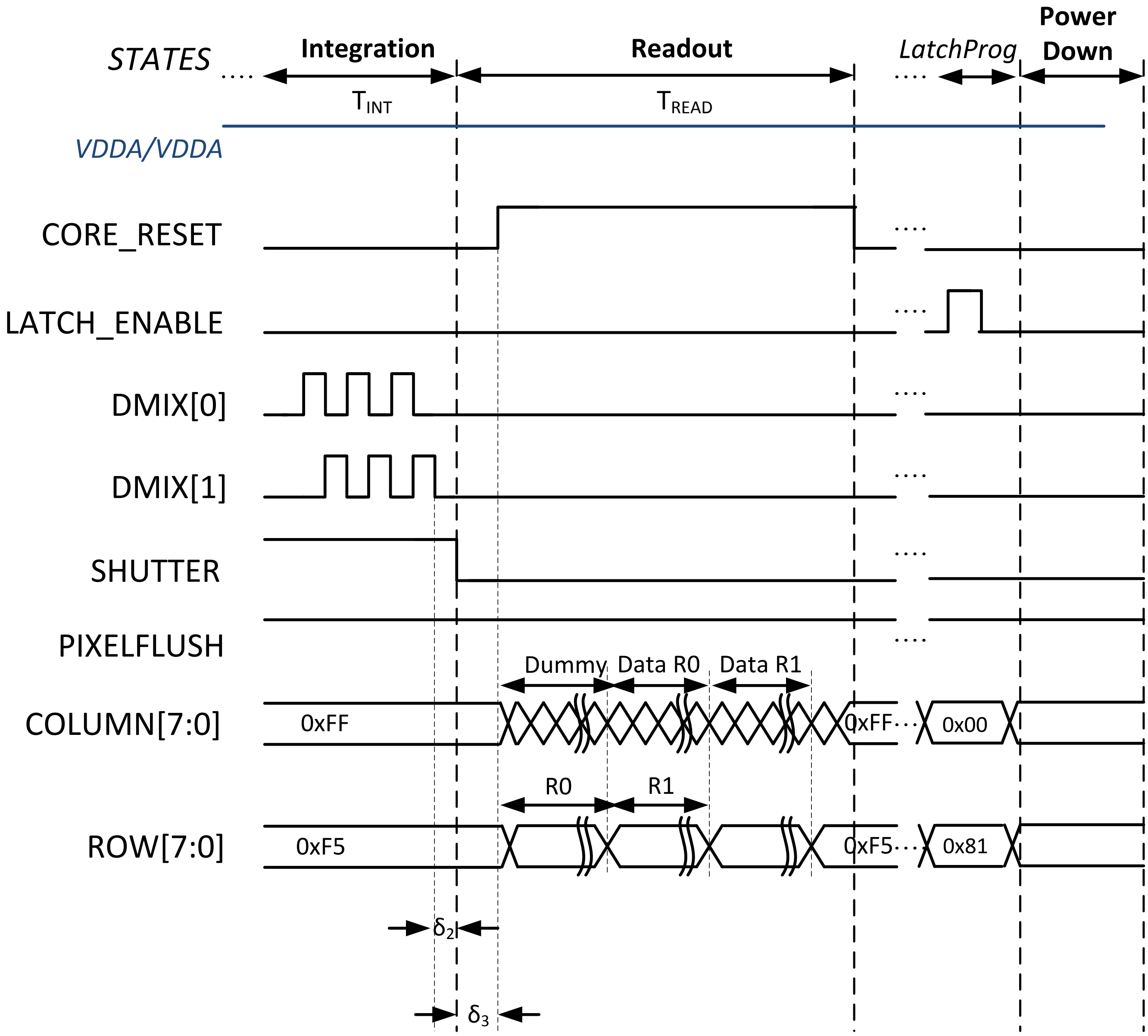

Figure 11: Global timing diagram from integration to power down. Each phase consists of a reset period, an integration period and a read-out phase. The last LatchProg phase here is used to put the sensor in Power Down mode.

Timing parameter	Condition
$\delta_{powerup}$	$\delta_{powerup} \geq 5$ ms
δ_{subs_flush}	$\delta_{subs\_flush} \geq 100$ ns
δ_1	$\delta_1 \geq 0.1$ us
δ_{pix_flush}	$\delta_{pix\_flush} = 5$ us
δ_{reset}	$\delta_{reset} \geq 5$ us
δ_2	$\delta_2 \geq 0.1$ us
δ_3	$\delta_3 \geq 1$ us

Table 16: Timing parameters table

10.2. Power Up and Initialization

The power up period shall last at least for a period of time equal to $\delta_{powerup}$ (defined in Table 16) after the supply reached the nominal value. This is indicated on the timing diagram by the $\delta_{powerup}$ value. After this power up period, the MLX75024 will be able to be programmed using the configuration latches[11]. A code of 0x00 must be applied to the ROW[X] bus and 0x40 to the COLUMN[X] bus at the falling edge of LATCH_ENABLE signal. Setting COLUMN[6] (INIT, see Table 15) during LATCH_EN falling edge prepares the image sensor for normal operation. This procedure ensures proper functionality and performance. The initialization period requires 256 ROW[7:0] counts as shown in Figure 10. Output data will be invalid during the initialization period. If the described initialization period has not been respected, the output data will also be invalid.

Note, that COLUMN[6] (INIT, see Table 15) during LATCH_EN falling edge 0 always starts the initialization period of the device and the content of the following 256 ROW counts must be neglected.

10.3. Latch Programming

Re-configuration changes the behaviour of the MLX75024 by using the LATCH_ENABLE input. It is recommended that latch programming period is executed before each integration period. The gain can be programmed during this phase, for example.

10.4. Reset

The Reset period will happen at the beginning of every phase capture. The electronic shutter shall be opened by setting SHUTTER to HIGH.

- Step 1 : Substrate flush

  During step 1, mix signals DMIX0 and DMIX1 are pulled HIGH for a period of time equal to δ_{subs_flush} (see Table 16).
  The step ends by pulling DMIX0 and DMIX1 terminal LOW.

- Step 2 : Pixel flush

  The second step implements a flushed reset by switching PIXELFLUSH low during a period of time equal to δ_{pix_flush}, (see Table 16) and with CORE_RESET HIGH.

- Step 3 : Reset

  The 3rd step of the reset period lasts for a period of time equal to δ_{reset} (see Table 16), where the PIXELFLUSH is asserted.
  During the 2nd and 3rd phase of the reset, DMIX0 and DMIX1 states shall be LOW.

10.5. Integration

After the reset period, the integration period is started. The electronic shutter shall be kept open (keep SHUTTER HIGH). The mix signals DMIX[0] and DMIX[1] are alternated using the Time-of-Flight modulation

[11] See 9.1 for additional details about the programming of the device.

pattern. These two signals are in opposition of phase. DMIX[0] is high when DMIX[1] is low and vice versa. When the integration is completed, the mix signals DMIX[0] and DMIX[1] shall be again put in idle state LOW. The electronic shutter must be closed by setting SHUTTER to LOW.

10.6. Read-out

Reading out the sensor is done by toggling both Row and Column addresses. Both addresses have 8 bit width. The Row binary word is directly mapped to the row number. The column binary word is toggled from 00h to 9Fh (0 to 159).

When selecting column 1, OUT0/3 offer the data from pixel 1, while OUT1/2 offer the data from pixel 9.
When selecting column 8, OUT0/3 offer the data from pixel 16, while OUT1/2 offer the data from pixel 24.
As such when selecting column N, the data at

OUT0/3 is output of pixel (N MOD 8) + 16*FLOOR(N/8)

OUT1/2 is output of pixel (N MOD 8) + 16*FLOOR(N/8) + 8

Column binary word	OUT0/3 : Pixel #	OUT1/2 : Pixel #
0	0	8
1	1	9
…	…	…
6	6	14
7	7	15
8	16	24
9	17	25
…	…	…
15	23	31
16	32	40
17	33	41
…	..	…

Table 17: Read-out table

For gain operation (GAIN_Mode = 1, 2, 3. See 9.2), the column addressing needs to toggle for proper operation, so it is required to toggle the column already when addressing the first row (ROW[0]), even though there might be no meaningful data (Dummy) shifted out. The MLX75123BA ToFCC is taking care of this automatically. This is not required in GAIN_Bypass = 1 mode.

The minimum number of columns which needs to be read out is 80 columns in GAIN_Mode = 1, 2 or 3. This is not required in GAIN_Bypass = 1 mode.

10.7. Test Rows Specification

MLX75024 has built in test patterns (the first 5 rows of the 8 test rows) that can be used to debug the analog to digital conversion or verify if the chipset and communication between the MLX75024 and the MLX75123 is working properly. Test rows are always enabled and can be read-out and addressed like any other pixel row. The test rows patterns will represent the column number presented in a binary way. It is used to test the column decoder. The pattern is described in the following table and shown in the images below:

Row No.	Figure 2	Col 0	Col 1	…	Col 255	Col 256	…	Col319
240	Tap A	! COLUMN[0][12]	! COLUMN[0]	…	! COLUMN [0]	! COLUMN [0]	…	! COLUMN[0]
241	Tap A	COLUMN[1]	COLUMN[1]	…	COLUMN[1]	COLUMN[1]	…	COLUMN[1]
242	Tap A	COLUMN[3]	COLUMN[3]	…	COLUMN[3]	COLUMN[3]	…	COLUMN[3]
243	Tap A	COLUMN[5]	COLUMN[5]	…	COLUMN[5]	COLUMN[5]	…	COLUMN[5]
244[13]	Tap A	COLUMN[7]	COLUMN[7]	…	COLUMN[7]	COLUMN[7]	…	COLUMN[7]
240	Tap B	COLUMN[8]	COLUMN[8]	…	COLUMN[8]	COLUMN[8]	…	COLUMN[8]
241	Tap B	COLUMN[0]	COLUMN[0]	…	COLUMN[0]	COLUMN[0]	…	COLUMN[0]
242	Tap B	COLUMN[2]	COLUMN[2]	…	COLUMN[2]	COLUMN[2]	…	COLUMN[2]
243	Tap B	COLUMN[4]	COLUMN[4]	…	COLUMN[4]	COLUMN[4]	…	COLUMN[4]
244[13]	Tap B	COLUMN[6]	COLUMN[6]	…	COLUMN[6]	COLUMN[6]	…	COLUMN[6]

Table 18: Test row description

[12] The test pattern of row 240 represents the opposite value of the LSB of the column index.

[13] Test row 244 test pattern can only be read-out in reverse mode using the REVERSE_ROW option setting the COLUMN[5] latch control bit to 1. See Configuration latches for additional information.

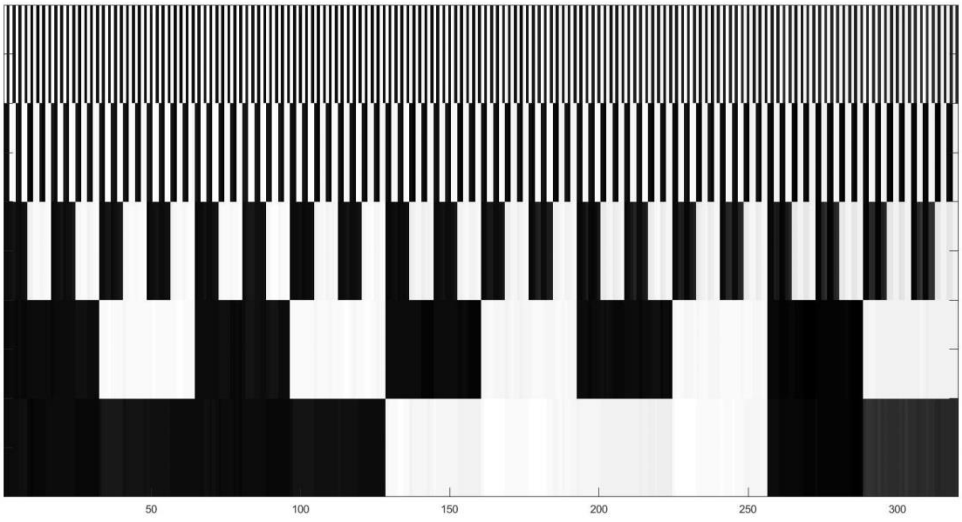

Figure 12 : Raw tap A image of the test rows readout in reverse mode. Top row being row 240, bottom one being row 244.

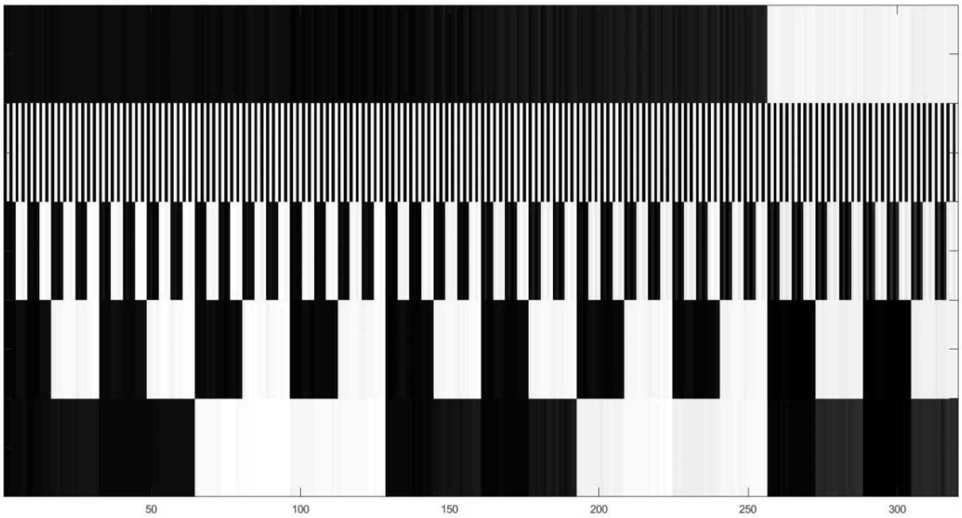

Figure 13: Raw tap B image of the test rows readout in reverse mode. Top row being row 240, bottom one being row 244.

10.8. Test Columns Specification

When TEST_COLUMN_OUT (ROW[1] latch control bit, see 9.1) is high, the first 4 columns of the array will be switched into the row ID addresses, or the row number presented in a binary way. It is used to test the row decoder.

The last 4 columns of the pixel array will also be switched into the row ID addresses, or the row number presented in a binary way. The reason to duplicate this is to be able to read the pattern with another set of the output terminals.

Col No.		Row 0	Row 1	...	Row 200	Row 201	Row 202	...	Row 239
0	Tap A	ROW[1]	ROW[1]	...	ROW[1]	ROW[1]	ROW[1]	...	ROW[1]
1	Tap A	ROW[3]	ROW[3]	...	ROW[3]	ROW[3]	ROW[3]	...	ROW[3]
2	Tap A	ROW[5]	ROW[5]	...	ROW[5]	ROW[5]	ROW[5]	...	ROW[5]
3	Tap A	ROW[7]	ROW[7]	...	ROW[7]	ROW[7]	ROW[7]	...	ROW[7]
316	Tap A	ROW[1]	ROW[1]	...	ROW[1]	ROW[1]	ROW[1]	...	ROW[1]
317	Tap A	ROW[3]	ROW[3]	...	ROW[3]	ROW[3]	ROW[3]	...	ROW[3]
318	Tap A	ROW[5]	ROW[5]	...	ROW[5]	ROW[5]	ROW[5]	...	ROW[5]
319	Tap A	ROW[7]	ROW[7]	...	ROW[7]	ROW[7]	ROW[7]	...	ROW[7]

Col No.		Row 0	Row 1	...	Row 200	Row 201	Row 202	...	Row 239
0	Tap B	ROW[0]	ROW[0]	...	ROW[0]	ROW[0]	ROW[0]	...	ROW[0]
1	Tap B	ROW[2]	ROW[2]	...	ROW[2]	ROW[2]	ROW[2]	...	ROW[2]
2	Tap B	ROW[4]	ROW[4]	...	ROW[4]	ROW[4]	ROW[4]	...	ROW[4]
3	Tap B	ROW[6]	ROW[6]	...	ROW[6]	ROW[6]	ROW[6]	...	ROW[6]
316	Tap B	ROW[0]	ROW[0]	...	ROW[0]	ROW[0]	ROW[0]	...	ROW[0]
317	Tap B	ROW[2]	ROW[2]	...	ROW[2]	ROW[2]	ROW[2]	...	ROW[2]
318	Tap B	ROW[4]	ROW[4]	...	ROW[4]	ROW[4]	ROW[4]	...	ROW[4]
319	Tap B	ROW[6]	ROW[6]	...	ROW[6]	ROW[6]	ROW[6]	...	ROW[6]

Figure 14: Raw tap A image with visible test columns.

Figure 15: Raw tap B image with visible test columns.

11. Depth & Confidence Calculation

11.1. Correlation Measurement

A depth and confidence measurement can be realized by a sequence of 4 correlation measurements, followed by a digital processing step. In one implementation, a single correlation measurement is realized by synchronous demodulation of the light signal of the active illumination source: during the integration time T_{int}, the active illumination must be turned on while the TOF pixel responsivity and the light signal are amplitude modulated at a frequency f_{MIX}. Between the illumination source and the TOF pixel modulation signal, a fixed phase delay $\phi \in \{45, 225, 135, 315\}$ degrees should be applied per correlation measurement. After each integration time, the light source should be switched off to cool down for a time $T_{cooldown}$. During this cool down time, there is a time T_{read} to read out the TOF pixel correlation values S_{ϕ}.

Figure 16 shows the sequence of 4 correlation measurements and the synchronization between the pixel and active illumination timings.

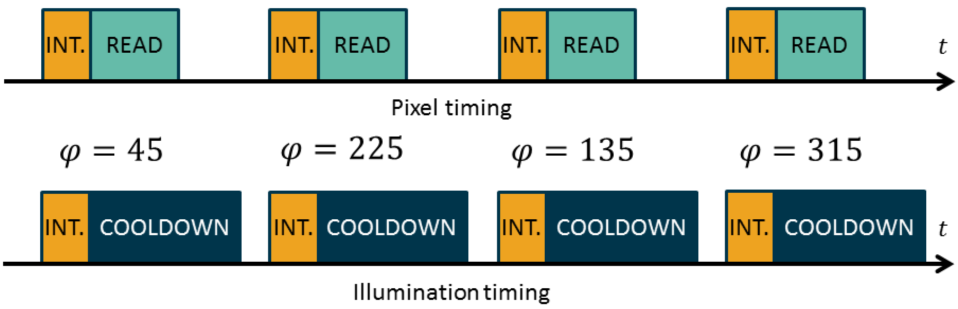

Figure 16: Pixel and illumination timing sequence(s)

The MLX75024 features a two-tap TOF pixel design. One tap measures the in-phase correlation, while the other tap measures the counter phase correlation. Following the described sequence, there will be 8 correlation values available per depth measurement sequence, per pixel: $S_{k,\phi}$ where $k \in \{0,1\}$ denotes the in-phase and counter phase correlation respectively, and $\phi \in \{45, 225, 135, 315\}$.

Two dual-ended outputs deliver the information from the MLX75024. The dual ended output terminal pairs are (OUT0, OUT3, respectively outputting TapA and TapB) and (OUT1, OUT2, respectively outputting TapB and TapA). During readout of the sensor, each dual ended pair will output the voltages of a two-tap pixel.
Each output pair can be assigned to readout one half of the pixel array.
For columns 0 … 7, 16 … 23, … :

$$OUT_0 \rightarrow S_{0,\phi}\ (TapA)$$

$$OUT_3 \rightarrow S_{1,\phi}\ (TapB)$$

For columns 8 … 15, 24 … 33, … :

$$OUT_1 \rightarrow S_{1,\phi}\ (TapB)$$

$$OUT_2 \rightarrow S_{0,\phi}\ (TapA)$$

The MLX75024 also features digital mix input terminals DMIX[0] (pin 35) and DMIX[1] (pin 34). During the integration time T_{int}, the modulation reference signal must be applied differentially to these terminals. During the remainder of the time, the timing requirements as detailed in Section 10.1 should be followed.

11.2. Active Illumination

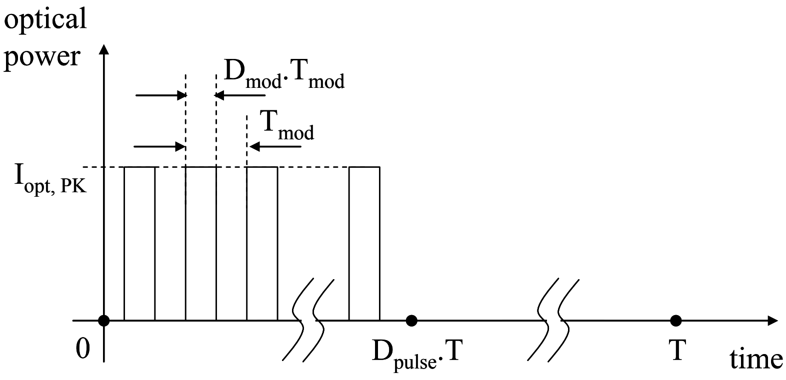

Figure 17: Active illumination waveform

A typical active illumination waveform is shown in Figure 17. The waveform consists of two parts: during the first, a pulse train of active illumination is emitted and during the second, no active light is emitted. During this time, the active light source can cool down and the pixel values can be read out.

The symbols in the graph have the following meaning:

- T is the time between consecutive measurements
- D_{pulse} is the ratio between the time that active pulses should be emitted and the total time of the measurement
- T_{mod} is the duration of each active pulse
- D_{mod} is the ratio between the duration of an active pulse and the time between consecutive pulses
- $I_{opt,PK}$ is the peak optical power or intensity level of the active pulse
- The average optical power or intensity $I_{opt,AVG}$ can be calculated as
- $I_{opt,AVG} = I_{opt,PK} * D_{mod} * D_{pulse}$
- The average duty cycle $D_{mod} * D_{pulse}$ should be chosen such that the active illumination can operate reliably i.e. does not exceed its critical temperature, while aiming for maximum peak power $I_{opt,PK}$ to achieve the best measurement SNR in high ambient light conditions.

Referring to Section 11.1, we note that:

- The integration time T_{int} equals $D_{pulse} * T$
- The cool down time $T_{cooldown}$ equals $\left(1 - D_{pulse}\right) * T$
- The modulation frequency f_{MIX} equals $1/T_{mod}$
- The modulation duty cycle D_{mod} equals 50% in case of square wave or sine modulation

12. Package information

12.1. Mechanical Dimensions

To avoid dust accumulation, scratches or other sources of damage during component storage, logistics or the assembly processes, we offer product variants that include a plastic cover tape to protect the sensitive area of the sensor.
In order to focus the lens over the sensor and capture the light in the most efficient way, it's important to have the sensor's sensitive part at the focal length of the lens. The sensitive area of the pixels is about 550 microns below the glass surface of the sensor. This glass surface is the last surface at the left of the SIDE VIEW on Figure 18 below.

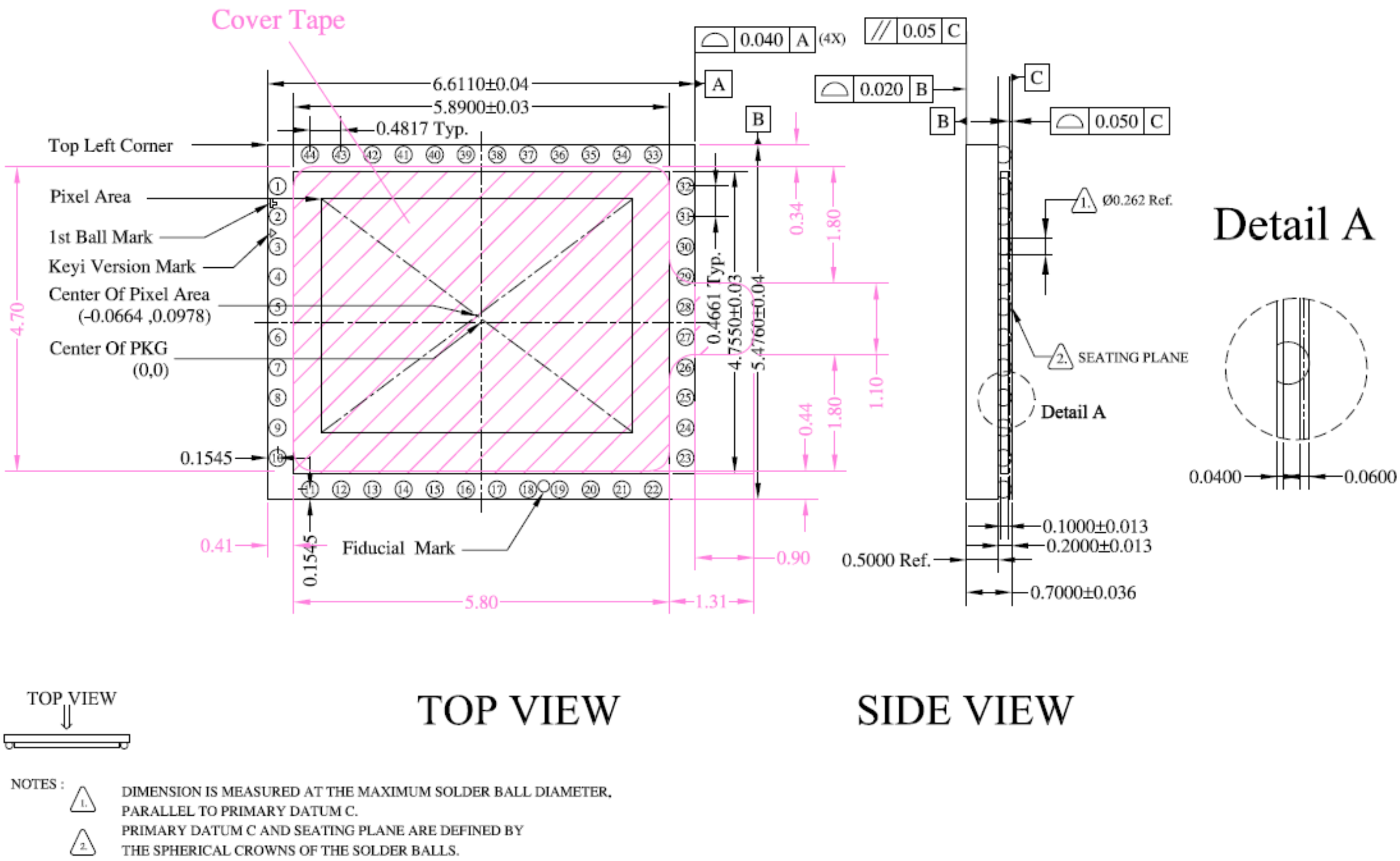

Figure 18: Mechanical dimensions

12.2. Moisture sensitivity level

The GBGA44 package is qualified as automotive grade 2 according to AEC-Q100. It is qualified for MSL1 with soldering temperature 260 degrees Celsius.

12.3. PCB Footprint Recommendations

It's recommended to use NSMD (Non Solder Mask Defined) type of pads on the PCB. In order to prevent the solder balls of the sensor to get in contact with each other after reflow, it's also recommended to shift the solder ball pads 50 um outward from the package position, as illustrated in Figure 19 and Figure 20.

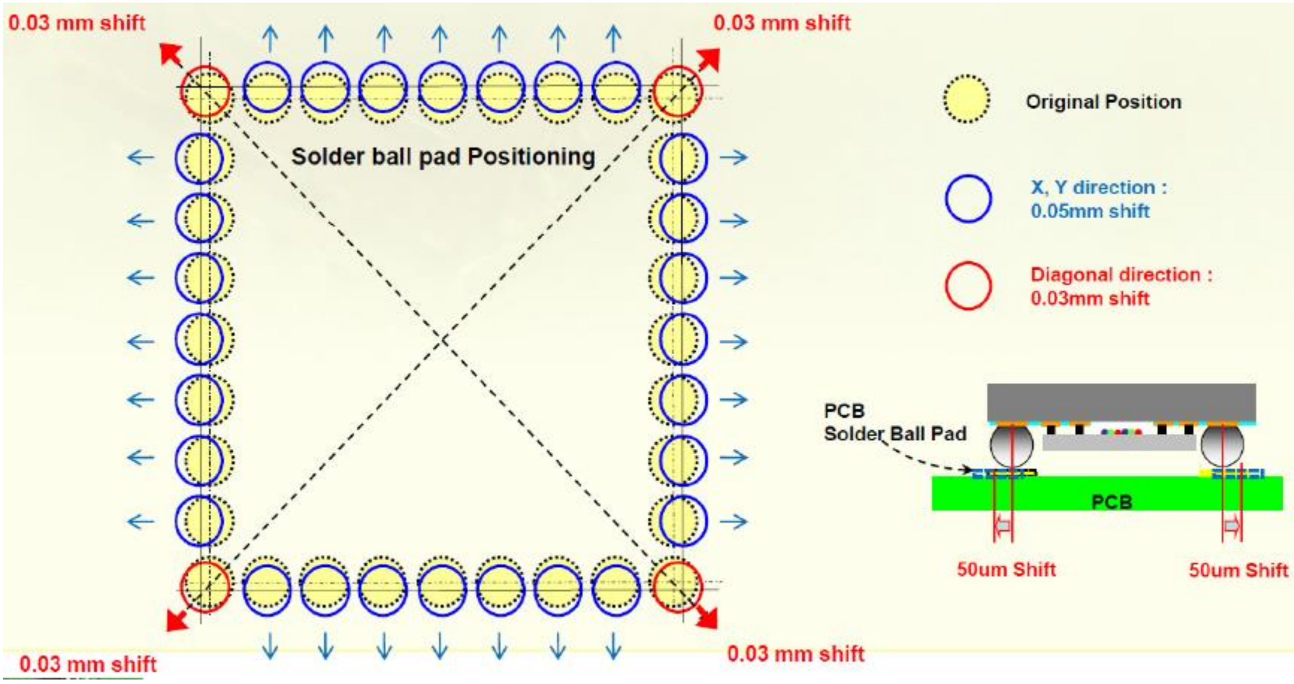

Figure 19: Recommended solder pad shift

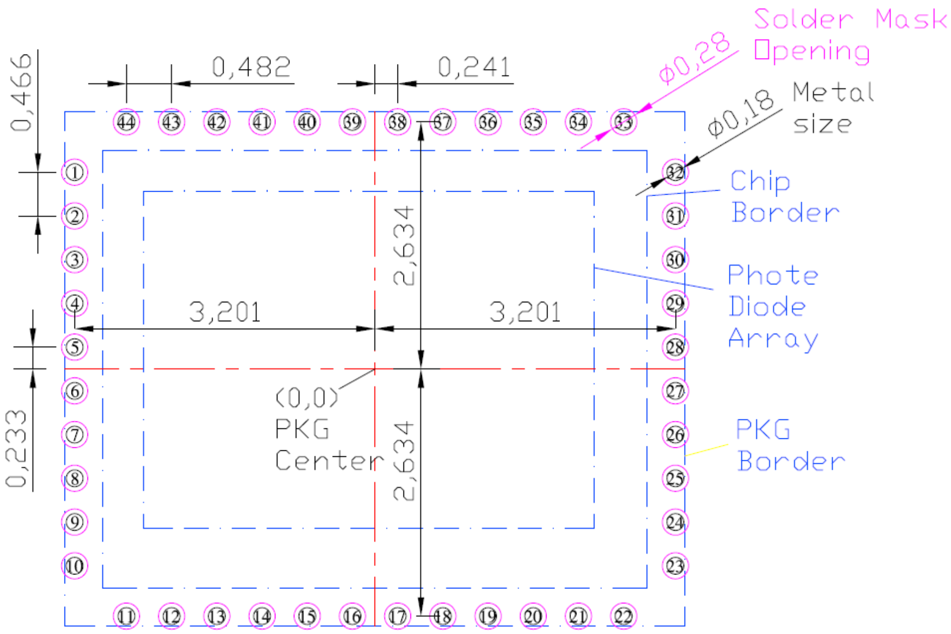

Figure 20: Recommended PCB land pattern (dimensions in mm), Pixel (0,0) is located on the top right corner of the pixel array here, close to pin 31.

12.4. PCB Trace Layout Recommendation

It is recommended to route the traces connected to the solder balls outside of the solder ball perimeter (see Figure 21, left). In case that traces shall be routed inside of the solder ball perimeter, the trace angle shall be greater than 45 deg (see Figure 21, right).

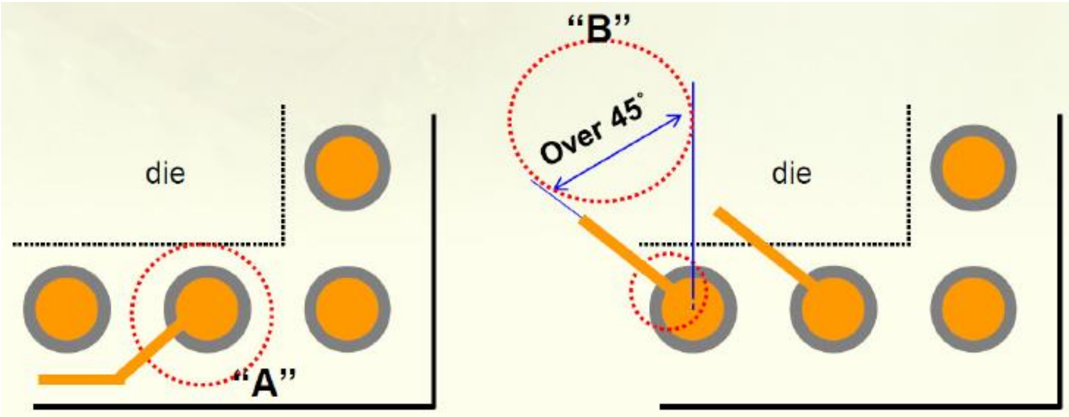

Figure 21: Recommended trace layout

12.5. Sensor Reflow Profile

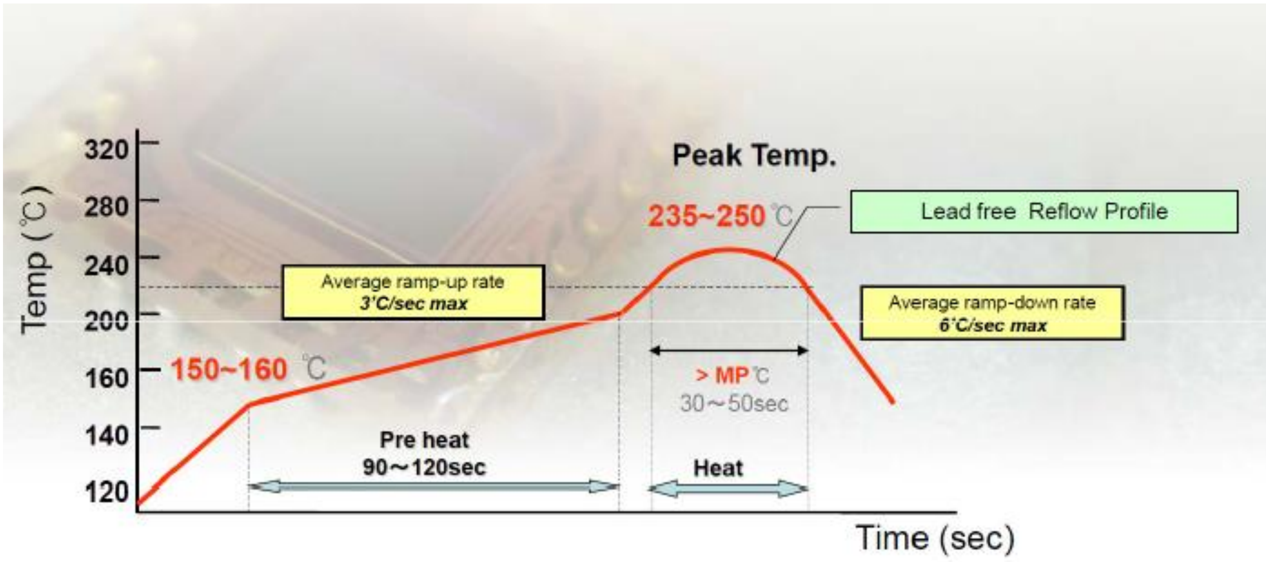

Figure 22: Recommended reflow profile

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