Femtoampere Input Bias Current Electrometer Amplifier

Data Sheet

ADA4530-1

FEATURES

- Low input bias current
  - ±20 fA maximum at T_A = 25°C (guaranteed at production test)
  - ± 20 fA maximum at −40°C < T_A < +85°C
  - ± 250 fA maximum at −40°C < T_A < +125°C (guaranteed at production test)
- Low offset voltage: 50 µV maximum over specified CMRR range
- Offset drift: 0.13 µV/°C typical, 0.5 µV/°C maximum
- Integrated guard buffer with 100 µV maximum offset
- Low voltage noise density: 14 nV/√Hz at 10 kHz
- Wide bandwidth: 2 MHz unity-gain crossover
- Supply voltage: 4.5 V to 16 V (±2.25 V to ±8 V)
- Operating temperature: −40°C to +125°C

APPLICATIONS

- Laboratory and analytical instrumentation: spectrophotometers, chromatographs, mass spectrometers, and potentiostatic and amperostatic coulometry
- Instrumentation: picoammeters and coulombmeters
- Transimpedance amplifier (TIA) for photodiodes, ion chambers, and working electrode measurements
- High impedance buffering for chemical sensors and capacitive sensors

PIN CONNECTION DIAGRAM

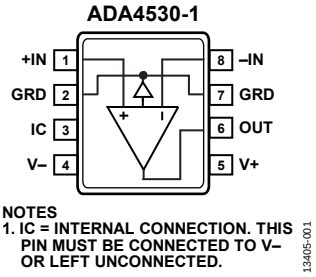

Figure 1.

GENERAL DESCRIPTION

The ADA4530-1 is a femtoampere (10^{-15} A) level input bias current operational amplifier suitable for use as an electrometer that also includes an integrated guard buffer. It has an operating voltage range of 4.5 V to 16 V enabling it to operate in conventional 5 V and 10 V single supply systems as well as ±2.5 V and ±5 V dual supply systems.

It provides ultralow input bias currents that are production tested at temperature to ensure the device meets its performance goals in user systems. The integrated guard buffer is provided to isolate the input pins from leakage in the printed circuit board (PCB), minimize board component count, and enable ease of system design. The ADA4530-1 is available in an industry-standard surface-mount 8-lead SOIC package with a unique pinout optimized to prevent signals from coupling between the sensitive input pins, the power supplies, and the output pin while enabling easy routing of the guard ring traces.

The ADA4530-1 also offers low offset voltage, low offset drift, and low voltage and current noise needed for the types of applications that require such low leakages. To maximize the dynamic range of the system, the ADA4530-1 has a rail-to-rail output stage that can typically drive to within 30 mV of the supply rails under a 10 kΩ load.

The ADA4530-1 operates over the −40°C to +125°C industrial temperature range and is available in an 8-lead SOIC package.

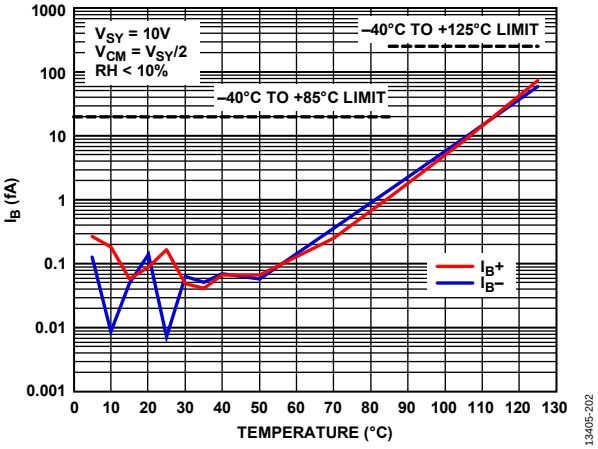

Figure 2. Input Bias Current (I_B) vs. Temperature, V_{SY} = 10 V

Rev. A
Document Feedback

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
Pin Connection Diagram ... 1
General Description ... 1
Revision History ... 2
Specifications ... 3
5 V Nominal Electrical Characteristics ... 3
10 V Nominal Electrical Characteristics ... 5
15 V Nominal Electrical Characteristics ... 7
Absolute Maximum Ratings ... 9
Thermal Resistance ... 9
ESD Caution ... 9
Pin Configuration and Function Descriptions ... 10
Typical Performance Characteristics ... 11
Main Amplifier, DC Performance ... 11
Main Amplifier, AC Performance ... 20
Guard Amplifier ... 26
Theory of Operation ... 28
ESD Structure ... 28
Input Stage ... 28
Gain Stage ... 29
Output Stage ... 29
Guard Buffer ... 29
Applications Information ... 30
Input Protection ... 30
Single-Supply and Rail-to-Rail Output ... 30
Capacitive Load Stability ... 30
EMI Rejection Ratio ... 31
High Impedance Measurements ... 32
Input Bias Current ... 32
Input Resistance ... 33
Input Offset Voltage ... 33
Insulation Resistance ... 33
Guarding ... 34
Dielectric Relaxation ... 34
Humidity Effects ... 36
Contamination ... 37
Cleaning and Handling ... 38
Solder Paste Selection ... 38
Current Noise Considerations ... 39
Layout Guidelines ... 42
Physical Implementation of Guarding Techniques ... 42
Guard Ring ... 42
Guard Plane ... 42
Via Fence ... 43
Cables and Connectors ... 43
Electrostatic Interferance ... 43
Photodiode Interface ... 44
DC Error Analysis ... 44
AC Error Analysis ... 44
Noise Analysis ... 45
Design Recommendations ... 46
Design Example ... 46
Power Supply Recommendations ... 49
Power Supply Considerations ... 49
Outline Dimensions ... 50
Ordering Guide ... 50

REVISION HISTORY

3/16—Rev. 0 to Rev. A

Changed DNC Pin to IC Pin ... Throughout
Changes to Figure 1 ... 1
Changes to Figure 3 and Table 6 ... 10
Changes to Figure 29 ... 15
Changes to Theory of Operation Section ... 28
Changes to Humidity Effects Section and Figure 112 ... 36
Added Power Supply Recommendations Section, Power Supply Considerations Section, Table 16, and Figure 133 to Figure 135 ... 49

10/15—Revision 0: Initial Version

SPECIFICATIONS

5 V NOMINAL ELECTRICAL CHARACTERISTICS

V_{SY} = 4.5 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise specified. Typical specifications are equal to the average of the distribution from characterization, unless otherwise noted. Minimum and maximum specifications are tested in production, unless otherwise noted.

Table 1.

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Bias Current[2, 3]	I_B	RH < 50%		<1	±20	fA
		−40°C < T_A < +85°C, RH < 50%			±20	fA
		−40°C < T_A < +125°C, RH < 50%			±250	fA
Input Offset Current[3]	I_{OS}	RH < 50%		<1	±20	fA
		−40°C < T_A < +125°C, RH < 50%			±150	fA
Offset Voltage[2, 4]	V_{OS}			+8	±40	µV
		V_{CM} = 1.5 V to 3 V		+9	±50	µV
		V_{CM} = 1.5 V to 3 V, 0°C < T_A < 125°C			±70	µV
		V_{CM} = 1.5 V to 3 V, −40°C < T_A < 0°C			±150	µV
		V_{CM} = 0 V to 3 V			±300	µV
Offset Voltage Drift[2, 4]	$\Delta V_{OS}/\Delta T$	0°C < T_A < 125°C		+0.13	±0.5	µV/°C
		−40°C < T_A < 0°C		−0.7	±2.8	µV/°C
Input Voltage Range	IVR		0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 1.5 V to 3 V	92	114		dB
		−40°C < T_A < +125°C	90			dB
		V_{CM} = 0 V to 3 V	73			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ to V_{CM}, V_{OUT} = 0.2 V to 4.3 V	120	143		dB
		−40°C < T_A < +125°C	120			dB
Input Resistance	R_{IN}	−40°C < T_A < +125°C		>100		TΩ
Input Capacitance	C_{IN}			8		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	4.47	4.49		V
		−40°C < T_A < +125°C	4.46			V
		R_L = 2 kΩ to V_{CM}	4.4	4.45		V
		−40°C < T_A < +125°C	4.38			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		10	30	mV
		−40°C < T_A < +125°C			40	mV
		R_L = 2 kΩ to V_{CM}		30	100	mV
		−40°C < T_A < +125°C			120	mV
Short-Circuit Current	I_{SC}					
Source				15		mA
Sink				−30		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		20		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 4.5 V to 16 V	130	150		dB
		−40°C < T_A < +125°C	130			dB
Supply Current	I_{SY}	I_{OUT} = 0 mA		0.9	1.3	mA
		−40°C < T_A < +125°C			1.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 10 pF, A_V = 1		1.4		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_V = 100		2		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		2		MHz
−3 dB Closed-Loop Bandwidth	f_{-3dB}	V_{IN}=10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		6		MHz

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Phase Margin	Φ_M	V_{IN} = 10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		62		Degrees
Settling Time to 0.1%	t_S	V_{IN} = 0.5 V step, R_L = 10 kΩ, C_L= 10 pF, A_V = −1		5		µs
EMI Rejection Ratio of +IN	EMIRR	V_{IN} = 100 mV peak, f = 400 MHz		50		dB
		V_{IN} = 100 mV peak, f = 900 MHz		60		dB
		V_{IN} = 100 mV peak, f = 1800 MHz		80		dB
		V_{IN} = 100 mV peak, f = 2400 MHz		90		dB
NOISE PERFORMANCE						
Peak-to-Peak Voltage Noise	e_N p-p	f = 0.1 Hz to 10 Hz		4		µV p-p
Voltage Noise Density	e_N	f = 10 Hz		80		nV/√Hz
		f = 1 kHz		16		nV/√Hz
		f = 10 kHz		14		nV/√Hz
Current Noise Density	I_N	f = 0.1 Hz		0.07		fA/√Hz
Total Harmonic Distortion + Noise	THD + N	A_V = 1, f = 1 kHz, V_{IN} = 0.5 V rms				
Bandwidth = 90 kHz				0.003		%
Bandwidth = 500 kHz				0.0045		%
GUARD BUFFER						
Guard Offset Voltage[2, 4, 5]	V_{GOS}	V_{CM} = 1.5 V to 3 V		15	100	µV
		V_{CM} = 1.5 V to 3 V, 0°C < T_A < 125°C			120	µV
		V_{CM} = 1.5 V to 3 V, −40°C < T_A < 0°C			250	µV
		V_{CM} = 0.1 V to 3 V			150	µV
Guard Offset Voltage Drift[2, 4]	$\Delta V_{GOS}/\Delta T$	0°C < T_A < +125°C		0.18	1	µV/°C
		−40°C < T_A < 0°C		1.4	7	µV/°C
Output Impedance	Z_{GOUT}			1		kΩ
Output Voltage Range		V_{GOS} < 150 µV	0.1		3	V
−3 dB Bandwidth	$f_{-3dBGUARD}$	V_{IN} = 10 mV rms, C_L = 10 pF		5.5		MHz

[1] These specifications represent the performance for 5 V ± 10% power supplies. All specifications are measured at the worst case 4.5 V supply voltage.
[2] The maximum specifications at −40°C < T_A < +85°C and −40°C < T_A < 0°C are guaranteed from characterization.
[3] RH is relative humidity (see the Humidity Effects section for more information).
[4] The typical specifications are equal to the average plus the standard deviation of the distribution from characterization.
[5] The guard offset voltage is the voltage difference between the guard output and the noninverting input.

10 V NOMINAL ELECTRICAL CHARACTERISTICS

V_{SY} = 10 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise noted. Typical specifications are equal to the average of the distribution from characterization, unless otherwise noted. Minimum and maximum specifications are tested in production, unless otherwise noted.

Table 2.

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Bias Current[2, 3]	I_B	RH < 50%		<1	±20	fA
		−40°C < T_A < +85°C, RH < 50%			±20	fA
		−40°C < T_A < +125°C, RH < 50%			±250	fA
Input Offset Current[3]	I_{OS}	RH < 50%		<1	±20	fA
		−40°C < T_A < +125°C, RH < 50%			±150	fA
Offset Voltage[2, 4]	V_{OS}			+8	±40	µV
		V_{CM} = 1.5 V to 8.5 V		+9	±50	µV
		V_{CM} = 1.5 V to 8.5 V, 0°C < T_A < 125°C			±70	µV
		V_{CM} = 1.5 V to 8.5 V, −40°C < T_A < 0°C			±150	µV
		V_{CM} = 0 V to 8.5 V			±300	µV
Offset Voltage Drift[2, 4]	$\Delta V_{OS}/\Delta T$	0°C < T_A < 125°C		+0.13	±0.5	µV/°C
		−40°C < T_A < 0°C		−0.7	±2.8	µV/°C
Input Voltage Range	IVR		0		8.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 1.5 V to 8.5 V	105	114		dB
		−40°C < T_A < +125°C	100			dB
		V_{CM} = 0 V to 8.5 V	87			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ to V_{CM}, V_{OUT} = 0.5 V to 9.5 V	125	150		dB
		−40°C < T_A < +125°C	125			dB
Input Resistance	R_{IN}	−40°C < T_A < +125°C		>100		TΩ
Input Capacitance	C_{IN}			8		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	9.96	9.97		V
		−40°C < T_A < +125°C	9.94			V
		R_L = 2 kΩ to V_{CM}	9.93	9.87		V
		−40°C < T_A < +125°C	9.75			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		15	40	mV
		−40°C < T_A < +125°C			60	mV
		R_L = 2 kΩ to V_{CM}		70	170	mV
		−40°C < T_A < +125°C			250	mV
Short-Circuit Current	I_{SC}					
Source				15		mA
Sink				−30		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		20		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 4.5 V to 16 V	130	150		dB
		−40°C < T_A < +125°C	130			dB
Supply Current	I_{SY}	I_{OUT} = 0 mA		0.9	1.3	mA
		−40°C < T_A < +125°C			1.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 10 pF, A_V = 1		1.4		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_V = 100		2		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		2		MHz
−3 dB Closed-Loop Bandwidth	f_{-3dB}	V_{IN} = 10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		6		MHz
Phase Margin	Φ_M	V_{IN} = 10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		62		Degrees

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Settling Time to 0.1%	t_S	V_{IN} = 1 V step, R_L = 10 kΩ, C_L = 10 pF, A_V = −1		6		µs
EMI Rejection Ratio of +IN	EMIRR	V_{IN} = 100 mV peak, f = 400 MHz		50		dB
		V_{IN} = 100 mV peak, f = 900 MHz		60		dB
		V_{IN} = 100 mV peak, f = 1800 MHz		80		dB
		V_{IN} = 100 mV peak, f = 2400 MHz		90		dB
NOISE PERFORMANCE						
Peak-to-Peak Voltage Noise	e_N p-p	f = 0.1 Hz to 10 Hz		4		µV p-p
Voltage Noise Density	e_N	f = 10 Hz		80		nV/√Hz
		f = 1 kHz		16		nV/√Hz
		f = 10 kHz		14		nV/√Hz
Current Noise Density	I_N	f = 0.1 Hz		0.07		fA/√Hz
Total Harmonic Distortion + Noise	THD + N	A_V = 1, f = 1 kHz, V_{IN} = 2 V rms				
Bandwidth = 90 kHz				0.0015		%
Bandwidth = 500 kHz				0.0025		%
GUARD BUFFER						
Guard Offset Voltage[2, 4, 5]	V_{GOS}	V_{CM} = 1.5 V to 8.5 V		15	100	µV
		V_{CM} = 1.5 V to 8.5 V, 0°C < T_A < 125°C			120	µV
		V_{CM} = 1.5 V to 8.5 V, −40°C < T_A < 0°C			250	µV
		V_{CM} = 0.1 V to 8.5 V			150	µV
Guard Offset Voltage Drift[2, 4]	$\Delta V_{GOS}/\Delta T$	0°C < T_A < 125°C		0.18	1	µV/°C
		−40°C < T_A < 0°C		1.4	7	µV/°C
Output Impedance	Z_{GOUT}			1		kΩ
Output Voltage Range		V_{GOS} < 150 µV	0.1		8.5	V
−3 dB Bandwidth	$f_{-3dBGUARD}$	V_{IN} = 10 mV rms, C_L = 10 pF		5.5		MHz

[1] These specifications represent the performance for 10 V ± 10% power supplies. All specifications are measured at the 10 V supply voltage.
[2] The maximum specifications at −40°C < T_A < +85°C and −40°C < T_A < 0°C are guaranteed from characterization.
[3] RH is relative humidity (see the Humidity Effects section for more information).
[4] These typical specifications are equal to the average plus the standard deviation of the distribution from characterization.
[5] The guard offset voltage is the voltage difference between the guard output and the noninverting input.

15 V NOMINAL ELECTRICAL CHARACTERISTICS

V_{SY} = 16 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise noted. Typical specifications are equal to the average of the distribution from characterization, unless otherwise noted. Minimum and maximum specifications are tested in production, unless otherwise noted.

Table 3.

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Input Bias Current[2, 3]	I_B	RH < 50%		<1	±20	fA
		−40°C < T_A < +85°C, RH < 50%			±20	fA
		−40°C < T_A < +125°C, RH < 50%			±250	fA
Input Offset Current	I_{OS}	RH < 50%		<1	±20	fA
		−40°C < T_A < +125°C, RH < 50%			±150	fA
Offset Voltage[2, 4]	V_{OS}			+8	±40	µV
		V_{CM} = 1.5 V to 14.5 V		+9	±50	µV
		V_{CM} = 1.5 V to 14.5 V, 0°C < T_A < 125°C			±70	µV
		V_{CM} = 1.5 V to 14.5 V, −40°C < T_A < 0°C			±150	µV
		V_{CM} = 0 V to 14.5 V			±300	µV
Offset Voltage Drift[2, 4]	$\Delta V_{OS}/\Delta T$	0°C < T_A < 125°C		+0.13	±0.5	µV/°C
		−40°C < T_A < 0°C		−0.7	±2.8	µV/°C
Input Voltage Range	IVR		0		14.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 1.5 V to 14.5 V	110	114		dB
		−40°C < T_A < +125°C	105			dB
		V_{CM} = 0 V to 14.5 V	93			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ to V_{CM}, V_{OUT} = 0.5 V to 15.5 V	130	155		dB
		−40°C < T_A < +125°C	125			dB
Input Resistance	R_{IN}	−40°C < T_A < +125°C		>100		TΩ
Input Capacitance	C_{IN}			8		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	15.93	15.95		V
		−40°C < T_A < +125°C	15.9			V
		R_L = 2 kΩ to V_{CM}	15.72	15.78		V
		−40°C < T_A < +125°C	15.58			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		25	70	mV
		−40°C < T_A < +125°C			100	mV
		R_L = 2 kΩ to V_{CM}		115	280	mV
		−40°C < T_A < +125°C			420	mV
Short-Circuit Current	I_{SC}					
Source				15		mA
Sink				−30		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		20		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 4.5 V to 16 V	130	150		dB
		−40°C < T_A < +125°C	130			dB
Supply Current	I_{SY}	I_{OUT} = 0 mA		0.9	1.3	mA
		−40°C < T_A < +125°C			1.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 10 pF, A_V = 1		1.4		V/µs
Gain bandwidth Product	GBP	V_{IN} = 10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_V = 100		2		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		2		MHz
−3 dB Closed-Loop Bandwidth	$f_{-3\ dB}$	V_{IN} = 10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_V = 1		6		MHz
Phase Margin	Φ_M	V_{IN} =10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1		62		Degrees

Parameter[1]	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Settling Time to 0.1%	t_S	V_{IN} = 1 V step, R_L = 10 kΩ, C_L = 10 pF, A_V = −1		6		µs
EMI Rejection Ratio of +IN	EMIRR	V_{IN} = 100 mV peak, f = 400 MHz		50		dB
		V_{IN} = 100 mV peak, f = 900 MHz		60		dB
		V_{IN} = 100 mV peak, f = 1800 MHz		80		dB
		V_{IN} = 100 mV peak, f = 2400 MHz		90		dB
NOISE PERFORMANCE						
Peak-to-Peak Voltage Noise	e_N p-p	f = 0.1 Hz to 10 Hz		4		µV p-p
Voltage Noise Density	e_N	f = 10 Hz		80		nV/√Hz
	e_N	f = 1 kHz		16		nV/√Hz
	e_N	f = 10 kHz		14		nV/√Hz
Current Noise Density	I_N	f = 0.1 Hz		0.07		fA/√Hz
Total Harmonic Distortion + Noise	THD + N	A_V = 1, f = 1 kHz, V_{IN} = 4.5 V rms				
Bandwidth = 90 kHz				0.0012		%
Bandwidth = 500 kHz				0.003		%
GUARD BUFFER						
Guard Offset Voltage[4, 5]	V_{GOS}	V_{CM} = 1.5 V to 14.5 V		15	100	µV
		V_{CM} = 1.5 V to 14.5 V, 0°C < T_A < 125°C			120	µV
		V_{CM} = 1.5 V to 14.5 V, −40°C < T_A < 0°C			250	µV
		V_{CM} = 0.1 V to 14.5 V			150	µV
Guard Offset Voltage Drift[2, 4]	$\Delta V_{GOS}/\Delta T$	0°C < T_A < +125°C		0.18	1	µV/°C
		−40°C < T_A < 0°C		1.4	7	µV/°C
Output Impedance	Z_{GOUT}			1		kΩ
Output Voltage Range		V_{GOS} < 150 µV	0.1		14.5	V
−3 dB Bandwidth	$f_{-3\ dB\ GUARD}$	V_{IN} = 10 mV rms, C_L = 10 pF		5.5		MHz

[1] These specifications represent the performance for 15 V ± 1 V power supplies. All specifications are measured at the worst case 16 V supply voltage.
[2] The maximum specifications at −40°C < T_A < +85°C and −40°C < T_A < 0°C are guaranteed from characterization.
[3] RH is relative humidity (see the Humidity Effects section for more information).
[4] These typical specifications are equal to the average plus the standard deviation of the distribution from characterization.
[5] The guard offset voltage is the voltage difference between the guard output and the noninverting input.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	17 V
Input Voltage	(V−) − 0.3 V to (V+) + 0.3 V
Input Current[1]	10 mA
Differential Input Voltage	±0.7 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
ESD	
Human Body Model[2]	4 kV
Field Induced Charged Device Model (FICDM)[3]	1.25 kV

[1] The input pins have clamp diodes to the power supply pins. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.
[2] Applicable Standard ESDA/JEDEC JS-001-2012.
[3] Applicable Standard JESD22-C101-E (ESD FICDM standard of JEDEC).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages using a standard 4-layer JEDEC board.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	122	41	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

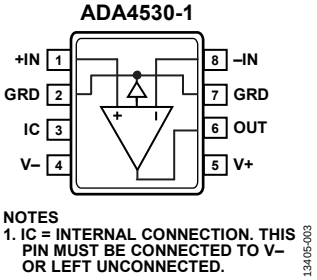


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	+IN	Noninverting Input.
2	GRD	Guard.
3	IC	Internal Connection. This pin must be connected to V– or left unconnected.
4	V–	Negative Supply Voltage.
5	V+	Positive Supply Voltage.
6	OUT	Output.
7	GRD	Guard.
8	–IN	Inverting Input.

TYPICAL PERFORMANCE CHARACTERISTICS

MAIN AMPLIFIER, DC PERFORMANCE

T_A = 25°C, unless otherwise noted.

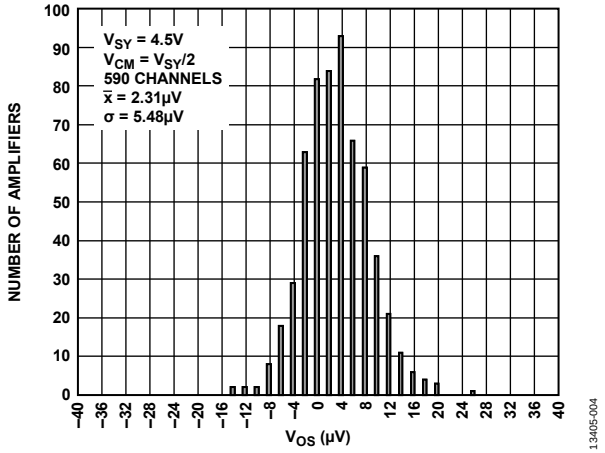


Figure 4. Input Offset Voltage Distribution, V_{SY} = 4.5 V

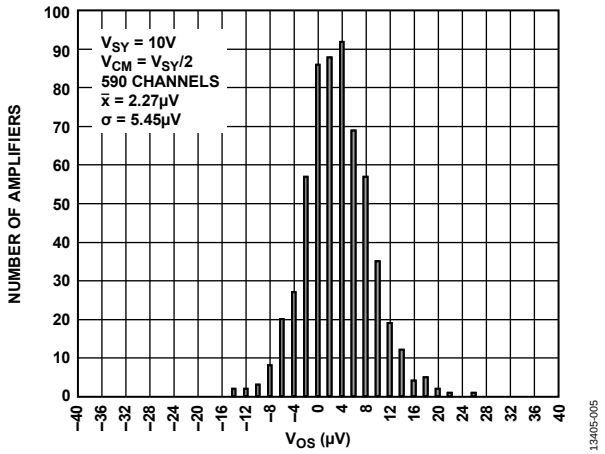


Figure 5. Input Offset Voltage Distribution, V_{SY} = 10 V

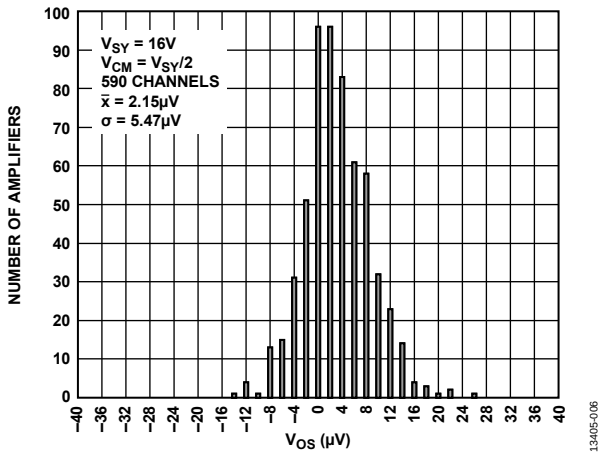


Figure 6. Input Offset Voltage Distribution, V_{SY} = 16 V

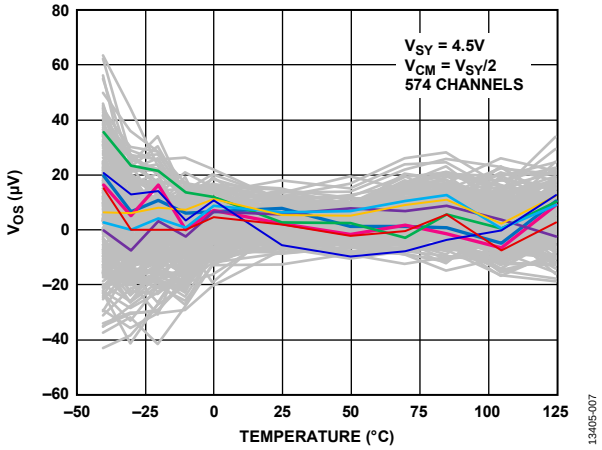


Figure 7. Input Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = 4.5 V

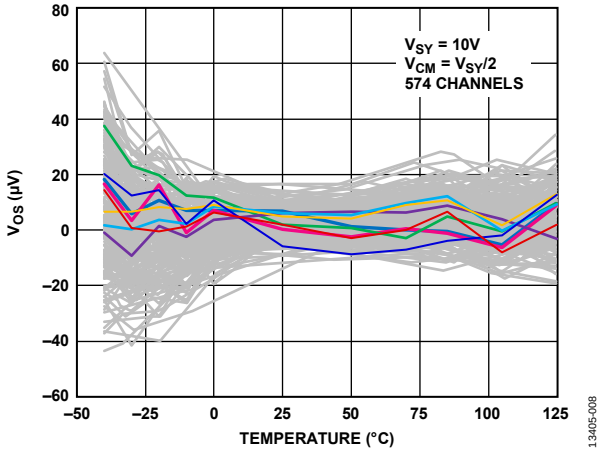


Figure 8. Input Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = 10 V

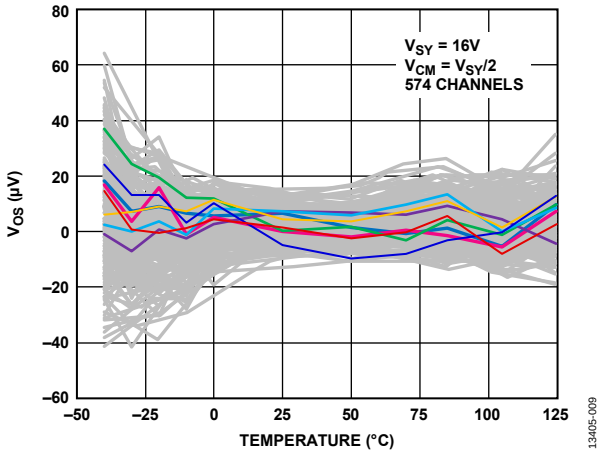


Figure 9. Input Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = 16 V

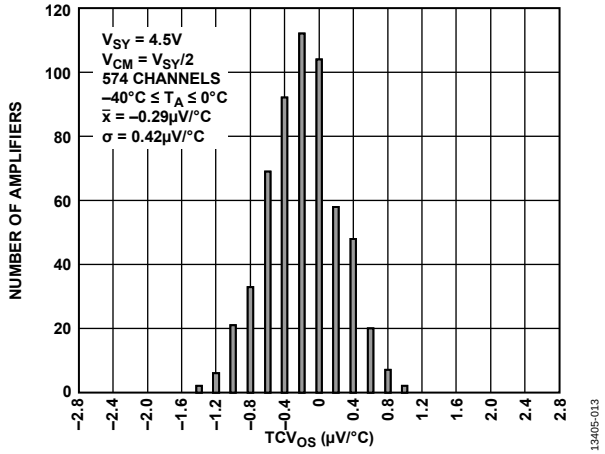


Figure 10. Input Offset Voltage Drift Distribution, −40°C ≤ T_A ≤ 0°C, V_{SY} = 4.5 V

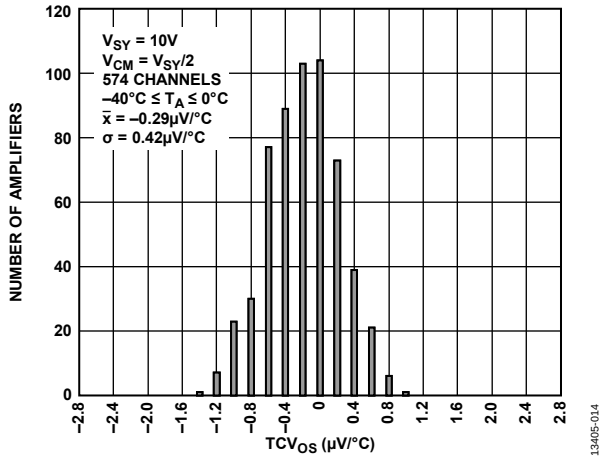


Figure 11. Input Offset Voltage Drift Distribution, −40°C ≤ T_A ≤ 0°C, V_{SY} = 10 V

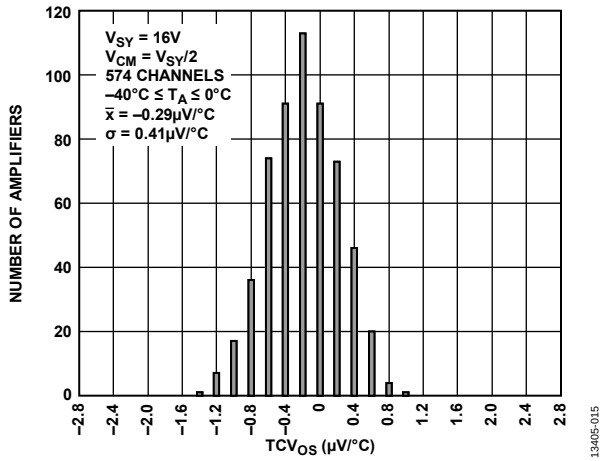


Figure 12. Input Offset Voltage Drift Distribution, −40°C ≤ T_A ≤ 0°C, V_{SY} = 16 V

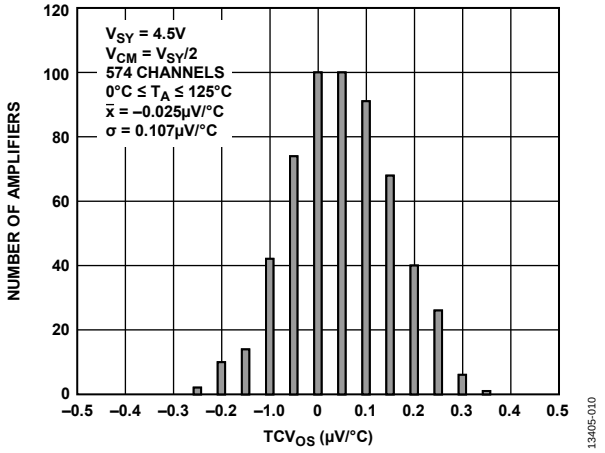


Figure 13. Input Offset Voltage Drift Distribution, 0°C ≤ T_A ≤ 125°C, V_{SY} = 4.5 V

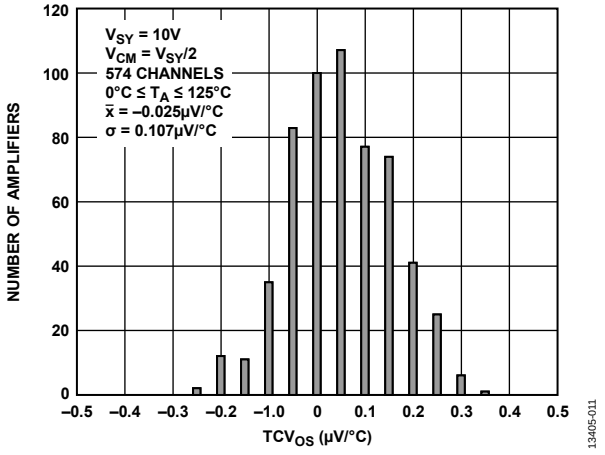


Figure 14. Input Offset Voltage Drift Distribution, 0°C ≤ T_A ≤ 125°C, V_{SY} = 10 V

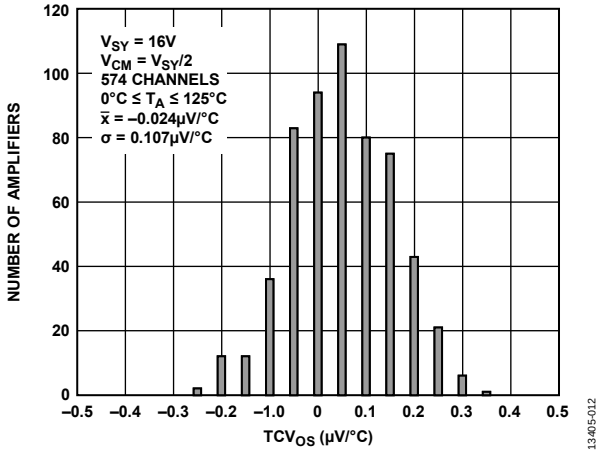


Figure 15. Input Offset Voltage Drift Distribution, 0°C ≤ T_A ≤ 125°C, V_{SY} = 16 V

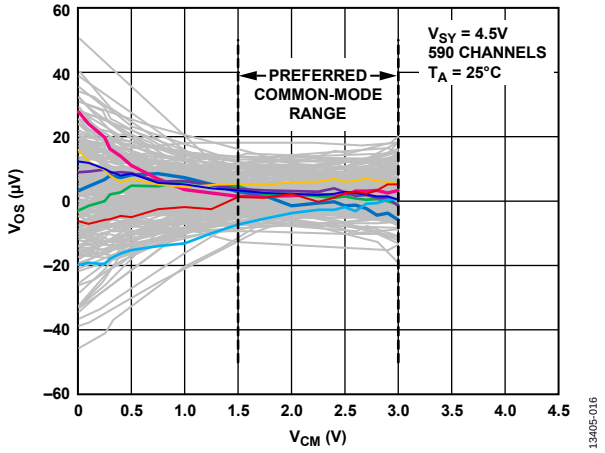


Figure 16. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 4.5 V

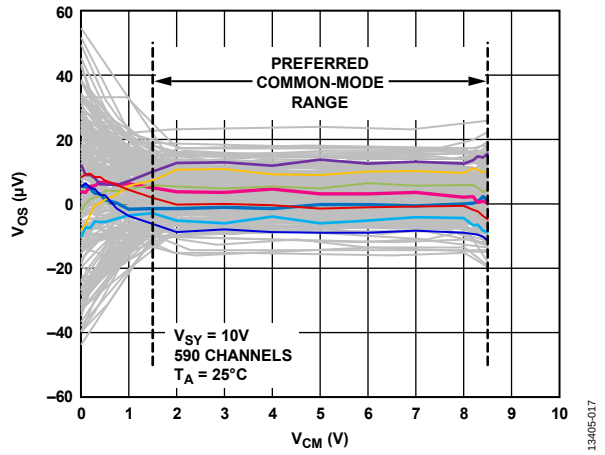


Figure 17. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 10 V

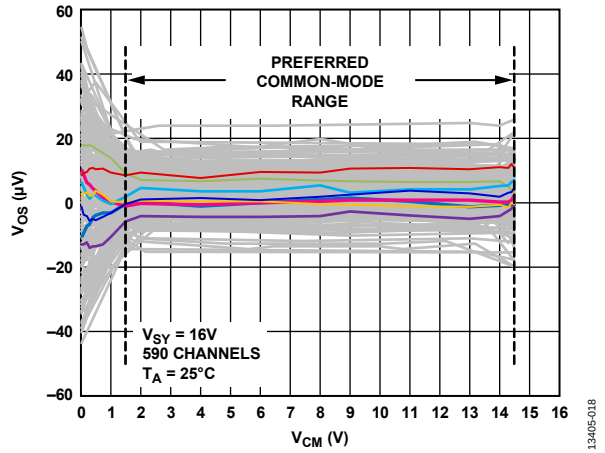


Figure 18. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 16 V

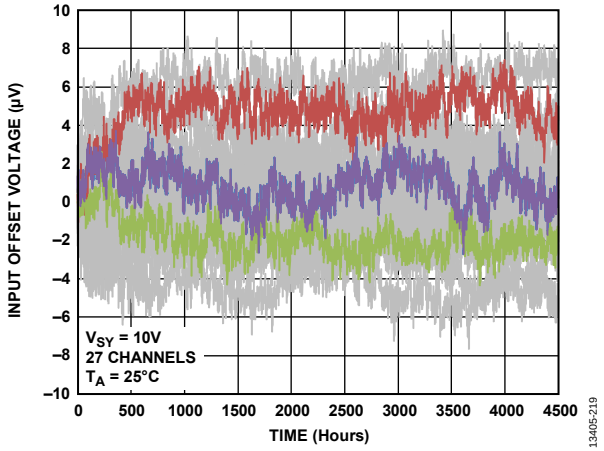


Figure 19. V_{OS} Long-Term Drift

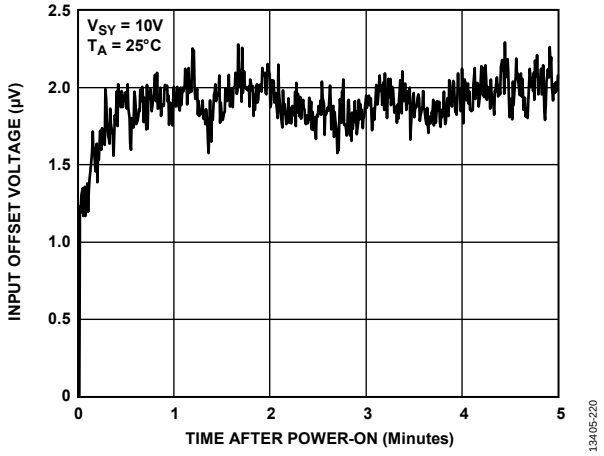


Figure 20. V_{OS} Warm-Up Time

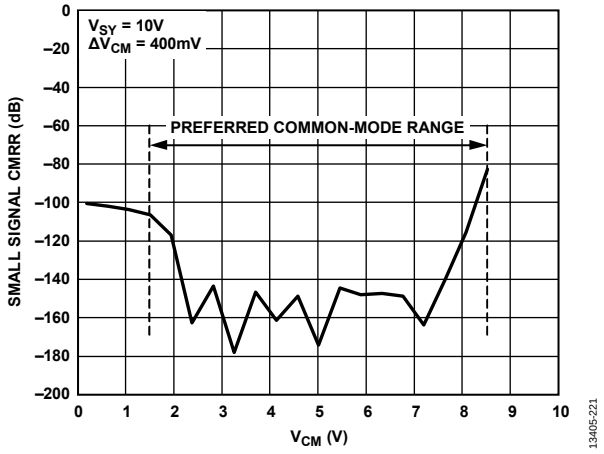


Figure 21. Small Signal CMRR vs. Common-Mode Voltage

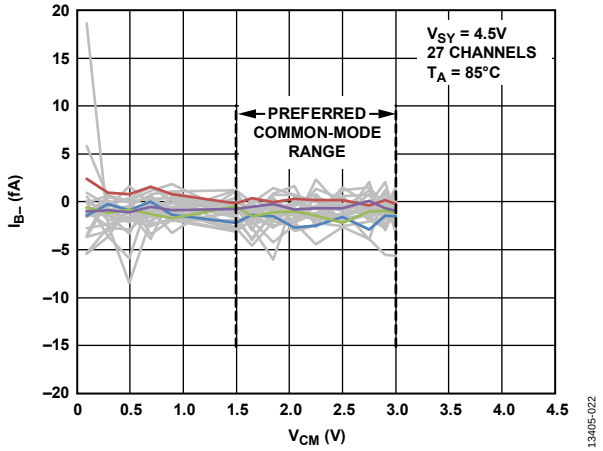


Figure 22. Inverting Input Bias Current (I_{B-}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 4.5 V, T_A = 85°C

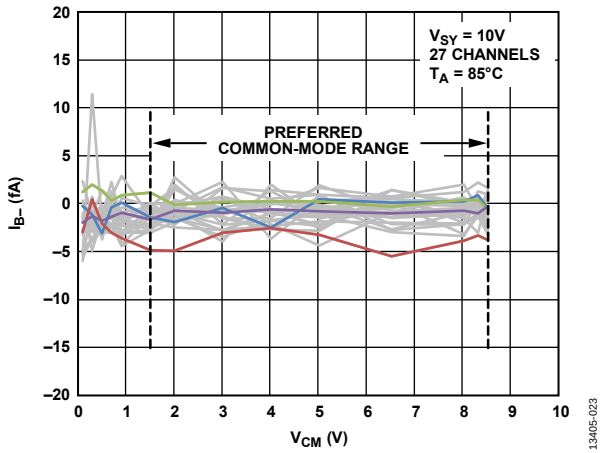


Figure 23. Inverting Input Bias Current (I_{B-}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 10 V, T_A = 85°C

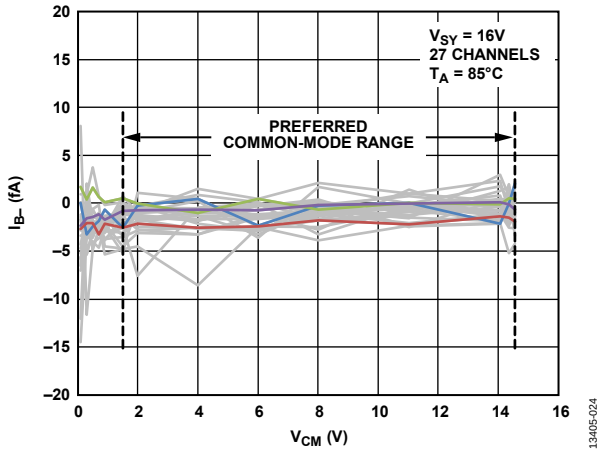


Figure 24. Inverting Input Bias Current (I_{B-}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 16 V, T_A = 85°C

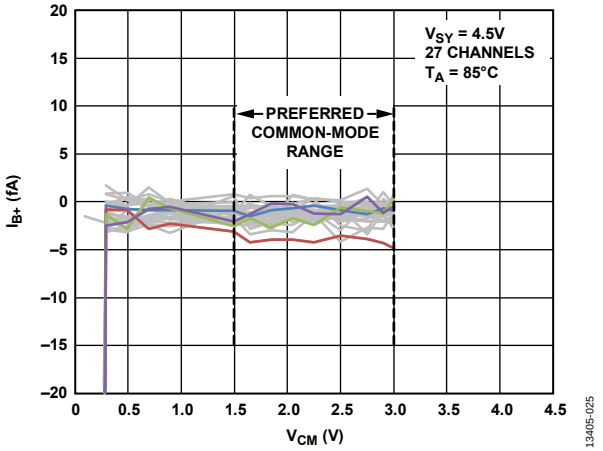


Figure 25. Noninverting Input Bias Current (I_{B+}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 4.5 V, T_A = 85°C

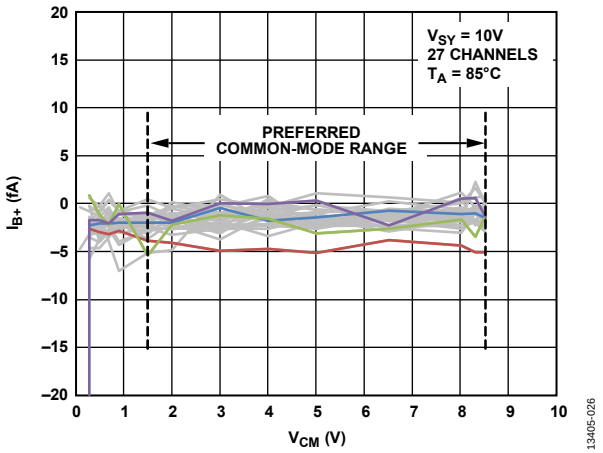


Figure 26. Noninverting Input Bias Current (I_{B+}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 10 V, T_A = 85°C

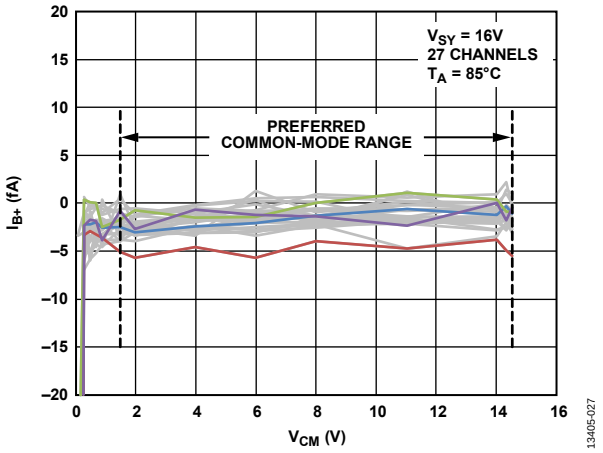


Figure 27. Noninverting Input Bias Current (I_{B+}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 16 V, T_A = 85°C

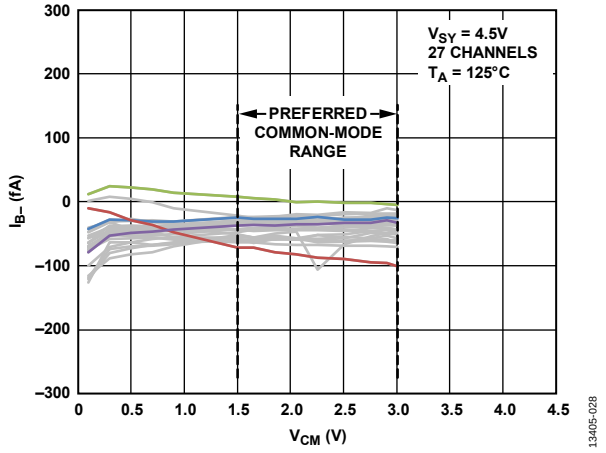


Figure 28. Inverting Input Bias Current (I_{B-}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 4.5 V, T_A = 125°C

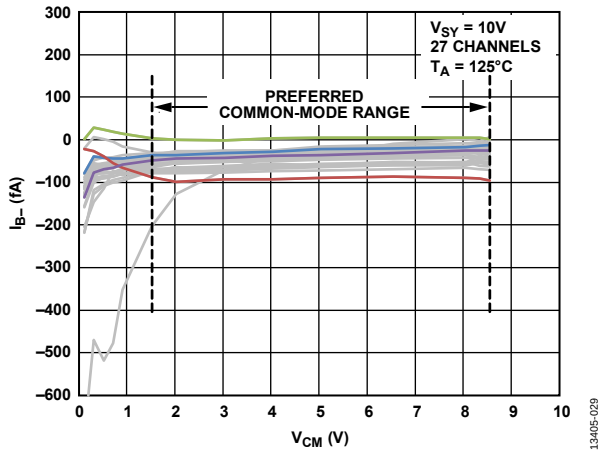


Figure 29. Inverting Input Bias Current (I_{B-}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 10 V, T_A = 125°C

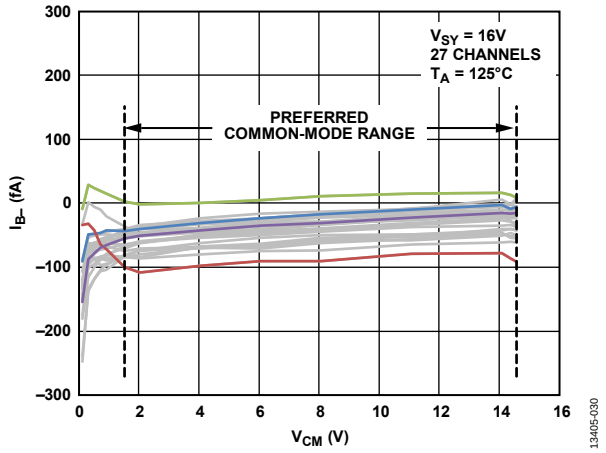


Figure 30. Inverting Input Bias Current (I_{B-}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 16 V, T_A = 125°C

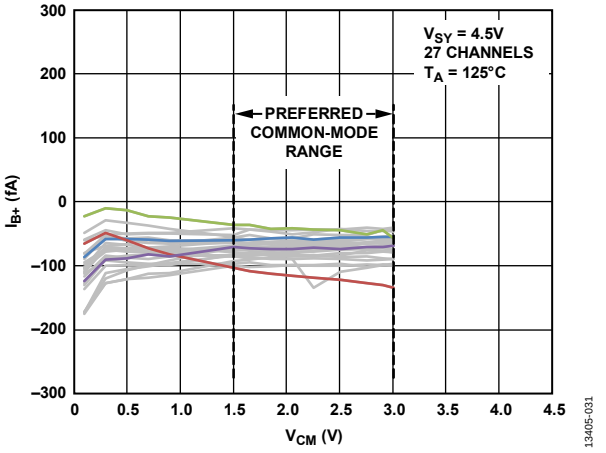


Figure 31. Noninverting Input Bias Current (I_{B+}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 4.5 V, T_A = 125°C

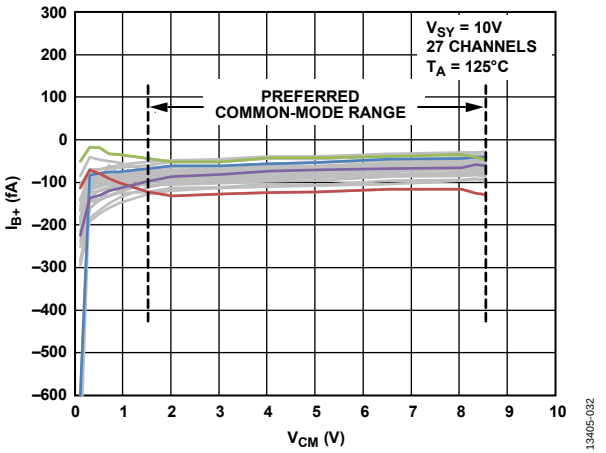


Figure 32. Noninverting Input Bias Current (I_{B+}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 10 V, T_A = 125°C

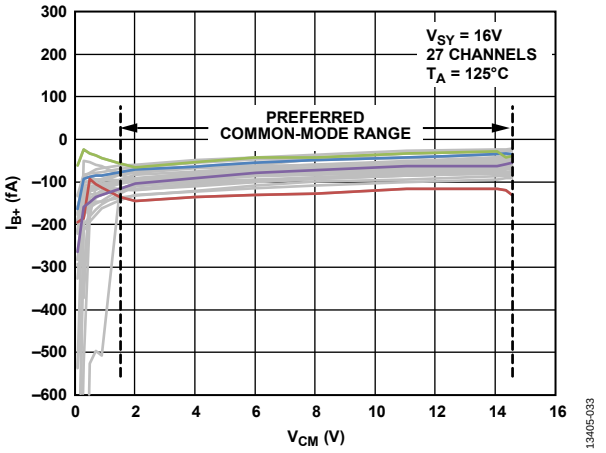


Figure 33. Noninverting Input Bias Current (I_{B+}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 16 V, T_A = 125°C

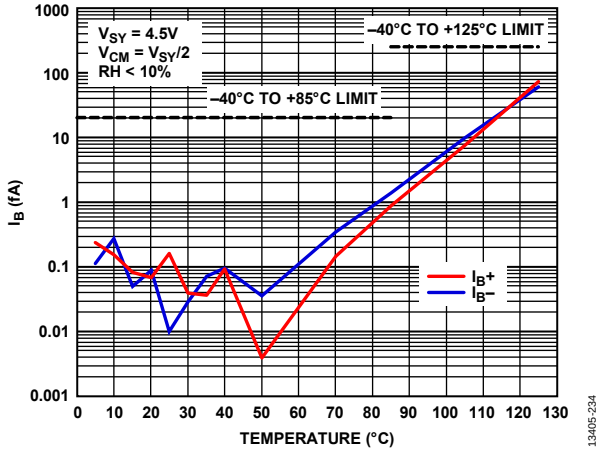


Figure 34. Input Bias Current (I_B) vs. Temperature, V_{SY} = 4.5 V

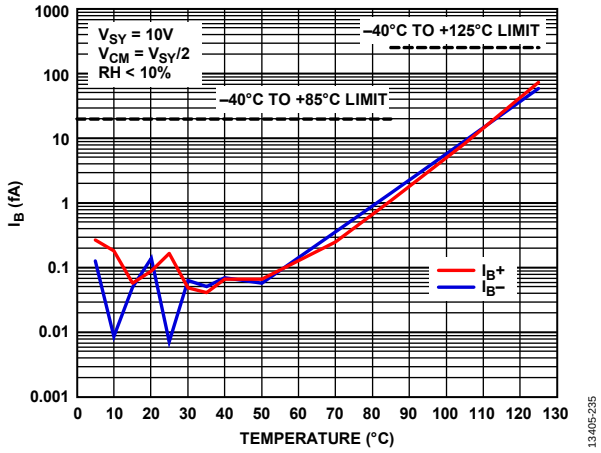


Figure 35. Input Bias Current (I_B) vs. Temperature, V_{SY} = 10 V

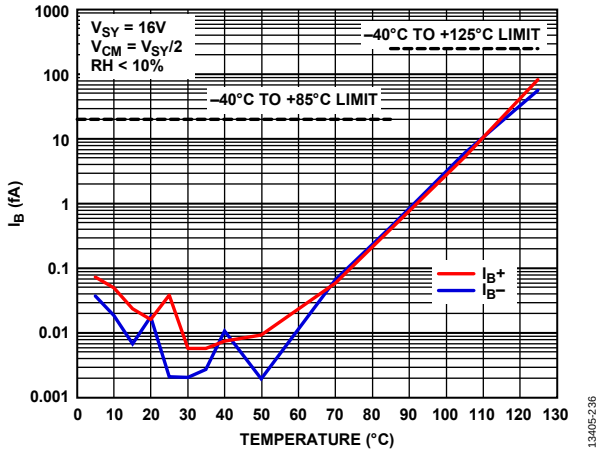


Figure 36. Input Bias Current (I_B) vs. Temperature, V_{SY} = 16 V

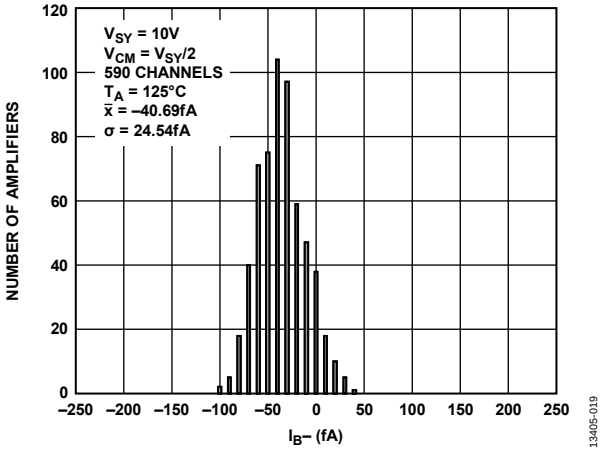


Figure 37. Inverting Input Bias Current Histogram, T_A = 125C, V_{SY} = 10 V

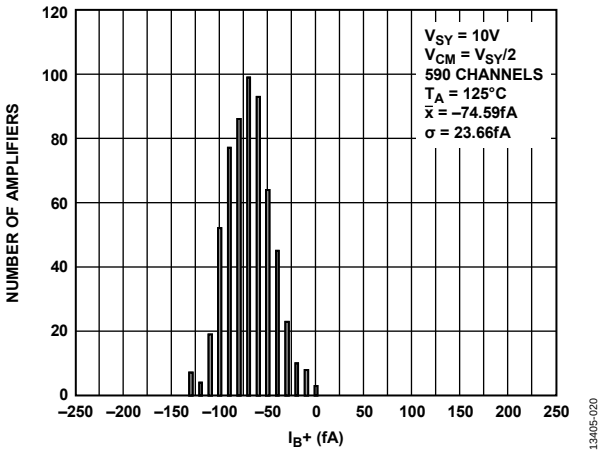


Figure 38. Noninverting Input Bias Current Histogram, T_A = 125°C, V_{SY} = 10 V

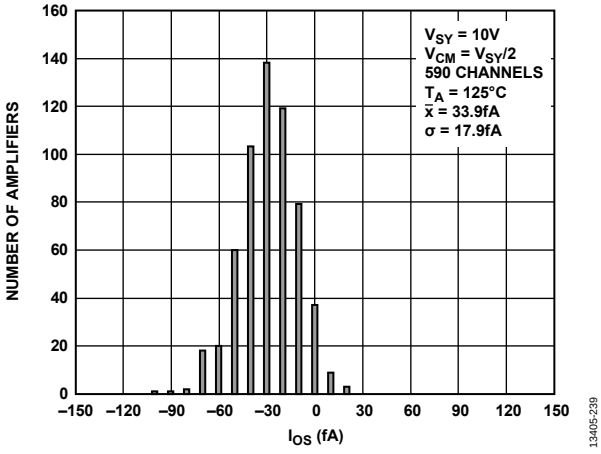


Figure 39. Input Offset Current Histogram

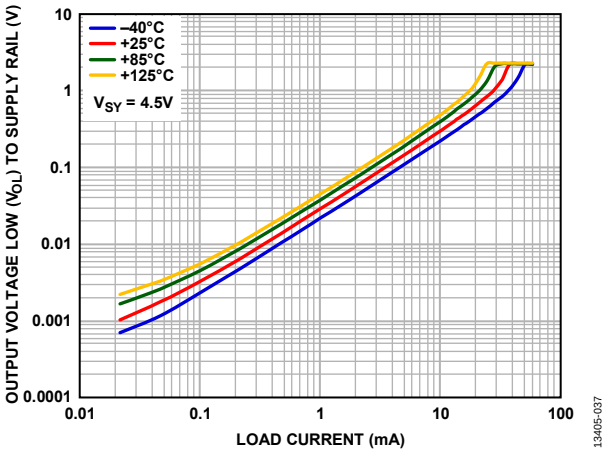


Figure 40. Output Voltage Low (V_{OL}) to Supply Rail vs. Load Current (I_{LOAD}), V_{SY} = 4.5 V

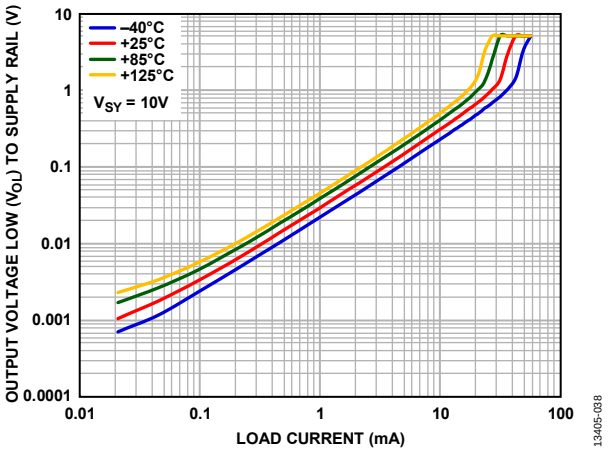


Figure 41 Output Voltage Low (V_{OL}) to Supply Rail vs. Load Current (I_{LOAD}), V_{SY} = 10 V

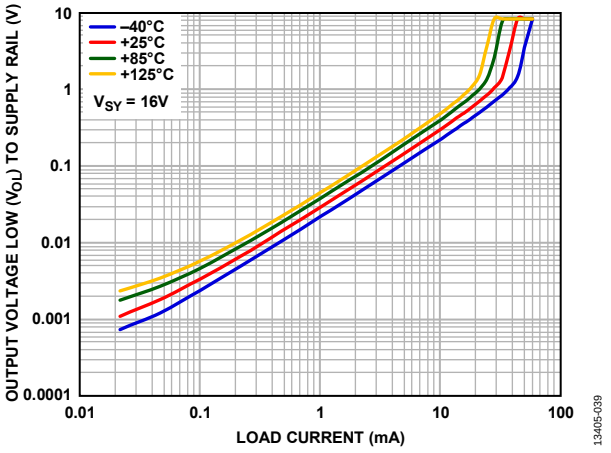


Figure 42. Output Voltage Low (V_{OL}) to Supply Rail vs. Load Current (I_{LOAD}), V_{SY} = 16 V

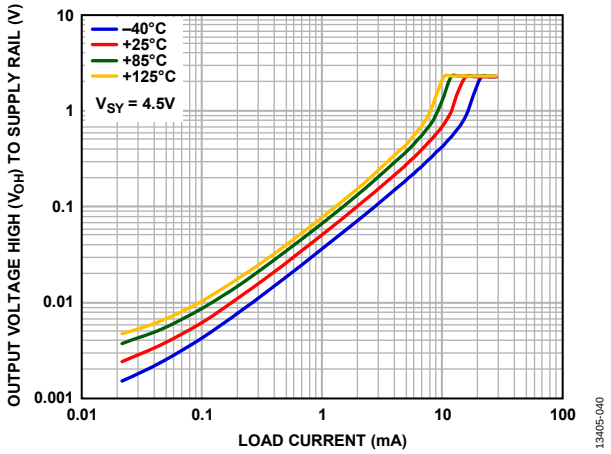


Figure 43. Output Voltage High (V_{OH}) to Supply Rail vs. Load Current (I_{LOAD}), V_{SY} = 4.5 V

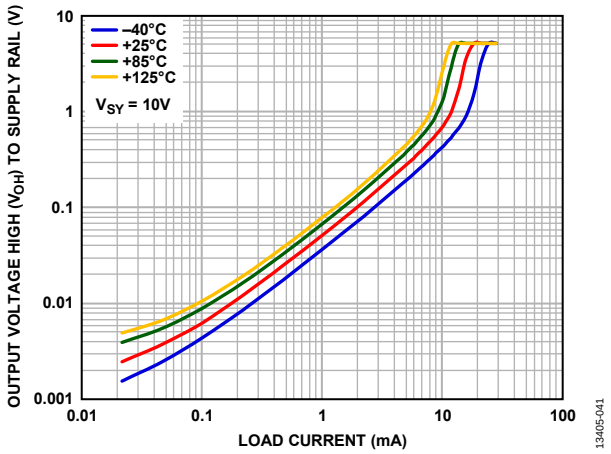


Figure 44. Output Voltage High (V_{OH}) to Supply Rail vs. Load Current (I_{LOAD}), V_{SY} = 10 V

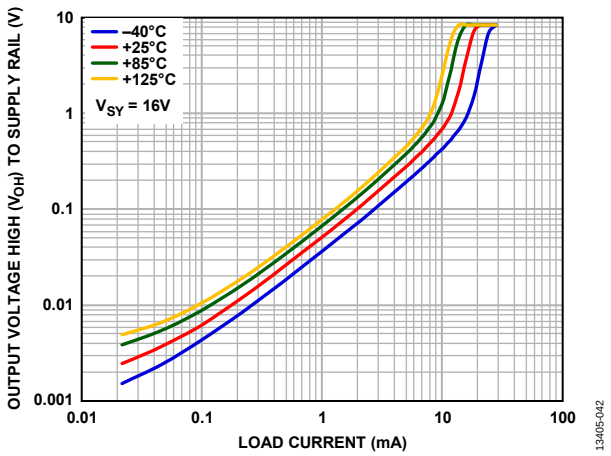


Figure 45. Output Voltage High (V_{OH}) to Supply Rail vs. Load Current (I_{LOAD}), V_{SY} = 16 V

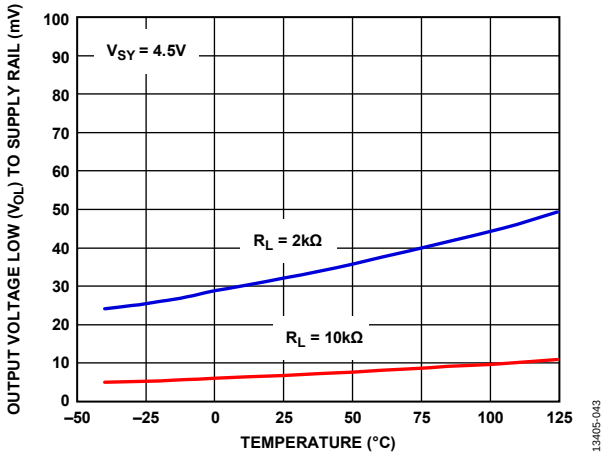


Figure 46. Output Voltage Low (V_{OL}) to Supply Rail vs. Temperature, V_{SY} = 4.5 V

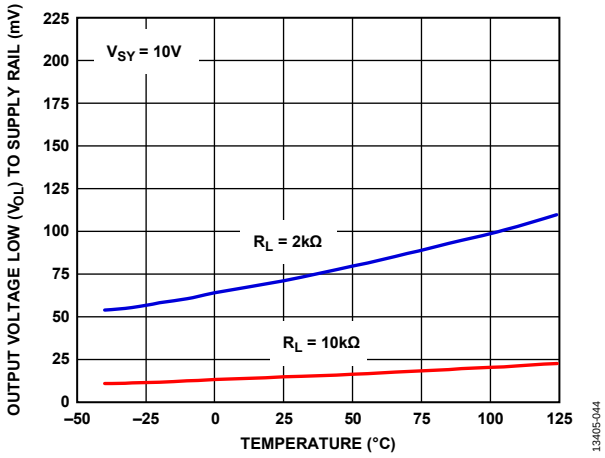


Figure 47. Output Voltage Low (V_{OL}) to Supply Rail vs. Temperature, V_{SY} = 10 V

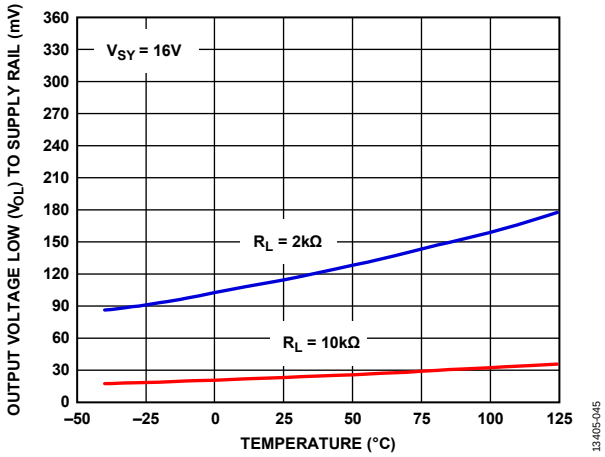


Figure 48. Output Voltage Low (V_{OL}) to Supply Rail vs. Temperature, V_{SY} = 16 V

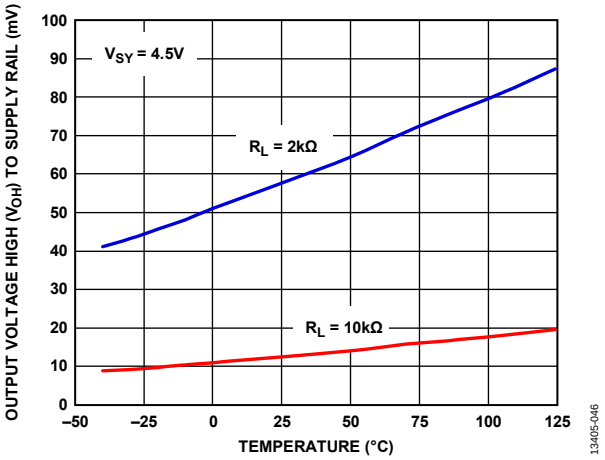


Figure 49. Output Voltage High (V_{OH}) to Supply Rail vs. Temperature, V_{SY} = 4.5 V

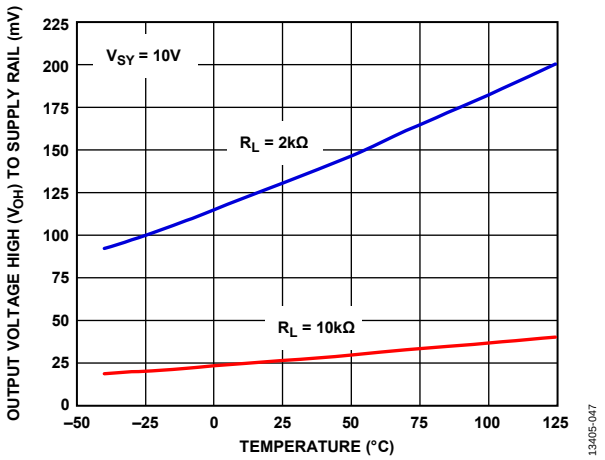


Figure 50. Output Voltage High (V_{OH}) to Supply Rail vs. Temperature, V_{SY} = 10 V

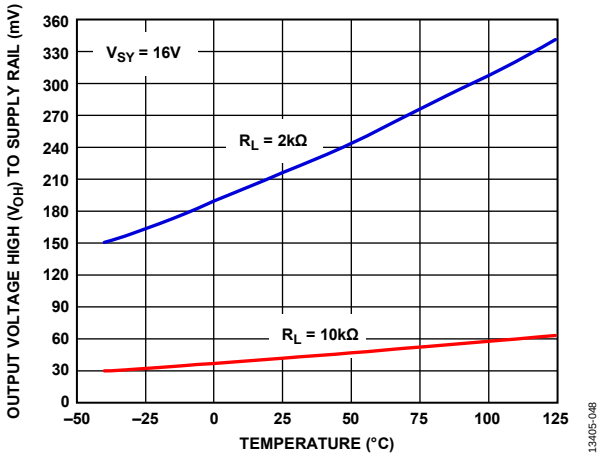


Figure 51. Output Voltage High (V_{OH}) to Supply Rail vs. Temperature, V_{SY} = 16 V

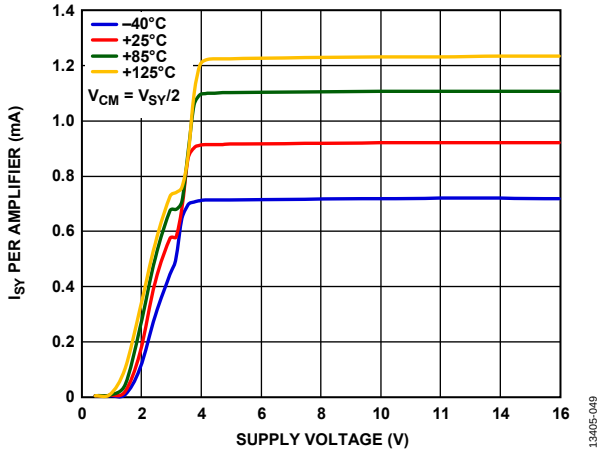


Figure 52. Supply Current (I_{SY}) per Amplifier vs. Supply Voltage (V_{SY})

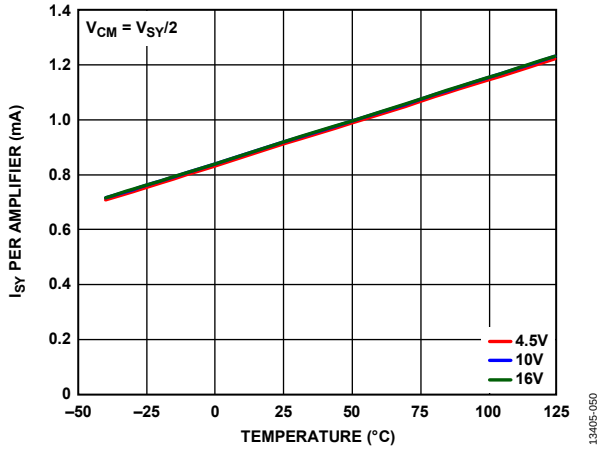


Figure 53. Supply Current (I_{SY}) per Amplifier vs. Temperature

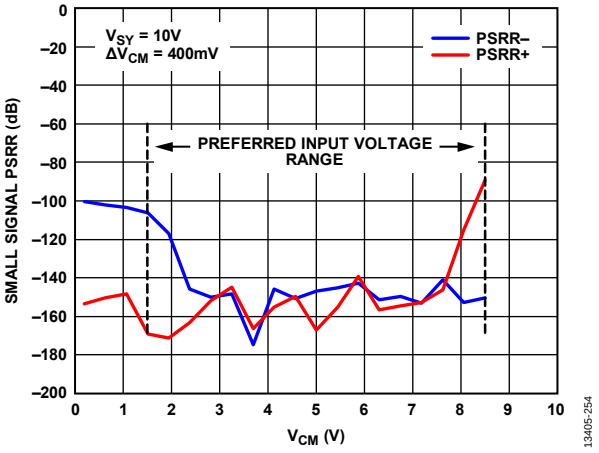


Figure 54. Small Signal PSRR vs. Common-Mode Voltage (V_{CM})

MAIN AMPLIFIER, AC PERFORMANCE

V_{SY} = 4.5 V to 16 V, data taken at V_{SY} = 10 V, T_A = 25°C, unless otherwise noted.

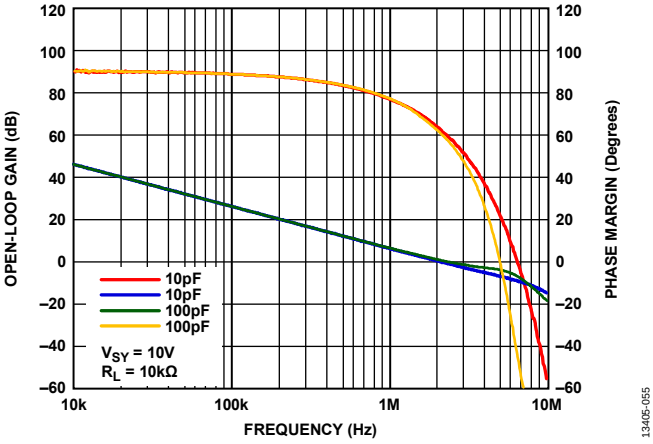


Figure 55. Open-Loop Gain and Phase Margin vs. Frequency

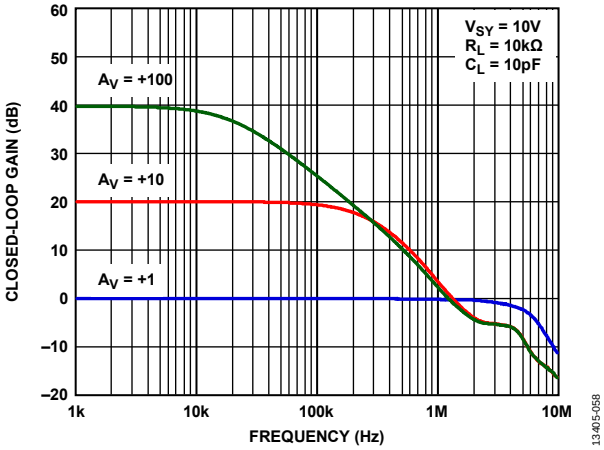


Figure 58. Closed-Loop Gain vs. Frequency

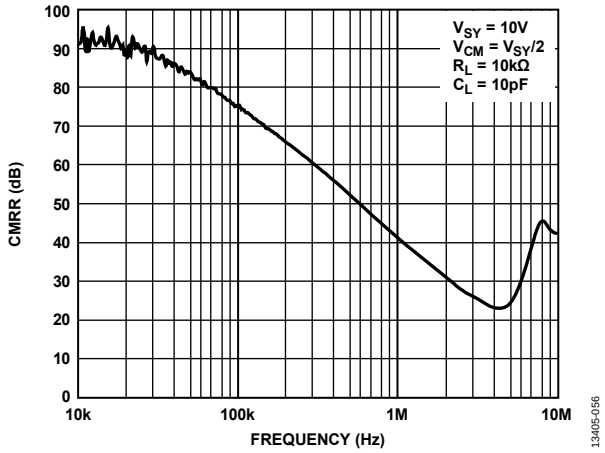


Figure 56. CMRR vs. Frequency

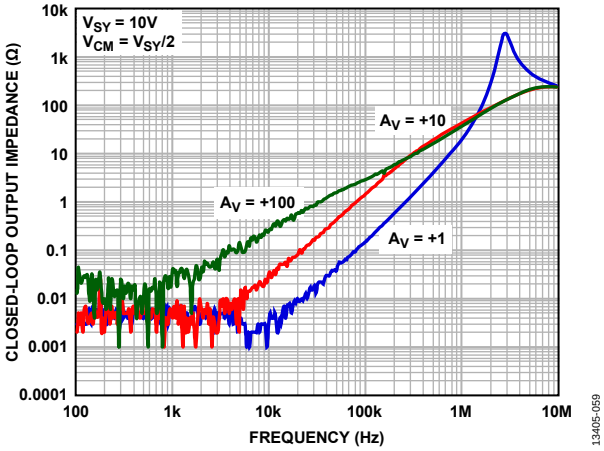


Figure 59. Closed-Loop Output Impedance vs. Frequency

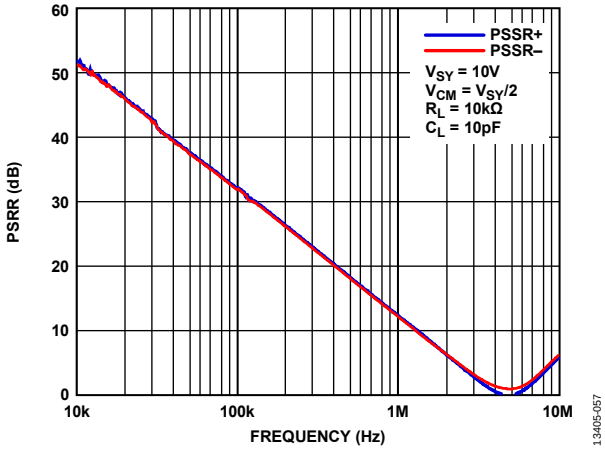


Figure 57. PSRR vs. Frequency

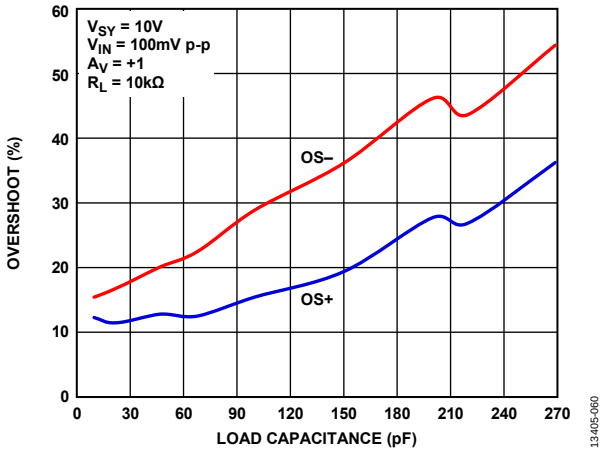


Figure 60. Small Signal Overshoot vs. Load Capacitance

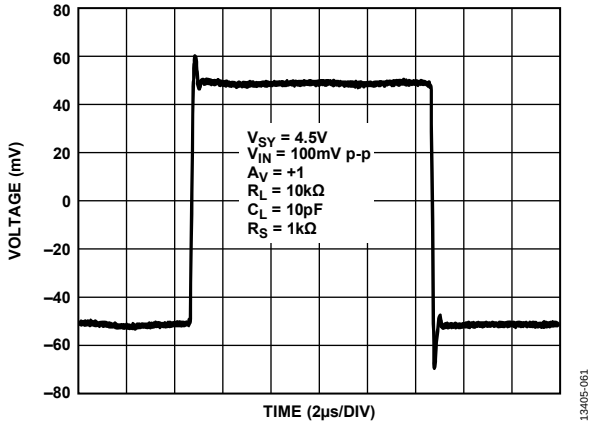


Figure 61. Small Signal Transient Response, V_{SY} = 4.5 V

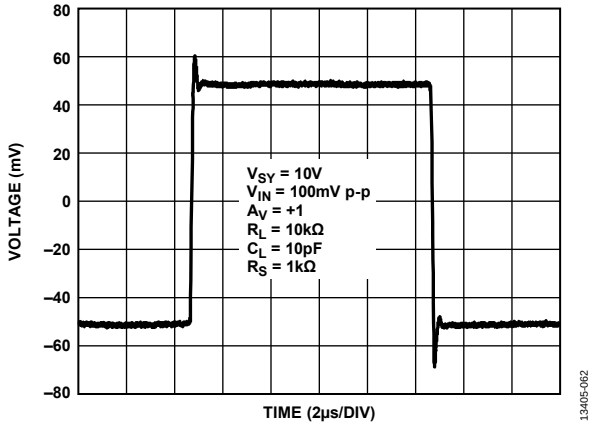


Figure 62. Small Signal Transient Response, V_{SY} = 10 V

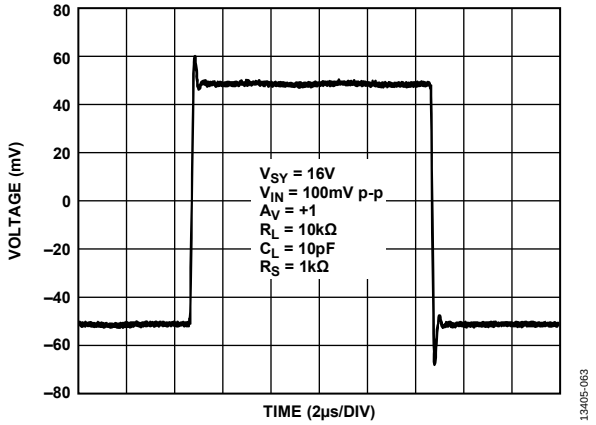


Figure 63. Small Signal Transient Response, V_{SY} = 16 V

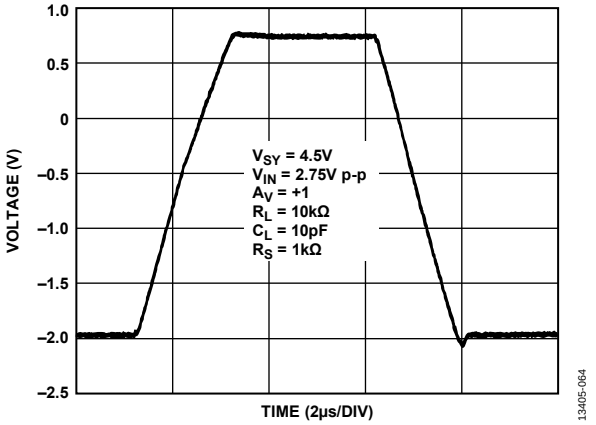


Figure 64. Large Signal Transient Response, V_{SY} = 4.5 V

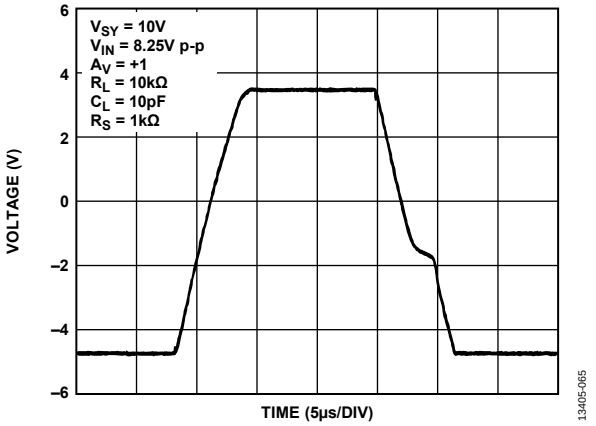


Figure 65. Large Signal Transient Response, V_{SY} = 10 V

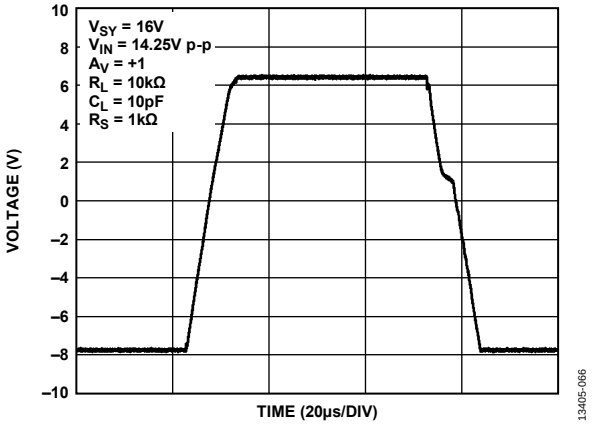


Figure 66. Large Signal Transient Response, V_{SY} = 16 V

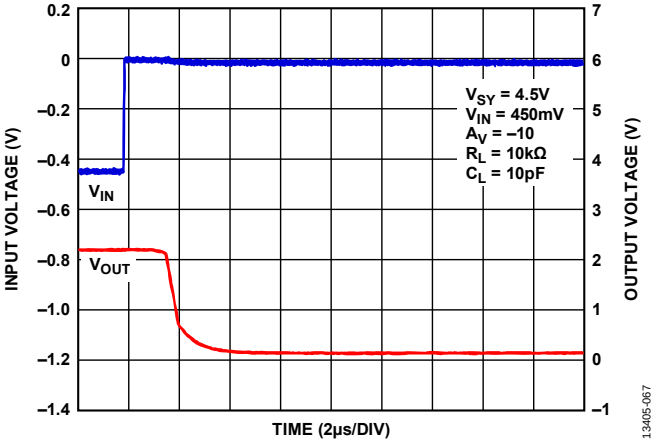


Figure 67. Positive Overload Recovery, V_{SY} = 4.5 V

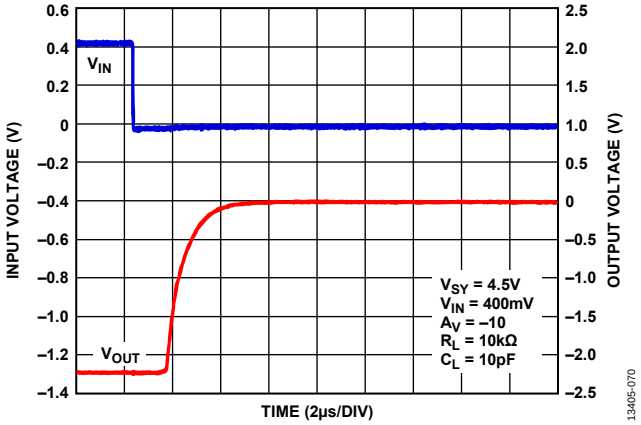


Figure 70. Negative Overload Recovery, V_{SY} = 4.5 V

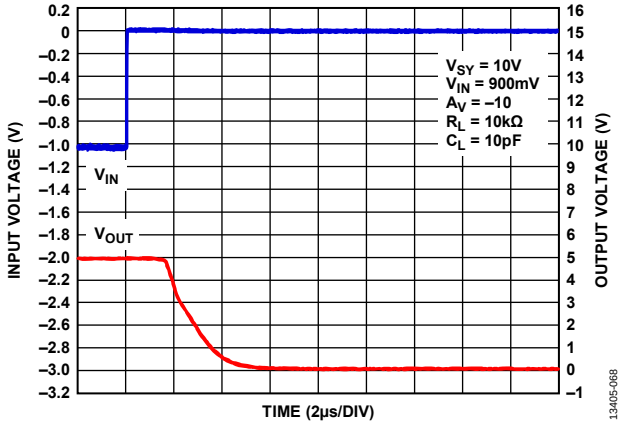


Figure 68. Positive Overload Recovery, V_{SY} = 10 V

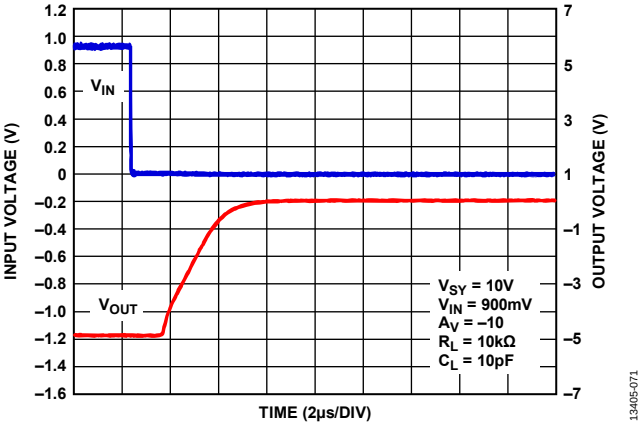


Figure 71. Negative Overload Recovery, V_{SY} = 10 V

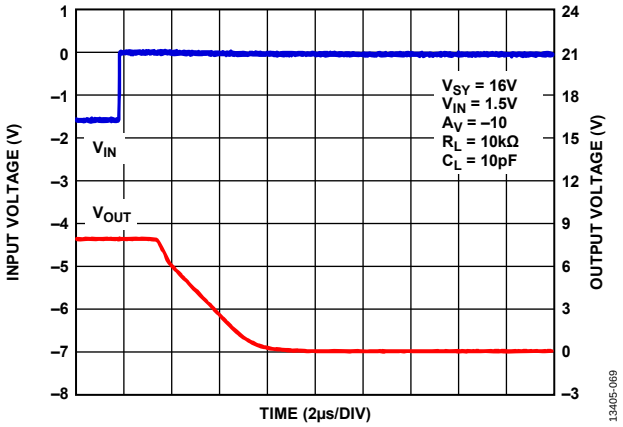


Figure 69. Positive Overload Recovery, V_{SY} = 16 V

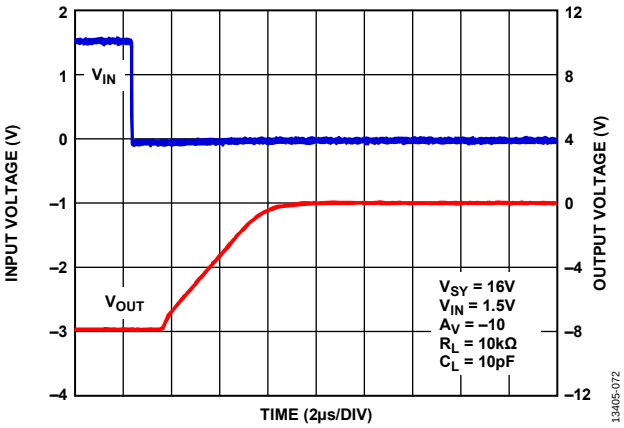


Figure 72. Negative Overload Recovery, V_{SY} = 16 V

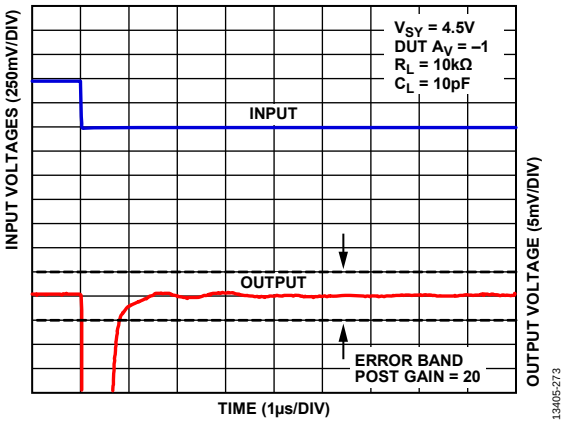


Figure 73. Negative Settling Time to 0.1%, V_{SY} = 4.5 V

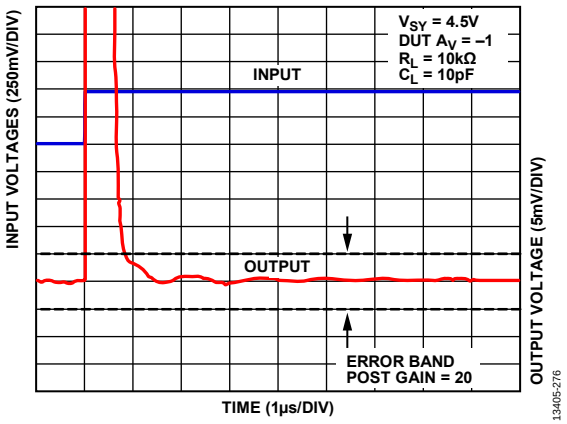


Figure 76. Positive Settling Time to 0.1%, V_{SY} = 4.5 V

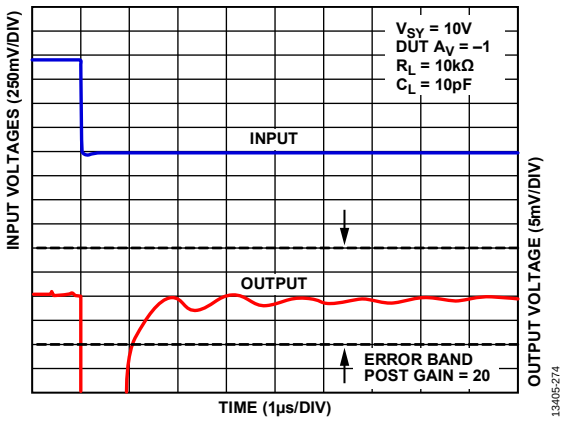


Figure 74. Negative Settling Time to 0.1%, V_{SY} = 10 V

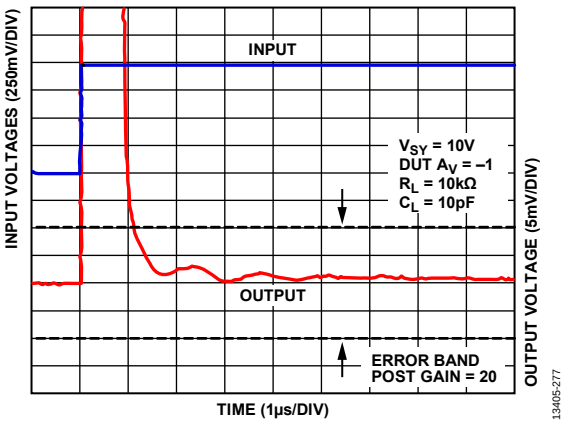


Figure 77. Positive Settling Time to 0.1%, V_{SY} = 10 V

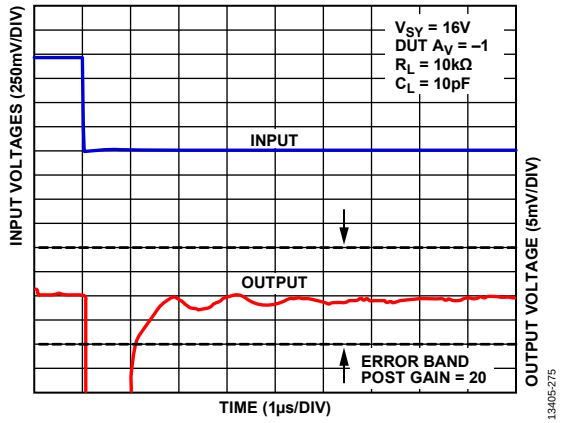


Figure 75. Negative Settling Time to 0.1%, V_{SY} = 16 V

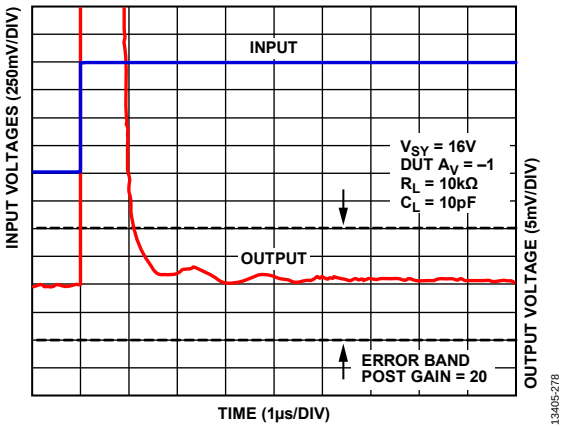


Figure 78. Positive Settling Time to 0.1%, V_{SY} = 16 V

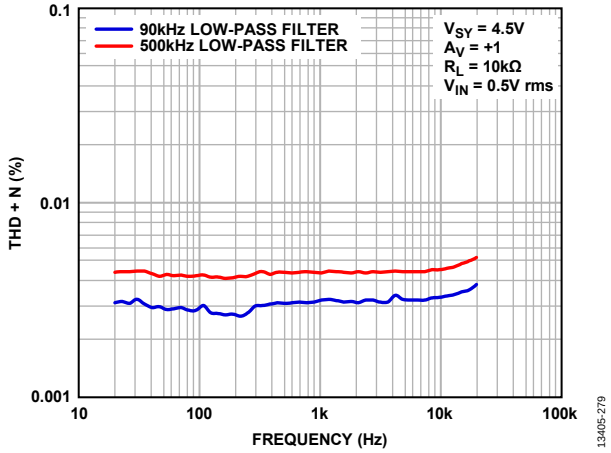


Figure 79. THD + N vs. Frequency, V_{SY} = 4.5 V

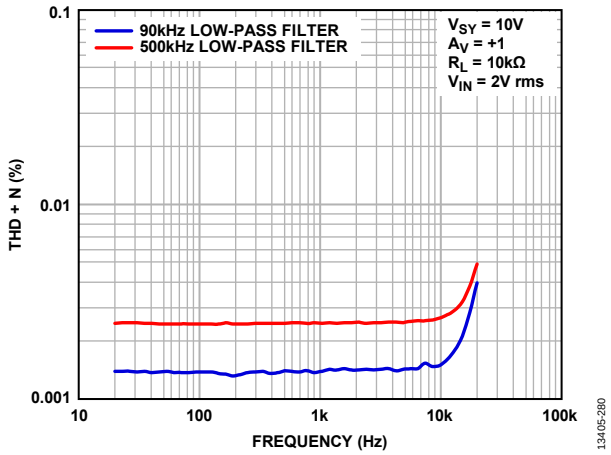


Figure 80. THD + N vs. Frequency, V_{SY} = 10 V

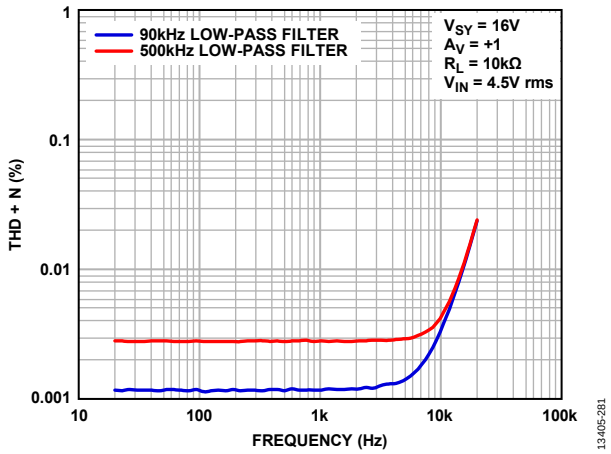


Figure 81. THD + N vs. Frequency, V_{SY} = 16 V

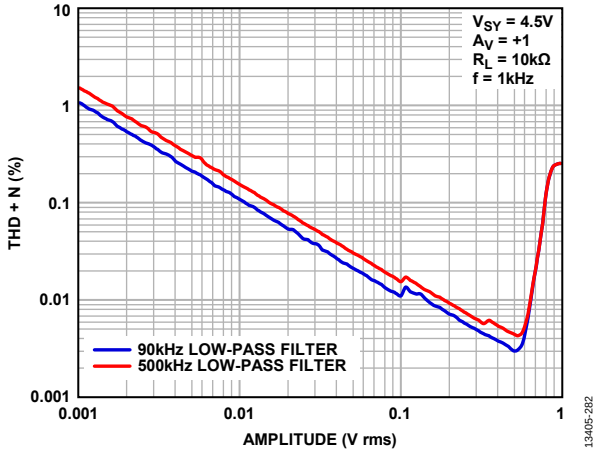


Figure 82. THD + N vs. Amplitude, V_{SY} = 4.5 V

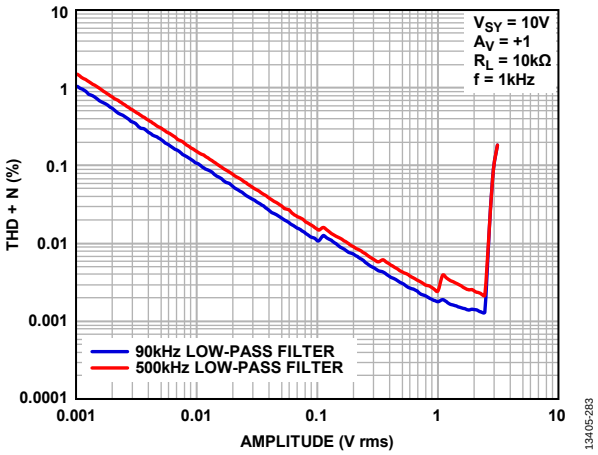


Figure 83. THD + N vs. Amplitude, V_{SY} = 10 V

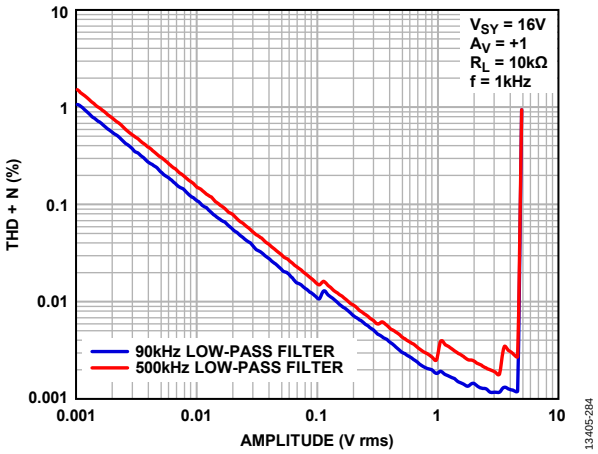


Figure 84. THD + N vs. Amplitude, V_{SY} = 16 V

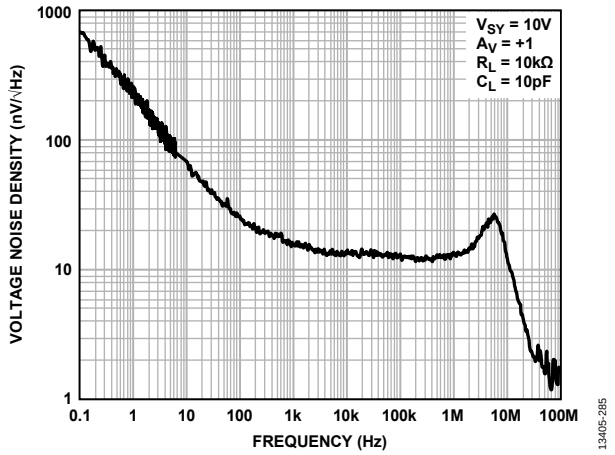


Figure 85. Voltage Noise Density, V_{SY} = 10 V

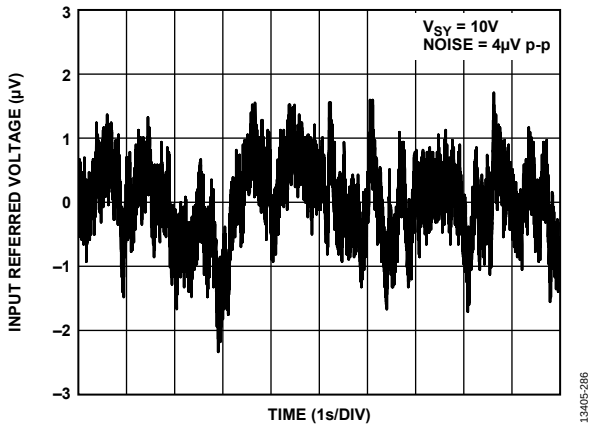


Figure 86. 0.1 Hz to 10 Hz Noise

GUARD AMPLIFIER

T_A = 25°C, unless otherwise noted.

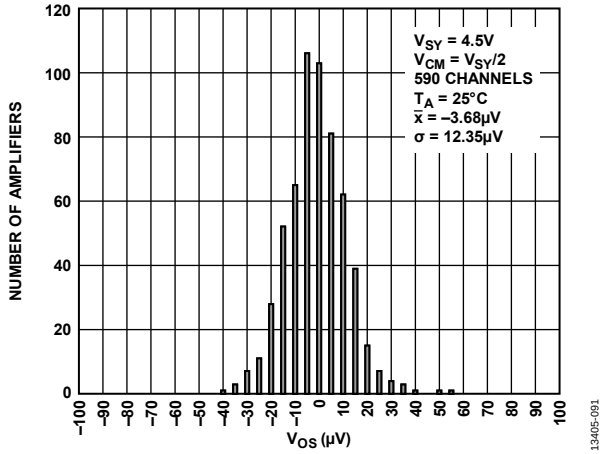


Figure 87. Input Offset Voltage Distribution, V_{SY} = 4.5 V

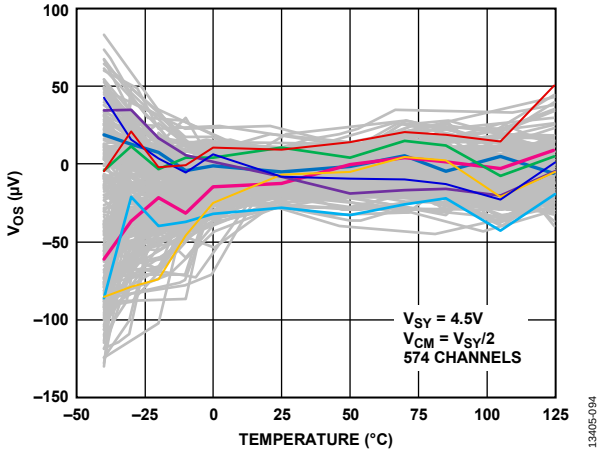


Figure 90. Input Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = 4.5 V

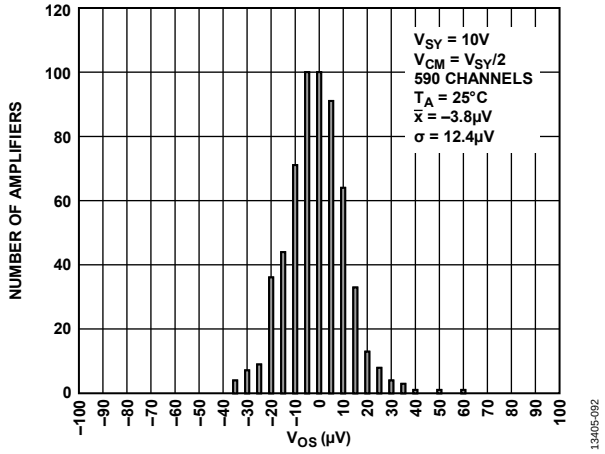


Figure 88. Input Offset Voltage Distribution, V_{SY} = 10 V

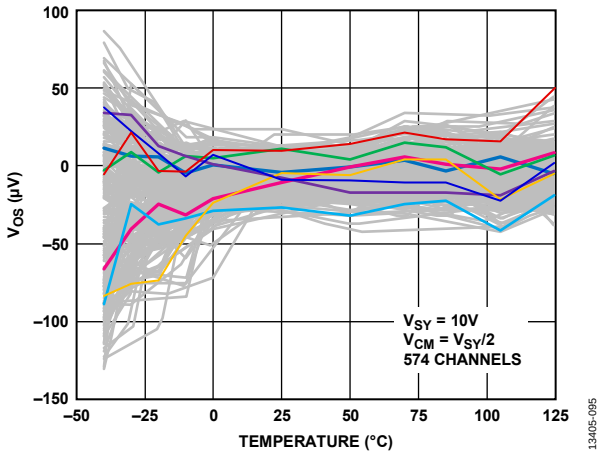


Figure 91. Input Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = 10 V

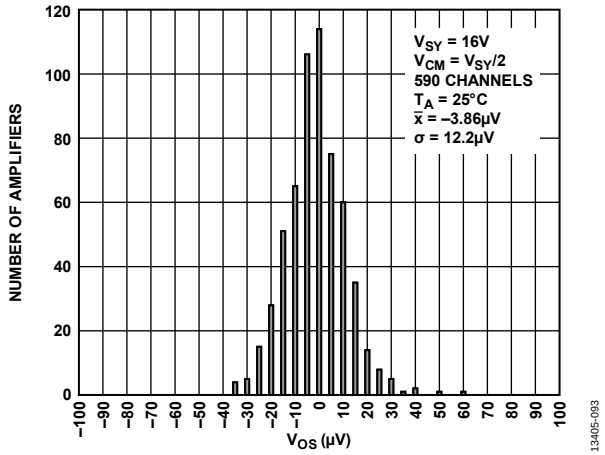


Figure 89. Input Offset Voltage Distribution, V_{SY} = 16 V

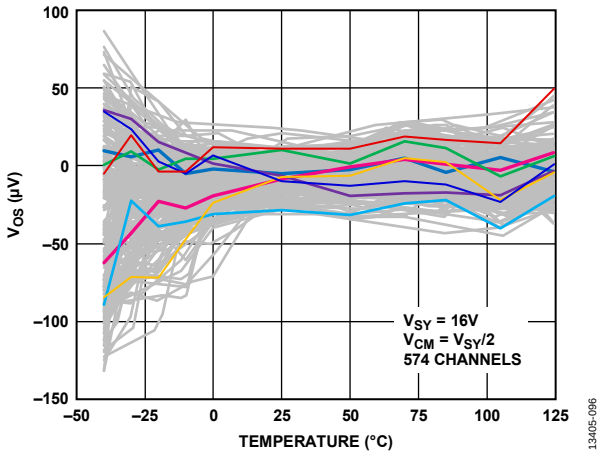


Figure 92. Input Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = 16 V

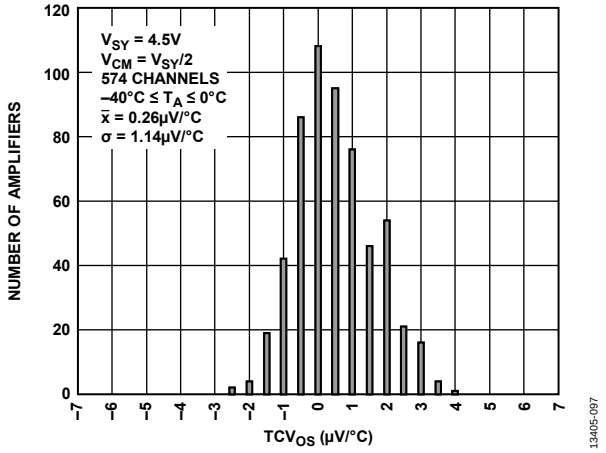


Figure 93. Input Offset Voltage Drift Distribution, −40°C ≤ T_A ≤ 0°C, V_{SY} = 4.5 V

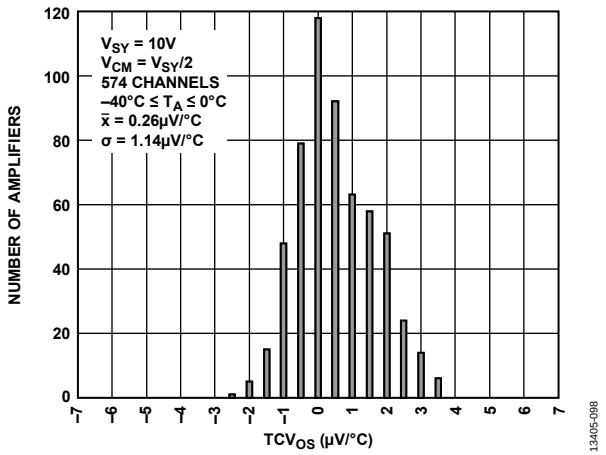


Figure 94. Input Offset Voltage Drift Distribution, −40°C ≤ T_A ≤ 0°C, V_{SY} = 10 V

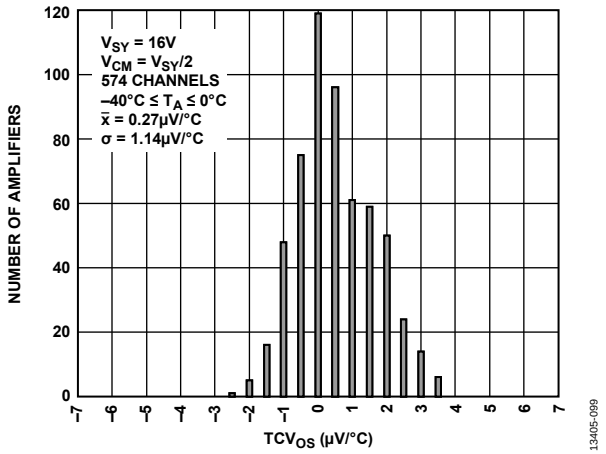


Figure 95. Input Offset Voltage Drift Distribution, −40°C ≤ T_A ≤ 0°C, V_{SY} = 16 V

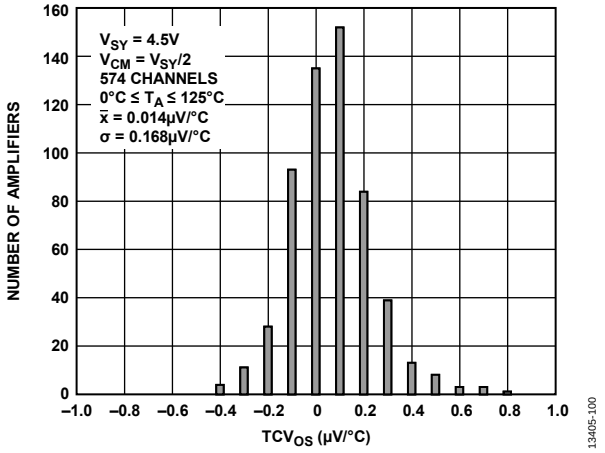


Figure 96. Input Offset Voltage Drift Distribution, 0°C ≤ T_A ≤ 125°C, V_{SY} = 4.5 V

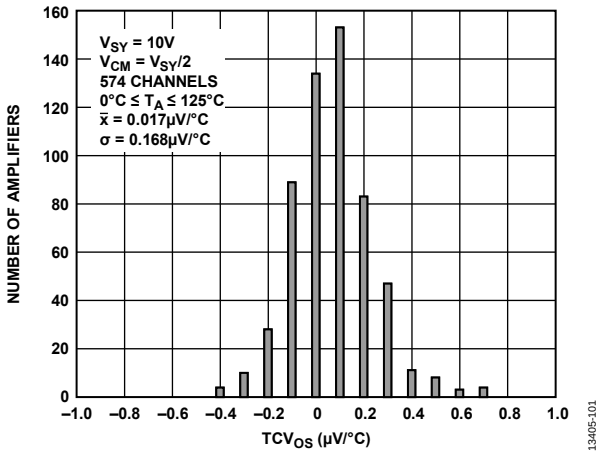


Figure 97. Input Offset Voltage Drift Distribution, 0°C ≤ T_A ≤ 125°C, V_{SY} = 10 V

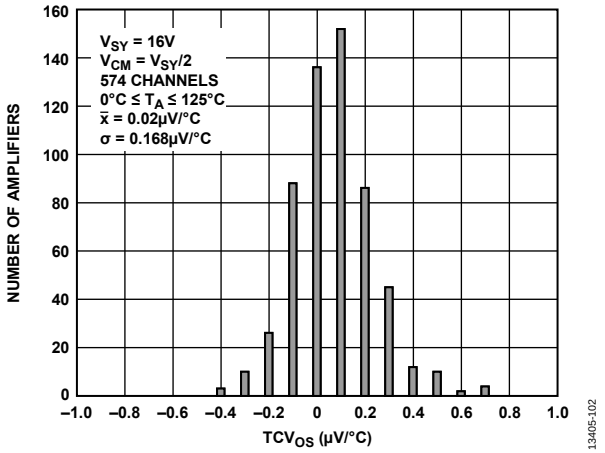


Figure 98. Input Offset Voltage Drift Distribution, 0°C ≤ T_A ≤ 125°C, V_{SY} = 16 V

THEORY OF OPERATION

The ADA4530-1 is an operational amplifier specifically designed to interface with the extremely high impedance sensors used in electrometer applications.

A MOSFET input stage eliminates the gate leakage currents associated with legacy junction gate field effect transistor (JFET) electrometers. The ADA4530-1 achieves extremely low input bias currents while simultaneously providing robust protection against ESD damage. A unique ESD diode structure provides protection while also allowing the diodes to be guarded to minimize leakage currents to the input pins. The ADA4530-1 integrates the precision buffer used to guard internal ESD diode leakage paths. The output of this guard buffer is also connected to external pins to allow the user to guard external components against leakage currents.

The input bias current is determined by the accuracy of the guard voltage applied across the ESD diodes. The offset voltages of the amplifier and guard buffer set the accuracy of the guard voltage and, therefore, the input bias current.

The ADA4530-1 uses Analog Devices, Inc., DigiTrim™ technology to achieve its superior performance.

DigiTrim is used to trim the offset voltage of the amplifier and guard buffer to reject changes in the common-mode voltage, power supply voltage, and temperature. This technique significantly improves V_{OS}, CMRR, PSRR, and TCV_{OS} specifications.

Figure 99 shows the simplified schematic of the ADA4530-1. The amplifier uses a three-stage architecture with a fully differential input stage to achieve excellent dc performance specifications.

ESD STRUCTURE

The input ESD structure consists of Diode D1 to Diode D6. The noninverting input is coupled to the guard pins (GRD) by the D1 and D2 antiparallel diodes. The inverting input is coupled to the guard pins by the D3 and D4 antiparallel diodes. The guard pins are connected to the power supplies through Diode D5 and Diode D6. During ESD events, the transient current flows from the input pins through one of the antiparallel diodes and harmlessly into the supplies through one of the power supply diodes. During normal operation, the guard buffer (BUF1) forces the voltage across the antiparallel diodes to 0 V. Resistor R1 shields the guard buffer from potentially large capacitances connected to the guard pins. Its value is nominally 1 kΩ.

INPUT STAGE

The input stage comprises a PMOS differential pair (M1, M2), folded cascode transistors (M5 to M12), and current source I1.

The ADA4530-1 achieves its high performance specifications by using low voltage MOS devices for its differential inputs. These low voltage MOS devices offer better 1/f noise and bandwidth per unit current compared to high voltage devices. The input stage is isolated from the high system voltages with proprietary protection circuitry. This regulation circuitry protects the input devices from the high supply voltages in which the amplifier can operate.

The proprietary high voltage protection circuitry in the ADA4530-1 operates in such a way that it minimizes the common-mode voltage changes seen by the amplifier input stage for most of the input common-mode range. This circuitry results in excellent disturbance rejection when operating in this preferred input common-mode range. The performance benefits of operating within this preferred range are shown in the V_{OS} vs. V_{CM} graphs (see Figure 16 to Figure 18), the small signal CMRR vs. V_{CM} graph (see Figure 21), and the small signal PSRR vs. V_{CM} graph (see Figure 54).

These input devices are protected from large differential input voltages by the antiparallel ESD diodes (D1 to D4). The diodes can conduct significant current when the differential voltage exceeds 700 mV. The user must ensure that the current flowing into the input pins is limited to the absolute maximum of 10 mA.

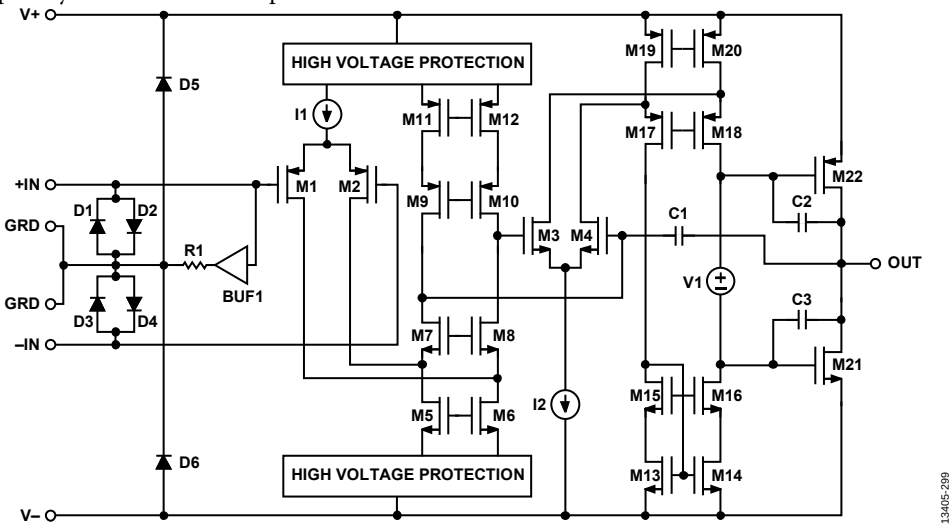


Figure 99. Simplified Schematic

GAIN STAGE

The second stage of the amplifier comprises an NMOS differential pair (M3, M4) and folded cascode transistors (M13 to M20). The amplifier features nested Miller compensation (C1 to C3).

OUTPUT STAGE

The ADA4530-1 features a complementary common-source output stage consisting of the M21 and M22 transistors. These transistors are configured in a Class AB topology and are biased by the voltage source, V1. This topology allows the output voltage to be within tens of millivolts of the supply rails, achieving a rail-to-rail output swing. The output voltage is limited by the output impedance of the transistors. The output voltage swing is a function of the load current and can be estimated using the output voltage to the supply rail vs. load current graphs (see Figure 40 to Figure 45).

GUARD BUFFER

The guard buffer (BUF1) is a unity-gain amplifier that creates a low impedance replica of the input common-mode voltage. The buffer input is connected to the noninverting input (IN+). The noninverting input voltage is approximately equal to the input common-mode voltage when the main amplifier feedback loop is settled.

The guard buffer uses a three-stage architecture similar to that of the amplifier. The guard buffer uses a rail-to-rail output stage that allows the guard voltage to swing within 100 mV of the supply rails. Because the guard buffer output follows the input common-mode voltage, this output swing limits the effectiveness of the guard buffer at low input common-mode voltages. This limit can be seen as a significant increase in input bias current at low common-mode voltages in the input bias current vs. common-mode voltage graphs (see Figure 22 to Figure 33). For this reason, it is not recommended to operate the circuit with an input common-mode voltage of less than 100 mV from the V− supply rail.

The guard buffer output voltage can be degraded from excessive loading. The 1 kΩ output resistance adds 1 µV of guard voltage error per 1 nA of load current. It is possible to drive the guard offset voltage out of its specifications with a few tens of nanoamperes of load current. For this reason, it is not recommended to drive anything except insulation resistance (see the Insulation Resistance and Guarding section) with the guard buffer. If more drive strength is needed, the guard voltage can be buffered with a low offset, low input bias current op amp such as the ADA4661-2.

APPLICATIONS INFORMATION

The ADA4530-1 is a single, electrometer grade, CMOS operational amplifier with femtoampere input bias current and ultralow offset voltage. It operates over a wide supply voltage range of 4.5 V (or ±2.25 V dual supply) to 16 V (or ±8 V dual supply). It is a single-supply amplifier, where its input voltage range includes the lower supply rail and has a rail-to-rail output. The ADA4530-1 also achieves a low offset voltage of ±40 µV maximum and offset voltage drift of ±0.5 µV/C maximum.

The ADA4530-1 has ultralow input bias currents that are production tested at 25°C and 125°C to ensure that the device meets its performance goals in a system application. An integrated guard buffer is provided to minimize input pin leakage in a printed circuit board (PCB) design, minimize board component count, and enable ease of system design. The guard buffer output pins are also strategically placed next to the input pins to enable easy routing of the guard ring and to prevent coupling between the inputs, power supplies, and the output pin.

The ADA4530-1 is suited for applications requiring very low input bias current and low offset voltage, including, but not limited to, preamplifier applications, for a wide variety of current output transducers (photodiodes, photomultiplier tubes), spectrometry, chromatography, and high impedance buffering for chemical sensors.

INPUT PROTECTION

When either input of the ADA4530-1 exceeds one of the supply rails by more than 300 mV, the input ESD diodes become forward-biased and large amounts of current begin to flow through them. Without current limiting, this excessive fault current causes permanent damage to the device. If the inputs are expected to be subject to overvoltage conditions, insert a resistor in series with each input to limit the input current to 10 mA maximum. However, consider the resistor thermal noise effect on the entire circuit.

SINGLE-SUPPLY AND RAIL-TO-RAIL OUTPUT

The ADA4530-1 is a single supply amplifier with an input voltage range (IVR) from V− to V+ − 1.5 V. The amplifier has a small keep alive input stage that allows it to function properly when the input common-mode voltage is greater than the specified IVR. This feature allows the ADA4530-1 to start up and recover quickly in certain types of circuits where the IVR is violated at power-up. The ac and dc performance of this keep alive stage is poor; do not rely upon this keep alive stage for normal use.

Figure 100 shows the input and output waveforms of the ADA4530-1 configured as a unity-gain buffer with a supply voltage of ±8 V. The output tracks the input voltage over the entire range until the output voltage is clamped at its maximum output swing. Note that the amplifier still operates even when the signal is outside the specified input voltage range (−8 V ≤ IVR ≤ +6.5 V); this is due to the keep alive stage. Additionally, it does not phase reverse. It is not recommended to apply an input voltage that is outside of the input voltage range.

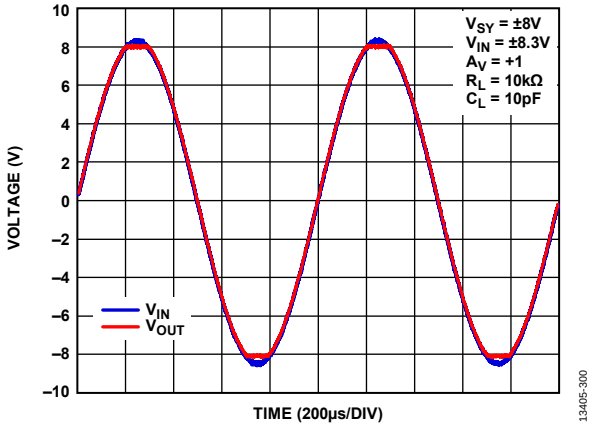


Figure 100. No Phase Reversal

CAPACITIVE LOAD STABILITY

The ADA4530-1 can safely drive capacitive loads of up to 250 pF in any configuration. As with most amplifiers, driving larger capacitive loads than specified may cause excessive overshoot and ringing, or even oscillation. A heavy capacitive load reduces phase margin and causes the amplifier frequency response to peak. Peaking corresponds to overshooting or ringing in the time domain. Therefore, it is recommended that external compensation be used if the ADA4530-1 must drive a load exceeding 250 pF. This compensation is particularly important in the unity-gain configuration, which is the worst case for stability.

A quick and easy way to stabilize the op amp for capacitive load drive is by adding a series resistor, R_{ISO}, between the amplifier output terminal and the load capacitance, as shown in Figure 101. R_{ISO} isolates the amplifier output and feedback network from the capacitive load. However, with this compensation scheme, the output impedance as seen by the load increases, and this reduces gain accuracy.

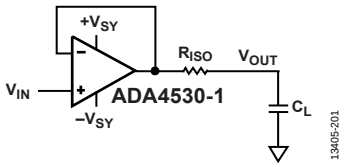


Figure 101. Stability Compensation with Isolating Resistor, R_{ISO}

Figure 102 shows the phase margin of the ADA4530-1 with different values of output isolating resistors and capacitive loads. Figure 103 shows the frequency response with 1 nF capacitive load and different isolating resistors.

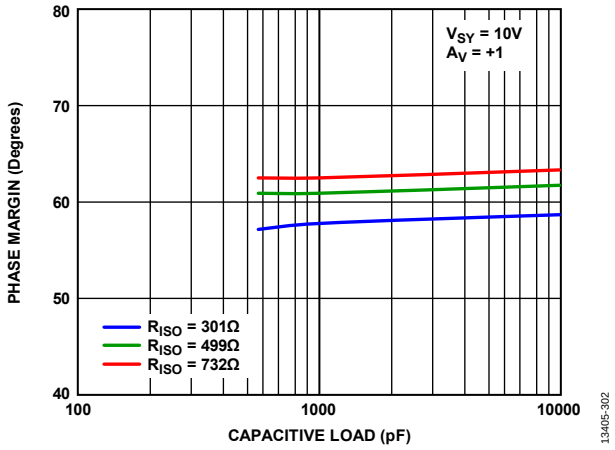


Figure 102. Phase Margin vs. Load Capacitance with Various Output Isolating Resistors

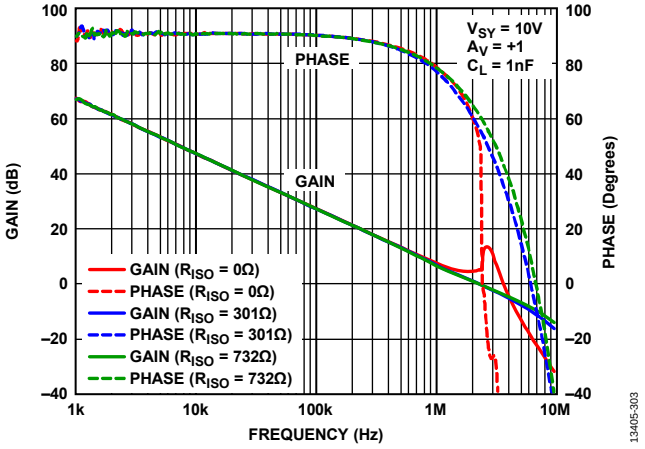


Figure 103. Frequency Response with C_L = 1 nF and Various Isolating Resistors

EMI REJECTION RATIO

Circuit performance is often adversely affected by high frequency electromagnetic interference (EMI). When the signal strength is low and transmission lines are long, an op amp must accurately amplify the input signals. However, all op amp pins—the noninverting input, inverting input, positive supply, negative supply, and output pins—are susceptible to EMI signals. These high frequency signals are coupled into an op amp by various means, such as conduction, near field radiation, or far field radiation. For example, wires and PCB traces can act as antennas and pick up high frequency EMI signals.

Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, op amps can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

To describe the ability of the ADA4530-1 to perform as intended in the presence of electromagnetic energy, the electromagnetic interference rejection ratio (EMIRR) of the noninverting pin is specified in Table 1, Table 2, and Table 3 of the Specifications section. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20\log(V_{IN_PEAK}/\Delta V_{OS})$$

Figure 104 shows the typical EMIRR vs. frequency performance for each of the specified supply voltages.

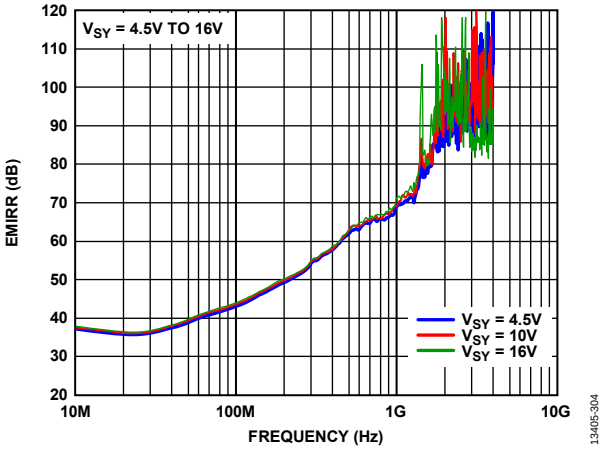


Figure 104. EMIRR vs. Frequency

HIGH IMPEDANCE MEASUREMENTS

The ADA4530-1 is designed to maximize the performance of very high impedance circuits. Its performance advantages make it useful for circuit impedances ranging from 100 MΩ to over 10 TΩ. Measurements of high impedance circuits are subject to a number of error sources. General information about making measurements from high resistance sources can be found in the *Low Level Measurements Handbook*, sixth edition (Keithley Instruments, Inc., 2004).

The ADA4530-1 is typically used in two kinds of circuits: a buffer and a TIA. Buffer circuits are useful for measuring voltage output sensors with high output resistance. Some example sensors include pH probes and reference electrodes (RE) in coulometry control loops. TIA circuits are useful for converting the signal from a current output sensor to an output voltage. Some example sensors include photodiodes and ion chambers.

The following sections describe some of the most important error sources when using the ADA4530-1 in these circuits. Simplified models with error sources are provided for the buffer (see Figure 105) and the TIA (see Figure 106).

The buffer circuit models the voltage output sensor as a voltage source (V_{SRC}) with an output resistance (R_{SRC}). The voltage on the A terminal is sensed by Pin 1 of the ADA4530-1 in a noninverting gain configuration (or a unity-gain configuration). The B terminal is driven to a suitable reference voltage (signal ground in this case).

If all errors sources are ignored, the output of the circuit is as follows:

$$V_{OUT} = V_{SRC}\left(1+\frac{R_F}{R_S}\right)$$

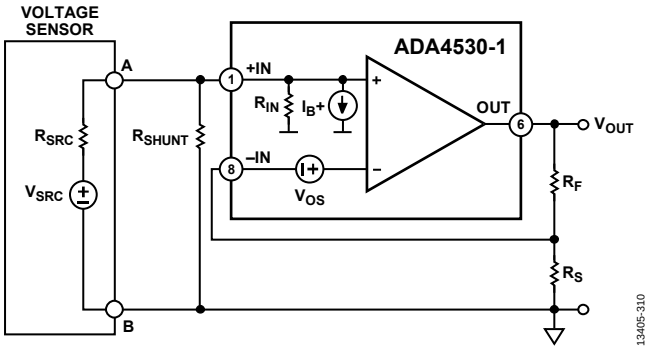


Figure 105. Voltage Buffer Circuit

The TIA circuit models the current output sensor as a current source (I_{SRC}) with a shunt resistance (R_{SRC}). The current from the A terminal is connected to the inverting input pin of the ADA4530-1 and the feedback resistor (R_F). The B terminal and the noninverting input of the amplifier are driven to a suitable reference voltage (signal ground in this case). The negative feedback of the circuit suppresses any voltage changes at the A terminal. This suppression is accomplished by forcing all current through the feedback resistor. If all error sources are ignored, the output of the circuit is as follows:

$$V_{OUT} = I_{SRC}R_F$$

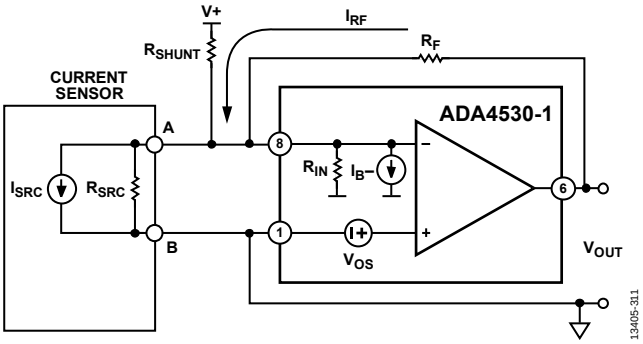


Figure 106. Transimpedance Amplifier Circuit

INPUT BIAS CURRENT

The input bias current of the amplifier is a major error source in high impedance electrometer circuits.

Like other semiconductor amplifiers, the input bias current of the ADA4530-1 has an exponential dependence on temperature. The input bias current of the ADA4530-1 increases by a factor of 2.5 for every 10°C increase in temperature. Refer to the input bias current vs. temperature graphs (see Figure 34 to Figure 36) for typical temperature performance. Notice that the exponential diode currents cease to be the dominate contributor to the input bias current at temperatures below 60°C to 70°C. The residual 100 aA to 200 aA (aA = 10^{-18} A) bias currents are dominated by other leakage paths that are highly sensitive to environmental conditions. These vanishingly small bias currents require highly controlled laboratory conditions to measure. Most practical applications are dominated by other errors, and the ADA4530-1 input bias current can be considered to be zero for temperatures less than 70°C. The input bias current of the ADA4530-1 can only be guaranteed to ±20 fA due to the measurement limitations of a production environment even though the achievable input bias currents are more than an order of magnitude lower.

The input bias current affects the buffer circuit by loading down the voltage sensor. The input bias current is forced to flow through the output resistance of the sensor, which creates an error voltage.

$$V_{ERR} = I_{B+}(R_{SRC})$$

The magnitude of this voltage error can be significant with very high impedance sensors operating at high temperature. For example, the input bias current can generate a maximum voltage error of 25 mV from a 100 GΩ sensor operating at 125°C.

The input bias current affects the TIA circuit by summing together with the sensor current. Both of these currents flow through the feedback resistor to generate the output voltage as follows:

$$V_{OUT} = (I_{SRC} + I_{B-})R_F$$

The magnitude of the input bias current limits how small of a signal current may be resolved accurately. For example, if the acceptable error level is 10%, the minimum measurable signal current is 2.25 pA for a circuit operating at 125°C.

$$I_{SRC} = I_{B-}(1/err - 1)$$

where *err* is the error level.

$$2.25\text{ pA} = 250\text{ fA}\left(\frac{1}{0.1} - 1\right)$$

INPUT RESISTANCE

The input resistance of the amplifier is another error source that must be considered. Input resistance typically has two components: differential and common mode. The differential input resistance is suppressed by the negative feedback of the circuit. The ADA4530-1 has enough gain that the differential input resistance is much too large to measure. The common-mode input resistance (hereafter referred to as input resistance) is a more important error source.

The input resistance is equal to the change in input bias current relative to the change in input voltage. This change is not caused by a physical resistance inside the ADA4530-1; it is the result of a complex relationship between the accuracy of the guard voltage across the ESD structures and the input common-mode voltage; that is, the input resistance changes with common mode voltage. It is also possible for the input resistance to be negative. Negative input resistance means the input bias current decreases as the common-mode voltage increases.

The input resistance, R_{IN}, can be approximated by calculating the slope of the input bias current vs. common-mode voltage graphs (see Figure 22 to Figure 33). For example, the noninverting input resistance can be calculated at 125°C from Figure 32. Note that the input bias current changes by approximately 20 fA for common-mode voltages from 4 V to 6 V.

$$R_{IN} = \frac{\Delta V_{CM}}{\Delta I_{B+}}$$

$$R_{IN} = \frac{2\text{ V}}{20\text{ fA}} = 100\text{ T}\Omega$$

The slope of the curves in the input bias current vs. common-mode voltage graphs increases rapidly outside the preferred common-mode range (see Figure 22 to Figure 33). The input resistance drops rapidly outside this range. This drop in input resistance must be considered before operating these circuits with input voltages close to the V− power supply.

Like the input bias current, the input resistance has a strong temperature dependence. At lower temperatures, the amplifier input resistance is so high that it is dominated by other error sources. It is important to recognize the limitations of calculating input resistance at lower temperatures. Measurement uncertainties make it difficult to accurately calculate the ΔI_B term. Consider the 85°C input bias current vs. common-mode voltage graphs (see Figure 22 to Figure 27); the measurement uncertainties are equal to a few fA, which is the same magnitude as the input bias current itself. These uncertainties make it impossible to calculate input resistances higher than a few hundred teraohms.

The input resistance affects the buffer circuit by loading down the voltage sensor. This resistance acts as a voltage divider so the voltage measured by the amplifier is some fraction of the unloaded voltage of the sensor. This voltage drop is calculated as follows:

$$V_A = V_{SRC}\frac{R_{IN}}{R_{IN} + R_{SRC}}$$

Consider the previous example of a 100 GΩ sensor operating at 125°C. The 100 TΩ input resistance causes the measured voltage to equal 99.9% of the actual voltage, a 0.1% gain error.

The input resistance has much less of an effect on the TIA circuit. The input common-mode voltage does not change in this circuit; therefore, the error created is vanishingly small. The input resistance affects the noise gain of the circuit, which changes the input offset voltage error (see the Photodiode Interface section for more information).

INPUT OFFSET VOLTAGE

The input offset voltage of the amplifier affects the buffer circuit by adding directly to the voltage output of the sensor. This error is typically much smaller than other errors.

The input offset voltage affects the TIA circuit in a different manner. The burden voltage of the TIA is equal to the input offset voltage. This burden voltage appears between the A and B terminals. An error current is created by applying this burden voltage across the sensor shunt resistance. For sensors with low output resistances such as photodiodes, this error can be significant. Consider a sensor with a 1 GΩ output resistance. The 50 µV maximum offset voltage of the ADA4530-1 creates a 50 fA error current.

INSULATION RESISTANCE

The ADA4530-1 has such low input bias current and such high input resistance that the insulation resistance of the materials that are used to construct the circuit is often the largest error source. Any insulators with finite resistance that come in contact with the high impedance conductor contribute to the error current. Some examples include the printed circuit board (PCB) laminate material, cable, and connector insulation.

The physical insulation resistance is distributed across the entire contact surface of the high impedance conductor, and it may end at several different conductors at different potentials. It is useful to make a simple model where all of these resistance paths are lumped into a single resistor. This lumped element is shown as R_{SHUNT} in the voltage buffer circuit (see Figure 105).

The insulation resistance affects the buffer circuit in the same way as the amplifier input resistance. This resistance acts as a voltage divider so that the voltage measured by the amplifier is some fraction of the unloaded voltage of the sensor. This error is significant because it is very difficult to maintain high

insulation resistance values in glass epoxy (such as FR-4) PCB materials. Resistance values of 10 TΩ to 100 TΩ are achievable. A 10 TΩ insulation resistance creates a 1% error with the 100 GΩ sensor used in previous examples. Insulation resistance does not have an exponential temperature dependence like the amplifier errors previously discussed in the Input Bias Current section and the Input Resistance section, which makes insulation resistance the dominate error source at lower temperatures (less than 70°C).

The effect on the insulation resistance on the TIA circuit depends on the leakage path. The insulation resistance between the A terminal and B terminal of the current sensor affects the circuit in the same way as the amplifier input resistance. This error is extremely small because the voltage across the insulation is equal to the offset voltage of the amplifier. A much more significant error is created from insulation paths to conductors with significantly different potentials. This type of leakage path is shown as lumped element, R_{SHUNT}, in the TIA circuit (see Figure 106). In this example, the leakage path is created from the positive supply voltage (V+) to the A terminal. If the positive supply voltage is 5 V relative to signal ground, 500 fA flows through the insulation resistance of 10 TΩ. This large error dominates the amplifier input bias current and input resistance errors over the entire temperature range.

Leakage paths to high voltages can also affect the buffer circuit with equally ruinous results.

GUARDING

High source impedances and low error requirements can create insulation resistance requirements that are unrealistically high. Fortunately, a technique called guarding can reduce these requirements to a reasonable level. The concept of guarding is to surround the high impedance conductor with another conductor (guard) that is driven to the same voltage potential. If there is no voltage across the insulation resistance (between high impedance conductor and guard), there cannot be any current flowing through it.

The ADA4530-1 uses guarding techniques internally, and it has a very high performance guard buffer integrated. The output of this buffer is made available externally to simplify the implementation of guarding at the circuit level.

The voltage buffer circuit (see Figure 105) has been modified to show the implementation of the guard (see Figure 107). In this model, a conductor (V_{GRD}) is added, and it completely separates the high impedance (A) node from the low impedance (B) node at a different voltage. The insulation resistance is modeled as two resistances: all of the insulation between the A conductor and the guard conductor (R_{SHUNT1}), and all of the insulation between the guard conductor and the B conductor (R_{SHUNT2}). The ADA4530-1 guard buffer then drives this guard conductor (through Pin 2 and Pin 7) to the A terminal voltage. If the A node and V_{GRD} node are exactly the same voltage, no current flows through the insulation resistance, R_{SHUNT1}.

In practice, the voltage across R_{SHUNT1} cannot be 0 V, the guard buffer offset voltage contributes to the difference in voltage potential between the A node and V_{GRD} node. For the ADA4530-1, this offset voltage is trimmed to provide offsets less than 100 µV when the input common-mode voltage is 1.5 V from the supply rails. The guard buffer offset voltage and drift are specified in Table 1, Table 2, and Table 3.

For example, assume that the voltage sensor produces an output of 1 V. Without guarding, the 10 TΩ insulation resistance creates an error current of 100 fA. With the guard, the voltage across the insulation resistance is limited to 100 µV. The guard limits the error current to 0.01 fA. In this example, the guard reduces the error by a factor of 10^4 to an insignificant level.

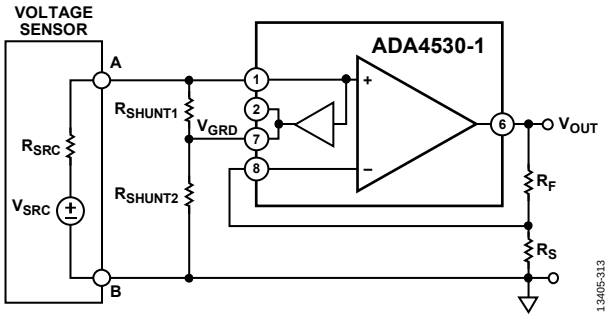


Figure 107. Voltage Buffer Circuit with Guard

DIELECTRIC RELAXATION

Dielectric relaxation (also known as dielectric absorption or soakage) is a property of all insulating materials that can limit the performance of electrometer circuits that need to settle to a few femtoamperes.

Dielectric relaxation is the delay in polarization of the dielectric molecules in response to a changing electric field. This delay is a property of all insulating materials. The magnitude and the time constant of the delay depend on the specific dielectric material. The delays in some materials can be minutes or even hours.

Dielectric relaxation is a problem for electrometer circuits because small displacement currents flow through the insulator in response to the polarization of the molecules. Delays in polarization cause delays in the dissipation of these currents, which can dominate the settling time in these circuits.

In the context of capacitors, dielectric relaxation is called dielectric absorption. Capacitors are specified with a test that measures the residual open-circuit voltage after a specific charge/discharge cycle. For electrometer circuits, it is more useful to consider the short-circuit currents produced from step changes in a test voltage.

A simple lumped circuit model of an insulator is connected to the test voltage source (see Figure 108). The majority of the dielectric polarizes instantly; this is modeled as Capacitor C1. A small percentage of the dielectric polarizes slowly with a time constant of τ2, modeled as Capacitor C2 and Resistor R2.

The size of C2 reflects the proportion of slow molecules. The size depends on the material but it is typically 100 to 10,000 times smaller than C1. The size of R2 sets the time constant.

$$\tau 2 = R2 \times C2$$

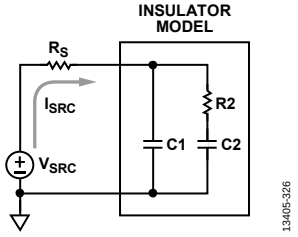


Figure 108. Dielectric Relaxation Model Test Circuit

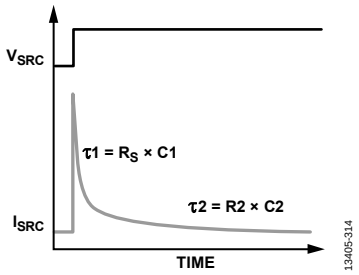


Figure 109. Step Response of Dielectric Relaxation Model

The current step response (I_{SRC}) of the insulator to a voltage step is shown in Figure 108. A large initial current charges Capacitor C1 with a fast time constant. This time constant, τ1, equals the source resistance $R_S \times C1$ (see Figure 109). Long after Capacitor C1 is charged, a much smaller current continues to flow, which charges Capacitor C2. The time constant of charging is not affected by the external circuitry; it depends only on the material properties of the insulator. The magnitude of the current depends on the magnitude of the voltage change across the insulator.

The dielectric relaxation performance was measured for a variety of PCB laminates using the test circuit in Figure 108. An electrometer grade source measurement unit (SMU), Keithley 6430, applies a ±100 V test stimulus and measures the resulting current. The large alternating polarity test voltage distinguishes the small dielectric relaxation current from the input offset current of the SMU.

The first PCB laminate tested is the industry-standard FR-4 glass epoxy. The measurement results are shown in Figure 110. The glass epoxy laminate requires 1 hour to dissipate the dielectric relaxation current to less than 10 fA. This result shows that glass epoxy laminates are unsuitable for the highest performance electrometer circuits.

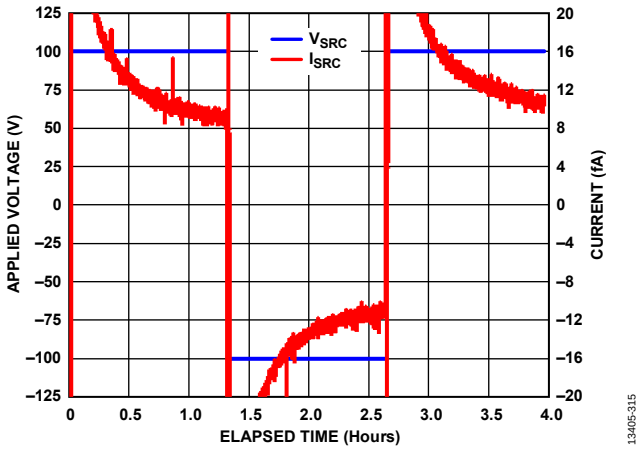


Figure 110. Glass Epoxy Dielectric Relaxation Performance

An alternative PCB laminate to consider is Rogers 4350B. Rogers 4350B is a ceramic laminate designed for RF/microwave circuits. Rogers 4350B is compatible with standard PCB production techniques and is widely available. The measurement results for the Rogers 4350B material are shown in Figure 111. This material requires less than 20 sec to dissipate the dielectric relaxation current to less than 1 fA.

Based on its superior performance, it is recommended to use Rogers 4350B laminates with the ADA4530-1 in the highest performance applications. All of the critical characterization measurements of the ADA4530-1 are taken using Rogers 4350B.

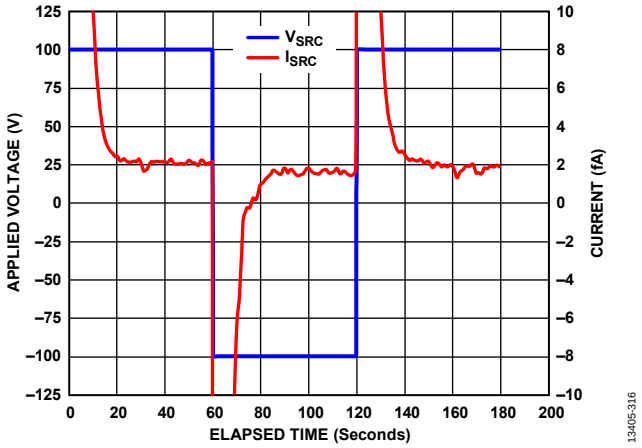


Figure 111. Rogers 4350B Dielectric Relaxation Performance

HUMIDITY EFFECTS

The insulation resistance of the materials used to construct circuits is sensitive to moisture. At lower temperatures (<70°C) the insulation resistance creates more significant leakage current errors than the amplifier itself. This means that the relative humidity of the air is the most important error source at lower temperatures. The dependence on humidity is evident in the input bias current vs. temperature graphs (see Figure 34 to Figure 36). There is significant deviation in the low temperature measurements due to the difficulty maintaining a consistently low relative humidity at low temperatures.

To evaluate the humidity sensitivity of insulation resistance, there are two mechanisms which must be considered: adsorption and absorption.

Adsorption is a process where thin films of molecules adhere to the surface of a material. Water molecules are subject to this process. The magnitude of the effect depends on the insulating material and the relative humidity. Thin films of moisture are conductive, and they act as leakage resistances in parallel with the insulation resistance of the material. Because this is a surface effect, guard ring techniques are effective at reducing it.

Absorption is a process where molecules enter the bulk of a material. Water molecules can diffuse into a material and affect the bulk conductivity of that material. Because the leakage paths are through the bulk of the material, guard rings are not effective at reducing it.

It is not possible to completely guard all the leakage paths: bulk or surface. A relevant example of this limitation is the molding compound of the SOIC package housing the ADA4530-1. Surface and bulk paths exist from the input pins to all other pins of the package. The nature of the resulting current depends on the specific leakage path: paths to V+ increase the bias current flowing out of the amplifier, paths to V− increase the bias current flowing into the amplifier, and paths to V_{OUT} lower the effective feedback resistance in TIA circuits.

Consider the example of a circuit powered from ±5 V power supplies with an input common-mode voltage of 0 V. Assume that all of the leakage resistance between the input and V+ is effectively 100 TΩ. This resistance creates a current equal to 50 fA flowing from V+. Assume that the leakage resistance between the input and V− is effectively 250 TΩ. This resistance creates a current equal to 20 fA flowing to V−. The net current equals −30 fA flowing out of the input pin.

All of these leakage currents can be combined with the amplifier input bias current and treated as an effective input bias current. The effective input bias current sensitivity to relative humidity of the ADA4530-1 is characterized for several units. The test amplifiers are configured in TIA and unity buffer circuits with 100 GΩ, hermetically sealed resistors (RX-1M1009FE) as the feedback and source resistors, respectively. These glass bodied resistors have a silicone coating (glass has poor humidity adsorption properties). The ADA4530-1 amplifiers are mounted on Rogers 4350B PCBs (glass epoxy boards have poor humidity absorption properties).

Figure 112 shows the effective input bias current vs. relative humidity for seven characterization units. Figure 112 is plotted with a split log axis to effectively show the magnitude and polarity of the bias current. The magnitude of the leakage currents changes by more than factor of 100 across the relative humidity span from 5% to 80%. The effective bias current is much less than 1 fA for typical conditioned environments (RH < 50%).

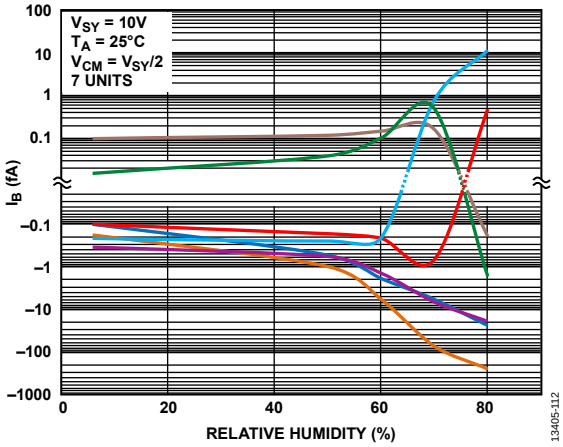


Figure 112. Effective Input Bias Current vs. Relative Humidity

The magnitude of the effective input bias current becomes very sensitive to the relative humidity at higher humidity levels (>60%). Some of the units show an exponential dependence on humidity (see the blue curve in Figure 112). Other units show a less predictable dependence; the leakage current magnitude increases rapidly, but the polarity can change. The net leakage current is the sum of the currents sourced from higher voltages (like V+) with the currents sunk by lower voltages (like V−). As the humidity changes, the relative magnitudes of each of these leakage paths can change, which can result in changes in the polarity of the leakage current (see the red and green curves in Figure 112).

The response time of these leakage currents depends on the physical process that causes them. Because adsorption is a surface effect, the film thickness rapidly achieves equilibrium with changes in the relative humidity of the air. Because absorption is a bulk diffusion process, it is very slow compared to the adsorption process.

These widely different time constants mean that the effective input bias current responds quickly to a step change in relative humidity, but has a very long settling time. The step response of one amplifier to a 50% to 60% relative humidity change is shown in Figure 113. The high frequency response of the initial humidity step (and the overshoot recovery) is on the order of seconds to tens of seconds. Complete settling takes over a week as the moisture slowly diffuses through the PCB insulation and package molding compound. Note that each data point in Figure 112 was taken after one week of settling time.

In practical applications, the relative humidity of the air changes rapidly with daily and seasonal variations. The effective input bias current response to these humidity changes has two parts. The response due to the adsorption process follows the rapid changes immediately. The response due to the absorption process low-pass filters the humidity changes. This low-pass response causes the effective input bias current to have long-term memory of the relative humidity fluctuations.

In this environment, measurements of the effective input bias current appear to drift with time because the leakage currents depend on the relative humidity for the previous week. This long-term memory due to the absorption process may need to be taken in account in certain circumstances (that is, long-term product storage in an unconditioned high humidity environment prior to use).

The rapid adsorption response can change the effective bias current in response to local fluctuations in humidity. These current fluctuations can be much larger than the low frequency current noise of the amplifier and thermal noise of the resistors. The sensitive circuitry can be isolated from these local humidity fluctuations by restricting the airflow around the circuitry with an air baffle. Electrostatic shielding added to reduce interference can also function as an air baffle. Remove or reduce the sources of humidity fluctuations whenever possible. Avoid breathing on the high impedance circuitry, for example.

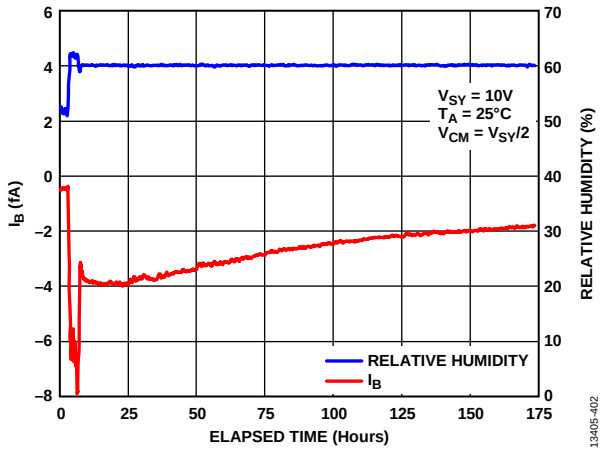


Figure 113. Effective Input Bias Current Transient Response to Humidity Step

It is important to note that all electrometer circuits are subject to humidity effects. The legacy circuits constructed with TO-99 packages using air wiring techniques have insulator leakage paths such as the epoxy between the pins and the Teflon® standoffs used to support the air wired components. The input bias currents of legacy amplifiers are high enough to mask the humidity effects.

In summary, the ADA4530-1 can be designed using the specified performance for normal laboratory (<60%) relative humidity conditions. In applications that must operate in uncontrolled or high humidity environments, some additional derating of the input bias current is prudent. Characterize the amount of derating on a per product basis because the net leakage depends on the material types and physical dimensions of the insulators.

CONTAMINATION

The effective insulation resistance of an electrometer circuit can be substantially degraded if the insulators are contaminated. Solder flux, body oils, dust, and dirt are all possible sources of contamination. Some of these contaminants form a parallel leakage path across the surface of the existing insulator effectively lowering the insulation resistance. Guarding techniques help to suppress these effects.

The effects are more severe when the source of contamination contains ionic compounds. In the presence of humidity, these contaminates act as an electrolyte, which can form a weak battery. Flux residue and body oils are particularly effective at creating these parasitic batteries.

As an example, the PCB insulation between two high impedance nodes was purposefully contaminated with a 3 mm drop of rosin mildly activated (RMA) type solder flux. This sample was dried and allowed to stabilize in laboratory conditions (25°C, 40% RH) for several days. After this time, the voltage vs. current relationship was measured with an electrometer grade SMU (see Figure 114).

This contamination formed a weak battery with an open circuit voltage (V_{BATT}) of 15 mV and an output resistance (R_{BATT}) of 300 GΩ. This sort of contamination is disastrous in electrometer circuits because guarding techniques cannot suppress it. A simplified model is made with the contamination battery applied across the A terminal and B terminal of a TIA circuit (see Figure 115). The A terminal and B terminal are both driven to the same voltage, which creates an error current (I_{BATT}) because the open circuit battery voltage is dropped across the output resistance as follows:

$$I_{BATT} = V_{BATT} \div R_{BATT}$$

All of this battery current flows through the feedback resistance, where it is summed with the signal and other error currents in the circuit. The error current in this example is 50 fA. The battery characteristics are subject to the environmental conditions; therefore, the error current drifts with time, temperature, and humidity.

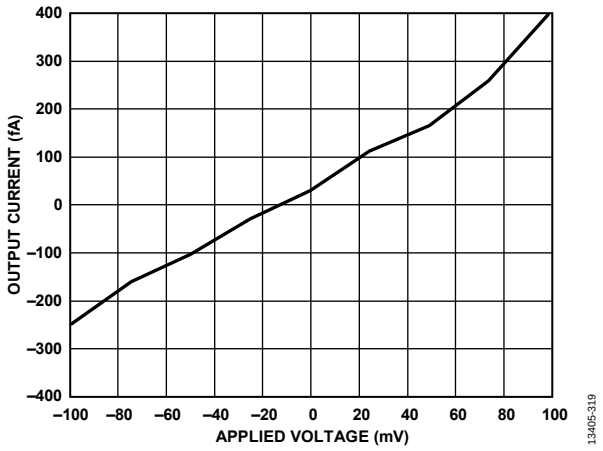


Figure 114. Current to Voltage Response of RMA Contaminated Insulation

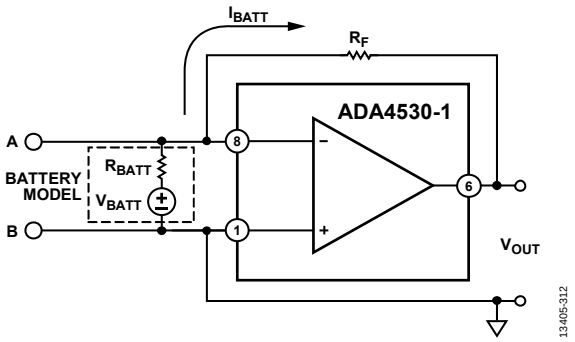


Figure 115. TIA Circuit with Contamination Battery

CLEANING AND HANDLING

The contamination described in the Contamination section can usually be removed by an appropriate cleaning process. Solvents like isopropyl alcohol (IPA) are effective at removing the residue from solder fluxes and body oils. Use high purity cleanroom grade solvents to ensure that there is no additional contamination from the solvent itself.

Insulators that are severely contaminated benefit from mechanical abrasion in addition to the solvent. Ultrasonic cleaners are highly effective. Scrubbing the area around the high impedance insulators with an acid brush also works. Flush the insulators with a final wash of fresh IPA to remove any contaminants suspended in the solvent.

The residual moisture must be allowed to completely evaporate before the insulator can be used. This evaporation may take many hours at room temperature; the process can be accelerated by baking the insulators in an oven at elevated temperature.

For detailed cleaning and handling procedures, refer to the ADA4530-1R-EBZ User Guide.

SOLDER PASTE SELECTION

Solder paste selection can drastically impact the performance of the board if not cleaned properly. Solder flux residue on a PCB degrades the low I_B performance of the amplifier. An experiment was performed to evaluate the cleaning procedure for different solder paste types. Table 7 shows the result of the experiment. The recommended cleaning procedure column lists the times required to restore the effective input bias currents to less than 1 fA. The suggested solder paste of choice is the RMA type.

Table 7. Recommended Cleaning Procedures for Different Solder Paste Material

Solder Paste Type	Solder Paste Part Number	Recommended Cleaning Procedure[1]
RMA	AIM RMA258-15R	15 min clean time in an ultrasonic cleaner with fresh IPA, followed by 1.5 hours of bake time at 125°C
Water Soluble	SAC305 Shenmao	1.5 hours clean time in an ultrasonic cleaner with fresh IPA, followed by 1.5 hours of bake time at 125°C
No Clean	SAC 305 AMTECH LF4300	3 hours clean time in an ultrasonic cleaner with fresh IPA, followed by 3 hours of bake time at 125°C

[1] Bake time was not optimized and was set equal to the cleaning time.

CURRENT NOISE CONSIDERATIONS

The current noise from an amplifier input pin is important when it flows through an impedance and generates a voltage noise. If the current noise and impedance are large enough, the resulting voltage noise can dominate the other noise sources in the circuit such as the voltage noise of the resistors and amplifier. For an electrometer amplifier such as the ADA4530-1, the typical circuit impedances are so large that the current noise of the amplifier can be the most important noise source.

To measure current noise, it is necessary to flow the noise current through a test impedance large enough that the resulting noise voltage is larger than the other noise voltages in the circuit. Practically, this test impedance is usually a resistor. All resistors have their own thermal noise. The value of thermal noise is usually presented as an output referred voltage noise spectral density (NSD), V_{NRTO}.

$$V_{NRTO} = \sqrt{(4kTR)}$$

where:
k is Boltzmann's constant.
T is the temperature in Kelvin.
R is the resistance value.

The resistor thermal noise can be interpreted as a current NSD by dividing the thermal noise with the resistance value, R, per Ohm's Law.

Table 8 shows the thermal noise of a series of resistor values presented as both voltage and current noise. The current noise of a resistor decreases as the resistance increases. This surprising result illustrates that it is necessary to use high valued resistors to measure low levels of current noise.

Table 8. Resistor Thermal Noise

Resistor Value	Voltage Noise	Current Noise
1 MΩ	128 nV/√Hz	128 fA/√Hz
100 MΩ	1.28 µV/√Hz	12.8 fA/√Hz
10 GΩ	12.8 µV/√Hz	1.28 fA/√Hz
1 TΩ	128 µV/√Hz	128 aA/√Hz

The measurement setup used to gather the current noise data is shown in Figure 116. The ADA4530-1 is configured as a TIA with a large value feedback resistor, R_F. All amplifier current noise from the inverting input flows through Resistor R_F to produce a voltage noise at V_{OUT}.

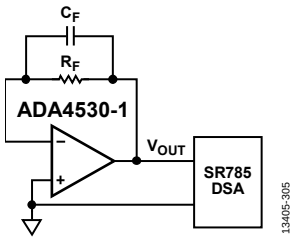


Figure 116. Current Noise Measurement Setup

The output referred voltage NSD, V_{NRTO}, is sampled by the SR785 high performance dynamic signal analyzer (DSA) and is equal to the root-sum-square of the amplifier current noise multiplied by R_F, the resistor thermal noise, and amplifier voltage noise.

$$V_{NRTO} = \sqrt{((I_{N-}R_F)^2 + 4kTR_F + V_N^2)}$$

where:
I_{N-} is the amplifier inverting current noise.
$4kTR_F$ is the resistor thermal noise.
V_N^2 is the amplifier voltage noise.

Calculate the current noise of the amplifier from V_{NRTO} as follows:

$$I_{N-} = \sqrt{\frac{V_{NRTO}^2 - 4kTR_F - V_N^2}{R_F}} \quad (1)$$

For Equation 1 to be valid, the measured noise must be somewhat larger than the resistor thermal noise plus the amplifier voltage noise. In practice, ensure that the resistor current noise is less than or equal to the amplifier current noise. For example, if the amplifier noise is expected to be 2 fA/√Hz, use a value of R_F that is at least 10 GΩ, according to Table 8.

The amplifier voltage noise is not a concern at most frequencies because the resistor thermal noise is much larger than the amplifier voltage noise. At very low frequencies, this assumption is not valid due to the 1/f characteristic of the amplifier voltage noise.

It is important to consider the bandwidth limitations of the current noise measurement system shown in Figure 116. The presence of stray capacitance makes it impossible to maintain the high impedances required for the measurement. All stray capacitance that couple the amplifier output to the inverting input can be lumped into a single capacitor, C_F, as shown in Figure 116.

The current noise must pass through R_F to become voltage noise. However, in practice, the current noise passes through the parallel combination of R_F and C_F to become voltage noise. At frequencies higher than the R_FC_F pole, most of the noise current flows through the capacitor and current noise calculations at these frequencies are error prone due to the distributed parasitic nature of C_F. A good guideline is to set the measurement bandwidth limit equal to the R_FC_F pole frequency.

The measurement bandwidth limitations for high valued resistors can be surprisingly low. Table 9 shows the −3 dB bandwidth of a series of resistor values with a practical minimum stray capacitance value.

Table 9. Bandwidth Limitations

Resistor Value	Capacitor Value	−3 dB Bandwidth
1 MΩ	100 fF	1.59 MHz
100 MΩ	100 fF	15.9 kHz
10 GΩ	100 fF	159 Hz
1 TΩ	100 fF	1.59 Hz

Reconsider the example amplifier with 2 fA/√Hz of current noise. The required R_F value of 10 GΩ also limits the measurement bandwidth to 159 Hz according to Table 9.

It is useful to construct a table that combines the resistor noise and measurement bandwidth guidelines. Table 10 shows the approximate bandwidth limitations for a variety of input current noise measurements.

Table 10. Measurement Current Noise Density vs. Bandwidth

Current Noise Density	Bandwidth
128 aA/√Hz	1.59 Hz
1.28 fA/√Hz	159 Hz
12.8 fA/√Hz	15.9 kHz
128 fA/√Hz	1.59 MHz

Table 10 demonstrates the error of the often claimed 0.1 fA/√Hz at 10 kHz presented in the specifications of low input bias current amplifiers. Measuring this value requires a 1 TΩ resistor with less than 15.9 aF (15.9×10^{-18} F) of stray capacitance, which is impossible.

These kinds of claims are simply shot noise calculations based on the specified input bias currents of a few tens of femtoamperes. Calculate the shot noise of a semiconductor as follows:

$$Shot\ Noise = \sqrt{(2qI_B)}$$

where:
q is the charge on an electron.
I_B is the current flowing through a junction.

Shot noise calculations are appropriate only for some legacy JFET-based electrometer amplifiers, where only a single junction is connected to the amplifier input pins. Modern high impedance amplifiers have several semiconductor junctions connected to the amplifier input pins. The most significant of these junctions are the ESD diode structures. The input bias currents are equal to the sum of these diode currents. The diode currents are designed to cancel each other, but the shot noise currents are uncorrelated and cannot cancel, which, in turn, makes calculating the shot noise from the input bias current impossible.

Even when appropriate, these shot noise calculations neglect all capacitive coupling effects so that they are valid only at very low frequencies. The gate to source capacitance of the input transistors couples noise currents from sources other than the input junctions for frequencies above a few tens of hertz. This blowback noise effect is present in all amplifiers, and it ensures that the current NSD always increases as frequency increases.

The complex relationship between current noise, feedback resistance, and bandwidth means that the proper way to characterize the current noise of an electrometer amplifier is by measuring the output NSD with a variety of feedback resistors that cover the entire span of values used in the end applications. Each feedback resistor establishes a boundary for the minimum measurable current noise over a range of frequencies.

It is critically important to use high quality resistors during this measurement. Many high valued resistors designed for high voltage operation are nonlinear at low voltage levels and are not suitable for electrometer work. Inferior resistors may also have their own 1/f noise that corrupts the measurement results. Table 11 lists the resistors used for the characterization of the ADA4530-1.

Table 11. Test Resistor Device Numbers

Resistor Value	Manufacturer	Device Number
100 MΩ	Vishay	RNX050100MDHLB
1 GΩ	Ohmite	RX-1M1007GE
10 GΩ	Ohmite	RX-1M1008JE
100 GΩ	Ohmite	RX-1M1009FE
1 TΩ	Ohmite	RX-1M100AKE

Figure 117 shows the output referred voltage NSD (V_{NRTO}) of the transimpedance test circuit for the test resistors listed in Table 11. The calculated thermal noise for each resistor is represented with the dashed line. The black dashed line represents the 1/f voltage noise of the amplifier.

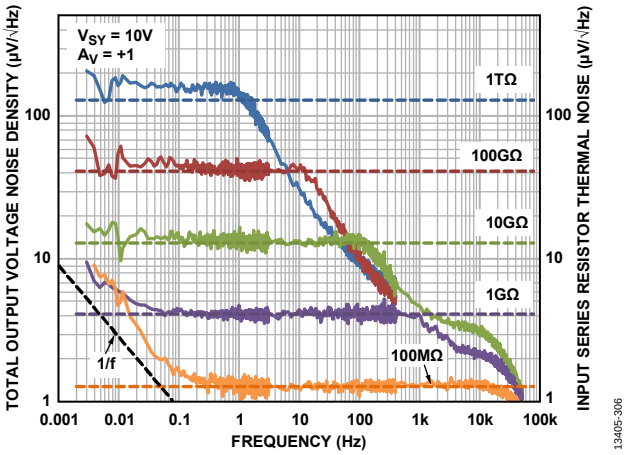


Figure 117. Transimpedance NSD Referred to Output

V_{NRTO} is dominated by the resistor noise for all of the test resistors up 1 TΩ. This means that the current noise contribution from the ADA4530-1 is insignificant relative to the thermal noise of these resistors.

It is possible to calculate the current noise of the ADA4530-1 with the 1 TΩ resistor. This result is shown in Figure 118. It is impossible to calculate the amplifier current noise for all of the other resistors. The most that can be said is that the amplifier current noise is much less than the resistor noise. The current noise densities of each of the test resistors are plotted as dashed lines in Figure 118. The current noise of the ADA4530-1 is below the resistor noise values.

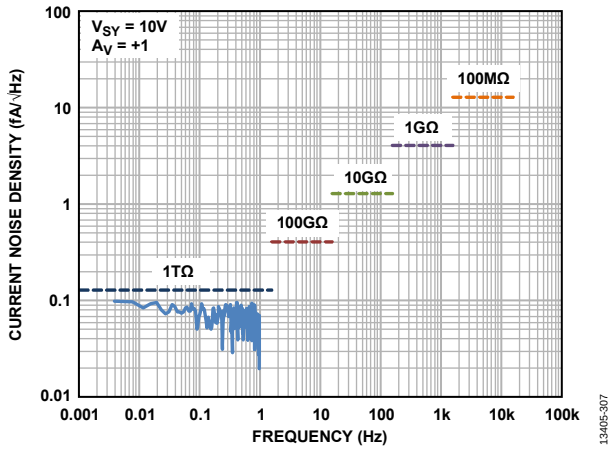


Figure 118. Current Noise Spectral Density

The current noise of the ADA4530-1 originates from the saturation current of the ESD diodes. The diode saturation current has an exponential dependence on temperature; therefore, it is expected that the current noise tracks this temperature behavior. The current noise of the ADA4530-1 is characterized over temperature using the transimpedance measurement circuit with a 1 TΩ resistor. The measurements are limited to 85°C because of the maximum operating temperature of the resistor. Figure 119 shows the current noise density at a frequency of 0.1 Hz for all of the test temperatures.

It can be useful to calculate an equivalent noise resistance from the current noise density data in Figure 119. This conversion facilitates comparisons between the current noise generated by the ADA4530-1 and the thermal noise of the feedback resistor used in the circuit.

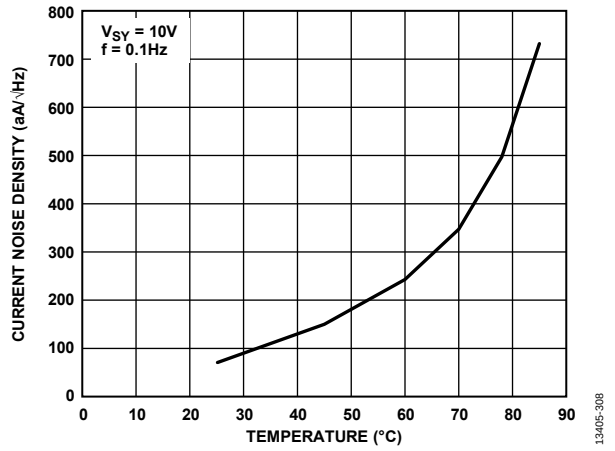


Figure 119. Current Noise Density vs. Temperature

Figure 120 shows the equivalent noise resistance vs. temperature. From Figure 120, it is simple to determine that the ADA4530-1 contributes less noise than a 1 TΩ resistor for temperatures less than 40°C. If the application requires 85°C operation, the ADA4530-1 contributes as much noise as a 30 GΩ resistor. This example illustrates the considerable impact that temperature plays in determining the noise performance of an application.

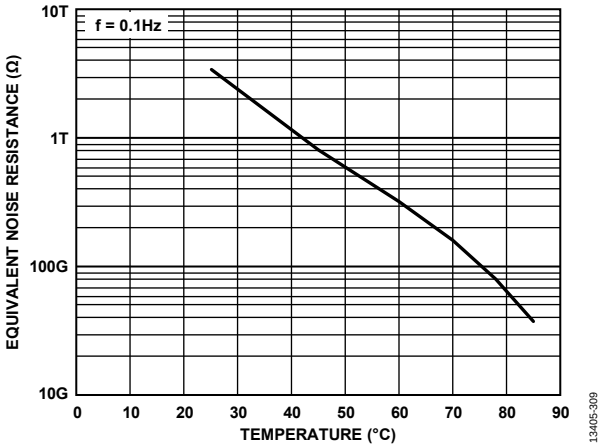


Figure 120. Equivalent Noise Resistance vs. Temperature

In summary, the excellent noise performance of the ADA4530-1 makes it ideal for electrometer applications. For impedances less than 1 TΩ, the amplifier noise is negligible. Also, unlike other amplifiers, the current noise has been fully characterized and is free of excessive blowback noise.

LAYOUT GUIDELINES

PHYSICAL IMPLEMENTATION OF GUARDING TECHNIQUES

In the Guarding section, guarding was introduced as a technique fundamental to high impedance work. The goal of guarding is to completely surround the insulation of high impedance node with another conductor that is driven to the guard voltage. This ideal is impossible to achieve in practice; however, there are several practical structures that provide good performance.

GUARD RING

A guard ring is a structure typically used to implement the guarding technique on the surface of the PCB. A simplified layout of the buffer circuit implements the guard ring around the high impedance (A) trace (see Figure 121). The output of the voltage sensor is wired directly to the A and B pads in Figure 121. The guard ring is a filled copper shape that completely surrounds the high impedance (A) trace from the sensor connection to the noninverting input (Pin 1). The guard ring is driven directly from the ADA4530-1 guard buffer (Pin 2) through a thermal relief shape connection. It is not necessary to connect the other guard buffer output (Pin 7).

The solder mask was removed from the high impedance trace and the guard trace to ensure that the guard makes electrical contact with any surface leakage paths. For the same reason, avoid printing any silkscreen in this section.

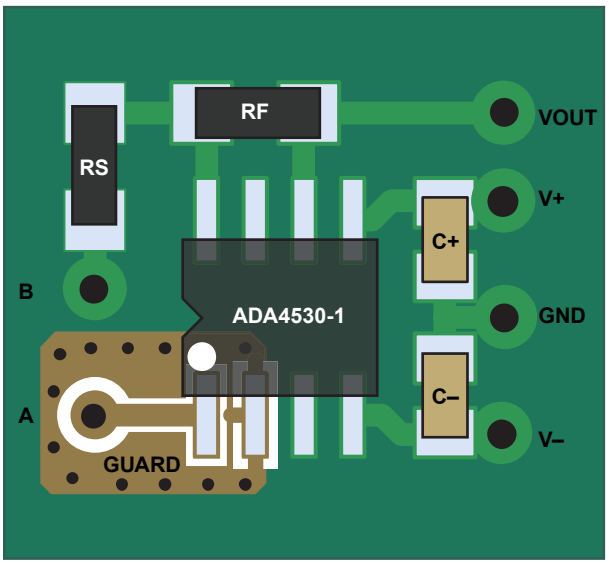


Figure 121. Buffer Circuit Layout

There is not a large amount of exposed insulation between the A trace and the guard ring. It is often counterproductive to increase this spacing to try to increase the insulation resistance because the exposed insulator tends to accumulate surface charges generated from piezoelectric or triboelectric effects. These charges are eventually swept across the insulator toward the high impedance conductor. The magnitude of this error current is dependent on the area of the exposed high impedance insulation. A gap of 15 mil between the A trace and the guard ring is sufficient.

Another simplified layout demonstrates the implementation of a guard ring in the TIA circuit (see Figure 122). The guard ring is implemented in the same manner as the buffer circuit. The primary difference is that the left half of the feedback resistor (RF) and feedback capacitor (CF) are connected to the high impedance node. The guard ring shape is extended around these passive components to ensure that the entire high impedance node is surrounded by guard. The guard ring is directly driven from the ADA4530-1 guard buffer (Pin 7).

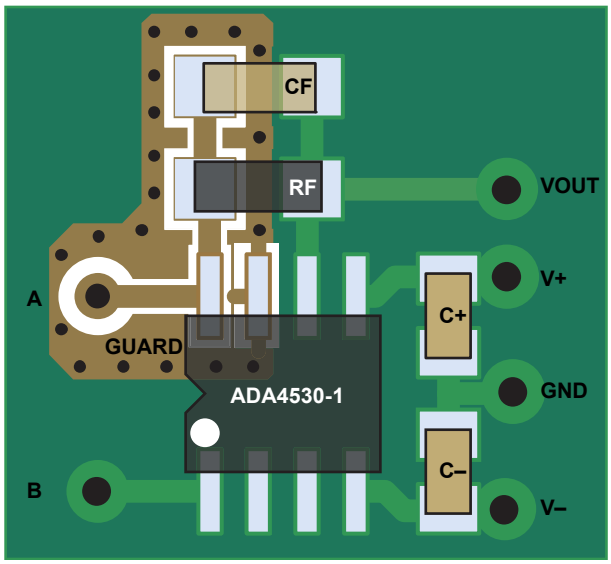


Figure 122. TIA Circuit Layout

The guard voltage in the TIA circuit is nominally equal to the B voltage, which makes it possible to drive the guard ring directly from the B voltage without using the ADA4530-1 guard buffer. When implementing the guard ring this way, do not make any connection to the guard buffer outputs (Pin 2 and Pin 7).

GUARD PLANE

A guard plane is a structure used to implement the guarding technique through the bulk of the PCB. The structure of the guard plane is shown in a cross section of the PCB (see Figure 123). The guard plane is a filled copper shape that is placed directly below the high impedance (A) trace. This plane is connected to the guard ring on the surface layer with vias.

If the circuit board is constructed using high performance PCB laminates such as Rogers 4350B, a hybrid stackup is required for mechanical strength. The outside layers are ceramic, whereas the core layers are conventional glass epoxy laminate. It is important to place the guard shield on the boundary of the ceramic and glass epoxy materials to protect the high impedance node from the poor dielectric relaxation characteristics of the glass epoxy materials.

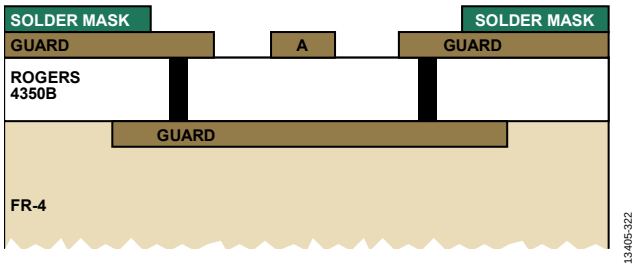


Figure 123. Layout Cross Section with Guard Plane

VIA FENCE

A via fence is an additional structure that guards the lateral leakage paths in the laminate between the guard ring and the guard plane (see Figure 123). The fence is implemented by surrounding the entire guard ring with vias that connect the guard ring to the guard plane (see Figure 121 and Figure 122).

CABLES AND CONNECTORS

Guarding techniques are required for all of high impedance wiring; not just on the PCB. Frequently, the high impedance sensor is not directly mounted on the PCB with the electrometer amplifier and external cables are used to make the connection.

The typical way to guard a cable connecting to a current output sensor is by using a coaxial cable. A coaxial cable consists of an inner conductor surrounded with insulation, which is, in turn, surrounded by a braided conductor. Use the inner conductor for the high impedance (A) terminal and the outer braided shield conductor for the low impedance (B) terminal. Conveniently, this arrangement effectively guards the coaxial insulation resistance because the A terminal and B terminal are nominally at the same voltage (when attached to a TIA interface circuit).

Voltage output sensors are more problematic because the A terminal and B terminal are not at the same voltage. The typical way to guard the voltage output sensor cable is to use triaxial cable. Triaxial cable is constructed with an inner conductor with two separate braided conductors. Each of these braided conductors is separated from each other with insulation. Use the inner conductor for the high impedance (A) terminal and the inner braided conductor for the guard (V_{GRD}) connection, and use the outer braided conductor for the low impedance (B) terminal. All the insulation around the inner conductor is completely surrounded by the guard conductor, which keeps the voltage drop across this insulation equal to zero.

ELECTROSTATIC INTERFERANCE

Very high impedance electrometer circuits are susceptible to interference through capacitive coupling. The amount of capacitance required to couple low frequency signals is surprisingly small. For example, line frequency (60 Hz) interference is coupled (with a −3 dB loss) to a 1 TΩ impedance with only 3 fF of coupling capacitance.

Traditional electrical interferers are not the only sources of concern. Calculate the displacement current, I, in a capacitor as follows:

$$I = C\frac{\partial V}{\partial t} + V\frac{\partial C}{\partial t} \quad (2)$$

The second term in this equation is frequently ignored in most circuits, but it can generate some unusual problems in electrometer circuits. The problem is that the movement of any charged object changes the coupling capacitance between the object and the electrometer, and this change in capacitance injects small currents into the circuit. The ADA4530-1 is so sensitive that it easily detects the movement of a hand or the movement of a piece of paper. These types of effects are not periodic or predictable, and they can appear as erratic dc shifts on the time scales of interest.

Both of these types of interference can be reduced by the addition of a shield. A shield is a piece of conductive material placed between the high impedance input and the interference source. This shield must be electrically connected to a low impedance source (such as signal ground). If the shield physically interrupts all of the capacitive coupling paths, all of the displacement current from the interference source is shunted to the low impedance source.

Notice that the construction of a shield is almost the same as the construction of a guard. Because of this similarity, many guard structures also provide shielding as well. The primary difference is that the dc voltage of the shield is not important, whereas the guard must have a voltage equal to that of the high impedance input. Shields that are driven by the guard buffer have the added benefit of bootstrapping the capacitance between the high impedance input and the shield. The disadvantage of this approach is that the guard buffer output impedance is 1 kΩ, which makes the shield less effective than a signal ground or a chassis ground connection. The most effective systems typically use the box within a box construction: the outer shield is driven with ground and the inner shield is driven with guard.

There is another capacitive interference effect that typically cannot be shielded. This displacement current is generated from a change in capacitance with respect to time (the second term of Equation 2). This change is due to the mechanical movement of the circuit components. This movement, which can be caused by mechanical impact or vibration, generates electrical interference. This interference typically appears at unexpected frequencies that are equal to the mechanical resonances of the components.

This effect must be considered when using traditional air wiring techniques for large feedback resistors or relays. It is important to ensure solid mechanical connections to Teflon standoffs for this type of construction.

PHOTODIODE INTERFACE

The low input bias current and low input offset voltage makes the ADA4530-1 an excellent choice for signal conditioning photodiodes at extremely low illumination levels. Figure 124 shows the ADA4530-1 configured in a transimpedance amplifier interfacing with a photodiode operating in photovoltaic mode (photodiode is zero biased). A photodiode produces an output current proportional to the illumination level. The amplifier converts the signal current, I_{PD}, into an output voltage with the following equation:

$$V_{OUT} = I_{PD} \times R_F$$

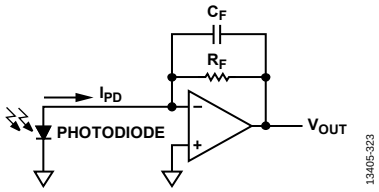


Figure 124. Transimpedance Amplifier with Photodiode

Figure 125 replaces the photodiode with an equivalent circuit model. I_{PD} is the photo current generated by incident light and is proportional to the light level. The shunt capacitance (C_{SHUNT}) models the depletion capacitance of the diode. This capacitance depends on the area of the photodiode and the voltage bias. The shunt resistance (R_{SHUNT}) represents the voltage vs. current slope of the exponential diode curve near zero bias voltage.

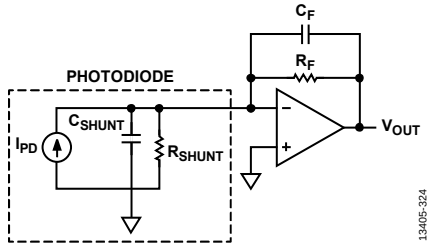


Figure 125. Transimpedance Amplifier with Photodiode Model

DC ERROR ANALYSIS

All of the errors described in the High Impedance Measurements section related to TIA circuits are applicable to photodiode interfaces.

The inverting input bias current, I_{B-}, sums directly with the photodiode current for a referred to input (RTI) error equal to I_{B-}. This current flows through the feedback resistor, creating a referred to output (RTO) error equal to

$$V_{IB_RTO} = I_{B-} \times R_F$$

The amplifier offset voltage, V_{OS}, is a major error source in photodiode interface circuits because of the relatively low shunt resistance of large area photodiodes. Typical values are in the range of 1 GΩ to100 GΩ at 25°C. More importantly, the shunt resistance decreases by half for every 10°C increase in temperature. An error current is created because the amplifier offset voltage is applied across this shunt resistance, resulting in an RTI error equal to

$$I_{VOS_RTI} = V_{OS}/R_{SHUNT}$$

It is equivalent to think that the shunt resistance increases the DC noise gain which multiplies the offset voltage to the output. The RTO error due to V_{OS} is equal to:

$$V_{OS_RTO} = V_{OS} \times Noise\ Gain$$

$$V_{OS_RTO} = V_{OS} \times (1 + R_F/R_{SHUNT})$$

The amplifier input resistance and insulation resistance appear in parallel with the photodiode shunt resistance. These additional resistances reduce the effective shunt resistance, but they are much larger than the photodiode shunt resistance and can usually be ignored.

AC ERROR ANALYSIS

Photodiode TIA circuits typically require external compensation to give satisfactory dynamic performance. The large feedback resistor (R_F) interacts with the large photodiode capacitance (C_{SHUNT}) to create a low frequency pole in the feedback network. Photodiode shunt capacitance, amplifier input capacitance, and trace capacitance are lumped into a single element, C_{SHUNT}. The phase shift due to this pole must be recovered prior to the crossover frequency for the feedback loop to be stable. The usual method to recover this phase shift is to create a zero in the feedback factor with the addition of the feedback capacitor (C_F).

The classic way of analyzing this circuit is by examining the noise gain vs. frequency (see Figure 126). At low frequencies, the noise gain is determined by the ratio of the feedback to the shunt resistance.

$$NG_1 = 1 + \frac{RF}{R_{SHUNT}}$$

The troublesome low frequency pole (which is a zero in the noise gain) occurs at Frequency f_1. From this frequency onward, the noise gain increases. If there is no feedback capacitor in the circuit, the noise gain follows the dotted line until it intersects with the amplifier open-loop gain curve. If these curves intersect at the 20 dB/decade slopes shown in Figure 126, the circuit is unstable.

The addition of C_F adds a zero to the feedback factor (which is a pole in the noise gain) at Frequency f_2. Beyond Frequency f_2, the noise gain is determined by the ratio of the shunt capacitance to the feedback capacitance.

$$NG_2 = 1 + \frac{C_{SHUNT}}{C_F}$$

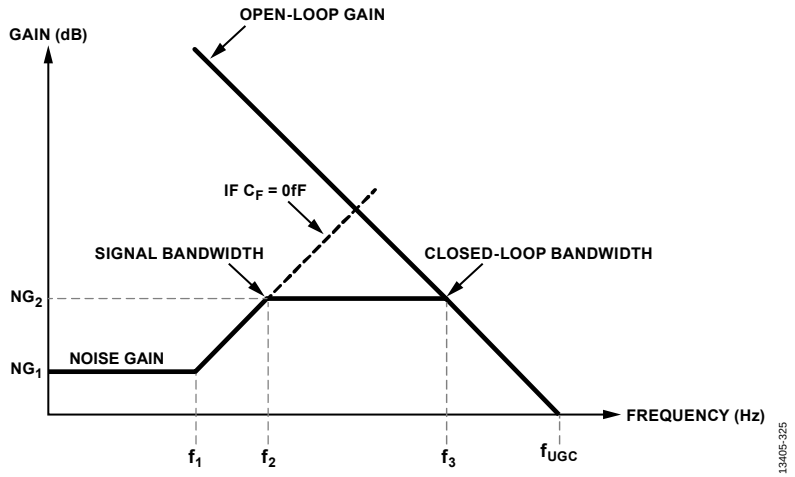


Figure 126. Transimpedance Noise Gain vs. Frequency

For completeness, the noise gain equations are as follows:

$$NG(f) = \left(1 + \frac{R_F}{R_S}\right)\left(\frac{\frac{2\pi f}{f_1} + 1}{\frac{2\pi f}{f_2} + 1}\right)$$

$$f_1 = \frac{1}{\frac{R_F R_{SHUNT}}{R_F + R_{SHUNT}}\left(C_F + C_{SHUNT}\right)}$$

$$f_2 = \frac{1}{R_F C_F}$$

For simplicity, bandwidth limitations are ignored in the noise gain equations. The noise gain starts to roll-off when it intersects with the open-loop gain of the amplifier. This pole frequency (f_3) is determined by the unity gain crossover frequency (f_{UGC}) of the amplifier and the high frequency noise gain, NG_2, as follows:

$$f_3 = \frac{f_{UGC}}{\left(1 + \frac{C_{SHUNT}}{C_F}\right)} \quad (3)$$

The addition of C_F has an impact on the signal frequency response. At low frequencies, the transimpedance gain is equal to R_F. As the frequency increases, the impedance of C_F drops below R_F and starts to reduce this transimpedance gain. This signal gain equation is as follows:

$$Signal\ Gain(f) = R_F\left(\frac{1}{\frac{2\pi f}{f_2} + 1}\right)$$

NOISE ANALYSIS

Photodiode TIA circuits have four noise sources that must be considered:

- The thermal noise of the feedback resistor (R_F)
- The saturation current noise of the photodiode
- The current noise of the amplifier
- The voltage noise of the amplifier

The noise contributions of these sources are typically referred to output for analysis. The thermal noise of R_F appears directly at the output. This noise is filtered by the feedback capacitance so that its −3 dB bandwidth is the same as the signal bandwidth (f_2).

The photocurrent of a photodiode, I_{PD}, produces shot noise equal to

$$I_{NPD} = \sqrt{(2qI_{PD})}$$

It is a mistake to assume that the noise goes to zero as the diode current goes to zero. Zero net current out of the diode simply means that the saturation current flowing in one direction is at thermal equilibrium with the saturation current flowing in the opposite direction. These currents are uncorrelated and add in a root sum square fashion. This net current noise is equivalent to the thermal noise of a physical resistor with a value of R_{SHUNT}. This convenient fact allows the photodiode to be accurately modeled with a simple resistor, R_{SHUNT}. The thermal noise of R_{SHUNT} is amplified by the ratio of the feedback resistance to the shunt resistance. This noise is also filtered to the signal bandwidth.

The current noise of the amplifier flows through the feedback resistor to become a noise voltage at the output. It is subject to the same bandwidth limitations as the previous noise contributors.

The voltage noise of the amplifier is multiplied by the noise gain of the circuit to the output. This noise source is significant for two reasons. First, the high frequency noise gain can be high due to the large ratio between the shunt capacitance and the feedback capacitance. Second, the voltage noise bandwidth is much higher than the other contributors. The noise bandwidth is limited only by bandwidth of the amplifier.

Each of these noise contributors is graphed vs. frequency in Figure 127. A summary of the noise sources and their RTO contributions is shown in Table 12. The total RTO noise adds the contributions of each noise source in root sum square.

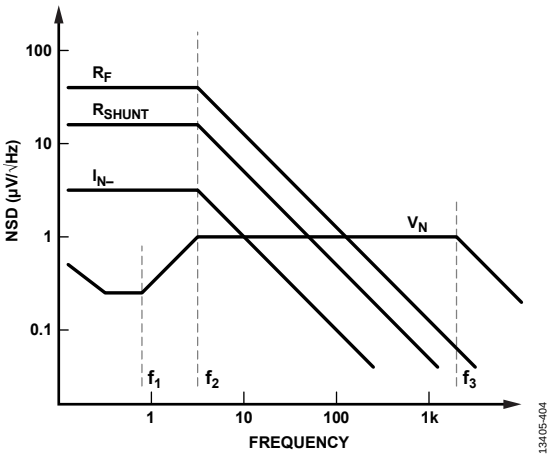


Figure 127. Photodiode TIA RTO Noise Spectral Density

Table 12. Photodiode Interface Noise Sources

Noise Source	RTO Noise	Noise Bandwidth
R_F	$\sqrt{(4kTR_F)}$	$\pi/2 \times f_2$
Photodiode	$(R_F/R_{SHUNT})\sqrt{(4kTR_{SHUNT})}$	$\pi/2 \times f_2$
I_{N-} Amplifier	$R_F \times I_{N-}$	$\pi/2 \times f_2$
V_N Amplifier	$V_N \times$ noise gain	$\pi/2 \times f_3$

DESIGN RECOMMENDATIONS

The design goal for a large area photodiode TIA circuit is usually to maximize SNR and minimize dc errors. Increasing the feedback resistor size accomplishes both goals. The signal gain increases directly with R_F, whereas the noise increases in a square root fashion. High gains also make the output signal large relative to output voltage errors (such as V_{OS}).

The upper limit for R_F is typically determined by one of the following:

- Amplifier output swing. The maximum photocurrent multiplied by R_F must be less than amplifier swing limitations.
- Signal bandwidth (or settling time). Signal bandwidth is dependent on $R_F \times C_F$. Achieving high signal bandwidths with large feedback resistors can require vanishingly small feedback capacitors to implement. The ultimate limitation is due to the parasitic feedback capacitance from the fringing electric fields in the circuit. Parasitic capacitances in the 50 fF to 100 fF range are possible. To put this in perspective, a 100 fF parasitic capacitance limits the signal bandwidth of a 100 GΩ TIA to 16 Hz.
- The thermal noise of the photodiode (R_{SHUNT}). When R_F is significantly larger than R_{SHUNT}, the total noise is dominated by the photodiode and the SNR stops improving.
- The current noise of the amplifier. When the current noise of the amplifier is larger than the noise of R_F, the SNR stops improving. The photodiode noise is higher than the amplifier current noise in nearly all practical photodiodes.
- The low frequency noise gain due to R_{SHUNT}. When R_F is larger than R_{SHUNT}, the noise gain multiplies V_{OS} and TCV_{OS} errors and the signal to error ratio stops improving.

The signal bandwidth increases as the feedback capacitance (C_F) decreases. The lower limit for C_F is typically limited by one of the following:

- Parasitic feedback capacitances limit the minimum value of C_F to 50 fF to 100 fF.
- Available component values. Physical components can be found in surface mount packages for values from 0.1 pF to 1 pF in 100 fF increments.
- Feedback loop stability. C_F must be large enough to recover enough phase shift prior to the loop crossover for stable operation. This capacitance value can be a significant consideration for smaller values of R_F. Large values (>1 GΩ) tend to be self compensating through the parasitic feedback capacitance.
- High frequency noise gain. The high frequency noise gain is set by the ratio of C_{SHUNT} to C_F. For very large noise gains, it is possible for the amplifier voltage noise to be greater than the feedback resistor noise.

DESIGN EXAMPLE

In this section, an example TIA circuit is designed using a photometry grade photodiode (Hamamatsu S1226-18BQ). This medium area (1.2 mm^2) silicon photodiode is responsive in the ultraviolet (UV) through visible frequency range. The minimum shunt resistance (R_{SHUNT}) is specified at 5 GΩ at 25°C. The shunt capacitance (C_{SHUNT}) is specified at 35 pF. The quartz window limits the maximum operating temperature to 60°C.

Based on the specified minimum shunt resistance and the recommendations in the Design Recommendations section, a value of 10 GΩ is chosen for R_F. This example circuit is powered from ±5 V with the input common-mode voltage set at 0 V, which allows a maximum photocurrent of approximately 500 pA.

An error budget is constructed based on the DC Error Analysis section (see Table 13). The amplifier offset voltage applies the maximum temperature drift limit to the maximum room temperature offset limit. The photo diode shunt resistance limit is reduced by half for every 10°C.

Table 13. Photodiode Interface DC Error Budget

Error Source	25°C	45°C	60°C
V_{OS}	40 μV	40 μV + 10 μV	40 μV + 18 μV
R_{SHUNT}	5 GΩ	1.25 GΩ	442 MΩ
Noise Gain	3	9	23
V_{OS} Error RTO	120 μV	450 μV	1.3 mV
I_B	20 fA	20 fA	20 fA
I_B Error RTO	200 μV	200 μV	200 μV
Total Error RTO	320 μV	650 μV	1.5 mV
Total Error RTI	32 fA	65 fA	150 fA

The total RTI error over the entire temperature range is less than 150 fA, which is equal to 300 ppm of the 500 pA full-scale range. Note that the extraordinarily low input bias current of the ADA4530-1 is not a significant contributor to the total error over temperature. The interaction of the offset voltage with the shunt resistance of the photodiode is the most significant error source.

This circuit was constructed as described with a 10 GΩ feedback resistor (Ohmite RX-1M1008JE). The dc error performance was measured over the 25°C to 60°C temperature range (see Figure 128). The error increases rapidly with temperature as the shunt resistance changes the noise gain exponentially. The total RTI error ranges from +2 fA to −10 fA, considerably lower than the worst case error budget, as expected.

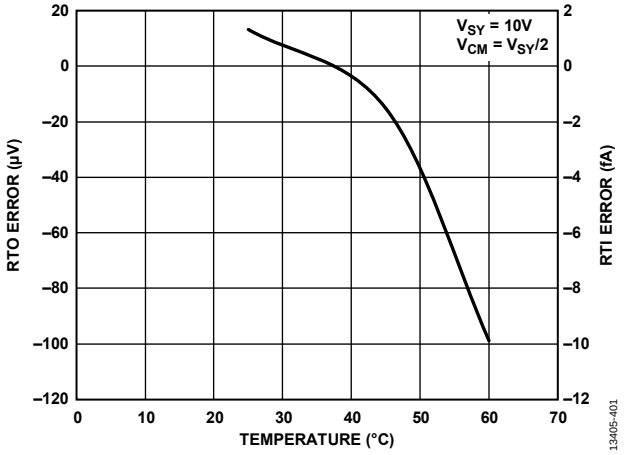


Figure 128. DC Error vs. Temperature

The ac performance of the circuit was also measured. The circuit was initially constructed without a physical feedback capacitor as a baseline. The transimpedance gain vs. frequency is shown in Figure 129. The 30% frequency peaking seen in the frequency response (red curve) indicates that the feedback loop is marginally compensated with parasitic capacitance.

A physical capacitor was added to improve the loop compensation. This capacitor is a 300 fF C0G ceramic in a Size 0805, surface-mount package (AVX UQCFVA0R3BAT2A\500). C0G ceramic capacitors are good candidates for electrometer circuits because they have adequate insulation resistance and dielectric absorption performance. These low valued capacitors are designed for RF use and are readily available. The 300 fF capacitor eliminates the frequency peaking completely (blue curve) but it reduces the −3 dB bandwidth from 390 Hz to 50 Hz.

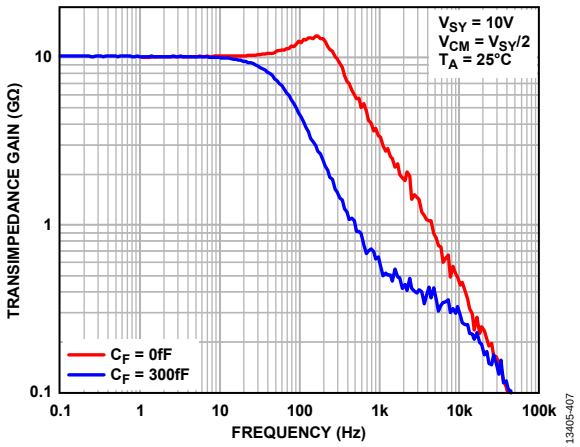


Figure 129. Transimpedance Gain vs. Frequency

The stability improvement can be seen in the time domain as well. The circuits step response to a 10 pA photocurrent is shown in Figure 130. The uncompensated circuit (red curve) shows considerable (20%) overshoot. The compensated circuit (blue curve) is overdamped.

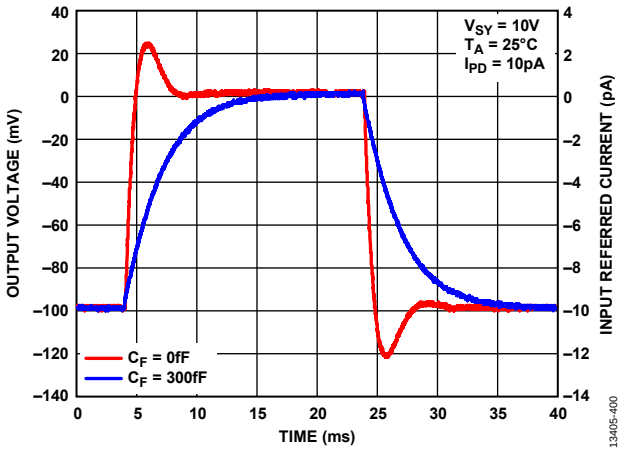


Figure 130. 10 pA Step Response

A noise budget is constructed based on the Noise Analysis section. The RTO noise budget is separated into noise sources integrated with a low bandwidth (see Table 14) and those integrated with a high bandwidth (see Table 15).

The low frequency noise contributors include the feedback resistance, the shunt resistance and the amplifier current noise. Each of these sources has a −3 dB bandwidth equal to the signal bandwidth (50 Hz); this is equivalent to a noise bandwidth of 79 Hz. The most significant noise source is the photodiode shunt resistance by a large margin. The second most significant source is the feedback resistor. The amplifier current noise is so low that it can be ignored.

Table 14. Low Frequency Noise Budget

Error Source	25°C	45°C	60°C
V_{NRF}	12.8 µV/√Hz	13.2 µV/√Hz	13.5 µV/√Hz
R_{SHUNT}	5 GΩ	1.25 GΩ	442 MΩ
$V_{NRSHUNT}$	9 µV/√Hz	4.7 µV/√Hz	2.8 µV/√Hz
R_F/R_{SHUNT}	2	8	22
$V_{NRSHUNT_RTO}$	18 µV/√Hz	37 µV/√Hz	61 µV/√Hz
I_{N-}	0.07 fA/√Hz	0.15 fA/√Hz	0.24 fA/√Hz
I_{N-_RTO}	700 nV/√Hz	1.5 µV/√Hz	2.4 µV/√Hz
Low Frequency NSD Total	22 µV/√Hz	39 µV/√Hz	62 µV/√Hz
Low Frequency RMS Total	194 µV rms	345 µV rms	549 µV rms

The sole high frequency noise contributor is the amplifier voltage noise, which is multiplied by the high frequency noise gain and band limited only by the amplifier gain. The −3 dB bandwidth of the amplifier is 17 kHz (refer to Equation 3, where $f_3 = f_{UGC} \div NG_2$ = 2 MHz ÷ 118). The equivalent noise bandwidth is 27 kHz. The high bandwidth is the reason the high frequency noise is significant even though the noise spectral density is much lower than the low frequency noise.

Table 15. High Frequency Noise Budget

Error Source	25°C	45°C	60°C
V_N	14 nV/√Hz	14.5 nV/√Hz	14.8 nV/√Hz
High Frequency Noise Gain	118	118	118
V_{N_RTO}	1.6 µV/√Hz	1.7 µV/√Hz	1.7 µV/√Hz
High Frequency RMS Total	271 µV rms	281 µV rms	286 µV rms

At low temperatures, the amplifier voltage noise is more significant than any other noise source. This is important because the majority of this noise occurs outside the useful bandwidth of the circuit. For this reason, it is prudent to add a low-pass filter to the output of a photodiode TIA circuit. This filter can be active or passive depending on the needs of the system. A simple RC filter with a −3 dB cutoff of 500 Hz has an insignificant impact on the frequency response of the signal path, but it lowers the integrated noise from 271 µV rms to 45 µV rms (a 6× reduction).

The NSD was measured for this circuit with (blue curve) and without (red curve) the 300 fF C_F capacitor (see Figure 131). At low frequencies, the NSD is approximately equal to the noise from the feedback resistor alone (12.8 µV/√Hz). The value of the low frequency NSD shows that the shunt resistance is much larger than the specified minimum (which is expected). As frequency increases, the resistor noise rolls off at the signal bandwidth (50 Hz). The NSD then plateaus at the amplifier voltage noise level until the bandwidth limitations of the amplifier roll off the NSD toward zero.

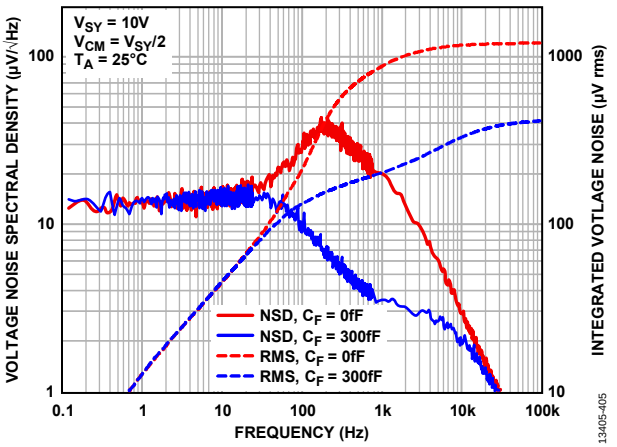


Figure 131. RTO Noise Spectral Density (25°C)

The dashed curves show the integration of the NSD across the frequency spectrum. These are useful to calculate the rms noise over a variety of bandwidths. For example, the rms noise over the entire 100 kHz measurement bandwidth is 400 µV rms, which is approximately the same as the calculated total noise of 333 µV rms. If a postfilter is added with a noise bandwidth of 1 kHz, Figure 131 shows that the integrated noise is 200 µV rms (a 2× improvement).

The uncompensated circuit (red curves) shows considerably worse noise performance. The frequency peaking due to the marginal loop stability multiplies the noise as well as the signal. In addition, the high frequency noise gain is larger, which adds much more noise outside the signal bandwidth. Both of these effects together generate 1.2 mV rms of total noise. Even if the transient and frequency response of an undercompensated TIA are acceptable, the large noise penalty may not be.

Lastly, the NSD was measured for this circuit at 60°C (see Figure 132). As expected, the low frequency noise increased as a result of the photodiode shunt resistance. The average low frequency NSD is 22 µV/√Hz. Removing the contribution of R_F gives an RTO contribution of 17 µV/√Hz, which is equivalent to an RTI current noise of 1.7 fA/√Hz. R_{SHUNT} must be approximately 6.5 GΩ at 60°C to generate this noise.

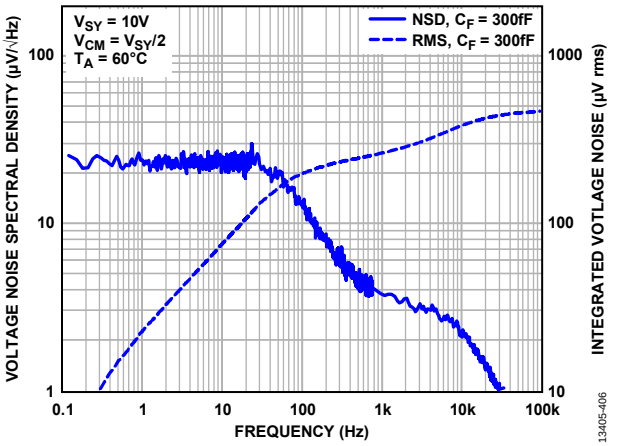


Figure 132. RTO Noise Spectral Density (60°C)

POWER SUPPLY RECOMMENDATIONS

Analog Devices offers a wide range of power management products to meet the requirements of most high performance signal chains.

Examples of a single- and dual-supply solution is shown in Figure 133. The ADP2370 and ADP5075, cascaded with the ADP7118 or ADM7170, and the ADP7182 generate clean positive and negative rails. These rails power the ADA4530-1, electrometer amplifier and/or the precision converter in a typical signal chain.

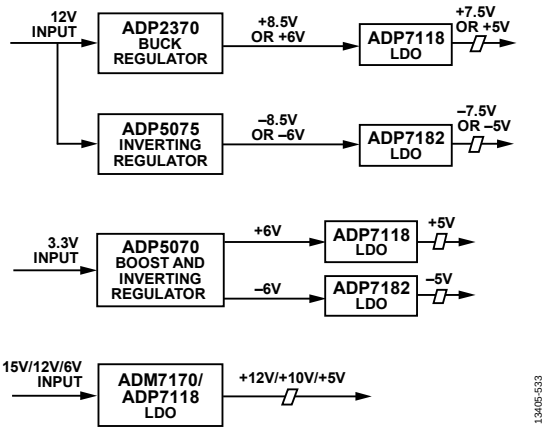


Figure 133. Recommended Power Solutions

Table 16. Recommended Power Management Devices

Product	Description
ADP5075	800 mA, dc-to-dc inverting regulator
ADP2370	High voltage, 1.2 MHz/600 kHz, 800 mA, low quiescent current buck regulator
ADP5070	1 A/0.6 A, dc-to-dc switching regulator with independent positive and negative outputs
ADM7170	6.5 V, 500 mA, ultralow noise, high PSRR, CMOS LDO
ADP7118	20 V, 200 mA, low noise, high PSRR, CMOS LDO
ADP7182	−28 V, −200 mA, low noise, linear regulator

POWER SUPPLY CONSIDERATIONS

The PSRR of the ADA4530-1 is excellent at dc (approximately 150 dB); however, it decreases as frequency increases. To achieve the best performance of the ADA4530-1, a low-noise supply is necessary. If switching supplies are used for input rails, a low dropout regulator (LDO) is essential to attenuate the switching spurs to a level that does not affect the ADA4530-1 output. Switching power supply noise typically spans a frequency range from 300 kHz and up. The switching spurs can effectively be attenuated using the LDO. Additional filtering around the LDO may be necessary, especially when using a switching regulator to generate an intermediate rail. Switching regulators also generate high frequency noise content (>100 MHz), even when running in the 100 kHz range, because of the high dv/dt of the switch node. In this case, ferrite beads can be used, as described in the AN-1120 Application Note and the AN-1368 Application Note.

For a single-supply application, the ADA4530-1 typically needs a 5 V, 10 V, or 12 V supply, although a 4.5 V to 16 V supply can also be used. An LDO like the ADM7170 or ADP7118 is ideal to generate the low noise rail.

For a dual-supply application, the ADA4530-1 typically needs a ±5 V supply, although in some applications, a ±2.5 V to ±8 V supply can be used. LDOs like the ADP7118 or ADM7170 are the optimum choices for the positive supply, and the ADP7182 for the negative supply. In addition, if a negative supply is not already available, the ADP5075 or the ADP5070 can generate the negative supply from a positive supply, as shown in Figure 133.

Figure 134 shows the combined PSRR of using the ADP7118 to provide +5 V on $+V_{SY}$ of the ADA4530-1, and the ADP7182 to provide –5 V on $–V_{SY}$, from a 9 V battery main supply. Figure 135 shows the maximum allowable ripple at the input so that the combined PSRR of the LDO and the amplifier can still attenuate the noise level down to the noise floor.

For example, if the main supply to the ADP7118 and ADA4530-1 has a switching noise of 20 mV p-p at 300 kHz, Figure 135 shows that it is below the maximum value of 90 mV p-p. Therefore, the combined PSRR of the system can still attenuate and bring the noise level down to the noise floor, in effect, the 300 kHz noise at the input is not seen at the output of the amplifier.

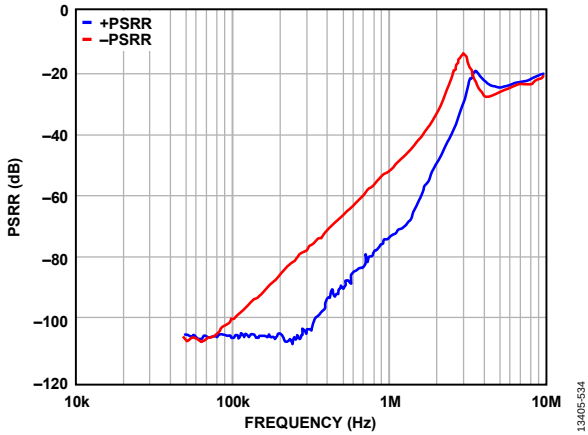


Figure 134. Positive and Negative PSRR for the ADP7118 and ADP7182 Powering ADA4530-1, $±V_{SY}$ = ±5 V, +IN = 0 V

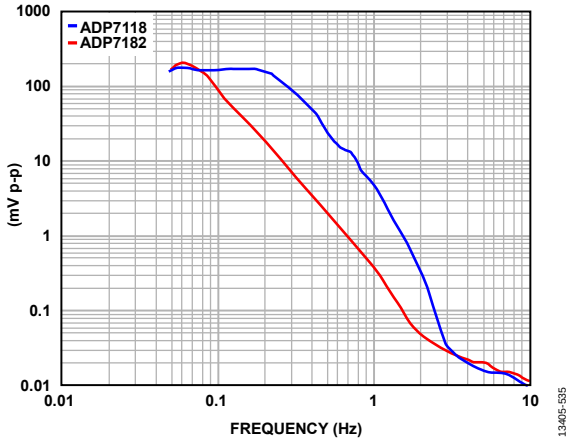
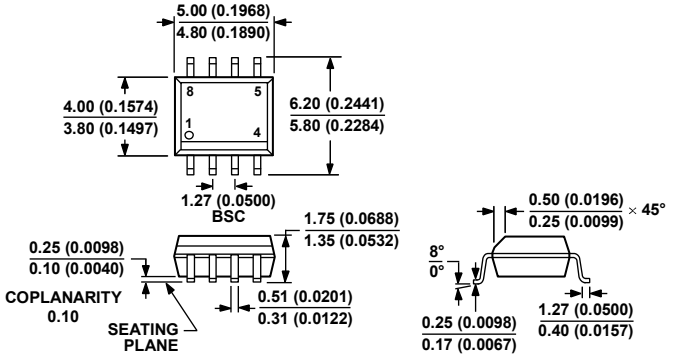


Figure 135. Maximum Allowable Ripple at the Input of the LDOs to Bring Spurs To Noise Floor Level (−120 dB)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 136. 8-Lead Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADA4530-1ARZ	−40°C to +125°C	8-Lead Small Outline Package [SOIC_N]	R-8
ADA4530-1ARZ-R7	−40°C to +125°C	8-Lead Small Outline Package [SOIC_N]	R-8
ADA4530-1ARZ-RL	−40°C to +125°C	8-Lead Small Outline Package [SOIC_N]	R-8
ADA4530-1R-EBZ-BUF		Evaluation Board Buffer Configuration for 8-Lead SOIC	
ADA4530-1R-EBZ-TIA		Evaluation Board Transimpedance Configuration for 8-Lead SOIC	

[1] Z = RoHS Compliant Part.

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