2.5V/3.3V 1.5GHz Low Skew 1-to-10 Differential to LVPECL Fanout Buffer with Sync OE

Features

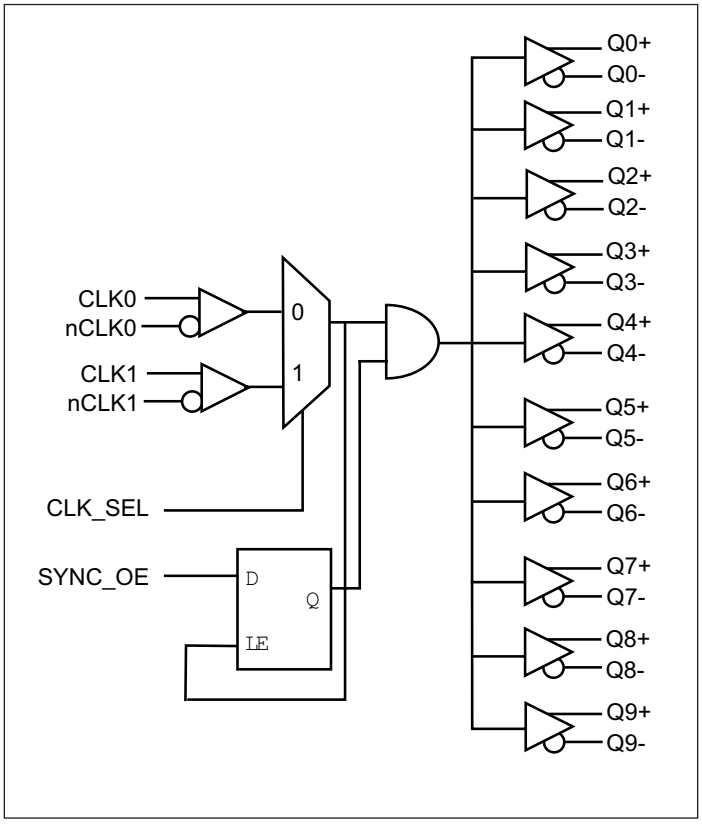
- ➔ F_{MAX} < 1.5GHz
- ➔ 10 pairs of differential LVPECL/ ECL outputs
- ➔ Low additive jitter, < 0.03ps (typ)
- ➔ Selectable differential input pairs with single ended input option
- ➔ Input CLK accepts: LVPECL, LVDS, CML, SSTL input level
- ➔ Output skew: 55ps (max)
- ➔ Operating Temperature: -40°C to 85°C
- ➔ ECL mode operating voltage range
  V_{DD}/ V_{DDO} = 0V, V_{EE} = -3.6V to -2.375V
- ➔ Power supply: 3.3V ±10% or 2.5V ±5%
- ➔ Packaging (Pb-free & Green), 32-pin TQFP available

Description

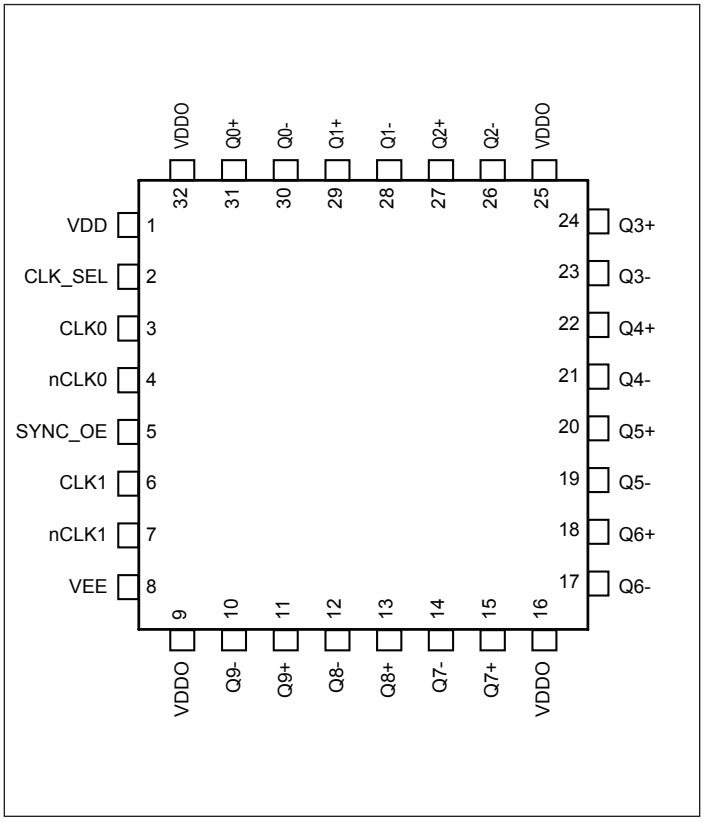
The PI6C4911510-05 is a high-performance low-skew 1-to-10 LVPECL/ ECL fanout buffer. The PI6C4911510-05 features two selectable differential clock inputs and translates to ten LVPECL/ ECL outputs. The CLK inputs accept LVPECL, LVDS, CML and SSTL signals.

PI6C4911510-05 is ideal for clock distribution applications such as providing fanout for low noise Pericom oscillators.

Block Diagram



Pin Configuration



Pin Description

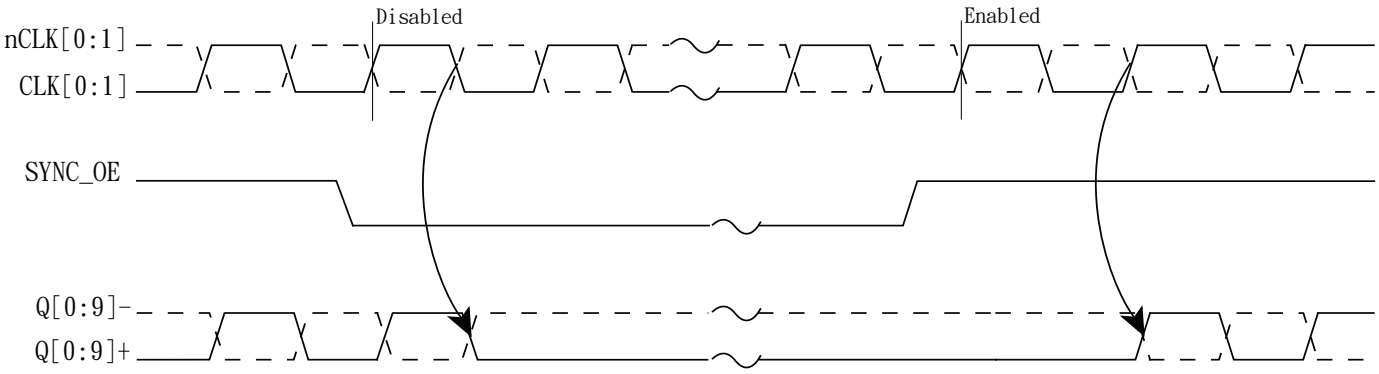
Pin #	Name	Type	Description
1	V_{DD}	Power	Core Power Supply
2	CLK_SEL	Input	Clock select input. When high, selects CLK1 input. When low, selects CLK0 input. LVCMOS/LVTTL level with 50kΩ pull down.
3	CLK0	Input	Differential clock input with pull-down
4	nCLK0	Input	Inverting differential clock input. Defaults to $V_{DD}/2$ if left floating.
5	SYNC_OE	Input	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTL interface levels.
6	CLK1	Input	Differential clock input with pull-down
7	nCLK1	Input	Inverting differential clock input. Defaults to $V_{DD}/2$ if left floating.
8	V_{EE}	Power	Connect to negative power supply
9, 16, 25, 32	V_{DDO}	Power	Output Power pin
11, 10	Q9+, Q9-	Output	Differential output pair, LVPECL interface level.
13,12	Q8+, Q8-	Output	Differential output pair, LVPECL interface level.
15,14	Q7+, Q7-	Output	Differential output pair, LVPECL interface level.
18,17	Q6+, Q6-	Output	Differential output pair, LVPECL interface level.
20,19	Q5+, Q5-	Output	Differential output pair, LVPECL interface level.
22,21	Q4+, Q4-	Output	Differential output pair, LVPECL interface level.
24, 23	Q3+, Q3-	Output	Differential output pair, LVPECL interface level.
27,26	Q2+, Q2-	Output	Differential output pair, LVPECL interface level.
29,28	Q1+, Q1-	Output	Differential output pair, LVPECL interface level.
31,30	Q0+, Q0-	Output	Differential output pair, LVPECL interface level.

CLK_SEL Input Function Table

Inputs	Outputs
0	CLK0
1	CLK1

SYNC_OE Input Function Table

Input	Outputs	
SYNC_OE	**Q[0:9]+**	**Q[0:9]-**
0	Disabled; LOW	Disabled; HIGH
1	Enabled	Enabled



Notes:

1. Exact enable/ disable time shown above only valid for frequencies <200MHz.

Clock Input Function Table

Inputs		Outputs		Input to Output Mode	Polarity
CLK0 or CLK1	nCLK0 or nCLK1	Q[0:9]+	Q[0:9]-		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased	HIGH	LOW	Single Endded to Differential	Non Inverting
Biased	0	HIGH	LOW	Single Endded to Differential	Inverting
Biased	1	LOW	HIGH	Single Endded to Differential	Inverting

Absolute Maximum Ratings(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply voltage	Referenced to GND			4.6	V
V_{IN}	Input voltage	Referenced to GND	-0.5		V_{DD}+0.5V	V
IOUT	Surge Current				100	mA
T_{STG}	Storage temperature		-55		150	°C

Note:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Core Power Supply Voltage		3.0		3.6	V
			2.375		2.625	
V_{DDO}	Output Power Supply Voltage		3.0		3.6	V
			2.375		2.625	
T_A	Ambient Temperature		-40		85	°C
I_{DD}	Core Power Supply Current				90	mA
I_{DDO}	Output Power Supply Current	All LVPECL outputs unloaded			110	

LVCMOS/LVTTL DC Characteristics (TA = -40°C to +85°C, VDD = 3.3V ±10%, VDDO = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage	CLK_SEL, SYNC_OE		1.7		V_{DD}+0.3	V
V_{IL}	Input Low Voltage	CLK_SEL, SYNC_OE		-0.3			
I_{IH}	Input High Current	CLK_SEL, SYNC_OE	$V_{IN} = V_{DD} = 3.6V$			150	µA
I_{IL}	Input Low Current	CLK_SEL, SYNC_OE	$V_{IN} = 0V, V_{DD} = 3.6V$	-150			µA

LVPECL DC Characteristics (T_A = -40°C to +85°C, V_{DD} = 3.3V ±10%, V_{DDO} = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
I_{IH}	Input High Current	CLK0, CLK1	$V_{IN} = V_{DD}$ = 3.6V			150	µA
		nCLK0, nCLK1	$V_{IN} = V_{DD}$ = 3.6V			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA
		nCLK0, nCLK1	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-peak Voltage			0.4		0.8	V
V_{CMR}	Common Mode Input Voltage(1)			V_{EE}+0.5		V_{DD}- 0.85	V
V_{OH}	Output High Voltage(2)		V_{DDO} = 2.5V or 3.3V		V_{DDO}-1.4	V_{DDO}-0.9	V
V_{OL}	Output Low Voltage(2)		V_{DDO} = 2.5V or 3.3V		V_{DDO}-2.0	V_{DDO}-1.7	V
V_{SWING}	Peak-to-peak Output Voltage Swing			0.6		1.0	V
R	Input Pullup/Pulldown Resistance				50		kΩ

Notes:

1. For single-ended applications, the maximum input voltage for CLK and /CLK is V_{DD}+0.3V
2. Outputs terminated with 50Ω to V_{DD}-2.0V

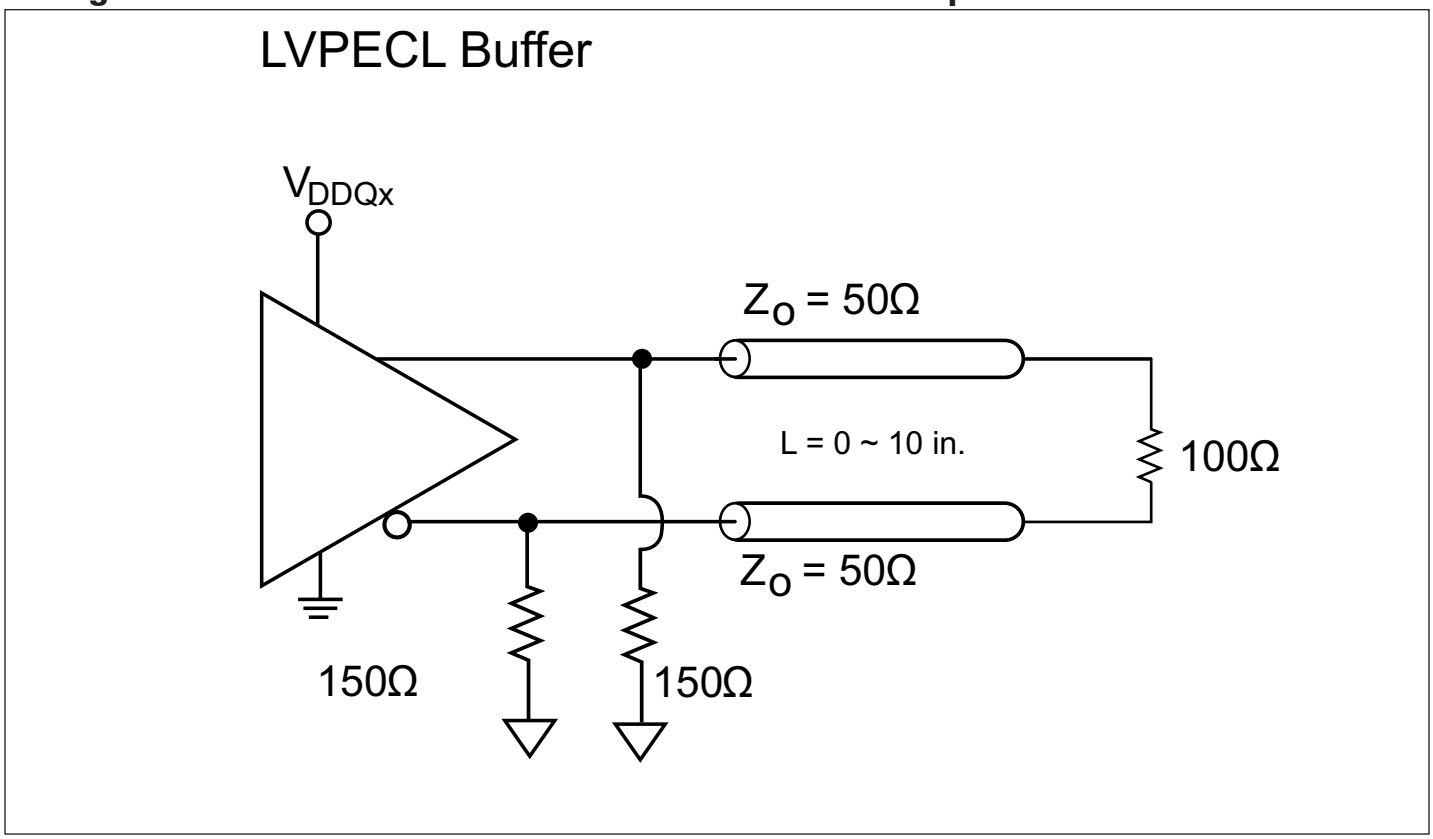
AC Characteristics (T_A = -40°C to +85°C, V_{DD} = 3.3V ±10%, V_{DDO} = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{max}	Output Frequency				1500	MHz
t_{pd}	Propagation Delay(1)			1200	2100	ps
Tsk	Output-to-output Skew(2)			40	55	ps
Tsk(p-p)	Part-to-Part Skew(3)				250	ps
t_r/t_f	Output Rise/Fall time	20% - 80%		150		ps
t_{odc}	Output duty cycle	f ≤ 650 MHz	48		52	%
V_{PP}	Output Swing	LVPECL outputs, f ≤ 650 MHz	400			mV
t_j	Buffer additive jitter RMS	156.25MHz with 12KHz to 20MHz integration range		0.03		ps

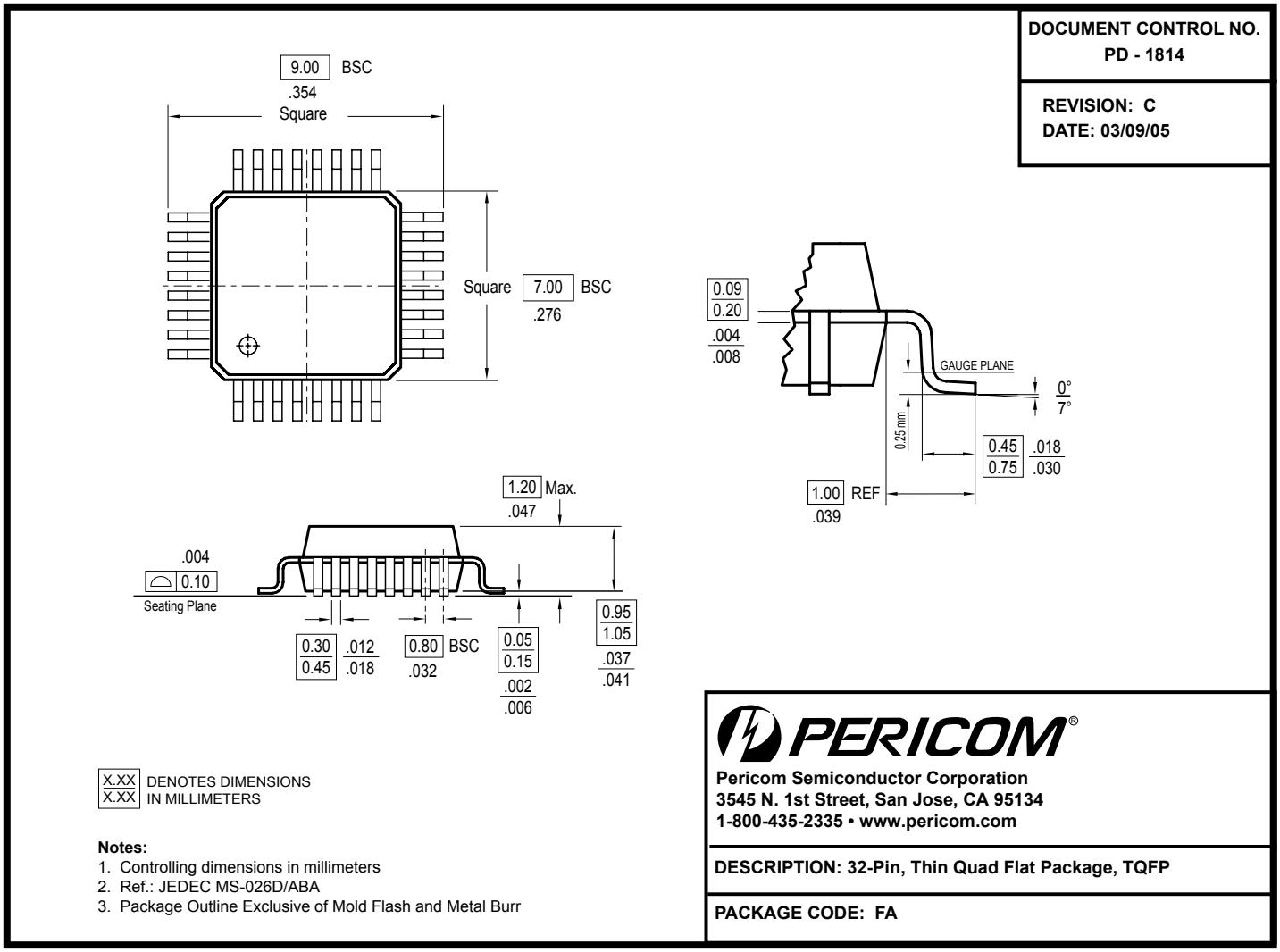
Notes:

1. Measured from the differential input to the differential output crossing point
2. Defined as skew between outputs at the same supply voltage and with equal loads. Measured at the output differential crossing point
3. This parameter is guaranteed by design

Configuration Test Load Board Termination for LVPECL outputs



Packaging Mechanical: 32-pin TQFP (FA)



Ordering Information[1,2,3]

Ordering Code	Package Code	Package Description
PI6C4911510-05FAIE	FA	Pb-free & Green, 32-pin TQFP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free & Green
3. X suffix = Tape/Reel

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