

FEATURES

- Up to 10.7 Gbps operation
- Very low power: 670 mW (IBIAS = 40 mA, IMOD = 40 mA)
- Typical 24 ps rise/fall times
- Full back-termination of output transmission lines
- Compatible with XMD-MSA TOSA
- Drives TOSAs with resistances ranging from 5 Ω to 50 Ω
- PECL-/CML-compatible data inputs
- Bias current range: 10 mA to 100 mA
- Differential modulation current range: 10 mA to 80 mA
- Automatic laser shutdown (ALS)
- 3.3 V operation
- Compact 3 mm $\times$ 3 mm LFCSP
- Voltage input control for bias and modulation currents
- XFP-compliant bias current monitor
- Optical evaluation board available

APPLICATIONS

- SONET OC-192 optical transceivers
- SDH STM-64 optical transceivers
- 10 Gb Ethernet optical transceivers
- XFP/X2/XENPAK/XPAK/MSA 300 optical modules
- SR and VSR optical links

GENERAL DESCRIPTION

The ADN2525 laser diode driver is designed for direct modulation of packaged laser diodes having a differential resistance ranging from 5 Ω to 50 Ω . The active back-termination technique provides excellent matching with the output transmission lines while reducing the power dissipation in the output stage. The back-termination in the ADN2525 absorbs signal reflections from the TOSA end of the output transmission lines, enabling excellent optical eye quality to be achieved even when the TOSA end of the output transmission lines is significantly miterminated. The small package provides the optimum solution for compact modules where laser diodes are packaged in low pin-count optical subassemblies.

The modulation and bias currents are programmable via the MSET and BSET control pins. By driving these pins with control voltages, the user has the flexibility to implement various average power and extinction ratio control schemes, including closed-loop control and look-up tables. The automatic laser shutdown (ALS) feature allows the user to turn on/off the bias and modulation currents by driving the ALS pin with the proper logic levels.

The product is available in a space-saving 3 mm $\times$ 3 mm LFCSP specified from -40°C to $+85^{\circ}\text{C}$.

FUNCTIONAL BLOCK DIAGRAM

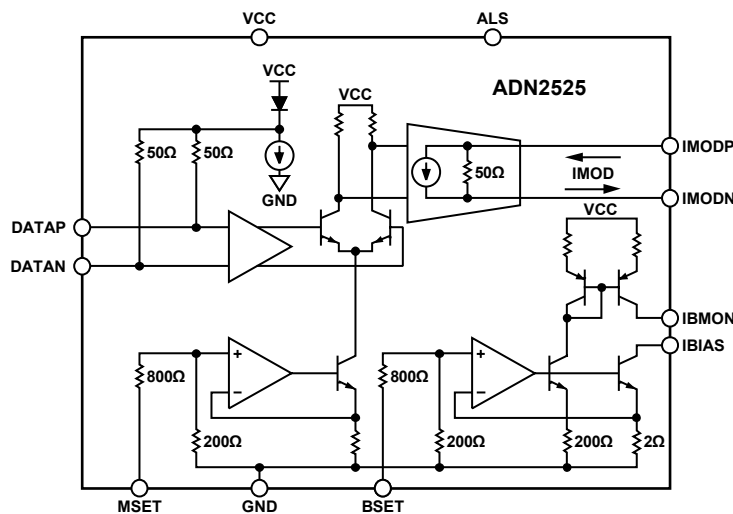


Figure 1.

Rev. A

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REVISION HISTORY

8/06—Rev. 0 to Rev. A

Changes to Format	Universal
Changes to Features and Figure 1.....	1
Changes to Table 1.....	3
Changes to Table 3.....	5
Changes to Figure 19.....	9
Changes to Figure 25.....	10
Changes to Modulation Current Section and Figure 29	11
Changes to Typical Application Circuit Section.....	13
Changes to Ordering Guide	15

3/05—Revision 0: Initial Version

SPECIFICATIONS

$V_{CC} = V_{CC_{MIN}}$ to $V_{CC_{MAX}}$, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $50\ \Omega$ differential load resistance, unless otherwise noted. Typical values are specified at 25°C , $I_{MOD} = 40\ \text{mA}$.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
BIAS CURRENT (IBIAS)					
Bias Current Range	10		100	mA	
Bias Current while ALS Asserted			100	μA	ALS = high
Compliance Voltage ¹	0.6		$V_{CC} - 1.2$	V	IBIAS = 100 mA
	0.6		$V_{CC} - 0.8$	V	IBIAS = 10 mA
MODULATION CURRENT (IMODP, IMODN)					
Modulation Current Range	10		80	mA diff	$R_{LOAD} = 5\ \Omega$ to $50\ \Omega$ differential
Modulation Current While ALS Asserted			0.5	mA diff	ALS = high
Rise Time (20% to 80%) ^{2, 3}		24	32.5	ps	
Fall Time (20% to 80%) ^{2, 3}		24	32.5	ps	
Random Jitter ^{2, 3}		0.4	0.9	ps rms	
Deterministic Jitter ^{3, 4}		7.2	12	ps p-p	Includes pulse-width distortion
Pulse-Width Distortion ^{2, 3}		2	5	ps	$PWD = \text{ABS}(T_{HIGH} - T_{LOW})/2$
Differential S22		-10		dB	$5\ \text{GHz} < f < 10\ \text{GHz}$, $Z_0 = 50\ \Omega$ differential
		-14		dB	$f < 5\ \text{GHz}$, $Z_0 = 50\ \Omega$ differential
Compliance Voltage ¹	$V_{CC} - 1.1$		$V_{CC} + 1.1$	V	
DATA INPUTS (DATAP, DATAN)					
Input Data Rate			10.7	Gbps	NRZ
Differential Input Swing	0.4		1.6	V p-p diff	Differential ac-coupled
Differential S11		-16.8		dB	$f < 10\ \text{GHz}$, $Z_0 = 100\ \Omega$ differential
Input Termination Resistance	85	100	115	Ω	Differential
BIAS CONTROL INPUT (BSET)					
BSET Voltage to IBIAS Gain	75	100	120	mA/V	
BSET Input Resistance	800	1000	1200	Ω	
MODULATION CONTROL INPUT (MSET)					
MSET Voltage to IMOD Gain	70	88	110	mA/V	See Figure 29
MSET Input Resistance	800	1000	1200	Ω	
BIAS MONITOR (IBMON)					
IBMON to IBIAS Ratio		10		$\mu\text{A}/\text{mA}$	
Accuracy of IBIAS to IBMON Ratio	-5.0		+5.0	%	$10\ \text{mA} \leq \text{IBIAS} < 20\ \text{mA}$, $R_{IBMON} = 1\ \text{k}\Omega$
	-4.0		+4.0	%	$20\ \text{mA} \leq \text{IBIAS} < 40\ \text{mA}$, $R_{IBMON} = 1\ \text{k}\Omega$
	-2.5		+2.5	%	$40\ \text{mA} \leq \text{IBIAS} < 70\ \text{mA}$, $R_{IBMON} = 1\ \text{k}\Omega$
	-2		+2	%	$70\ \text{mA} \leq \text{IBIAS} < 100\ \text{mA}$, $R_{IBMON} = 1\ \text{k}\Omega$
AUTOMATIC LASER SHUTDOWN (ALS)					
V_{IH}	2.4			V	
V_{IL}			0.8	V	
I_{IL}	-20		+20	μA	
I_{IH}	0		200	μA	
ALS Assert Time			2	μs	Rising edge of ALS to fall of IBIAS and IMOD below 10% of nominal; see Figure 2
ALS Negate Time			10	μs	Falling edge of ALS to rise of IBIAS and IMOD above 90% of nominal; see Figure 2
POWER SUPPLY					
V_{CC}	3.07	3.3	3.53	V	
I_{CC}^5		39	45	mA	$V_{BSET} = V_{MSET} = 0\ \text{V}$
I_{SUPPLY}^6		157	176	mA	$V_{BSET} = V_{MSET} = 0\ \text{V}$; $I_{SUPPLY} = I_{CC} + I_{MODP} + I_{MODN}$

See notes on next page.

ADN2525

¹ Refers to the voltage between the pin for which the compliance voltage is specified and GND.
² The pattern used is composed by a repetitive sequence of eight 1s followed by eight 0s at 10.7 Gbps.
³ Measured using the high speed characterization circuit shown in Figure 3.
⁴ The pattern used is K28.5 (00111110101100000101) at a 10.7 Gbps rate.
⁵ Only includes current in the ADN2525 VCC pins.
⁶ Includes current in ADN2525 VCC pins and dc current in IMODP and IMODN pull-up inductors. See the Power Consumption section for total supply current calculation.

THERMAL SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Conditions/Comments
θ_{J-PAD}	2.6	5.8	10.7	°C/W	Thermal resistance from junction to bottom of exposed pad
θ_{J-TOP}	65	72.2	79.4	°C/W	Thermal resistance from junction to top of package
IC Junction Temperature			125	°C	

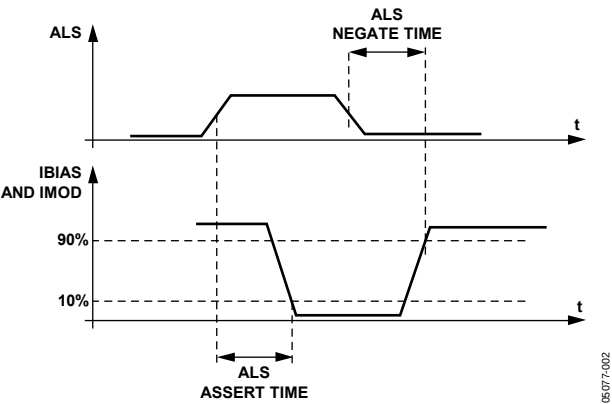


Figure 2. ALS Timing Diagram

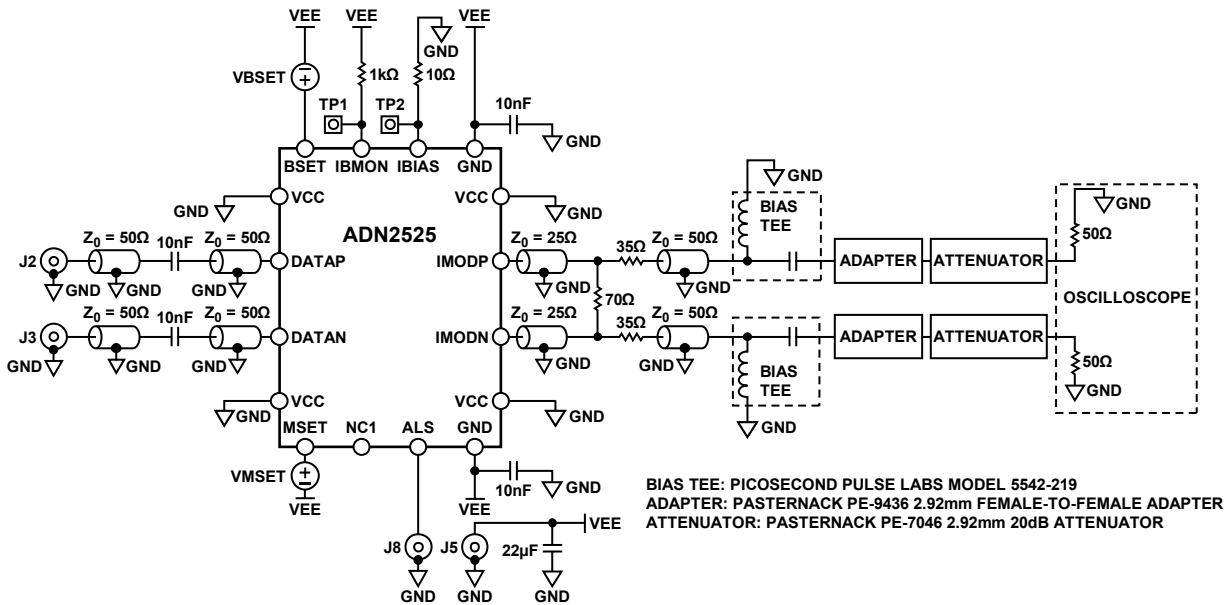


Figure 3. High Speed Characterization Circuit

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Min	Max	Unit
Supply Voltage, VCC to GND	-0.3	+4.2	V
IMODP, IMODN to GND	VCC - 1.5	4.75	V
DATAP, DATAN to GND	VCC - 1.8	VCC - 0.4	V
All Other Pins	-0.3	VCC + 0.3	V
Junction Temperature		150	°C
Storage Temperature Range	-65	+150	°C
Soldering Temperature (Less than 10 sec)		300	°C

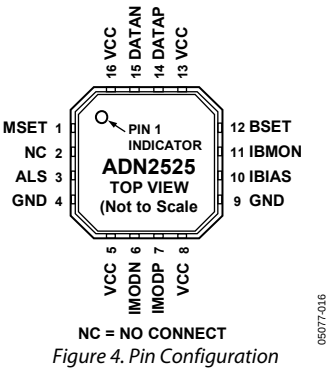
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



Note that the exposed pad on the bottom of the package must be connected to the VCC or GND plane.

Table 4. Pin Function Description

Pin No.	Mnemonic	I/O	Description
1	MSET	Input	Modulation Current Control Input
2	NC	N/A	No Connect—Leave Floating
3	ALS	Input	Automatic Laser Shutdown
4	GND	Power	Negative Power Supply
5	VCC	Power	Positive Power Supply
6	IMODN	Output	Modulation Current Negative Output
7	IMODP	Output	Modulation Current Positive Output
8	VCC	Power	Positive Power Supply
9	GND	Power	Negative Power Supply
10	IBIAS	Output	Bias Current Output
11	IBMON	Output	Bias Current Monitoring Output
12	BSET	Input	Bias Current Control Input
13	VCC	Power	Positive Power Supply
14	DATAP	Input	Data Signal Positive Input
15	DATAN	Input	Data Signal Negative Input
16	VCC	Power	Positive Power Supply
Exposed Pad	Pad	Power	Connect to GND or VCC

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.3 V, unless otherwise noted.

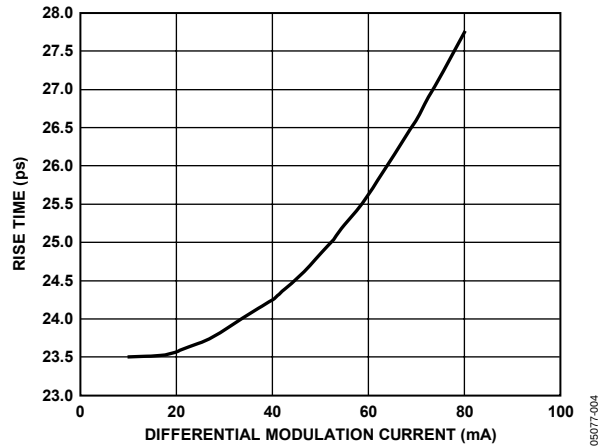


Figure 5. Rise Time vs. IMOD

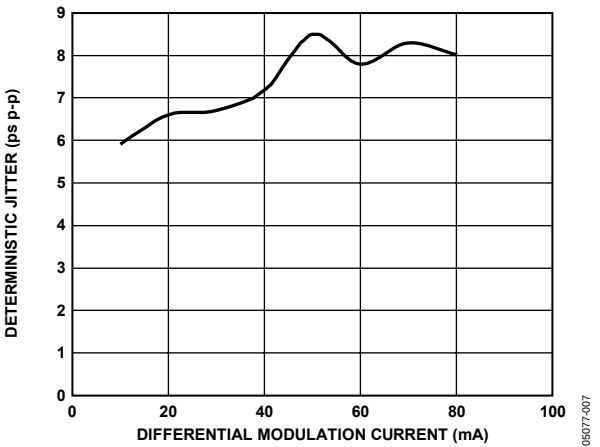


Figure 8. Deterministic Jitter vs. IMOD

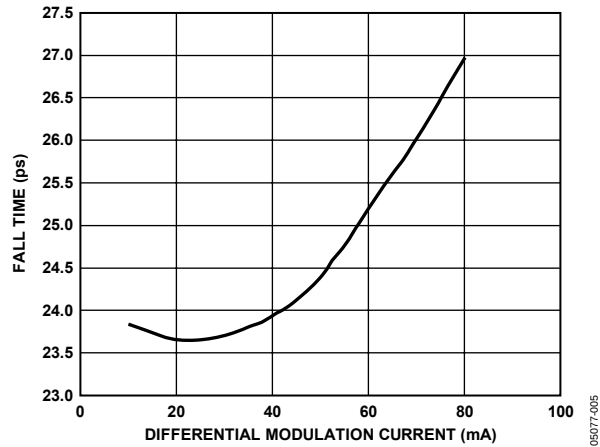


Figure 6. Fall Time vs. IMOD

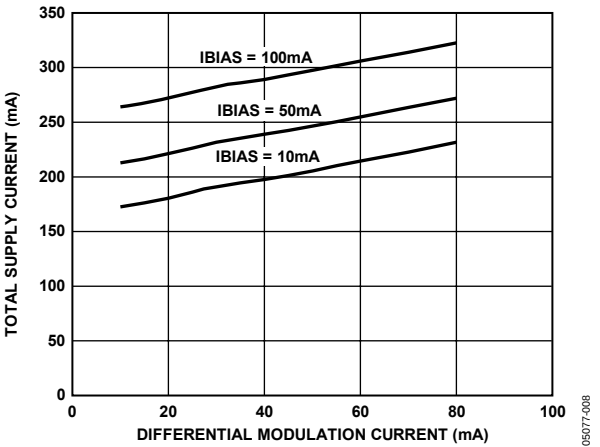


Figure 9. Total Supply Current vs. IMOD

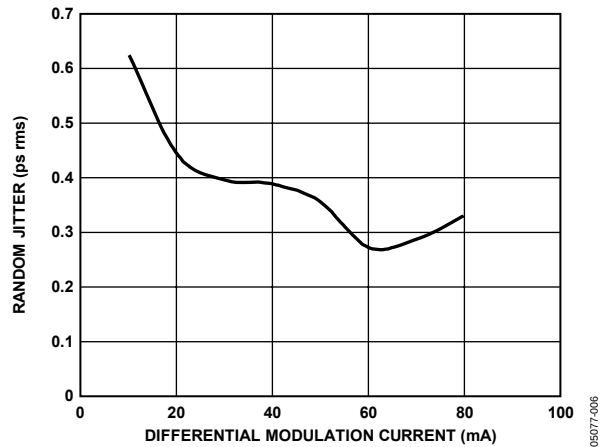


Figure 7. Random Jitter vs. IMOD

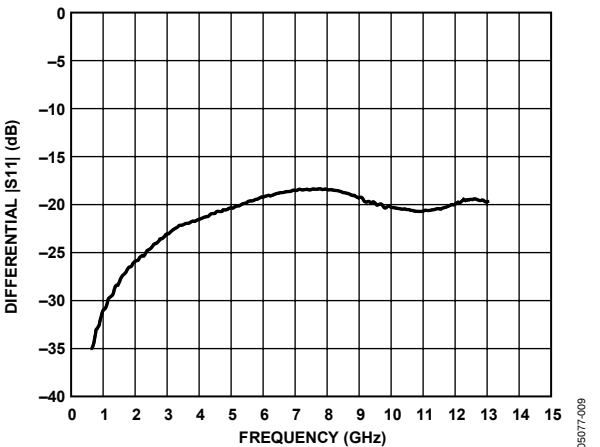


Figure 10. Differential |S11|

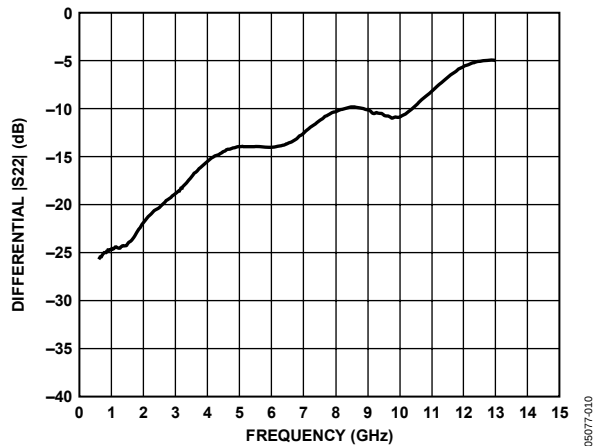


Figure 11. Differential $|S_{22}|$

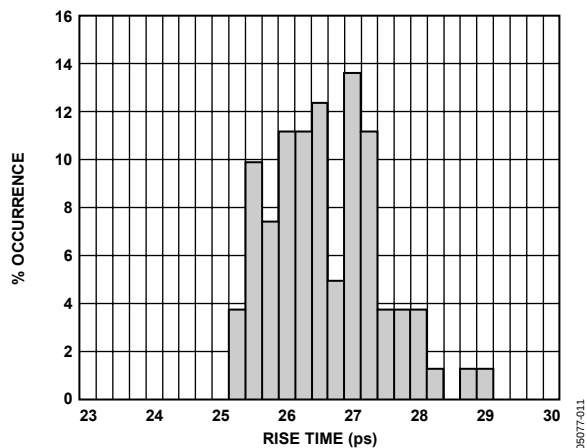


Figure 12. Worst-Case Rise Time Distribution
($V_{CC} = 3.07$ V, $I_{BIAS} = 100$ mA, $I_{MOD} = 80$ mA, $T_A = 85^\circ\text{C}$)

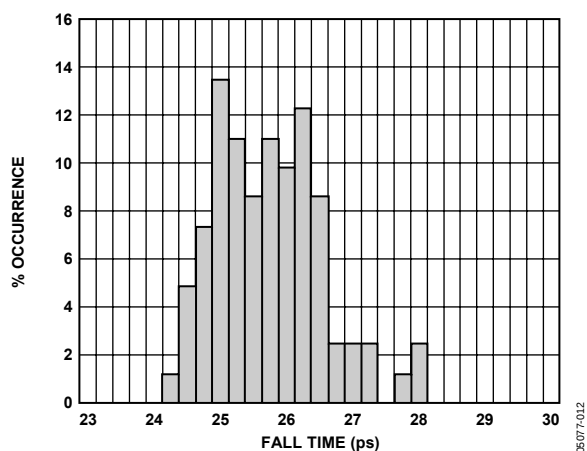


Figure 13. Worst-Case Fall Time Distribution
($V_{CC} = 3.07$ V, $I_{BIAS} = 100$ mA, $I_{MOD} = 80$ mA, $T_A = 85^\circ\text{C}$)

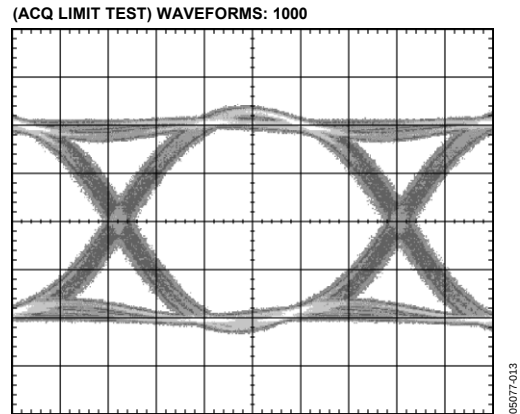


Figure 14. Electrical Eye Diagram
(10.7 Gbps, PRBS31, IMOD = 80 mA)

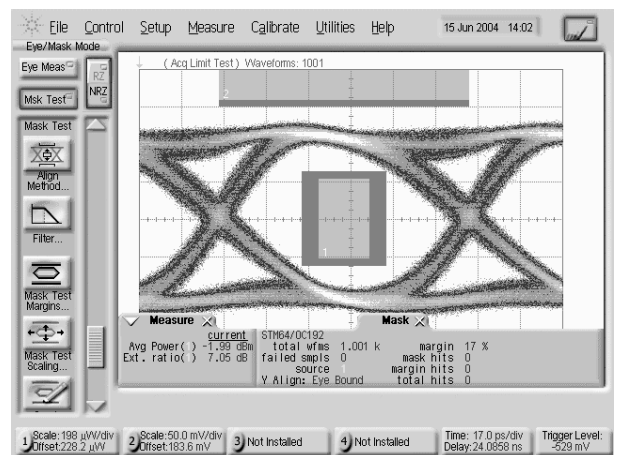


Figure 15. Filtered SONET OC192 Optical Eye Diagram (for Reference)
(PRBS31 Pattern, $P_{AV} = -2$ dBm, ER = 7 dB, 17% Mask Margin, NEC NX8341UJ TOSA)

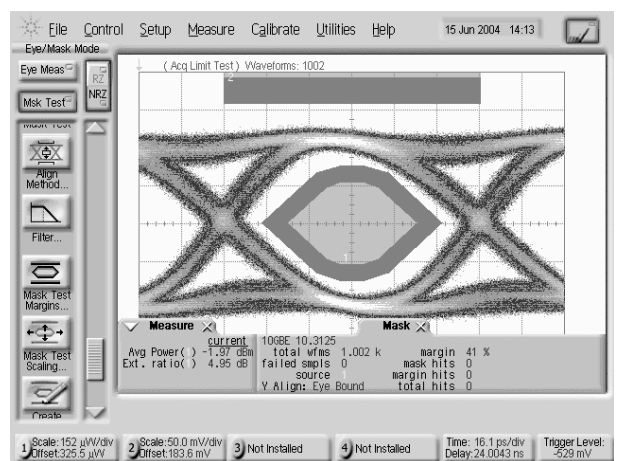


Figure 16. Filtered 10G Ethernet Optical Eye
(PRBS31 Pattern, $P_{AV} = -2$ dBm, ER = 5 dB, 41% Mask Margin, NEC NX8341UJ TOSA)

ADN2525

The equivalent circuits of the BSET, IBIAS, and IBMON pins are shown in Figure 20, Figure 21, and Figure 22.

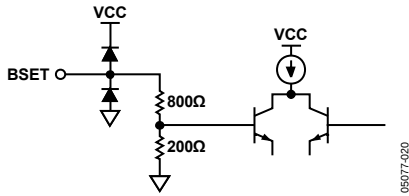


Figure 20. Equivalent Circuit of the BSET Pin

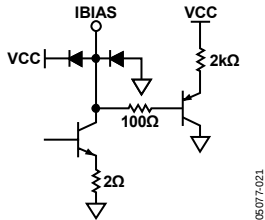


Figure 21. Equivalent Circuit of the IBIAS Pin

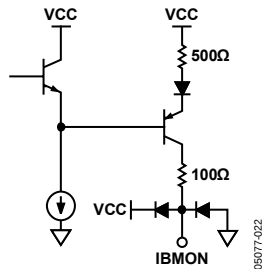


Figure 22. Equivalent Circuit of the IBMON Pin

The recommended configuration for BSET, IBIAS, and IBMON is shown in Figure 23.

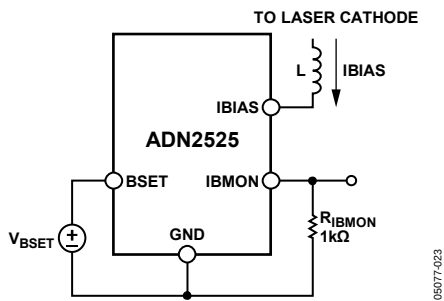


Figure 23. Recommended Configuration for the BSET, IBIAS, and IBMON Pins

The circuit used to drive the BSET voltage must be able to drive the 1 kΩ input resistance of the BSET pin. For proper operation of the bias current source, the voltage at the IBIAS pin must be between the compliance voltage specifications for this pin over supply, temperature, and bias current range (see Table 1). The maximum compliance voltage is specified for only two bias current levels (10 mA and 100 mA), but it can be calculated for any bias current by

$$V_{\text{COMPLIANCE_MAX}} (V) = V_{\text{CC}} (V) - 0.75 - 4.4 \times \text{IBIAS} (A)$$

See the Applications Information section for examples of headroom calculations.

The function of the inductor L is to isolate the capacitance of the IBIAS output from the high frequency signal path. For recommended components, see Table 6.

AUTOMATIC LASER SHUTDOWN (ALS)

The ALS pin is a digital input that enables/disables both the bias and modulation currents, depending on the logic state applied, as shown in Table 5.

Table 5.

ALS Logic State	IBIAS and IMOD
High	Disabled
Low	Enabled
Floating	Enabled

The ALS pin is compatible with 3.3 V CMOS and TTL logic levels. Its equivalent circuit is shown in Figure 24.

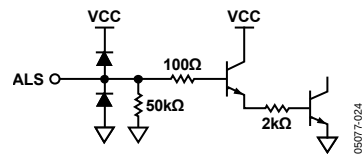


Figure 24. Equivalent Circuit of the ALS Pin

MODULATION CURRENT

The modulation current can be controlled by applying a dc voltage to the MSET pin. This voltage is converted into a dc current by using a voltage-to-current converter using an operational amplifier and a bipolar transistor, as shown in Figure 25.

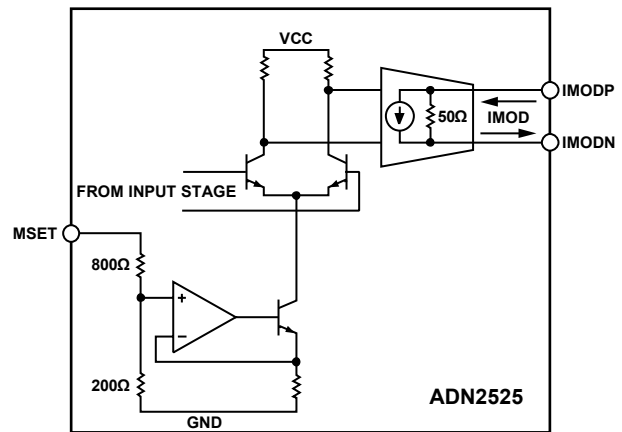


Figure 25. Generation of Modulation Current on the ADN2525

This dc current is switched by the data signal applied to the input stage (DATAP and DATAN pins) and gained up by the output stage to generate the differential modulation current at the IMODP and IMODN pins.

The output stage also generates the active back-termination, which provides proper transmission line termination. Active back-termination uses feedback around an active circuit to synthesize a broadband termination resistance. This provides

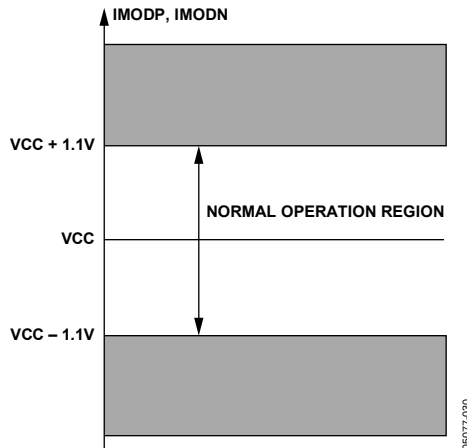


Figure 30. Allowable Range for the Voltage at IMODP and IMODN

LOAD MISTERMINATION

Due to its excellent S22 performance, the ADN2525 can drive differential loads that range from 5 Ω to 50 Ω . In practice, many TOSAs have differential resistance less than 50 Ω . In this case, with 50 Ω differential transmission lines connecting the ADN2525 to the load, the load end of the transmission lines are mismismatched. This mismatch leads to signal reflections back to the driver. The excellent back-termination in the ADN2525 absorbs these reflections, preventing their reflection back to the load. This enables excellent optical eye quality to be achieved, even when the load end of the transmission lines is significantly mismismatched. The connection between the load and the ADN2525 must be made with 50 Ω differential (25 Ω single-ended) transmission lines so that the driver end of the transmission lines is properly terminated.

POWER CONSUMPTION

The power dissipated by the ADN2525 is given by

$$P = V_{CC} \times \left(\frac{V_{MSET}}{13.5} + I_{SUPPLY} \right) + V_{IBIAS} \times I_{IBIAS}$$

where:

V_{CC} is the power supply voltage.

I_{IBIAS} is the bias current generated by the ADN2525.

V_{MSET} is the voltage applied to the MSET pin.

I_{SUPPLY} is the sum of the current that flows into the VCC, IMODP, and IMODN pins of the ADN2525 when $I_{IBIAS} = I_{MOD} = 0$ expressed in amps (see Table 1).

V_{IBIAS} is the average voltage on the IBIAS pin.

Considering $V_{BSET}/I_{IBIAS} = 10$ as the conversion factor from V_{BSET} to I_{IBIAS} , the dissipated power becomes

$$P = V_{CC} \times \left(\frac{V_{MSET}}{13.5} + I_{SUPPLY} \right) + \frac{V_{BSET}}{10} \times V_{IBIAS}$$

To ensure long-term reliable operation, the junction temperature of the ADN2525 must not exceed 125°C, as specified in

Table 2. For improved heat dissipation, the module's case can be used as heat sink, as shown in Figure 31. A compact optical module is a complex thermal environment, and calculations of device junction temperature using the package θ_{JA} (junction-to-ambient thermal resistance) do not yield accurate results.

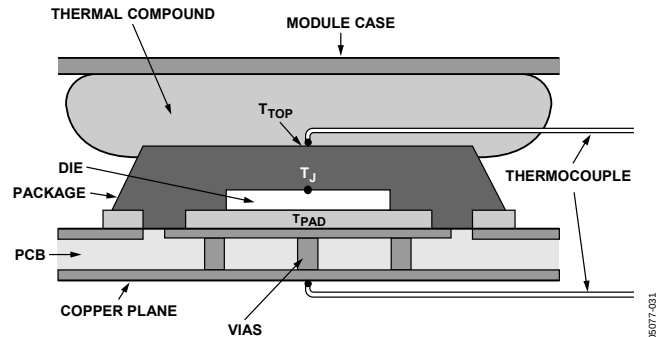


Figure 31. Typical Optical Module Structure

The following procedure can be used to estimate the IC junction temperature:

- T_{TOP} is the temperature at top of package in °C.
- T_{PAD} is the temperature at package exposed paddle in °C.
- T_J is the IC junction temperature in °C.
- P is the power dissipation in W.
- θ_{J-TOP} is the thermal resistance from IC junction to package top.
- θ_{J-PAD} is the thermal resistance from IC junction to package exposed pad.

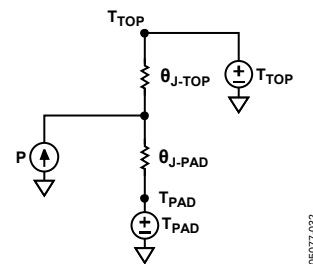


Figure 32. Electrical Model for Thermal Calculations

T_{TOP} and T_{PAD} can be determined by measuring the temperature at points inside the module, as shown in Figure 31. The thermocouples should be positioned to obtain an accurate measurement of the package top and paddle temperatures. Using the model shown in Figure 32, the junction temperature can be calculated by

$$T_J = \frac{P \times (\theta_{J-PAD} \times \theta_{J-TOP}) + T_{TOP} \times \theta_{J-PAD} + T_{PAD} \times \theta_{J-TOP}}{\theta_{J-PAD} + \theta_{J-TOP}}$$

where:

θ_{J-TOP} and θ_{J-PAD} are given in Table 2.

P is the power dissipated by the ADN2525.

DESIGN EXAMPLE

This design example covers:

- Headroom calculations for IBIAS, IMODP, and IMODN pins.
- Calculation of the typical voltage required at the BSET and MSET pins to produce the desired bias and modulation currents.

This design example assumes that the resistance of the TOSA is 25 Ω , the forward voltage of the laser at low current is $V_F = 1$ V, IBIAS = 40 mA, IMOD = 60 mA, and VCC = 3.3 V.

Headroom Calculations

To ensure proper device operation, the voltages on the IBIAS, IMODP, and IMODN pins must meet the compliance voltage specifications in Table 1.

Considering the typical application circuit shown in Figure 33, the voltage at the IBIAS pin can be written as

$$V_{IBIAS} = VCC - V_F - (IBIAS \times R_{TOSA}) - V_{LA}$$

where:

VCC is the supply voltage.

V_F is the forward voltage across the laser at low current.

R_{TOSA} is the resistance of the TOSA.

V_{LA} is the dc voltage drop across L5, L6, L7, and L8.

V_{LB} is the dc voltage drop across L1, L2, L3, and L4.

For proper operation, the minimum voltage at the IBIAS pin should be greater than 0.6 V, as specified by the minimum IBIAS compliance specification in Table 1.

Assuming that the voltage drop across the 25 Ω transmission lines is negligible and that $V_{LA} = 0$ V, $V_F = 1$ V, and IBIAS = 40 mA,

$$V_{IBIAS} = 3.3 - 1 - (0.04 \times 25) = 1.3 \text{ V}$$

$$V_{IBIAS} = 1.3 \text{ V} > 0.6 \text{ V, which satisfies the requirement}$$

The maximum voltage at the IBIAS pin must be less than the maximum IBIAS compliance specification as described by

$$V_{COMPLIANCE_MAX} = VCC - 0.75 - 4.4 \times IBIAS \text{ (A)}$$

For this example:

$$V_{COMPLIANCE_MAX} = VCC - 0.75 - 4.4 \times 0.04 = 2.53 \text{ V}$$

$$V_{IBIAS} = 1.3 \text{ V} < 2.53 \text{ V, which satisfies the requirement}$$

To calculate the headroom at the modulation current pins (IMODP and IMODN), the voltage has a dc component equal to VCC due to the ac-coupled configuration and a swing equal to $IMOD \times 25 \Omega$. For proper operation of the ADN2525, the voltage at each modulation output pin should be within the normal operation region shown in Figure 30.

Assuming $V_{LB} = 0$ V and IMOD = 60 mA, the minimum voltage at the modulation output pins is equal to

$$VCC - (IMOD \times 25)/2 = VCC - 0.75$$

$$VCC - 0.75 > VCC - 1.1 \text{ V, which satisfies the requirement}$$

The maximum voltage at the modulation output pins is equal to

$$VCC + (IMOD \times 25)/2 = VCC + 0.75$$

$$VCC + 0.75 < VCC + 1.1 \text{ V, which satisfies the requirement}$$

Headroom calculations must be repeated for the minimum and maximum values of the required IBIAS and IMOD ranges to ensure proper device operation over all operating conditions.

BSET and MSET Pin Voltage Calculation

To set the desired bias and modulation currents, the BSET and MSET pins of the ADN2525 must be driven with the appropriate dc voltage. The voltage range required at the BSET pin to generate the required IBIAS range can be calculated using the BSET voltage to IBIAS gain specified in Table 1. Assuming that IBIAS = 40 mA and the typical IBIAS/ V_{BSET} ratio of 100 mA/V, the BSET voltage is given by

$$V_{BSET} = \frac{IBIAS \text{ (mA)}}{100 \text{ mA/V}} = \frac{40}{100} = 0.4 \text{ V}$$

The BSET voltage range can be calculated using the required IBIAS range and the minimum and maximum BSET voltage to IBIAS gain values specified in Table 1.

The voltage required at the MSET pin to produce the desired modulation current can be calculated using

$$V_{MSET} = \frac{IMOD}{K}$$

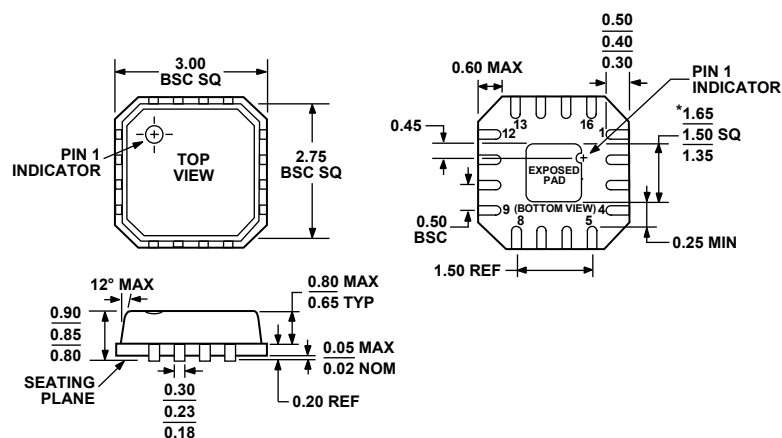
where K is the MSET voltage to IMOD ratio.

The value of K depends on the actual resistance of the TOSA. It can be read using the plot shown in Figure 29. For a TOSA resistance of 25 Ω , the typical value of K = 120 mA/V. Assuming that IMOD = 60 mA and using the preceding equation, the MSET voltage is given by

$$V_{MSET} = \frac{IMOD \text{ (mA)}}{120 \text{ mA/V}} = \frac{60}{120} = 0.5 \text{ V}$$

The MSET voltage range can be calculated using the required IMOD range and the minimum and maximum K values. These can be obtained from the minimum and maximum curves in Figure 29.

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-2
EXCEPT FOR EXPOSED PAD DIMENSION.

Figure 34. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body, Very Thin Quad
(CP-16-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADN2525ACPZ-WP ¹	–40°C to +85°C	16-Lead LFCSP_VQ, 50-Piece Waffle Pack	CP-16-3	F06
ADN2525ACPZ-R2 ¹	–40°C to +85°C	16-Lead LFCSP_VQ, 250-Piece Reel	CP-16-3	F06
ADN2525ACPZ-REEL7 ¹	–40°C to +85°C	16-Lead LFCSP_VQ, 7" 1,500-Piece Reel	CP-16-3	F06

¹ Z = Pb-free part.

ADN2525

NOTES

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- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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