# 16-Bit, Isolated Sigma-Delta Modulator

Data Sheet **AD7402**

## FEATURES

**10 MHz internal clock rate**
**16 bits, no missing codes**
**Signal-to-noise ratio (SNR): 87 dB typical**
**Effective number of bits (ENOB): 13.5 bits typical**
**Typical offset drift vs. temperature: 1.7 µV/°C**
**On-board digital isolator**
**On-board reference**
**Full-scale analog input range: ±320 mV**
**−40°C to +105°C operating range**
**High common-mode transient immunity: >25 kV/µs**
**8-lead, wide-body SOIC, with increased creepage package**
**Slew rate limited output for low electromagnetic interference (EMI)**
**Safety and regulatory approvals**
- **UL recognition**
  - **5000 V rms for 1 minute per UL 1577**
- **CSA Component Acceptance Notice 5A**
- **VDE Certificate of Conformity**
  - **DIN V VDE V 0884-10 (VDE V 0884-10):2006-12**
  - **$V_{IORM}$ = 1250 $V_{PEAK}$**

## APPLICATIONS

**Shunt current monitoring**
**AC motor controls**
**Power and solar inverters**
**Wind turbine inverters**
**Data acquisition systems**
**Analog-to-digital and opto-isolator replacements**

## FUNCTIONAL BLOCK DIAGRAM

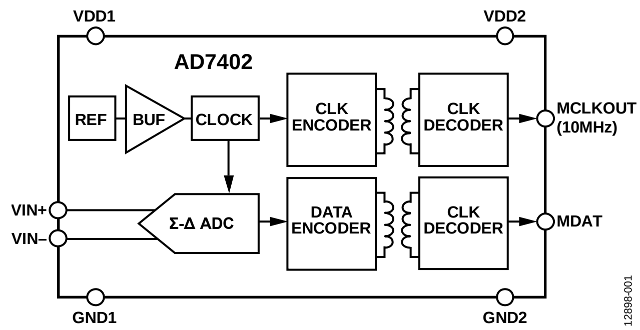


*Figure 1.*

## GENERAL DESCRIPTION

The AD7402[1] is a high performance, second-order, Σ-Δ modulator that converts an analog input signal into a high speed, single-bit data stream, with on-chip digital isolation based on Analog Devices, Inc., *i*Coupler® technology. The AD7402 operates from a 4.5 V to 5.5 V ($V_{DD1}$) power supply and accepts a differential input signal of ±250 mV (±320 mV full scale). The differential input is ideally suited to shunt voltage monitoring in high voltage applications where galvanic isolation is required.

The analog input is continuously sampled by a high performance analog modulator, and converted to a ones density, digital output stream with a data rate of 10 MHz. The original information can be reconstructed with an appropriate digital filter to achieve 87 dB signal to noise ratio (SNR) at 39 kSPS. The serial input/output can use a 3 V to 5.5 V or a 3.3 V supply ($V_{DD2}$).

The serial interface is digitally isolated. High speed complementary metal oxide semiconductor (CMOS) technology, combined with monolithic transformer technology, means the on-chip isolation provides outstanding performance characteristics, superior to alternatives such as optocoupler devices. The AD7402 device is offered in an 8-lead, wide body SOIC package and has an operating temperature range of −40°C to +105°C.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329.

**Rev. A** Document Feedback



**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 781.329.4700**

**Technical Support** **www.analog.com**

# TABLE OF CONTENTS



## REVISION HISTORY

**6/15—Rev. 0 to Rev. A**

Changes to Figure 1 ... 1
Changes to Ordering Guide ... 20

**2/15—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{DD1}$ = 4.5 V to 5.5 V, $V_{DD2}$ = 3 V to 5.5 V, $V_{IN}+$ = −250 mV to +250 mV, $V_{IN}−$ = 0 V, $T_A$ = −40°C to +105°C, tested with sinc3 filter, 256 decimation rate, as defined by Verilog code, unless otherwise noted. All voltages are relative to their respective ground.

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| STATIC PERFORMANCE | | | | | |
| Resolution | 16 | | | Bits | Filter output truncated to 16 bits |
| Integral Nonlinearity (INL)[1] | | ±1 | ±5 | LSB | |
| Differential Nonlinearity (DNL)[1] | | | ±0.99 | LSB | Guaranteed no missed codes to 16 bits |
| Offset Error[1] | | ±0.2 | ±0.75 | mV | |
| Offset Drift vs. Temperature | | 1.7 | 5 | μV/°C | |
| Offset Drift vs. $V_{DD1}$ | | 85 | | μV/V | |
| Gain Error[1] | | 0.2 | ±0.5 | % FSR | |
| Gain Error Drift vs. Temperature | | 18 | 32 | ppm/°C | |
| | | 11 | 20 | μV/°C | |
| Gain Error Drift vs. $V_{DD1}$ | | 0.2 | | mV/V | |
| ANALOG INPUT | | | | | |
| Input Voltage Range | −320 | | +320 | mV | |
| Input Common-Mode Voltage Range | | −200 to +300 | | | |
| Dynamic Input Current | | ±19 | ±28 | μA | $V_{IN}+$ = ±250 mV, $V_{IN}−$ = 0 V |
| | | 0.05 | | μA | $V_{IN}+$ = 0 V, $V_{IN}−$ = 0 V |
| Input Capacitance | | 14 | | pF | |
| DYNAMIC SPECIFICATIONS | | | | | $V_{IN}+$ = 35 Hz |
| Signal-to-(Noise + Distortion) Ratio (SINAD)[1] | 74 | 82 | | dB | |
| Signal-to-Noise Ratio (SNR)[1] | 86 | 87 | | dB | |
| Total Harmonic Distortion (THD)[1] | | −84 | | dB | |
| Peak Harmonic or Spurious Noise (SFDR)[1] | | −84 | | dB | |
| Effective Number of Bits (ENOB)[1] | 12 | 13.5 | | Bits | |
| Noise Free Code Resolution[1] | 14 | | | Bits | |
| ISOLATION TRANSIENT IMMUNITY[1] | 25 | 30 | | kV/μs | |
| LOGIC OUTPUTS | | | | | |
| Output High Voltage, $V_{OH}$ | $V_{DD2}$ − 0.1 | | | V | $I_O$ = −200 μA |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | $I_O$ = +200 μA |
| POWER REQUIREMENTS | | | | | |
| $V_{DD1}$ | 4.5 | | 5.5 | V | |
| $V_{DD2}$ | 3 | | 5.5 | V | |
| $I_{DD1}$ | | 26 | 31 | mA | $V_{DD1}$ = 5.5 V |
| $I_{DD2}$ | | 6 | 7 | mA | $V_{DD2}$ = 5.5 V |
| | | 4.5 | 5.5 | mA | $V_{DD2}$ = 3.3 V |
| POWER DISSIPATION | | | 209 | mW | $V_{DD1}$ = $V_{DD2}$ = 5.5 V |

[1] See the Terminology section.

## TIMING SPECIFICATIONS

$V_{DD1}$ = 4.5 V to 5.5 V, $V_{DD2}$ = 3 V to 5.5 V, $T_A$ = −40°C to +105°C, unless otherwise noted.

**Table 2.**

| Parameter[1] | Min | Typ | Max | Unit | Description |
|---|---|---|---|---|---|
| $f_{MCLKOUT}$[2] | 9.4 | 10 | 10.6 | MHz | Master clock output frequency |
| $t_1$[3] | | | ±10 | ns | Data access time after MCLKOUT rising edge |
| $t_2$[3] | 44 | | | ns | Data hold time after MCLKOUT falling edge |
| $t_3$ | 33 | | | ns | Master clock low time |
| $t_4$ | 33 | | | ns | Master clock high time |

[1] Sample tested during initial release to ensure compliance.
[2] Mark space ratio for clock output is 45/55 to 55/45.
[3] Defined as the time required for the output to cross 0.8 V or 2.0 V for VDD2 = 3 V to 3.6 V, or when the output crosses 0.8 V or 0.7 × VDD2 for VDD2 = 4.5 V to 5.5 V, as outlined in Figure 2. Measured with a ±200 µA load and a 25 pF load capacitance.

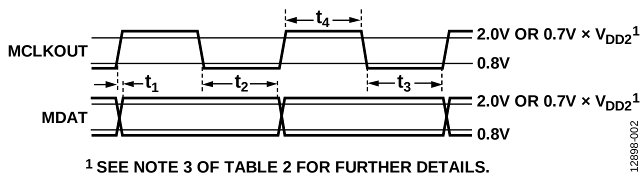


*Figure 2. Data Timing*

## PACKAGE CHARACTERISTICS

Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| Resistance (Input to Output)[1] | $R_{I-O}$ | | $10^{12}$ | | Ω | |
| Capacitance (Input to Output)[1] | $C_{I-O}$ | | 2.2 | | pF | f = 1 MHz |
| IC Junction to Ambient Thermal Resistance | $θ_{JA}$ | | 105 | | °C/W | Thermocouple located at center of package underside, test conducted on 4-layer board with thin traces |

[1] The device is considered a 2-terminal device: Pin 1 to Pin 4 are shorted together, and Pin 5 to Pin 8 are shorted together.

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

| Parameter | Symbol | Value | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| Input-to-Output Momentary Withstand Voltage | $V_{ISO}$ | 5000 min | V | 1-minute duration |
| Minimum External Air Gap (Clearance) | L(I01) | 8.1 min[1, 2] | mm | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L(I02) | 8.1 min[1] | mm | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Internal Gap (Internal Clearance) | | 0.034 min | mm | Insulation distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >400 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | II | | Material Group (DIN VDE 0110, 1/89, Table I) |

[1] In accordance with IEC 60950-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 meters.
[2] Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

## REGULATORY INFORMATION

Table 5.

| UL[1] | CSA | VDE[2] |
|---|---|---|
| Recognized under 1577 Component Recognition Program[1] | Approved under CSA Component Acceptance Notice 5A | Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2] |
| 5000 V rms Isolation Voltage Single Protection | Basic insulation per CSA 60950-1-07 and IEC 60950-1, 810 V rms (1145 $V_{PEAK}$) maximum working voltage[3] | Reinforced insulation per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12, 1250 $V_{PEAK}$ |
| | Reinforced insulation per CSA 60950-1-07 and IEC 60950-1, 405 V rms (583 $V_{PEAK}$) maximum working voltage[3] | |
| | Reinforced insulation per IEC 60601-1, 250 V rms (353 $V_{PEAK}$) maximum working voltage | |
| File E214100 | File 205078 | File 2471900-4880-0001 |

[1] In accordance with UL 1577, each AD7402-8 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 15 µA).
[2] In accordance with DIN V VDE V 0884-10, each AD7402-8 is proof tested by applying an insulation test voltage ≥ 2344 $V_{PEAK}$ for 1 second (partial discharge detection limit = 5 pC).
[3] Rating is calculated for a pollution degree of 2 and a Material Group III. The AD7402 RI-8-1 package material is rated by CSA to a CTI of >400 V and therefore Material Group II.

## DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits.

**Table 6.**

| Description | Symbol | Characteristic | Unit |
|---|---|---|---|
| INSTALLATION CLASSIFICATION PER DIN VDE 0110 | | | |
| For Rated Mains Voltage ≤ 300 V rms | | I to IV | |
| For Rated Mains Voltage ≤ 450 V rms | | I to IV | |
| For Rated Mains Voltage ≤ 600 V rms | | I to IV | |
| For Rated Mains Voltage ≤ 1000V rms | | I to IV | |
| CLIMATIC CLASSIFICATION | | 40/105/21 | |
| POLLUTION DEGREE (DIN VDE 0110, TABLE 1) | | 2 | |
| MAXIMUM WORKING INSULATION VOLTAGE | $V_{IORM}$ | 1250 | $V_{PEAK}$ |
| INPUT TO OUTPUT TEST VOLTAGE, METHOD B1 | $V_{PD(M)}$ | 2344 | $V_{PEAK}$ |
| $V_{IORM}$ × 1.875 = $V_{PR}$, 100% Production Test, $t_m$ = 1 Second, Partial Discharge < 5 pC | | | |
| INPUT TO-OUTPUT TEST VOLTAGE, METHOD A | $V_{PR(M)}$ | | |
| After Environmental Test Subgroup 1 | | 2000 | $V_{PEAK}$ |
| $V_{IORM}$ × 1.6 = $V_{PR}$, $t_m$ = 60 Seconds, Partial Discharge < 5 pC | | | |
| After Input and/or Safety Test Subgroup 2/Safety Test Subgroup 3 | | 1500 | $V_{PEAK}$ |
| $V_{IORM}$ × 1.2 = $V_{PR}$, $t_m$ = 60 Seconds, Partial Discharge < 5 pC | | | |
| HIGHEST ALLOWABLE OVERVOLTAGE (TRANSIENT OVERVOLTAGE, $t_{TR}$ = 10 Seconds) | $V_{IOTM}$ | 8000 | $V_{PEAK}$ |
| SURGE ISOLATION VOLTAGE | | | |
| 1.2 µs Rise Time, 50 µs, 50% Fall Time | $V_{IOSM}$ | 12000 | $V_{PEAK}$ |
| SAFETY LIMITING VALUES (MAXIMUM VALUE ALLOWED IN THE EVENT OF A FAILURE, SEE Figure 3) | | | |
| Case Temperature | $T_S$ | 150 | °C |
| Side 1 ($P_{VDD1}$) and Side 2 ($P_{VDD2}$) Power Dissipation | $P_{SO}$ | 1.19 | W |
| INSULATION RESISTANCE AT $T_S$, $V_{IO}$ = 500 V | $R_{IO}$ | $>10^9$ | Ω |

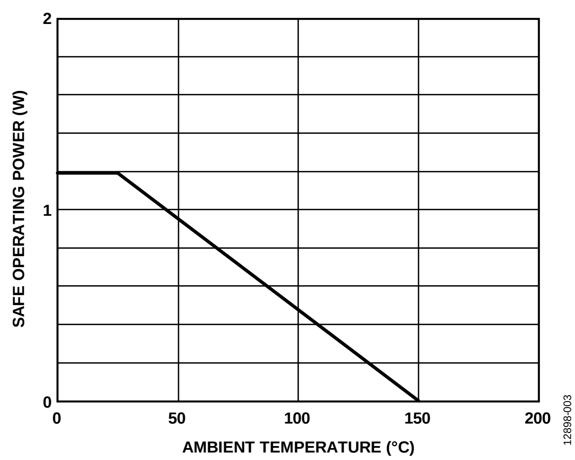


*Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted. All voltages are relative to their respective ground.

**Table 7.**

| Parameter | Rating |
|---|---|
| VDD1 to GND1 | −0.3 V to +6.5 V |
| VDD2 to GND2 | −0.3 V to +6.5 V |
| Analog Input Voltage to GND1 | −1 V to $V_{DD1}$ + 0.3 V |
| Output Voltage to GND2 | −0.3 V to $V_{DD2}$ + 0.3 V |
| Input Current to Any Pin Except Supplies[1] | ±10 mA |
| Operating Temperature Range | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| Pb-Free Temperature, Soldering | |
| Reflow | 260°C |
| ESD | 2 kV |
| FICDM[2] | ±1250 V |
| HBM[3] | ± 4000 V |

[1] Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) to latch up.
[2] JESD22-C101; RC network: 1 Ω, package capacitance ($C_{PKG}$); Class: IV.
[3] ESDA/JEDEC JS-001-2011; RC network: 1.5 kΩ, 100 pF; Class: 3A.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

**Table 8. Maximum Continuous Working Voltage[1]**

| Parameter | Max | Unit | Constraint |
|---|---|---|---|
| AC Voltage | | | |
| Bipolar Waveform | 1250 | $V_{PEAK}$ | 20-year minimum lifetime (VDE approved working voltage) |
| Unipolar Waveform | 1250 | $V_{PEAK}$ | 20-year minimum lifetime |
| DC Voltage | 1250 | $V_{PEAK}$ | 20-year minimum lifetime |

[1] Refers to continuous voltage magnitude imposed across the isolation barrier.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

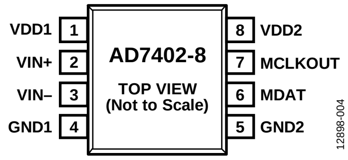


*Figure 4. Pin Configuration*

**Table 9. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | VDD1 | Supply Voltage, 4.5 V to 5.5 V. This is the supply voltage for the isolated side of the AD7402 and is relative to GND1. |
| 2 | VIN+ | Positive Analog Input. |
| 3 | VIN− | Negative Analog Input. Normally connected to GND1. |
| 4 | GND1 | Ground 1. This is the ground reference point for all circuitry on the isolated side. |
| 5 | GND2 | Ground 2. This is the ground reference point for all circuitry on the nonisolated side. |
| 6 | MDAT | Serial Data Output. The single bit modulator output is supplied to this pin as a serial data stream. The bits are clocked out on the rising edge of the MCLKOUT input and are valid on the following MCLKOUT falling edge. |
| 7 | MCLKOUT | Master Clock Logic Output, 10 MHz (Typical). The bit stream from the modulator is valid on the falling edge of MCLKOUT. |
| 8 | VDD2 | Supply Voltage, 3 V to 5.5 V. This is the supply voltage for the nonisolated side and is relative to GND2. |

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, VDD1 = 5 V, VDD2 = 5 V, using sinc3 filter with a 256 oversampling ratio (OSR), unless otherwise noted.

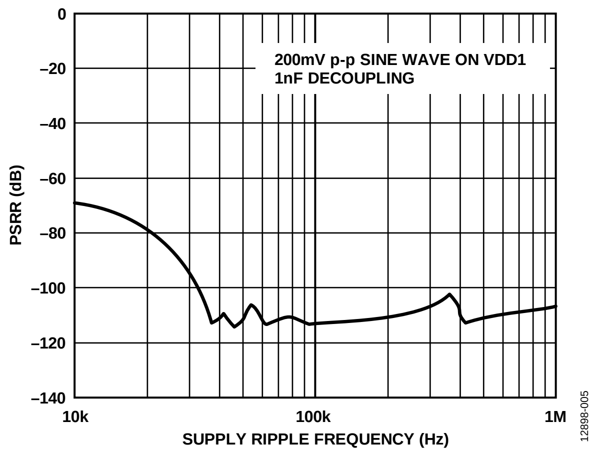


*Figure 5. PSRR vs. Supply Ripple Frequency*

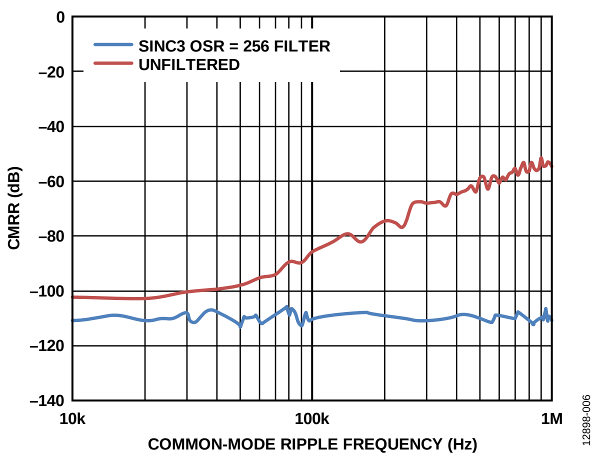


*Figure 6. CMRR vs. Common-Mode Ripple Frequency*

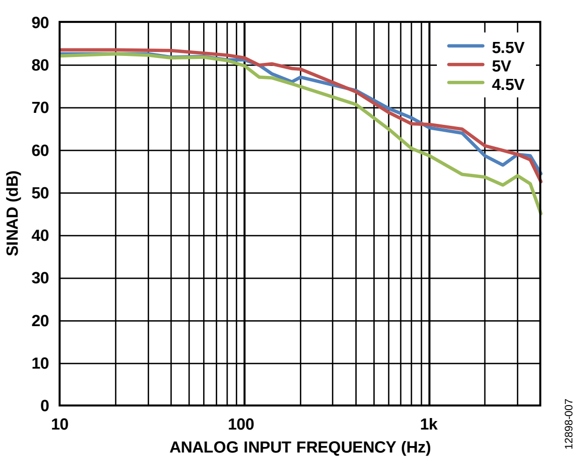


*Figure 7. SINAD vs. Analog Input Frequency*

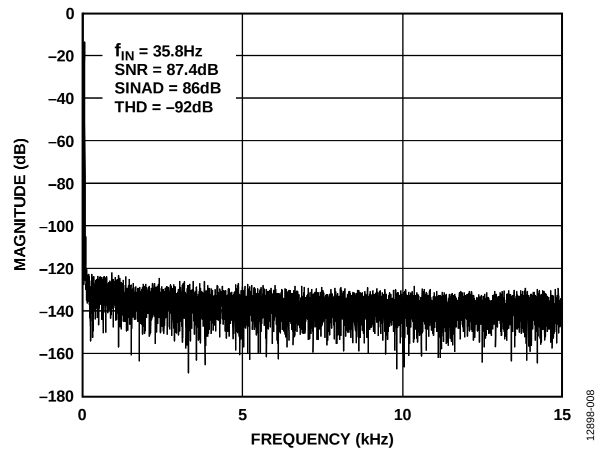


*Figure 8. Fast Fourier Transform (FFT)*

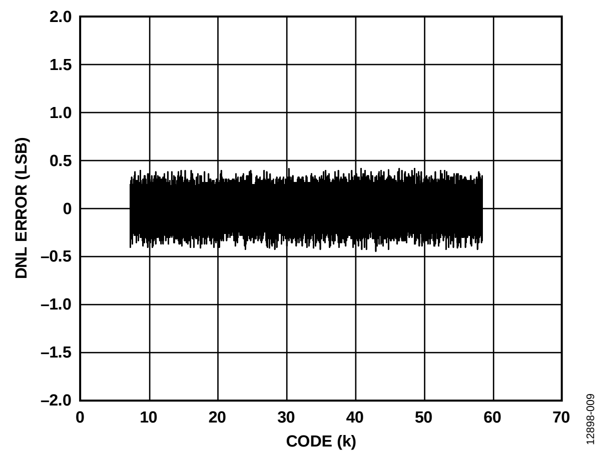


*Figure 9. Typical DNL Error*

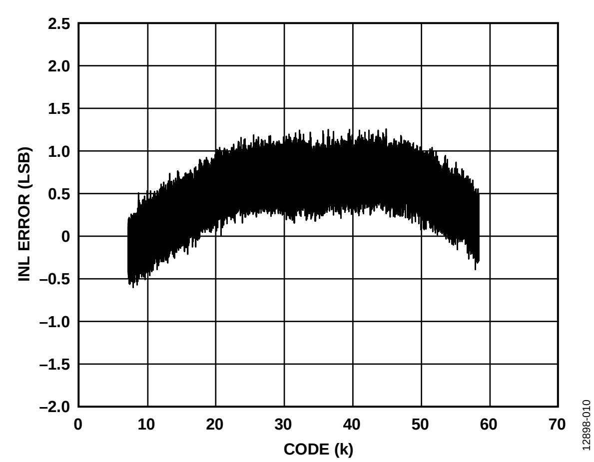


*Figure 10. Typical INL Error*

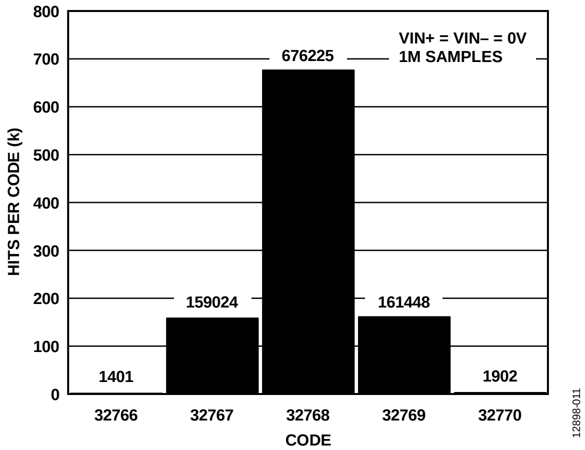


*Figure 11. Histogram of Codes at Code Center*

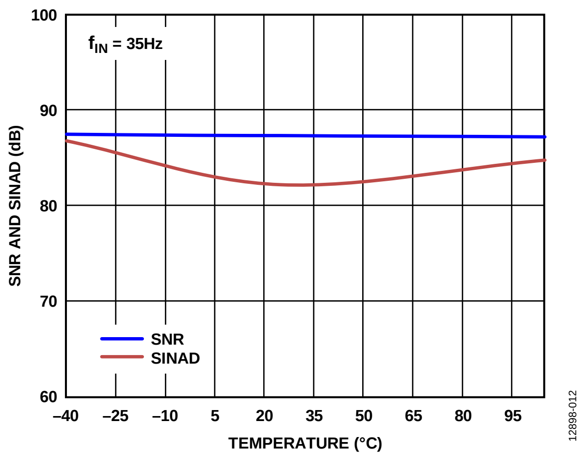


*Figure 12. SNR and SINAD vs. Temperature*

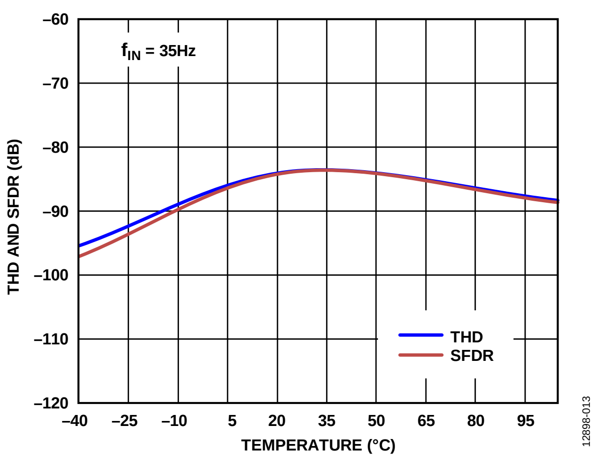


*Figure 13. THD and SFDR vs. Temperature*

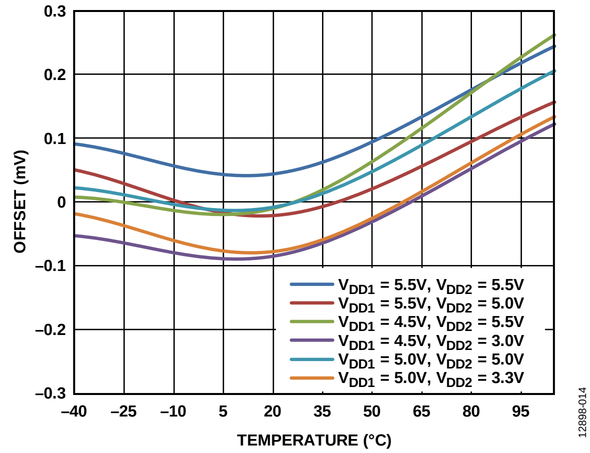


*Figure 14. Offset vs. Temperature*

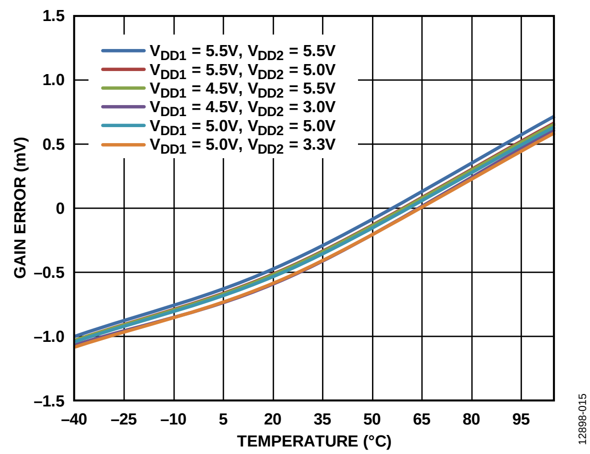


*Figure 15. Gain Error vs. Temperature*

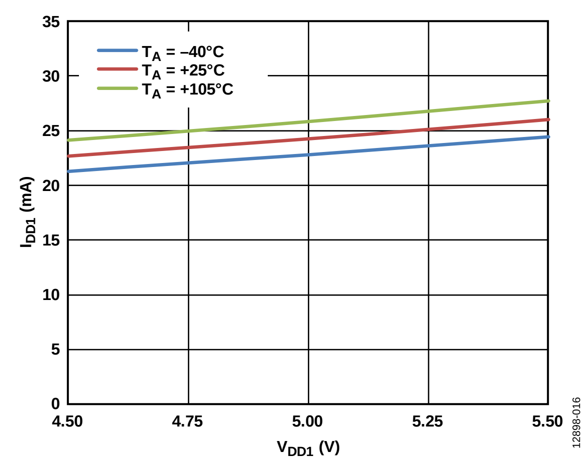


*Figure 16. $I_{DD1}$ vs. $V_{DD1}$ at Various Temperatures*

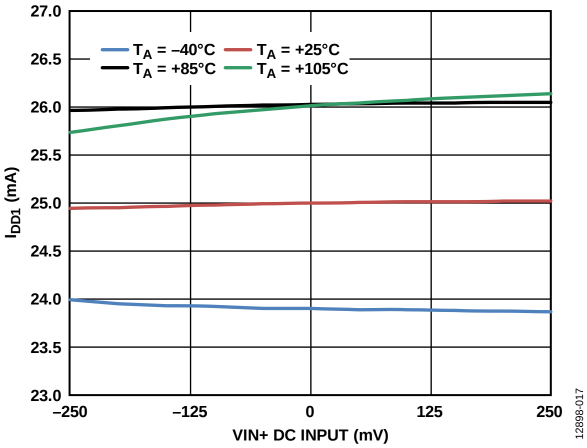


Figure 17. $I_{DD1}$ vs. VIN+ DC Input at Various Temperatures

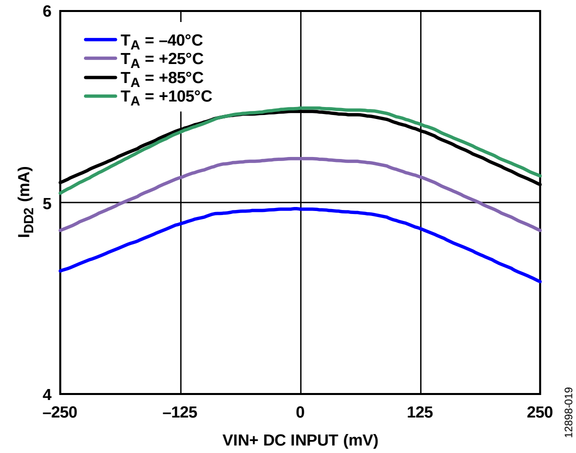


Figure 19. $I_{DD2}$ vs. VIN+ DC Input at Various Temperatures

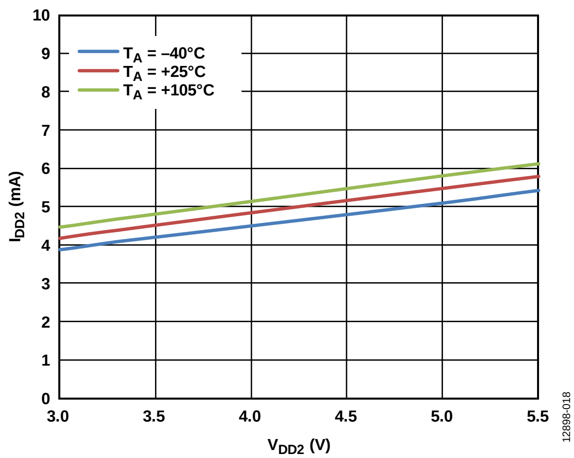


Figure 18. $I_{DD2}$ vs. $V_{DD2}$ at Various Temperatures

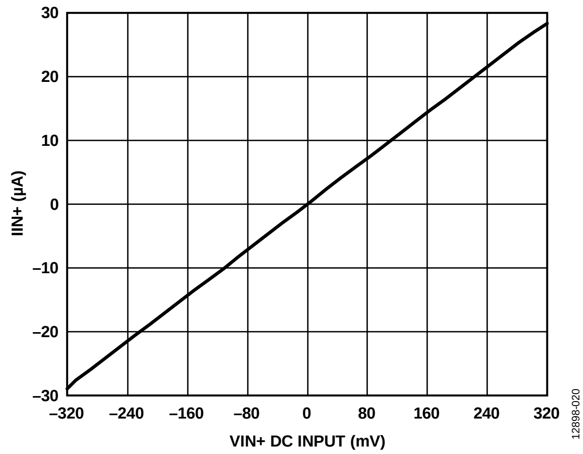


Figure 20. IIN+ vs. VIN+ DC Input

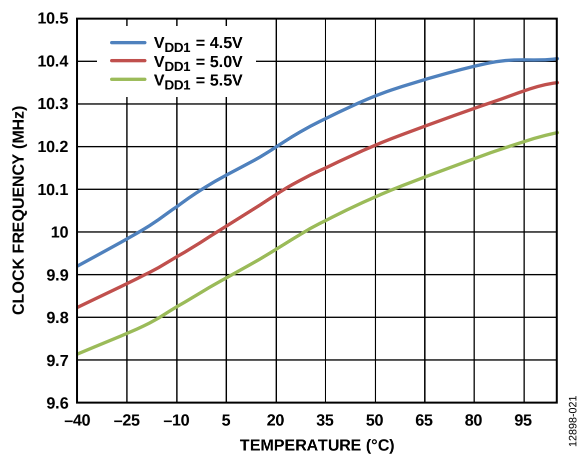


Figure 21. Clock Frequency vs. Temperature for Various Supply Voltages

# TERMINOLOGY

**Differential Nonlinearity (DNL)**
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

**Integral Nonlinearity (INL)**
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are specified negative full scale, −250 mV ($V_{IN+} − V_{IN−}$), Code 7168 for the 16-bit level, and specified positive full scale, +250 mV ($V_{IN+} − V_{IN−}$), Code 58,368 for the 16-bit level.

**Offset Error**
Offset error is the deviation of the midscale code (32,768 for the 16-bit level) from the ideal $V_{IN+} − V_{IN−}$ (that is, 0 V).

**Gain Error**
The gain error includes both positive full-scale gain error and negative full-scale gain error. Positive full-scale gain error is the deviation of the specified positive full-scale code (58,368 for the 16-bit level) from the ideal $V_{IN+} − V_{IN−}$ (250 mV) after the offset error is adjusted out. Negative full-scale gain error is the deviation of the specified negative full-scale code (7168 for the 16-bit level) from the ideal $V_{IN+} − V_{IN−}$ (−250 mV) after the offset error is adjusted out.

**Signal-to-Noise-and-Distortion Ratio (SINAD)**
SINAD is the measured ratio of signal to noise and distortion at the output of the ADC. The signal is the rms value of the sine wave, and noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), including harmonics, but excluding dc.

**Signal-to-Noise Ratio (SNR)**
SNR is the measured ratio of signal to noise at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc.

The ratio is dependent on the number of quantization levels in the digitization process: the greater the number of levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for an ideal N-bit converter with a sine wave input is given by

$$\textit{Signal-to-Noise Ratio} = (6.02N + 1.76)\ \text{dB}$$

Therefore, for a 12-bit converter, the SNR is 74 dB.

**Isolation Transient Immunity**
The isolation transient immunity specifies the rate of rise and fall of a transient pulse applied across the isolation boundary, beyond which clock or data is corrupted. The AD7402 was tested using a transient pulse frequency of 100 kHz.

**Total Harmonic Distortion (THD)**
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7402, it is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
$V_1$ is the rms amplitude of the fundamental.
$V_2$, $V_3$, $V_4$, $V_5$, and $V_6$ are the rms amplitudes of the second through the sixth harmonics.

**Peak Harmonic or Spurious Noise (SFDR)**
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

**Effective Number of Bits (ENOB)**
ENOB is defined by

$$ENOB = (SINAD − 1.76)/6.02\ \text{bits}$$

**Noise Free Code Resolution**
Noise free code resolution represents the resolution in bits for which there is no code flicker. The noise free code resolution for an N-bit converter is defined as

$$\textit{Noise Free Code Resolution (Bits)} = \log_2(2^N/\textit{Peak-to-Peak Noise})$$

The peak-to-peak noise in LSBs is measured with $V_{IN+} = V_{IN−} = 0$ V.

**Common-Mode Rejection Ratio (CMRR)**
CMRR is defined as the ratio of the power in the ADC output at ±250 mV frequency, f, to the power of a +250 mV peak-to-peak sine wave applied to the common-mode voltage of $V_{IN+}$ and $V_{IN−}$ of frequency, $f_S$, as

$$CMRR\ (\text{dB}) = 10\log(Pf/Pf_S)$$

where:
$Pf$ is the power at frequency, f, in the ADC output.
$Pf_S$ is the power at frequency, $f_S$, in the ADC output.

**Power Supply Rejection Ratio (PSRR)**
Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the specified full-scale (±250 mV) transition point due to a change in power supply voltage from the nominal value.

# THEORY OF OPERATION

## CIRCUIT INFORMATION

The AD7402 isolated Σ-Δ modulator converts an analog input signal into a high speed (10 MHz maximum), single-bit data stream; the time average single-bit data from the modulator is directly proportional to the input signal. Figure 22 shows a typical application circuit where the AD7402 is used to provide isolation between the analog input, a current sensing resistor or shunt, and the digital output, which is then processed by a digital filter to provide an N-bit word.

## ANALOG INPUT

The differential analog input of the AD7402 is implemented with a switched capacitor circuit. This circuit implements a second-order modulator stage that digitizes the input signal into a single-bit output stream. The sample clock (MCLKOUT) provides the clock signal for the conversion process as well as the output data framing clock. This clock source is internal on the AD7402. The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. A digital stream that accurately represents the analog input over time appears at the output of the converter (see Figure 23).

A differential signal of 0 V ideally results in a stream of alternating 1s and 0s at the MDAT output pin. This output is high 50% of the time and low 50% of the time. A differential input of 250 mV produces a stream of 1s and 0s that are high 89.06% of the time. A differential input of −250 mV produces a stream of 1s and 0s that are high 10.94% of the time.

A differential input of 320 mV ideally results in a stream of all 1s. A differential input of −320 mV ideally results in a stream of all 0s. The absolute full-scale range is ±320 mV and the specified full-scale performance range is ±250 mV, as shown in Table 10.

**Table 10. Analog Input Range**

| Analog Input | Voltage Input (mV) |
|---|---|
| Positive Full-Scale Value | +320 |
| Positive Specified Performance Input | +250 |
| Zero | 0 |
| Negative Specified Performance Input | −250 |
| Negative Full-Scale Value | −320 |

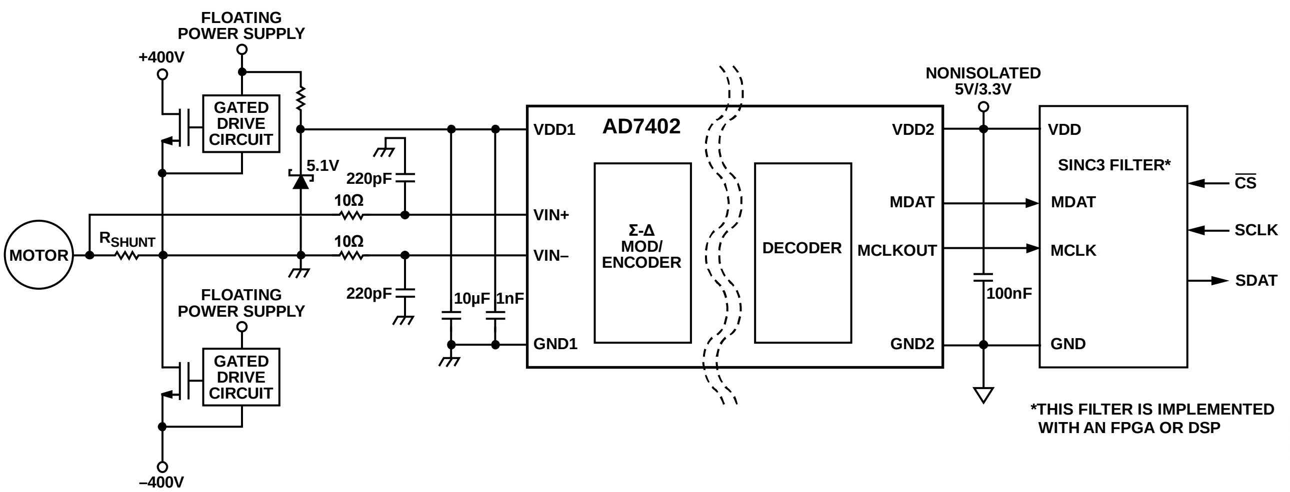


*Figure 22. Typical Application Circuit*

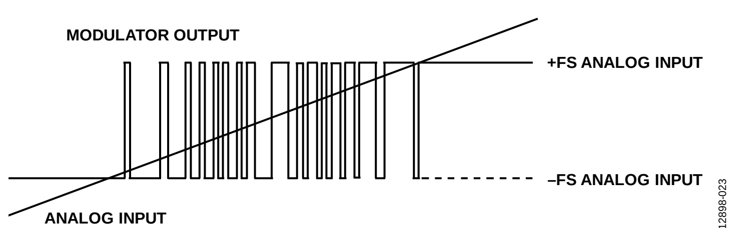


*Figure 23. Analog Input vs. Modulator Output*

To reconstruct the original information, this output must be digitally filtered and decimated. A sinc3 filter is recommended because it is one order higher than that of the AD7402 modulator, which is a second-order modulator. If a 256 decimation rate is used, the resulting 16-bit word rate is 39 kSPS. See the Digital Filter section for more detailed information on the sinc filter implementation. Figure 24 shows the transfer function of the AD7402 relative to the 16-bit output.

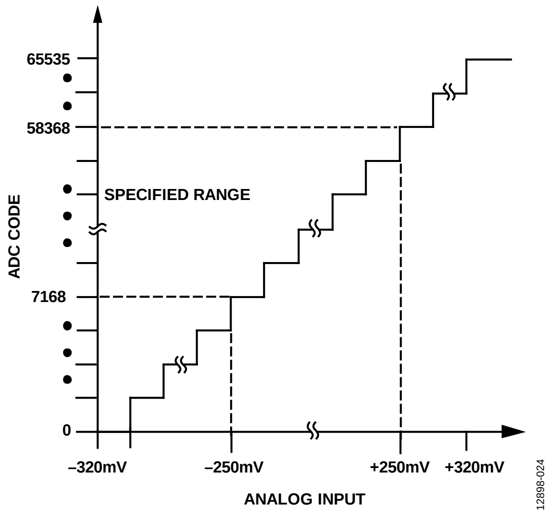


*Figure 24. Filtered and Decimated 16-Bit Transfer Function*

## DIFFERENTIAL INPUTS

The analog input to the modulator is a switched capacitor design. The analog signal is converted into charge by highly linear sampling capacitors. A simplified equivalent circuit diagram of the analog input is shown in Figure 25. A signal source driving the analog input must provide the charge onto the sampling capacitors every half MCLKOUT cycle and settle to the required accuracy within the next half cycle.

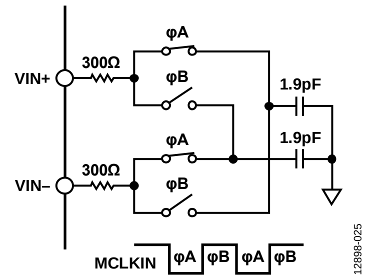


*Figure 25. Analog Input Equivalent Circuit*

Because the AD7402 samples the differential voltage across its analog inputs, low noise performance is attained with an input circuit that provides low common-mode noise at each input.

## DIGITAL OUTPUT

The AD7402 MDAT output driver is a slew rate limited driver. This driver lowers electromagnetic emissions, thus minimizing electromagnetic interference, both conducted and radiated.

# APPLICATIONS INFORMATION

## CURRENT SENSING APPLICATIONS

The AD7402 is ideally suited for current sensing applications where the voltage across a shunt resistor ($R_{SHUNT}$) is monitored. The load current flowing through an external shunt resistor produces a voltage at the input terminals of the AD7402. The AD7402 provides isolation between the analog input from the current sensing resistor and the digital outputs. By selecting the appropriate shunt resistor value, a variety of current ranges can be monitored.

### *Choosing $R_{SHUNT}$*

The shunt resistor ($R_{SHUNT}$) values used in conjunction with the AD7402 are determined by the specific application requirements in terms of voltage, current, and power. Small resistors minimize power dissipation, whereas low inductance resistors prevent any induced voltage spikes, and good tolerance devices reduce current variations. The final values chosen are a compromise between low power dissipation and accuracy. Higher value resistors use the full performance input range of the ADC, thus achieving maximum SNR performance. Low value resistors dissipate less power but do not use the full performance input range. The AD7402, however, delivers excellent performance, even with lower input signal levels, allowing low value shunt resistors to be used while maintaining system performance.

To choose a suitable shunt resistor, first determine the current through the shunt. The shunt current for a 3-phase induction motor can be expressed as

$$I_{RMS} = \frac{P_W}{1.73 \times V \times EF \times PF}$$

where:
$I_{RMS}$ is the motor phase current (A rms)
$P_W$ is the motor power (Watts)
$V$ is the motor supply voltage (V ac)
$EF$ is the motor efficiency (%)
$PF$ is the power efficiency (%)

To determine the shunt peak sense current, $I_{SENSE}$, consider the motor phase current and any overload that may be possible in the system. When the peak sense current is known, divide the voltage range of the AD7402 (±250 mV) by the peak sense current to yield a maximum shunt value.

If the power dissipation in the shunt resistor is too large, the shunt resistor can be reduced and less of the ADC input range can be used. Figure 26 shows the SINAD performance characteristics and the ENOB of resolution for the AD7402 for different input signal amplitudes. Figure 27 shows the rms noise performance for dc input signal amplitudes. The AD7402 performance at lower input signal ranges allows smaller shunt values to be used while still maintaining a high level of performance and overall system efficiency.

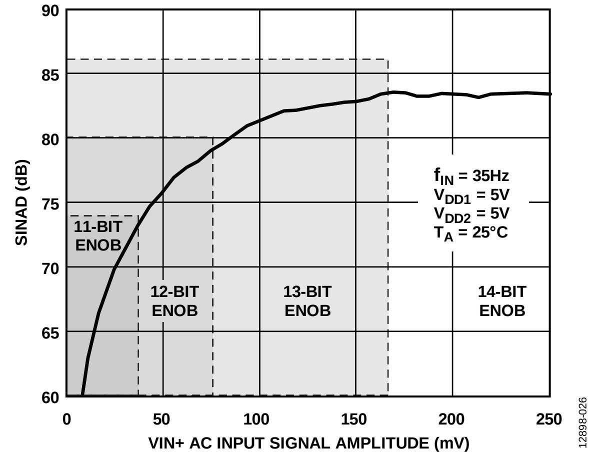


*Figure 26. SINAD vs. $V_{IN+}$ AC Input Signal Amplitude*

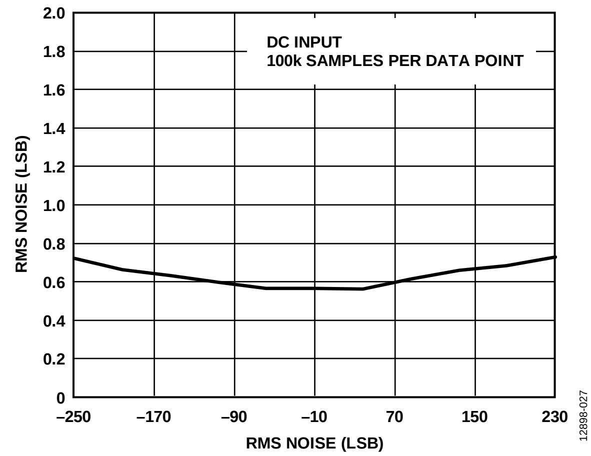


*Figure 27. RMS Noise vs. $V_{IN+}$ DC Input Signal Amplitude*

$R_{SHUNT}$ must be able to dissipate the I2R power losses. If the power dissipation rating of the resistor is exceeded, its value may drift or the resistor may be damaged, resulting in an open circuit. This open circuit can result in a differential voltage across the terminals of the AD7402, in excess of the absolute maximum ratings. If $I_{SENSE}$ has a large high frequency component, choose a resistor with low inductance.

## VOLTAGE SENSING APPLICATIONS

The AD7402 can also be used for isolated voltage monitoring. For example, in motor control applications, it can be used to sense the bus voltage. In applications where the voltage being monitored exceeds the specified analog input range of the AD7402, a voltage divider network can be used to reduce the voltage being monitored to the required range.

## INPUT FILTER

In a typical use case for directly measuring the voltage across a shunt resistor, the AD7402 can be connected directly across the shunt resistor with a simple RC low-pass filter on each input.

The recommended circuit configuration for driving the differential inputs to achieve best performance is shown in Figure 28. An RC low-pass filter is placed on both the analog input pins. Recommended values for the resistors and capacitors are 10 Ω and 220 pF, respectively. If possible, equalize the source impedance on each analog input to minimize offset.

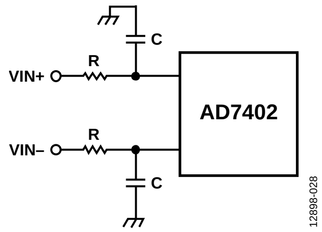


*Figure 28. RC Low-Pass Filter Input Network*

The input filter configuration for the AD7402 is not limited to the low-pass structure shown in Figure 28. The differential RC filter configuration shown in Figure 29 also achieves excellent performance. Recommended values for the resistors and capacitor are 22 Ω and 47 pF, respectively.

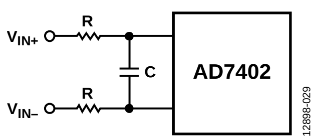


*Figure 29. Differential RC Filter Network*

Figure 30 compares the typical performance for the input filter structures outlined in Figure 28 and Figure 29 for different resistor and capacitor values.

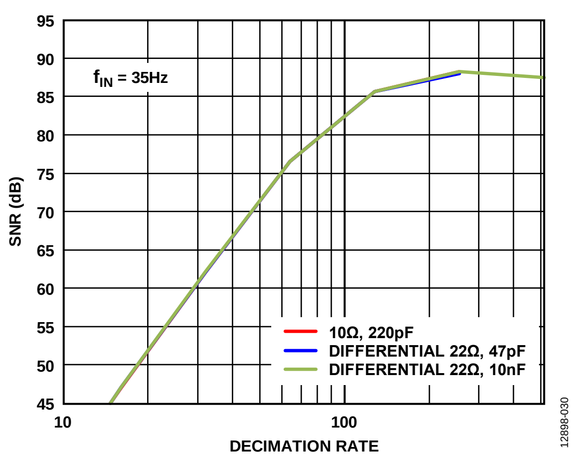


*Figure 30. SNR vs. Decimation Rate for Different Filter Structures for Different Resistor and Capacitor Values*

## DIGITAL FILTER

The output of the AD7402 is a continuous digital bit stream. To reconstruct the original input signal information, this output bit stream needs to be digitally filtered and decimated. A sinc filter is recommended due to its simplicity. A sinc3 filter is recommended because it is one order higher than that of the AD7402 modulator, which is a second-order modulator. The type of filter selected, the decimation rate, and the modulator clock used determines the overall system resolution and throughput rate. The higher the decimation rate, the greater the system accuracy, as illustrated in Figure 31. However, there is a trade-off between accuracy and throughput rate and, therefore, higher decimation rates result in lower throughput solutions.

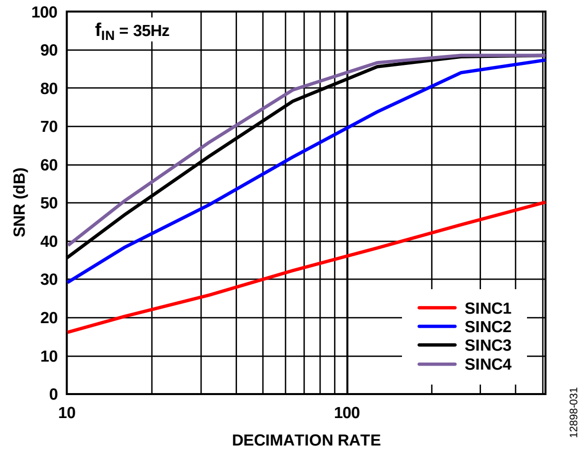


*Figure 31. SNR vs. Decimation Rate for Different Sincx Filter Orders*

A sinc3 filter is recommended for use with the AD7402. This filter can be implemented on a field programmable gate array (FPGA) or a digital signal processor (DSP).

Equation 1 describes the transfer function of a sinc filter.

$$H(z) = \left( \frac{1}{DR} \frac{(1 - Z^{-DR})}{(1 - Z^{-1})} \right)^N \quad (1)$$

where *DR* is the decimation rate and *N* is the sinc filter order.

The throughput rate of the sinc filter is determined by the modulator clock and the decimation rate selected.

$$Throughput = \frac{MCLK}{DR} \quad (2)$$

where *MCLK* is the modulator clock frequency

As the decimation rate increases, the data output size from the sinc filter increases. The output data size is expressed in Equation 3. The 16 most significant bits are used to return a 16-bit result.

$$Data\ size = N \times \log_2 DR \quad (3)$$

For a $sinc^3$ filter, the −3 dB filter response point can be derived from the filter transfer function, Equation 1, and is 0.262 times the throughput rate. The filter characteristics for a third-order sinc filter are summarized in Table 11.

**Table 11. Sinc3 Filter Characteristics for 10 MHz**

| Decimation Ratio (DR) | Throughput Rate (kHz) | Output Data Size (Bits) | Filter Response (kHz) |
|---|---|---|---|
| 32 | 312.5 | 15 | 81.8 |
| 64 | 156.2 | 18 | 40.9 |
| 128 | 78.1 | 21 | 20.4 |
| 256 | 39.1 | 24 | 10.2 |
| 512 | 19.55 | 27 | 5.1 |

The following Verilog code provides an example of a sinc3 filter implementation on a Xilinx® Spartan®-6 FPGA. Note that the data is read on the negative clock edge. It is recommended to read in the data on the negative clock edge. The code is configurable to accommodate decimation rates from 32 to 4096.

```
module dec256sinc24b
(
input mclk1,  /* used to clk filter */
input reset,  /* used to reset filter */
input mdata1, /* input data to be filtered
*/
output reg [15:0] DATA, /* filtered output
*/
output reg data_en,
input [15:0] dec_rate
);

/* Data is read on negative clk edge */

reg [36:0] ip_data1;
reg [36:0] acc1;
reg [36:0] acc2;
reg [36:0] acc3;
reg [36:0] acc3_d2;
reg [36:0] diff1;
reg [36:0] diff2;
reg [36:0] diff3;
reg [36:0] diff1_d;
reg [36:0] diff2_d;

reg [15:0] word_count;

reg word_clk;
reg enable;

/*Perform the Sinc action*/
always @ (mdata1)
if(mdata1==0)
       ip_data1 <= 37'd0;
       /* change 0 to a -1 for twos
complement */
else
       ip_data1 <= 37'd1;

/*Accumulator (Integrator)
Perform the accumulation (IIR) at the speed
of the modulator.
Z = one sample delay MCLKOUT = modulators
conversion bit rate */
```

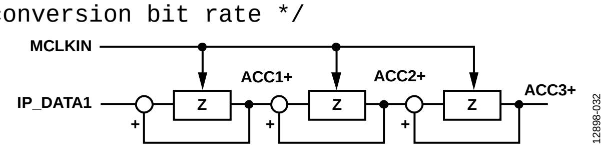


*Figure 32. Accumulator*

```
always @ (negedge mclk1, posedge reset)
begin
       if (reset)
       begin
       /* initialize acc registers on reset
*/
              acc1 <= 37'd0;
              acc2 <= 37'd0;
              acc3 <= 37'd0;
       end
       else
       begin
       /*perform accumulation process */
              acc1 <= acc1 + ip_data1;
              acc2 <= acc2 + acc1;
              acc3 <= acc3 + acc2;
       end
end

/*decimation stage (MCLKOUT/WORD_CLK) */
always @ (negedge mclk1, posedge reset)
begin
       if (reset)
              word_count <= 16'd0;

       else
       begin
              if ( word_count == dec_rate -
1 )
                     word_count <= 16'd0;
              else
                     word_count <= word_count
+ 16'b1;
       end
end

always @ ( negedge mclk1, posedge reset )
begin
       if ( reset )
              word_clk <= 1'b0;
       else
       begin
              if ( word_count == dec_rate/2 -
1 )
                     word_clk <= 1'b1;
              else if ( word_count ==
dec_rate - 1 )
                     word_clk <= 1'b0;
       end
end

/*Differentiator (including decimation
stage)
Perform the differentiation stage (FIR) at a
lower speed.
Z = one sample delay WORD_CLK = output word
rate */
```

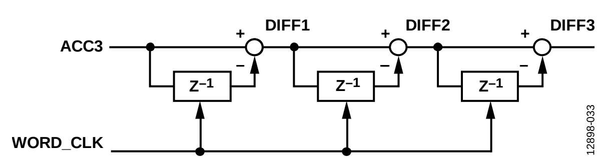


*Figure 33. Differentiator*

```
always @ (negedge word_clk, posedge reset)
begin
       if(reset)
       begin
              acc3_d2 <= 37'd0;
              diff1_d <= 37'd0;
              diff2_d <= 37'd0;
```

```
            diff1 <= 37'd0;
            diff2 <= 37'd0;
            diff3 <= 37'd0;

      end
      else
      begin

            diff1 <= acc3 - acc3_d2;
            diff2 <= diff1 - diff1_d;
            diff3 <= diff2 - diff2_d;
            acc3_d2 <= acc3;
            diff1_d <= diff1;
            diff2_d <= diff2;


      end

end

/* Clock the Sinc output into an output
register
WORD_CLK = output word rate */
```

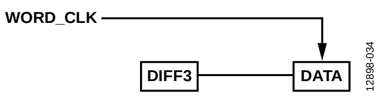


*Figure 34. Clocking Sinc3 Output into an Output Register*

```
always @ (negedge word_clk )
begin

      case ( dec_rate )
            16'd32:begin
                  DATA <= (diff3[15:0] ==
16'h8000) ? 16'hFFFF : {diff3[14:0], 1'b0};
            end
            16'd64:begin
                  DATA <= (diff3[18:2] ==
17'h10000) ? 16'hFFFF : diff3[17:2];
            end
            16'd128:begin
                  DATA <= (diff3[21:5] ==
17'h10000) ? 16'hFFFF : diff3[20:5];
            end
            16'd256:begin
                  DATA <= (diff3[24:8] ==
17'h10000) ? 16'hFFFF : diff3[23:8];
            end
            16'd512:begin
                  DATA <= (diff3[27:11] ==
17'h10000) ? 16'hFFFF : diff3[26:11];
            end
            16'd1024:begin
                  DATA <= (diff3[30:14] ==
17'h10000) ? 16'hFFFF : diff3[29:14];
            end
            16'd2048:begin
                  DATA <= (diff3[33:17] ==
17'h10000) ? 16'hFFFF : diff3[32:17];
            end
            16'd4096:begin
                  DATA <= (diff3[36:20] ==
17'h10000) ? 16'hFFFF : diff3[35:20];
            end
            default:begin
                  DATA <= (diff3[24:8] ==
17'h10000) ? 16'hFFFF : diff3[23:8];
            end
      endcase

end

/* Synchronize Data Output*/
always@ (negedge mclk1, posedge reset )
begin
      if ( reset )
      begin
            data_en <= 1'b0;
            enable <= 1'b1;
      end
      else
      begin
            if ( (word_count == dec_rate/2
- 1) && enable )
            begin
                  data_en <= 1'b1;
                  enable <= 1'b0;
            end
            else if ( (word_count ==
dec_rate - 1)  && ~enable )
            begin
                  data_en <= 1'b0;
                  enable <= 1'b1;
            end
            else
                  data_en <= 1'b0;

      end
end

endmodule
```

## POWER SUPPLY CONSIDERATIONS

The AD7402 requires a 5 V VDD1 supply, and there are various means of achieving this. One method is to use an isolated dc-to-dc converter such as the ADuM6000. This method provides a 5 V regulated dc supply across the isolation barrier. Note that the inherent isolation of the ADuM6000 is lower than the AD7402.

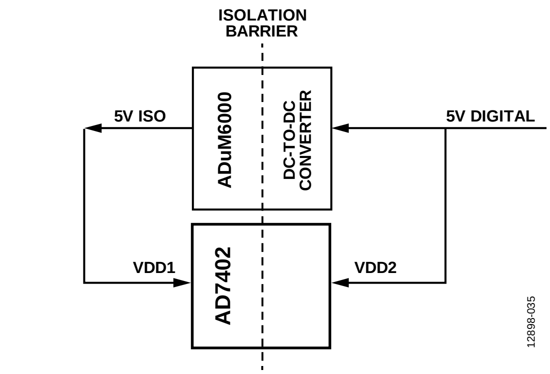


*Figure 35. ADuM6000 Isolated 5 V DC-to-DC Regulator Example*

Another method is to regulate a dc supply on the high voltage side of the isolation barrier using a step-down dc-to-dc regulator, such as the ADP2441.

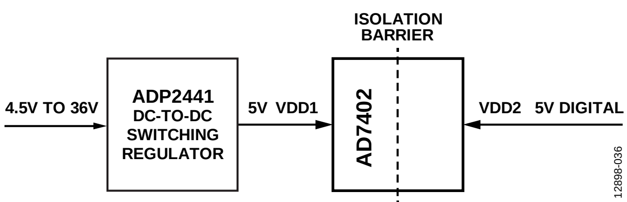


*Figure 36. ADP2441 Step-Down DC-to-DC Regulator Example*

## GROUNDING AND LAYOUT

It is recommended to decouple the $V_{DD1}$ supply with a 10 µF capacitor in parallel with a 1 nF capacitor to $GND_1$. Decouple the $V_{DD2}$ supply with a 100 nF value to $GND_2$. In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout so that any coupling that occurs equally affects all pins on a given component side. Failure to ensure equal coupling can cause voltage differentials between pins to exceed the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage. Place any decoupling used as close to the supply pins as possible.

Minimize series resistance in the analog inputs to avoid any distortion effects, especially at high temperatures. If possible, equalize the source impedance on each analog input to minimize offset. Check for mismatch and thermocouple effects on the analog input printed circuit board (PCB) tracks to reduce offset drift.

## INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the AD7402.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 8 summarize the peak voltage for 20 years of service life for a bipolar, ac operating condition and the maximum VDE approved working voltages.

These tests subjected the AD7402 to continuous cross isolation voltages. To accelerate the occurrence of failures, the selected test voltages were values exceeding those of normal use. The time to failure values of these units were recorded and used to calculate the acceleration factors. These factors were then used to calculate the time to failure under the normal operating conditions. The values shown in Table 8 are the lesser of the following two values:

- The value that ensures at least a 20-year lifetime of continuous use.
- The maximum VDE approved working voltage.

Note that the lifetime of the AD7402 varies according to the waveform type imposed across the isolation barrier. The *i*Coupler insulation structure is stressed differently, depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 37, Figure 38, and Figure 39 illustrate the different isolation voltage waveforms.

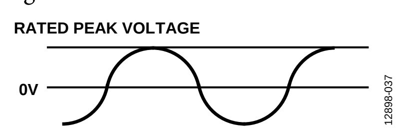


*Figure 37. Bipolar AC Waveform, 50 Hz or 60 Hz*

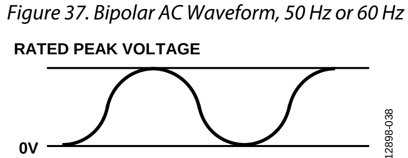


*Figure 38. Unipolar AC Waveform, 50 Hz or 60 Hz*

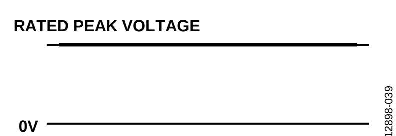


*Figure 39. DC Waveform*

# OUTLINE DIMENSIONS

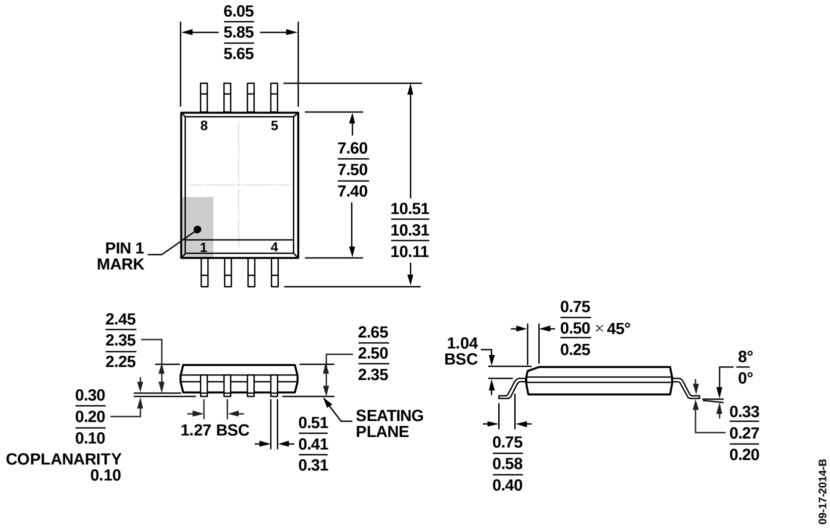


*Figure 40. 8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]*
*Wide Body*
*(RI-8-1)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD7402-8BRIZ | −40°C to +105°C | 8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC] | RI-8-1 |
| AD7402-8BRIZ-RL | −40°C to +105°C | 8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC] | RI-8-1 |
| AD7402-8BRIZ-RL7 | −40°C to +105°C | 8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC] | RI-8-1 |
| EVAL-AD7402-8FMCZ | | Evaluation Board | |

[1] Z = RoHS Compliant Part.

LifeElectronics
Живое партнерство

ООО «ЛайфЭлектроникс» "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

*Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.*

*С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров*

*Мы предлагаем:*

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

*В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.*

*Конструкторский отдел помогает осуществить:*

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

*Тел: +7 (812) 336 43 04 (многоканальный)*
*Email: org@lifeelectronics.ru*

***www.lifeelectronics.ru***