

ADG451/ADG452/ADG453
FEATURES

- Low on resistance (4 Ω)**
- On resistance flatness (0.2 Ω)**
- 44 V supply maximum ratings**
- ±15 V analog signal range**
- Fully specified at ±5 V, 12 V, ±15 V**
- Ultralow power dissipation (18 μW)**
- ESD 2 kV**
- Continuous current (100 mA)**
- Fast switching times**
- t_{ON} 70 ns**
- t_{OFF} 60 ns**
- TTL-/CMOS-compatible**
- Pin-compatible upgrade for ADG411/ADG412/ADG413 and ADG431/ADG432/ADG433**

APPLICATIONS

- Relay replacement**
- Audio and video switching**
- Automatic test equipment**
- Precision data acquisition**
- Battery-powered systems**
- Sample-and-hold systems**
- Communication systems**
- PBX, PABX systems**
- Avionics**

GENERAL DESCRIPTION

The ADG451/ADG452/ADG453 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process that provides low power dissipation yet gives high switching speed and low on resistance.

The on resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals. Fast switching speed, coupled with high signal bandwidth, makes the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

The ADG451/ADG452/ADG453 contain four independent, single-pole/single-throw (SPST) switches. The ADG451 and ADG452 differ only in that the digital control logic is inverted. The ADG451 switches are turned on with a logic low on the appropriate control input, while a logic high is required for the ADG452.

Rev. C

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FUNCTIONAL BLOCK DIAGRAMS


SWITCHES SHOWN FOR A LOGIC 1 INPUT.

Figure 1. ADG451

05239-001



SWITCHES SHOWN FOR A LOGIC 1 INPUT.

Figure 2. ADG452

05239-101



SWITCHES SHOWN FOR A LOGIC 1 INPUT.

Figure 3. ADG453

05239-102

The ADG453 has two switches with digital control logic similar to that of the ADG451, while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when on, and each has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

The ADG453 exhibits break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

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REVISION HISTORY

10/06—Rev. B to Rev. C

| | |
|---------------------------------|----|
| Changes to Table 4..... | 9 |
| Changes to Ordering Guide | 18 |

12/04—Rev. A to Rev. B

| | |
|-------------------------------------------------------------------------|-----------|
| Updated Format..... | Universal |
| Changes to Specifications Section | 3 |
| Changes to Absolute Maximum Ratings Section | 8 |
| Changes to Pin Configuration and Function Descriptions Section | 9 |
| Updated Outline Dimensions | 16 |
| Changes to Ordering Guide | 17 |

2/98—Rev. 0 to Rev. A

10/97—Revision 0: Initial Version

PRODUCT HIGHLIGHTS

1. Low R_{ON} (5 Ω maximum).
2. Ultralow Power Dissipation.
3. Extended Signal Range.
The ADG451/ADG452/ADG453 are fabricated on an enhanced LC²MOS process, giving an increased signal range that fully extends to the supply rails.
4. Break-Before-Make Switching.
This prevents channel shorting when the switches are configured as a multiplexer (ADG453 only.)
5. Single-Supply Operation.
For applications in which the analog signal is unipolar, the ADG451/ADG452/ADG453 can be operated from a single rail power supply. The parts are fully specified with a single 12 V power supply and remain functional with single supplies as low as 5.0 V.
6. Dual-Supply Operation.
For applications where the analog signal is bipolar, the ADG451/ADG452/ADG453 can be operated from a dual power supply ranging from ± 4.5 V to ± 20 V.

ADG451/ADG452/ADG453

SPECIFICATIONS

15 V DUAL SUPPLY

$V_{DD} = 15\text{ V}$, $V_{SS} = -15\text{ V}$, $V_L = 5\text{ V}$, $GND = 0\text{ V}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 1.

| Parameter | B Version ¹ | | Unit | Test Conditions/Comments |
|----------------------------------------------------------|------------------------|------------------------|-------------------|-----------------------------------------------------------------------------------------------|
| | 25°C | T_{MIN} to T_{MAX} | | |
| ANALOG SWITCH | | | | |
| Analog Signal Range | | | V | |
| On Resistance (R_{ON}) | 4 | | Ω typ | $V_D = -10\text{ V}$ to $+10\text{ V}$, $I_S = -10\text{ mA}$ |
| | 5 | 7 | Ω max | |
| On Resistance Match Between Channels (ΔR_{ON}) | 0.1 | | Ω typ | $V_D = \pm 10\text{ V}$, $I_S = -10\text{ mA}$ |
| | 0.5 | 0.5 | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 0.2 | | Ω typ | $V_D = -5\text{ V}$, 0 V , $+5\text{ V}$, $I_S = -10\text{ mA}$ |
| | 0.5 | 0.5 | Ω max | |
| LEAKAGE CURRENTS² | | | | |
| Source Off Leakage, I_S (OFF) | ± 0.02 | | nA typ | $V_D = \pm 10\text{ V}$, $V_S = \pm 10\text{ V}$; see Figure 17 |
| | ± 0.5 | ± 2.5 | nA max | |
| Drain Off Leakage, I_D (OFF) | ± 0.02 | | nA typ | $V_D = \pm 10\text{ V}$, $V_S = \pm 10\text{ V}$; see Figure 17 |
| | ± 0.5 | ± 2.5 | nA max | |
| Channel On Leakage, I_D , I_S (ON) | ± 0.04 | | nA typ | $V_D = V_S = \pm 10\text{ V}$; see Figure 18 |
| | ± 1 | ± 5 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.005 | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} ; all others = 2.4 V or 0.8 V, respectively |
| | | ± 0.5 | μA max | |
| DYNAMIC CHARACTERISTICS³ | | | | |
| t_{ON} | 70 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = \pm 10\text{ V}$; see Figure 19 |
| | 180 | 220 | ns max | |
| t_{OFF} | 60 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = \pm 10\text{ V}$; see Figure 19 |
| | 140 | 180 | ns max | |
| Break-Before-Make Time Delay, t_D (ADG453 Only) | 15 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = +10\text{ V}$; see Figure 20 |
| | 5 | 5 | ns min | |
| Charge Injection | 20 | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1.0\text{ nF}$; see Figure 21 |
| | 30 | | pC max | |
| Off Isolation | 65 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 22 |
| Channel-to-Channel Crosstalk | -90 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 23 |
| C_S (OFF) | 37 | | pF typ | $f = 1\text{ MHz}$ |
| C_D (OFF) | 37 | | pF typ | $f = 1\text{ MHz}$ |
| C_D , C_S (ON) | 140 | | pF typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.0001 | | μA typ | $V_{DD} = 16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$; digital inputs = 0 V or 5 V |
| | 0.5 | 5 | μA max | |
| I_{SS} | 0.0001 | | μA typ | |
| | 0.5 | 5 | μA max | |
| I_L | 0.0001 | | μA typ | |
| | 0.5 | 5 | μA max | |
| I_{GND} ³ | 0.0001 | | μA typ | |
| | 0.5 | 5 | μA max | |

¹ Temperature range for B version is -40°C to $+85^\circ\text{C}$.

² $T_{MAX} = 70^\circ\text{C}$.

³ Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$, $V_L = 5\text{ V}$, $GND = 0\text{ V}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 2.

| Parameter | B Version ¹ | | Unit | Test Conditions/Comments |
|----------------------------------------------------------|------------------------|------------------------|-------------------|---------------------------------------------------------------------------------------------|
| | 25°C | T_{MIN} to T_{MAX} | | |
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 V to V_{DD} | V | |
| On Resistance (R_{ON}) | 6 | | Ω typ | $V_D = 0\text{ V}$ to $+10\text{ V}$, $I_S = -10\text{ mA}$ |
| | 8 | 10 | Ω max | |
| On Resistance Match Between Channels (ΔR_{ON}) | 0.1 | | Ω typ | $V_D = 10\text{ V}$, $I_S = -10\text{ mA}$ |
| | 0.5 | 0.5 | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 1.0 | 1.0 | Ω typ | $V_D = 0\text{ V}$, 5 V , $I_S = -10\text{ mA}$ |
| LEAKAGE CURRENTS^{2, 3} | | | | |
| Source Off Leakage, I_S (OFF) | ± 0.02 | | nA typ | $V_D = 0\text{ V}$, 10 V , $V_S = 0\text{ V}$, 10 V ; see Figure 17 |
| | ± 0.5 | ± 2.5 | nA max | |
| Drain Off Leakage, I_D (OFF) | ± 0.02 | | nA typ | $V_D = 0\text{ V}$, 10 V , $V_S = 0\text{ V}$, 10 V ; see Figure 17 |
| | ± 0.5 | ± 2.5 | nA max | |
| Channel On Leakage, I_D , I_S (ON) | ± 0.04 | | nA typ | $V_D = V_S = 0\text{ V}$, 10 V ; see Figure 18 |
| | ± 1 | ± 5 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.005 | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | ± 0.5 | μA max | |
| DYNAMIC CHARACTERISTICS⁴ | | | | |
| t_{ON} | 100 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 8\text{ V}$; see Figure 19 |
| | 220 | 260 | ns max | |
| t_{OFF} | 80 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 8\text{ V}$; see Figure 19 |
| | 160 | 200 | ns max | |
| Break-Before-Make Time Delay, t_D (ADG453 Only) | 15 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 8\text{ V}$; see Figure 20 |
| | 10 | 10 | ns min | |
| Charge Injection | 10 | | pC typ | $V_S = 6\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1.0\text{ nF}$; see Figure 21 |
| Channel-to-Channel Crosstalk | -90 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 23 |
| C_S (OFF) | 60 | | pF typ | $f = 1\text{ MHz}$ |
| C_D (OFF) | 60 | | pF typ | $f = 1\text{ MHz}$ |
| C_D , C_S (ON) | 100 | | pF typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.0001 | | μA typ | $V_{DD} = 13.2\text{ V}$; digital inputs = 0 V or 5 V |
| | 0.5 | 5 | μA max | |
| I_L | 0.0001 | | μA typ | |
| | 0.5 | 5 | μA max | $V_L = 5.5\text{ V}$ |
| I_{GND} ⁴ | 0.0001 | | μA typ | |
| | 0.5 | 5 | μA max | $V_L = 5.5\text{ V}$ |

¹ Temperature range for B version is -40°C to $+85^\circ\text{C}$.

² $T_{MAX} = 70^\circ\text{C}$.

³ Tested with dual supplies.

⁴ Guaranteed by design, not subject to production test.

ADG451/ADG452/ADG453

5 V DUAL SUPPLY

$V_{DD} = +5\text{ V}$, $V_{SS} = -5\text{ V}$, $V_L = +5\text{ V}$, $GND = 0\text{ V}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 3.

| Parameter | B Version ¹ | | Unit | Test Conditions/Comments |
|----------------------------------------------------------|------------------------|------------------------|-------------------|---------------------------------------------------------------------------------------------|
| | 25°C | T_{MIN} to T_{MAX} | | |
| ANALOG SWITCH | | | | |
| Analogue Signal Range | | V_{SS} to V_{DD} | V | |
| On Resistance (R_{ON}) | 7 | | Ω typ | $V_D = -3.5\text{ V}$ to $+3.5\text{ V}$, $I_S = -10\text{ mA}$ |
| | 12 | 15 | Ω max | |
| On Resistance Match Between Channels (ΔR_{ON}) | 0.3 | | Ω typ | $V_D = 3.5\text{ V}$, $I_S = -10\text{ mA}$ |
| | 0.5 | 0.5 | Ω max | |
| LEAKAGE CURRENTS^{2, 3} | | | | |
| Source Off Leakage, I_S (OFF) | ± 0.02 | | nA typ | $V_D = \pm 4.5$, $V_S = \pm 4.5$; see Figure 17 |
| | ± 0.5 | ± 2.5 | nA max | |
| Drain Off Leakage, I_D (OFF) | ± 0.02 | | nA typ | $V_D = 0\text{ V}$, 5 V , $V_S = 0\text{ V}$, 5 V ; see Figure 17 |
| | ± 0.5 | ± 2.5 | nA max | |
| Channel On Leakage, I_D , I_S (ON) | ± 0.04 | | nA typ | $V_D = V_S = 0\text{ V}$, 5 V ; see Figure 18 |
| | ± 1 | ± 5 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.005 | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | ± 0.5 | μA max | |
| DYNAMIC CHARACTERISTICS⁴ | | | | |
| t_{ON} | 160 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; see Figure 19 |
| | 220 | 300 | ns max | |
| t_{OFF} | 60 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_S = 3\text{ V}$; see Figure 19 |
| | 140 | 180 | ns max | |
| Break-Before-Make Time Delay, t_D (ADG453 Only) | 50 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $V_{S1} = V_{S2} = 3\text{ V}$; see Figure 20 |
| | 5 | 5 | ns min | |
| Charge Injection | 10 | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1.0\text{ nF}$; see Figure 21 |
| Off Isolation | 65 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 22 |
| Channel-to-Channel Crosstalk | -76 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 23 |
| C_S (OFF) | 48 | | pF typ | $f = 1\text{ MHz}$ |
| C_D (OFF) | 48 | | pF typ | $f = 1\text{ MHz}$ |
| C_D , C_S (ON) | 148 | | pF typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.0001 | | μA typ | $V_{DD} = 5.5\text{ V}$; digital inputs = 0 V or 5 V |
| | 0.5 | 5 | μA max | |
| I_{SS} | 0.0001 | | μA typ | |
| | 0.5 | 5 | μA max | |
| I_L | 0.0001 | | μA typ | |
| | 0.5 | 5 | μA max | $V_L = 5.5\text{ V}$ |
| I_{GND}^4 | 0.0001 | | μA typ | |
| | 0.5 | 5 | μA max | $V_L = 5.5\text{ V}$ |

¹ Temperature range for B version is -40°C to $+85^\circ\text{C}$.

² $T_{MAX} = 70^\circ\text{C}$.

³ Tested with dual supplies.

⁴ Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

| Parameters | Ratings |
|---------------------------------------------------------------|-------------------------------------------------------------------|
| V_{DD} to V_{SS} | 44 V |
| V_{DD} to GND | -0.3 V to +32 V |
| V_{SS} to GND | +0.3 V to -32 V |
| V_L to GND | -0.3 V to $V_{DD} + 0.3$ V |
| Analog, Digital Inputs ¹ | $V_{SS} - 2$ V to $V_{DD} + 2$ V or 30 mA, whichever occurs first |
| Continuous Current, S or D | 100 mA |
| Peak Current, S or D (pulsed at 1 ms, 10% duty cycle maximum) | 300 mA |
| Operating Temperature Range | |
| Industrial (B Version) | -40°C to +85°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| Plastic DIP Package, Power Dissipation | 470 mW |
| θ_{JA} Thermal Impedance | 117°C/W |
| Lead Temperature, Soldering (10 sec) | 260°C |
| SOIC Package, Power Dissipation | 600 mW |
| θ_{JA} Thermal Impedance | 77°C/W |
| TSSOP Package, Power Dissipation | 450 mW |
| θ_{JA} Thermal Impedance | 115°C/W |
| θ_{JC} Thermal Impedance | 35°C/W |
| Lead Temperature, Soldering | |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |
| ESD | 2 kV |

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADG451/ADG452/ADG453

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-----------------|-------------------------------------------------------------------------------------------------------------------|
| 1 | IN1 | Logic Control Input. |
| 2 | D1 | Drain Terminal. Can be an input or an output. |
| 3 | S1 | Source Terminal. Can be an input or an output. |
| 4 | V _{SS} | Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it can be connected to GND. |
| 5 | GND | Ground (0 V) Reference. |
| 6 | S4 | Source Terminal. Can be an input or an output. |
| 7 | D4 | Drain Terminal. Can be an input or an output. |
| 8 | IN4 | Logic Control Input. |
| 9 | IN3 | Logic Control Input. |
| 10 | D3 | Drain Terminal. Can be an input or an output. |
| 11 | S3 | Source Terminal. Can be an input or an output. |
| 12 | V _L | Logic Power Supply (5 V). |
| 13 | V _{DD} | Most Positive Power Supply Potential. |
| 14 | S2 | Source Terminal. Can be an input or an output. |
| 15 | D2 | Drain Terminal. Can be an input or an output. |
| 16 | IN2 | Logic Control Input. |

Table 6. Truth Table (ADG451/ADG452)

| ADG451 In | ADG452 In | Switch Condition |
|-----------|-----------|------------------|
| 0 | 1 | On |
| 1 | 0 | Off |

Table 7. Truth Table (ADG453)

| Logic | Switch 1, Switch 4 | Switch 2, Switch 3 |
|-------|--------------------|--------------------|
| 0 | Off | On |
| 1 | On | Off |

TYPICAL PERFORMANCE CHARACTERISTICS



Figure 5. On Resistance as a Function of V_D (V_S) for Various Dual Supplies

05239-003

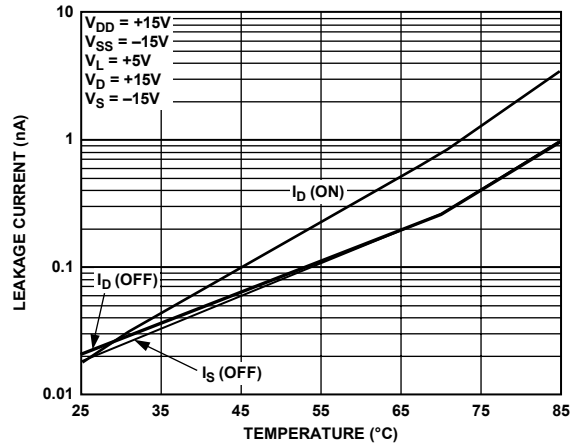


Figure 8. Leakage Currents as a Function of Temperature

05239-006



Figure 6. On Resistance as a Function of V_D (V_S) for Different Temperatures with Dual Supplies

05239-004

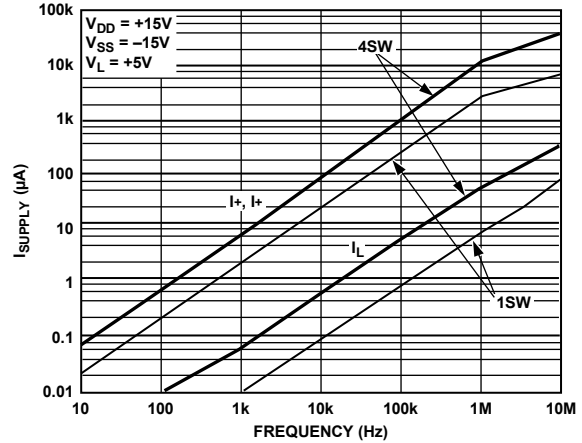


Figure 9. Supply Current vs. Input Switching Frequency

05239-007



Figure 7. On Resistance as a Function of V_D (V_S) for Various Single Supplies

05239-005

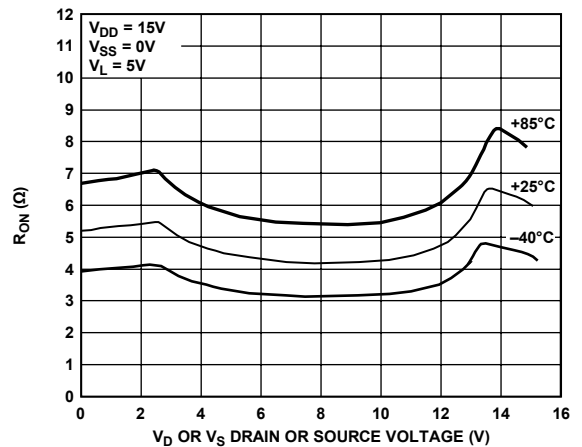


Figure 10. On Resistance as a Function of V_D (V_S) for Different Temperatures with Single Supplies

05239-008

ADG451/ADG452/ADG453



Figure 11. Leakage Currents as a Function of V_D (V_S)

05239-009



Figure 13. Crosstalk vs. Frequency

05239-011



Figure 12. Off Isolation vs. Frequency

05239-010



Figure 14. Frequency Response with Switch On

05239-012

TERMINOLOGY

R_{ON}

Ohmic resistance between D and S.

ΔR_{ON}

On resistance match between any two channels, that is, R_{ON} maximum minus R_{ON} minimum.

$R_{FLAT(ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

I_S (OFF)

Source leakage current with the switch off.

I_D (OFF)

Drain leakage current with the switch off.

I_D, I_S (ON)

Channel leakage current with the switch on.

V_D (V_S)

Analog voltage on Terminal D and Terminal S.

C_S (OFF)

Off switch source capacitance.

C_D (OFF)

Off switch drain capacitance.

C_D (ON), C_S (ON)

On switch capacitance.

t_{ON}

Delay between applying the digital control input and the output switching on. See Figure 19.

t_{OFF}

Delay between applying the digital control input and the output switching off.

t_D

Off time or on time measured between the 90% points of both switches, when switching from one address state to another. See Figure 20.

Crosstalk

A measure of unwanted signal coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

APPLICATIONS

Figure 15 illustrates a precise, fast, sample-and-hold circuit. An [AD845](#) is used as the input buffer, and the output operational amplifier is an [AD711](#). During track mode, SW1 is closed, and the output, V_{OUT} , follows the input signal, V_{IN} . In hold mode, SW1 is opened, and the signal is held by the hold capacitor, C_H .



Figure 15. Fast, Accurate Sample-and-Hold Circuit

05239-013

Due to switch and capacitor leakage, the voltage on the hold capacitor decreases with time. The ADG451/ADG452/ADG453 minimize this droop due to their low leakage specifications. The droop rate is further minimized by the use of a polystyrene hold capacitor. The droop rate for the circuit shown is typically $30 \mu\text{V}/\mu\text{s}$.

A second switch, SW2, which operates in parallel with SW1, is included in this circuit to reduce pedestal error. Because both switches are at the same potential, they have a differential effect on the op amp, AD711, which minimizes charge injection effects. Pedestal error is also reduced by the compensation network, R_C and C_C . This compensation network reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the $\pm 10 \text{ V}$ input range. Both the acquisition and settling times are 850 ns.

TEST CIRCUITS



Figure 16. On Resistance

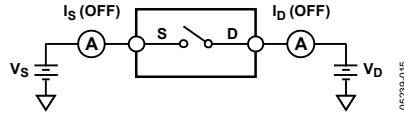


Figure 17. Off Leakage



Figure 18. On Leakage



Figure 19. Switching Times

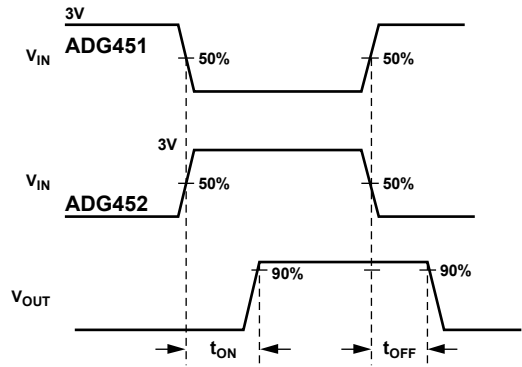


Figure 20. Break-Before-Make Time Delay

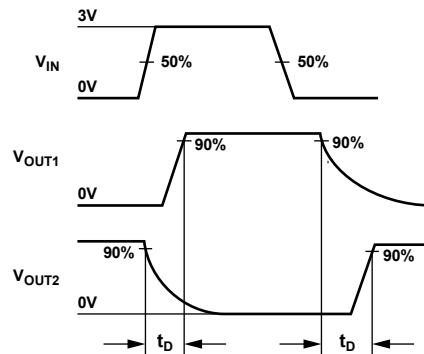
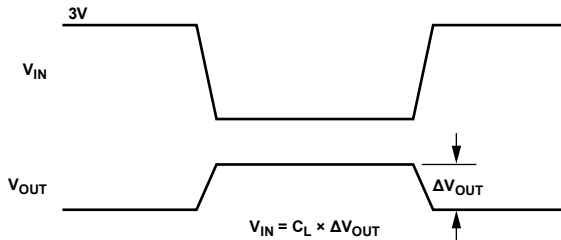


Figure 21. Charge Injection



ADG451/ADG452/ADG453



Figure 22. Off Isolation

05239-020



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \times \log |V_s/V_{out}|$$

Figure 23. Channel-to-Channel Crosstalk

05239-021

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 24. 16-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-16)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 25. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-001-AB

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 26. 16-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-16)
Dimensions shown in inches and (millimeters)

ADG451/ADG452/ADG453

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|-------------------------------|-------------------|---------------------------------------------------|----------------|
| ADG451BN | -40°C to +85°C | 16-Lead Plastic Dual In-Line Package [PDIP] | N-16 |
| ADG451BNZ ¹ | -40°C to +85°C | 16-Lead Plastic Dual In-Line Package [PDIP] | N-16 |
| ADG451BR | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG451BR-REEL | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG451BR-REEL7 | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG451BRZ ¹ | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG451BRZ-REEL ¹ | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG451BRZ-REEL7 ¹ | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG451BRUZ ¹ | -40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG451BRUZ-REEL ¹ | -40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG451BRUZ-REEL7 ¹ | -40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG451BCHIPS | | DIE | |
| ADG452BN | -40°C to +85°C | 16-Lead Plastic Dual In-Line Package [PDIP] | N-16 |
| ADG452BNZ ¹ | -40°C to +85°C | 16-Lead Plastic Dual In-Line Package [PDIP] | N-16 |
| ADG452BR | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG452BR-REEL | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG452BR-REEL7 | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG452BRZ ¹ | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG452BRZ-REEL ¹ | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG452BRZ-REEL7 ¹ | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG452BRUZ ¹ | -40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG452BRUZ-REEL ¹ | -40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG452BRUZ-REEL7 ¹ | -40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG453BN | -40°C to +85°C | 16-Lead Plastic Dual In-Line Package [PDIP] | N-16 |
| ADG453BNZ ¹ | -40°C to +85°C | 16-Lead Plastic Dual In-Line Package [PDIP] | N-16 |
| ADG453BR | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG453BR-REEL | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG453BR-REEL7 | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG453BRZ ¹ | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG453BRZ-REEL ¹ | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG453BRZ-REEL7 ¹ | -40°C to +85°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADG453BRUZ ¹ | -40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG453BRUZ-REEL ¹ | -40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |
| ADG453BRUZ-REEL7 ¹ | -40°C to +85°C | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16 |

¹ Z = Pb-free part.

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- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
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- Комплексную поставку.
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- Тестирование поставляемой продукции.
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- Входной контроль качества.
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- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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