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S1R72C05***
Data Sheet

SEIKO EPSON CORPORATION

Rev.1.0

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Scope

This document applies to the “S1R72C05” USB 2.0 Device Host Controller LSI.

Table of Contents

1. OVERVIEW

The S1R72C05** is a USB host and device controller LSI that supports USB 2.0 high-speed mode. Separate host and device ports are provided to allow use as a USB host or USB device, depending on how control is switched.

An IDE I/F is also provided, making it ideal for mobile or car-mounted electronic devices with built-in HDDs.

2. FEATURES

<<USB 2.0 device functions>>

- HS (480 Mbps) and FS (12 Mbps) transfer support
- Built-in FS/HS termination (no external circuits required)
- VBUS 5V I/F (requires external protection circuit)
- Support for control, bulk, interrupt, and isochronous transfers
- Support for bulk, interrupt, isochronous transfer endpoints x5 and endpoint 0

<<USB 2.0 host functions>>

- Support for HS (480 Mbps), FS (12 Mbps), and LS (1.5 Mbps) transfers
- Built-in pull-down resistor for downstream port (no external circuit required)
- Built-in HS termination (no external circuit required)
- Support for control, bulk, interrupt, and isochronous transfers
  Channel architecture
  Dedicated control transfer channel x1
  Dedicated bulk transfer channel x1
  Bulk, interrupt, and isochronous transfer channels x4
- USB power switch interface

<<Media data transfer functions>>

- Media FIFO independent of USB allows data transfer between IDE and CPU.

<<CPU I/F>>

- Supports 16-bit width standard CPU I/F
- Includes DMA 2ch. (Multi-word procedure)
- Big Endian (Includes bus swapping function to support Little Endian CPUs)
- I/F variable voltage (3.3 V to 1.8 V)

<<IDE I/F>>

- Supports ATA/ATAPI6
  PIO mode 0 to 4, Multi-word DMA, UDMA mode 0 to 5

<<Miscellaneous>>

- Clock input: Supports 12 MHz or 24 MHz quartz oscillator. (Built-in oscillator circuit and 1 MΩ feedback resistor)
- Power supply voltage: 3-voltage system, featuring 3.3 V, 1.8 V, and CPU I/F power supply (3.3 V to 1.8 V)
- Supports Boundary-Scan
- Package type: QFP15-128, PFBGA8UX121, PFBGA10UX121
- Guaranteed operating temperature range: -40°C to 85°C

3. BLOCK DIAGRAM

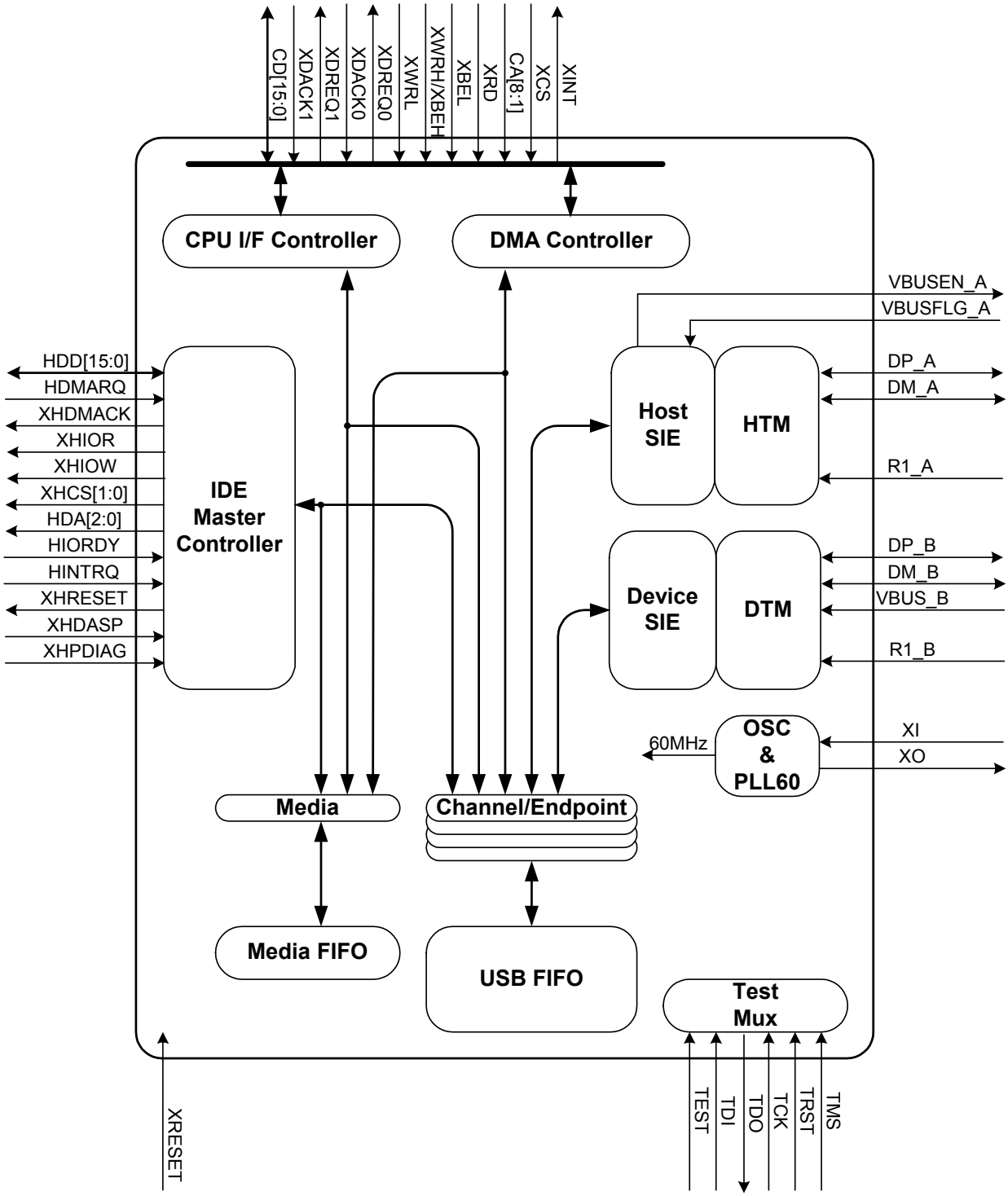


Fig.3.1 Overall block diagram

4. FUNCTIONS

4.1 Power Supply

This LSI has three power supply circuits and a common ground. The power supply circuits consist of HVDD (3.3 V) for USB I/O, IDE I/O, and TEST I/O; CVDD (3.3 V to 1.8 V) for CPU I/F I/O; and LVDD (1.8 V) for internal circuits. (See Fig.4.1)

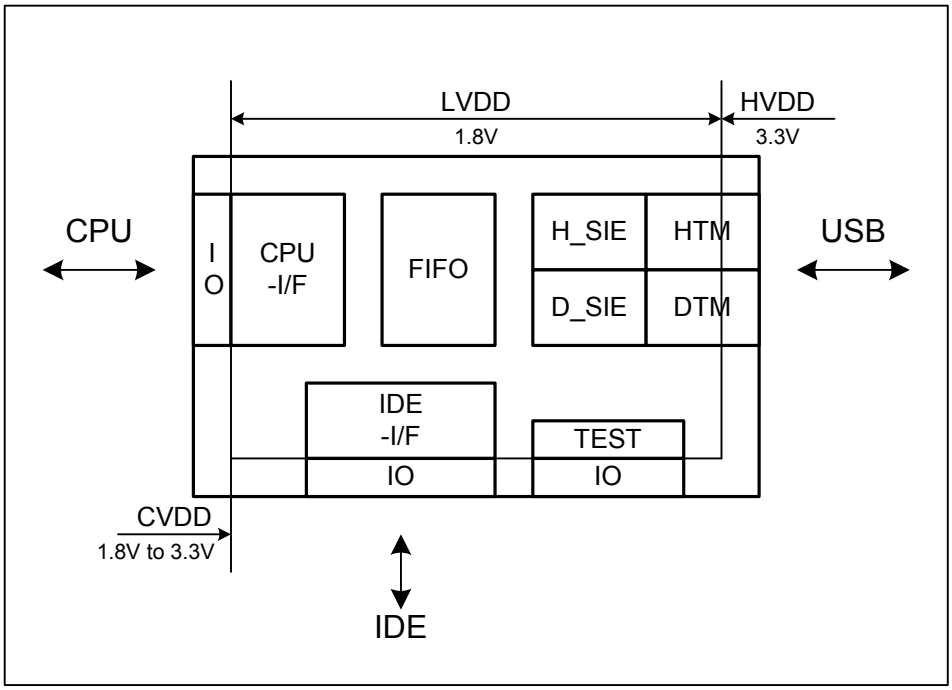


Fig.4.1 S1R72C05 power supplies

Given below are the sequences for turning the power supplies on and off.

This LSI will not operate with only some of the power supplies turned on or off. The following restrictions apply to the sequence for turning the CVDD/HVDD I/O power supplies and LVDD internal power supply on or off. There are no restrictions on the sequence for turning the CVDD and HVDD power supplies on or off.

- The LVDD must be turned on before turning on the CVDD and HVDD power supplies.
- The CVDD and HVDD power supplies must be turned off before turning off the LVDD.

If adherence to this sequence is not possible for reasons related to power supply circuit characteristics or load, the CVDD or HVDD must be on for no longer than 1 second while the LVDD is off.

4.2 Boundary Scan

Boundary scanning (JTAG) may be used when the TEST terminal is set to “Low” (default). Boundary scanning consists of a BSR (Boundary Scan Register) conforming to the JTAG (IEEE 1149.1) specifications, a connecting scan path, and a TAP controller. Boundary scan connection information may be provided in BSDL format.

4.2.1 Instructions Supported

This LSI has a JTAG instruction bit width of 4 bits and supports the following JTAG instructions.

Table 4.1 JTAG instruction codes

Instruction	Description	Code
SAMPLE/PRELOAD	Loads LSI internal status to BSR and sets data.	0010
BYPASS	Bypasses the scan path using BSR.	1111
EXTEST	Physical device connection check.	0000
CLAMP	Bypasses the scan path while maintaining output values.	0011
HIGHZ	Sets all outputs to Hi-Z.	0100
IDCODE	Outputs the specified DEVICE_CODE.	0001

4.2.2 DEVICE_CODE

The DEVICE_CODE corresponding to an IDCODE instruction is composed of the following elements.

Table 4.2 DEVICE_CODE

Version	1
Part Number	0x0015
Manufacturer	0x0BE

The DEVICE_CODE response for an IDCODE instruction will therefore be 0001_0000000000010101_00010111110_1.

4.2.3 Terminals Excluded from Boundary Scan

The following terminals do not include boundary scan cells and are therefore excluded from boundary scanning in this LSI: DP_A, DM_A, DP_B, DM_B, R1_A, R1_B, XI, XO, VBUS_B, and TEST.

4.3 Reset

This LSI includes a hard reset function via the external XRESET terminal and soft reset function via register settings.

4.3.1 Hard Reset

Start from reset status when power is turned on, then cancel the reset after confirming power on.

4.3.2 Soft Reset

All LSI circuits can be reset via software, or internal USB analog macros can be reset individually. The ChipReset.AllReset bit is used to reset all circuits in this LSI, or the D_Reset.ResetDTM or H_Reset.ResetHTM bits are used to reset the respective device analog macro or host analog macro. However, note that the analog macro should be reset only in the SLEEP state.

4.4 Clock

This LSI contains an internal oscillator and feedback resistor (1 MΩ) and supports clock generation using an external resonator. The oscillator frequency can be set to 12 MHz or 24 MHz via the register settings.

Fig.4.2 shows a typical connection arrangement for an oscillator circuit. Cd, Cg, and Rd in the oscillator circuit must be matched based on the resonator. Contact the resonator manufacturer to obtain circuit constants.

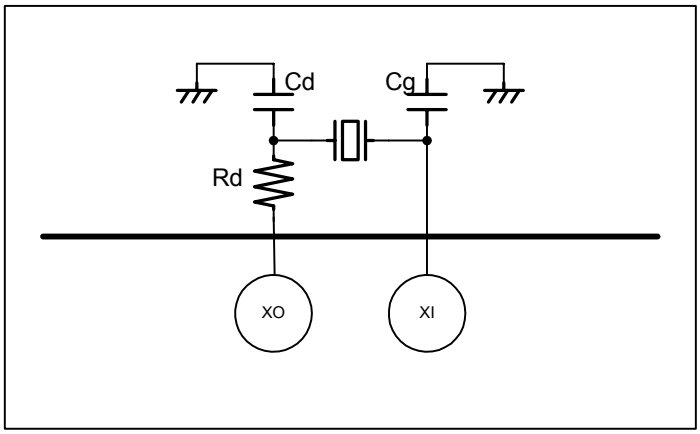


Fig.4.2 Clock generation via the internal oscillator and external resonator

4.5 Power Management

This LSI includes a power management function that features six power management states: SLEEP, SNOOZE, ACTIVE60, ACT_DEVICE, ACT_HOST, and ACT_ALL. (See Fig.4.3)

All function blocks are active in the ACT_ALL state (although the USB host function and USB device function cannot be used simultaneously). In the SLEEP state, however, only the circuits necessary for restarting from standby mode are active. Intermediate power management states exist between ACT_ALL and SLEEP, depending on the required activation status.

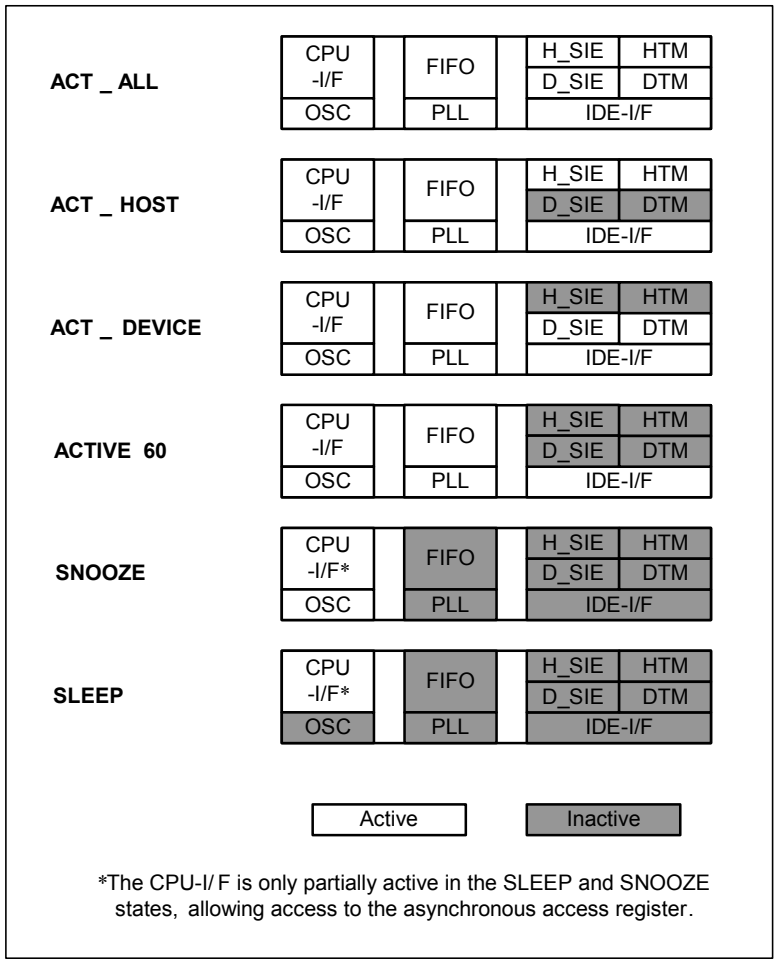


Fig.4.3 Power management states

4.6 CPU-I/F

This LSI is connected to the CPU via a 16-bit interface. Endian settings can be set as Big Endian or Little Endian in 16-bit steps. For Big Endian, registers with even addresses can be accessed above the bus (CD[15:8]), while registers with odd addresses can be accessed below the bus (CD[7:0]). For Little Endian, registers with even addresses can be accessed below the bus (CD[7:0]), while registers with odd addresses can be accessed above the bus (CD[15:8]).

The bus mode can be set to either Strobe mode for accessing using high/low strobe (XWRH/XWRL) or Byte Enable mode for accessing using high/low byte enable (XBEH/XBEL) for writing in 8-bit. Endian and bus mode are set by the CPUIF_MODE register immediately after resetting.

The CPU-I/F on this LSI includes 2-ch DMA (slave).

The registers that are accessible will depend on the power management state. For detailed information, refer to the LSI Technical Manual.

4.7 IDE-I/F

This LSI includes an IDE host function supporting ATA/ATAPI6, which supports PIO modes 0 to 4, Multi Word DMA, and UDMA modes 0 to 5 transfer modes.

4.8 USB Device I/F

This LSI supports high-speed specification USB device functions that comply with USB 2.0 (Universal Serial Bus Specification Revision 2.0) standards.

4.8.1 Speed Mode and Transfer Type

This LSI supports HS (480 Mbps) and FS (12 Mbps) speed modes when operating USB devices. The speed mode is automatically set by the speed negotiations performed when the bus is reset. For example, HS transfer mode will be selected automatically by speed negotiations if connected to a USB host that supports HS speed mode. (Note that FS speed mode can be set deliberately via register settings.)

All transfer types stipulated in the USB 2.0 standard are supported, including control transfer (endpoint 0), bulk, interrupt, and isochronous transfers.

4.8.2 Resources

4.8.2.1 Endpoint

This LSI includes endpoint 0 and five standard endpoints. Endpoint 0 supports control transfer. The standard endpoints support bulk, interrupt, and isochronous transfers. The standard endpoint numbers, maximum packet size, and transfer direction (IN/OUT) can be set as desired.

4.8.2.2 FIFO

This LSI includes 4.5 kB of FIFO for use with USB data transfer. This forms the data transfer route with USB. The FIFO capacity for each endpoint can be assigned as desired through software. For example, performance can be improved by assigning an adequate FIFO area to the endpoints for bulk transfers.

4.8.3 Data Flow

Endpoints are assigned to USB FIFO areas on a one-to-one basis. Responses are returned to USB transactions automatically, depending on the USB FIFO effective free capacity (for OUT transfer) or effective data quantity (for IN transfer). Thus, the software need not be directly involved in individual transactions, allowing USB data

transfers to be controlled as data flow on the USB FIFO.

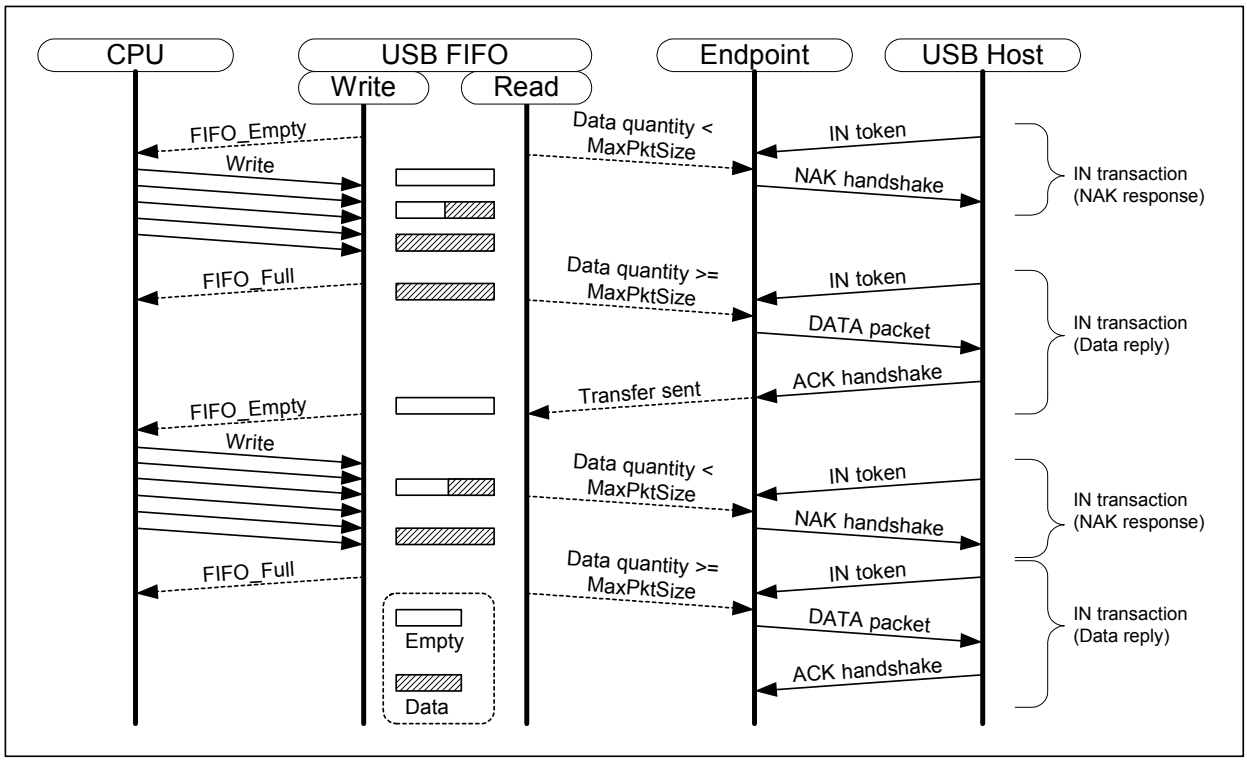


Fig.4.4 Typical data flow (with FIFO assigned for MaxPktSize and IN transfer)

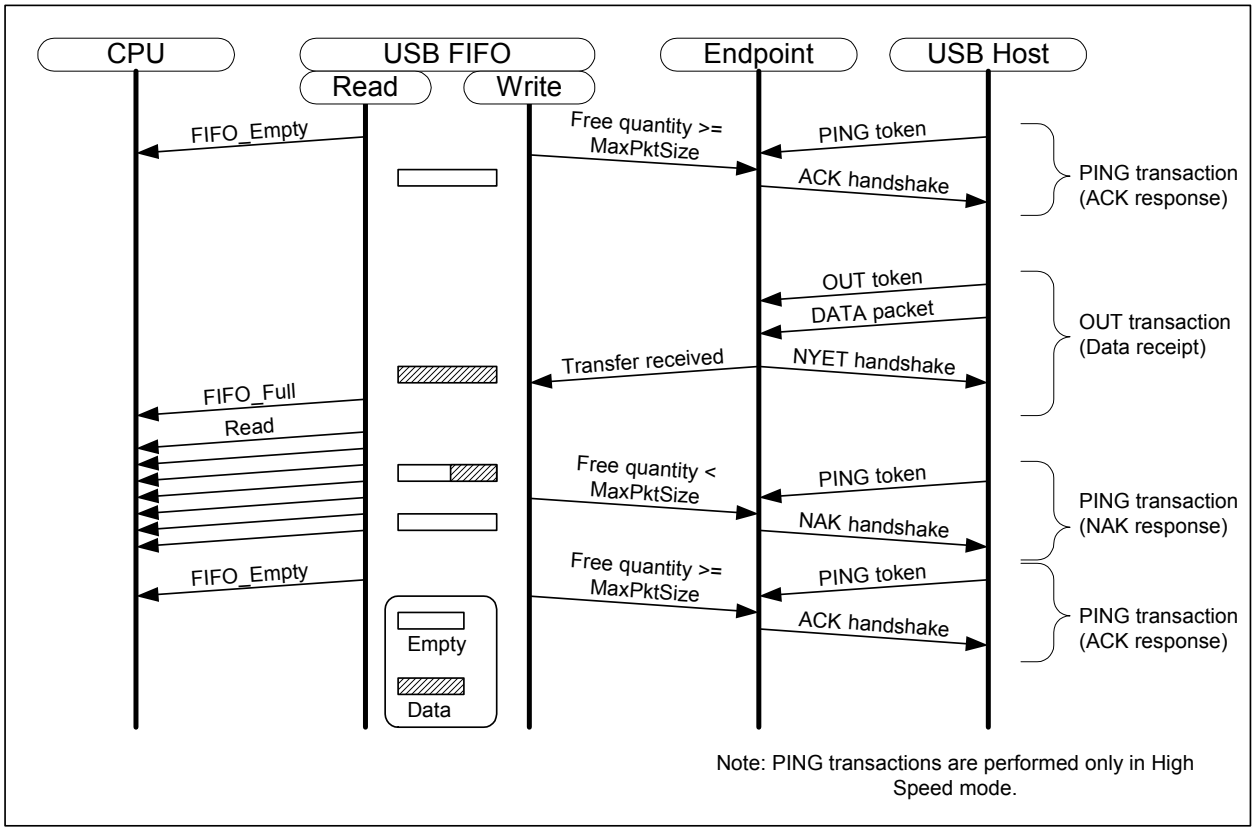


Fig.4.5 Typical data flow (with FIFO assigned for MaxPktSize and OUT transfer)

4.8.4 USB Device Port External Circuits

This LSI has internal FS and HS device termination resistors, eliminating the need for additional components normally used to adjust impedance. This allows a DP/DM line to be connected between the LSI terminal and the connector. The appropriate components should be used to protect against static electricity and implement EMI precautions.

The VBUS terminal uses a 5 V input and does not require external voltage conversion. However, a protection circuit is recommended since certain commercially available USB host and hub products may apply surge voltages that exceed VBUS ratings.

Refer to the "PCB Design Guidelines for S1R72V Series USB 2.0 High-Speed Devices" provided separately.

4.9 USB Host I/F

This LSI supports high-speed specification USB host functions that comply with USB 2.0 (Universal Serial Bus Specification Revision 2.0) standards.

4.9.1 Speed Mode and Transfer Type

This LSI supports HS (480 Mbps), FS (12 Mbps) and LS (1.5 Mbps) speed modes when operating USB hosts. The speed mode is automatically set through speed negotiation performed when the bus is reset.

All transfer types stipulated in the USB 2.0 standard are supported, including control, bulk, interrupt, and isochronous transfers.

4.9.2 Resources

4.9.2.1 Channel

In this LSI, the setting register sets for transfers with end points on a one-to-one basis are referred to as channels. This LSI features one dedicated channel for control transfers, one dedicated channel for bulk transfers, and four general channels that support bulk, interrupt, and isochronous transfers. The endpoint number, maximum packet size, and transfer direction (in/out) can be set as desired for all channels. Transfers are also possible for a number of endpoints exceeding the number of channels using time-multiplexing for channels via software.

4.9.2.2 FIFO

This LSI includes 4.5 kB of FIFO for use with USB data transfers. This forms the data transfer route with USB. The FIFO capacity for each channel can be assigned as desired via software. For example, performance can be improved by assigning a sufficient FIFO area to the channels for bulk transfers.

4.9.3 Data Flow

The channels are assigned to FIFO areas on a one-to-one basis, and transactions are automatically sent via USB, depending on the FIFO effective free capacity (for IN transfers) or effective data quantity (for OUT transfers). The software need not be directly involved in individual transactions, allowing the USB data transfer to be controlled as data flow on the FIFO.

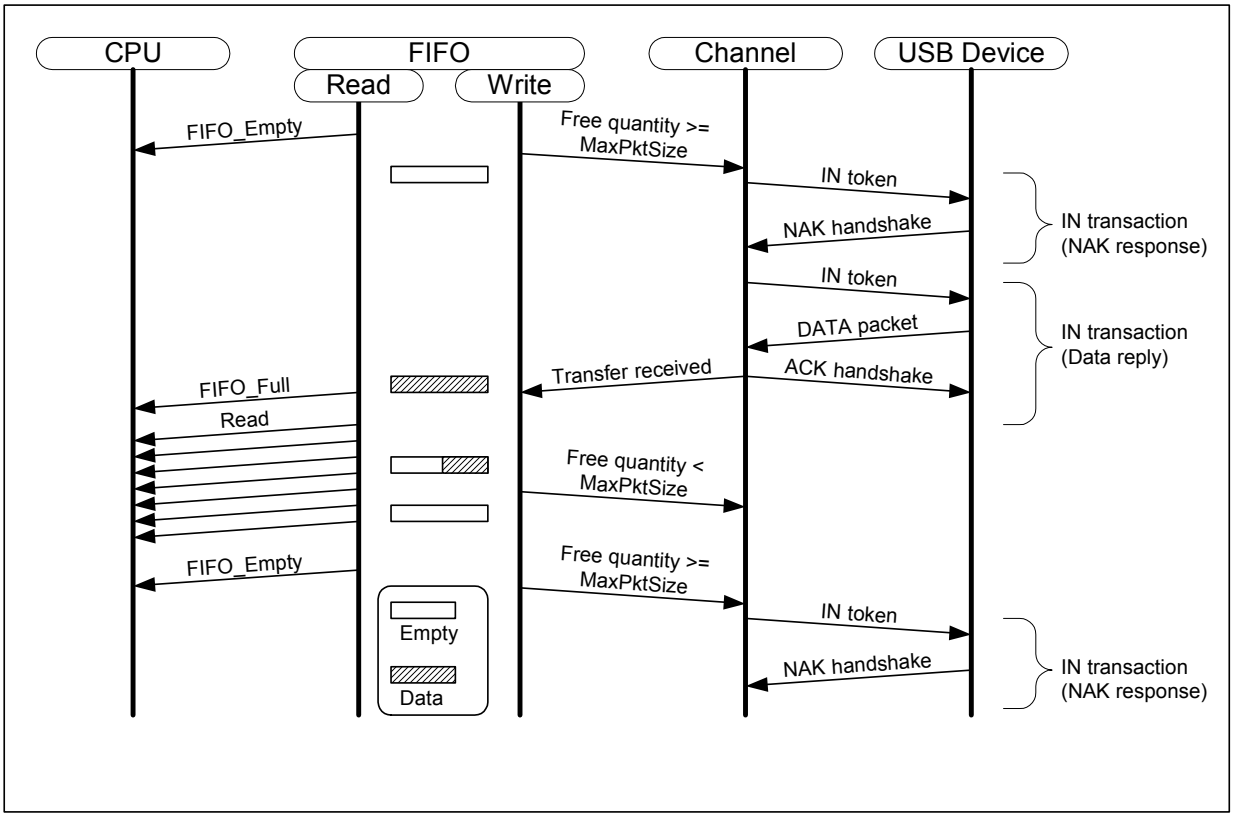


Fig.4.6 Typical data flow (with FIFO assigned for MaxPktSize and IN transfers)

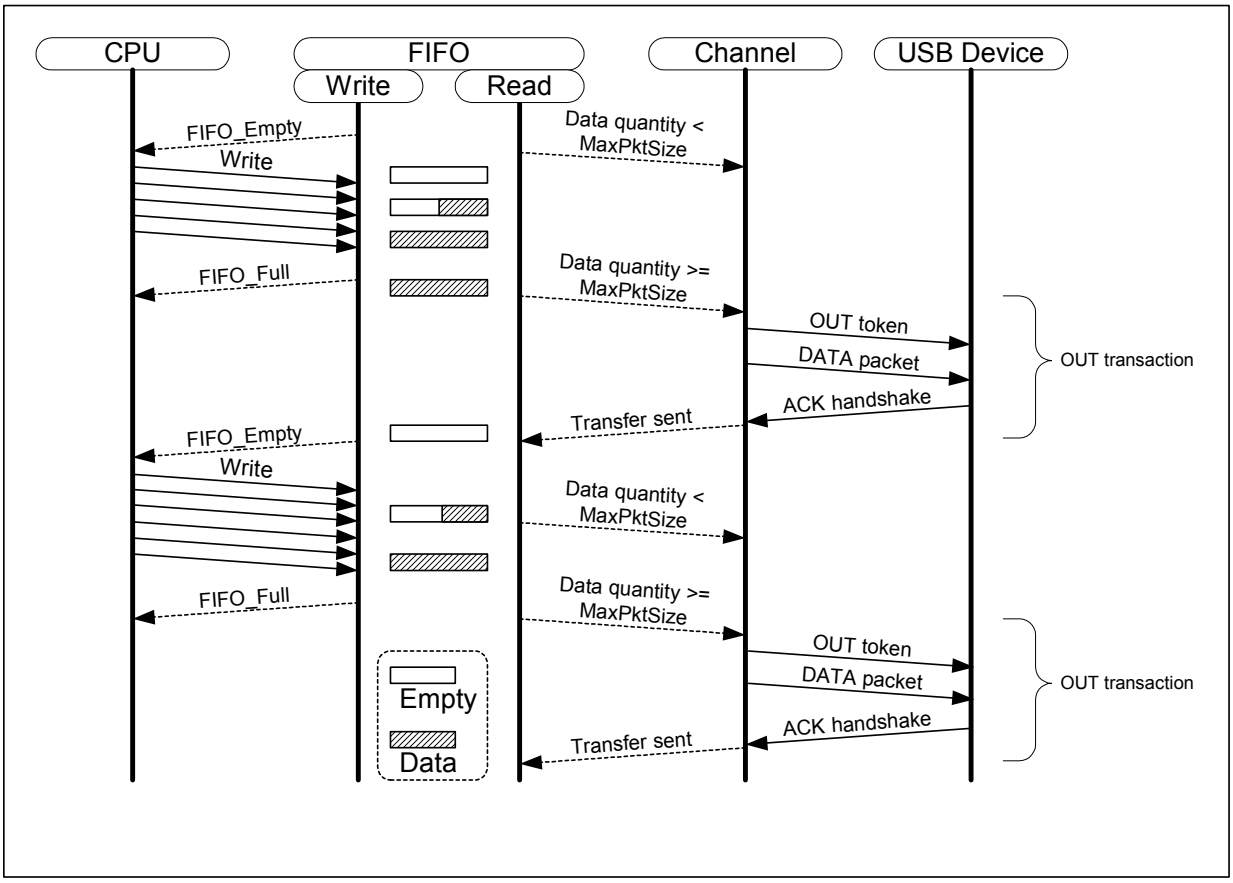


Fig.4.7 Typical data flow (with FIFO assigned for MaxPktSize and OUT transfers)

4.9.4 USB Host Port External Circuits

This LSI features internal USB host termination resistors, including HS termination resistors, eliminating the need for the external components typically used to adjust impedance. This allows the connection of a DP/DM line between the LSI terminal and the connector. However, note that the appropriate components should be used to protect against static electricity and to implement EMI precautions. External VBUS control components are required for VBUS.

4.10 FIFO

4.10.1 USB FIFO

This LSI includes 4.5 kB of USB FIFO for use with USB data transfers. This is shared between USB device I/F and USB host I/F. The USB FIFO capacity for each endpoint or channel can be assigned as desired via software.

Transfers are possible between the USB-I/F and CPU-I/F via the USB FIFO or directly between the USB-I/F and IDE-I/F.

4.10.2 Media FIFO

This LSI includes 64 B of Media FIFO for use with IDE data transfers. This forms the data transfer route with the IDE-I/F and CPU-I/F. Data cannot be transferred to or from the USB-I/F with Media FIFO.

5. TERMINAL LAYOUT DIAGRAMS

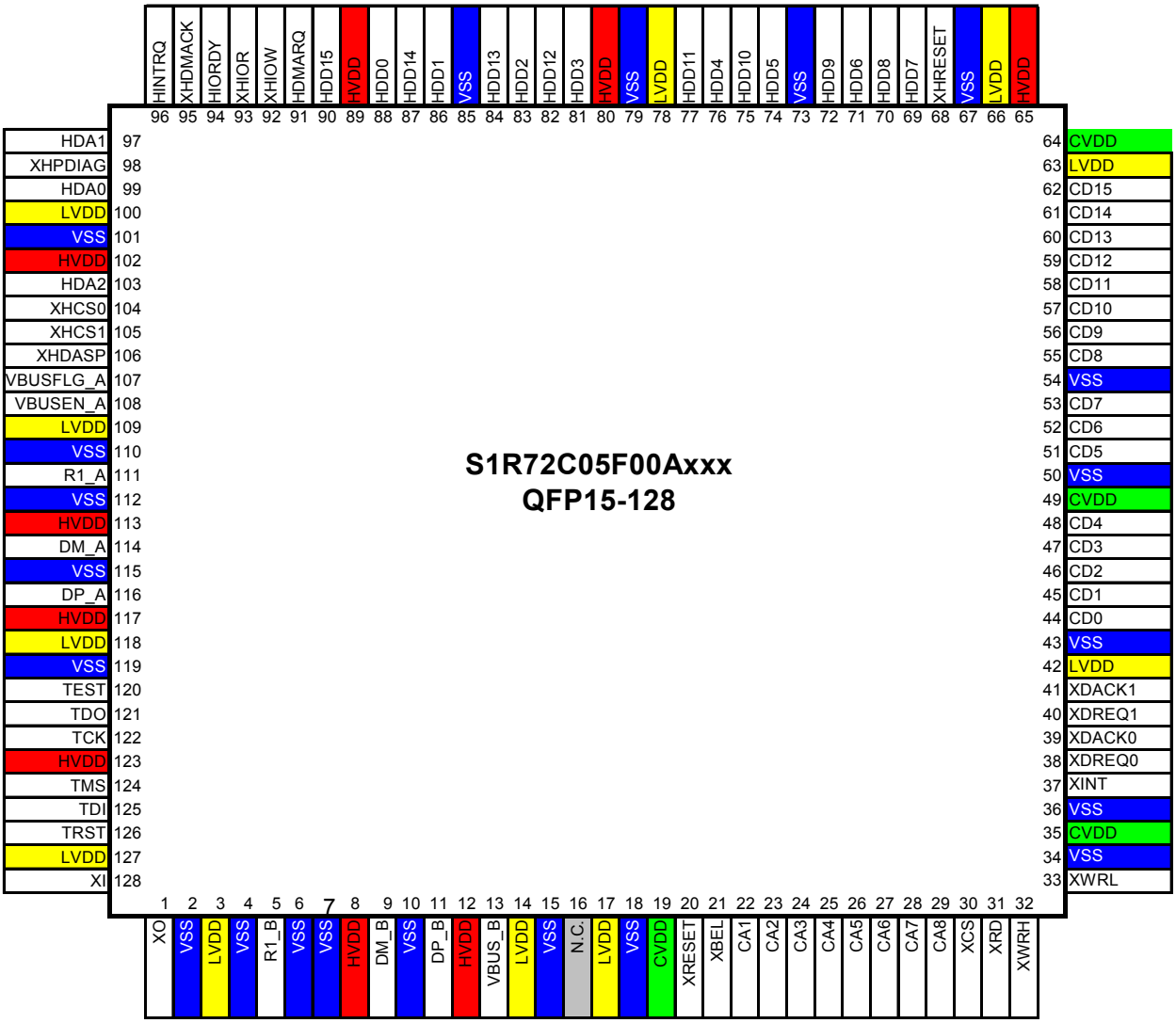


Fig.5.1 QFP package terminal layout diagram

S1R72C05/PFBGA8UX121,PFBGA10UX121
TOP View

1	2	3	4	5	6	7	8	9	10	11	
NC	XI	LVDD	LVDD	DP_A	DM_A	HVDD	R1_A	LVDD	HDA0	NC	A
XO	VSS	TRST	VSS	HVDD	VSS	VBUSEN_A	VSS	VSS	HDA2	XHPDIAG	B
LVDD	VSS	TDI	TCK	TEST	XHCS0	VBUSFLG_A	VSS	XHCS1	HDA1	HINTRQ	C
R1_B	VSS	TDO	XHDASP	HVDD	XHDMACK	HIORDY	XHIOW	XHIOR	HDD0	HDMARQ	D
HVDD	TMS	VSS	LVDD	VSS	HDD14	HDD15	HDD12	VSS	HDD2	HDD13	E
DM_B	VSS	VSS	CA2	VSS	LVDD	HDD3	VSS	HDD1	VSS	HVDD	F
DP_B	HVDD	VBUS_B	CA3	XINT	XDACK1	HVDD	HDD11	HDD5	HDD10	HDD4	G
LVDD	VSS	CVDD	CA4	XDACK0	CD3	CD6	CVDD	CD13	HDD8	HDD9	H
LVDD	XRESET	CA1	XBEL	XDREQ1	CD0	CD4	CD7	CD10	HDD6	HDD7	J
CA8	XCS	CA5	CA6	CA7	CD1	CD5	CD9	CD12	CD14	XHRESET	K
NC	XRD	XWRH	XWRL	XDREQ0	CD2	CVDD	CD8	CD11	CD15	NC	L
1	2	3	4	5	6	7	8	9	10	11	

Fig.5.2 BGA package terminal layout diagram

6. TERMINAL FUNCTIONS

OSC

Pin	Ball	Name	I/O	RESET	Terminal type	Terminal description
128	A2	XI	IN	—	Analog	Internal oscillator circuit input (12 MHz, 24 MHz)
1	B1	XO	OUT	—	Analog	Internal oscillator circuit output

TEST

Pin	Ball	Name	I/O	RESET	Terminal type	Terminal description
120	C5	TEST	IN	—	—	Test terminal (Must be fixed at Low)
121	D3	TDO	OUT	Hi-Z	2mA	Boundary scan TDO terminal
122	C4	TCK	IN	—	—	Boundary scan TCK terminal
124	E2	TMS	IN	—	—	Boundary scan TMS terminal
125	C3	TDI	IN	—	—	Boundary scan TDI terminal
126	B3	TRST	IN	—	—	Boundary scan TRST terminal

If the boundary scan function is not used, the TEST, TCK, TMS, TDI, and TRST terminals should all be set to Low and the TDO terminal left open.
PD: Pull Down
PU: Pull Up

USB

Pin	Ball	Name	I/O	RESET	Terminal type	Terminal description
111	A8	R1_A	IN	—	Analog	Internal operation reference current setting terminal (Connect 6.2 kΩ ±1% resistance between VSS)
116	A5	DP_A	BI	Hi-Z	Analog	USB host data line (Data +)
114	A6	DM_A	BI	Hi-Z	Analog	USB host data line (Data -)
107	C7	VBUSFLG_A	IN	(PU)	Schmitt (PU)	USB power switch fault detection signal (1: Normal, 0: Error)
108	B7	VBUSEN_A	OUT	Lo	2mA	USB power switch control signal
5	D1	R1_B	IN	—	Analog	Internal operation reference current setting terminal (Connect 6.2 kΩ ±1% resistance between VSS)
11	G1	DP_B	BI	Hi-Z	Analog	USB device data line (Data +)
9	F1	DM_B	BI	Hi-Z	Analog	USB device data line (Data -)
13	G3	VBUS_B	IN	(PD)	(PD)	USB device bus detection signal

PD: Pull Down
PU: Pull Up

CPU I/F

Pin	Ball	Name	I/O	RESET	Terminal type	Terminal description	
					Bus Mode ⇒	16bit Strobe mode	16bit BE mode
20	J2	XRESET	IN	—	—	Reset signal	
31	L2	XRD	IN	—	—	Read strobe	
33	L4	XWRL (XWR)	IN	—	—	Write strobe (lower)	Write strobe
32	L3	XWRH (XBEH)	IN	—	—	Write strobe (upper)	High-byte enable
30	K2	XCS	IN	—	—	Chip select signal	
37	G5	XINT	OUT	High	2mA (Tri-state)	Interrupt signal	
38	L5	XDREQ0	OUT	High	2mA	DMA0 request	
39	H5	XDACK0	IN	—	—	DMA0 acknowledge	
40	J5	XDREQ1	OUT	High	2mA	DMA1 request	
41	G6	XDACK1	IN	—	—	DMA1 acknowledge	
21	J4	XBEL	IN	—	—	Must be fixed at High or Low	Low-byte enable
22	J3	CA1	IN	—	—	CPU bus address	
23	F4	CA2	IN	—	—		
24	G4	CA3	IN	—	—		
25	H4	CA4	IN	—	—		
26	K3	CA5	IN	—	—		
27	K4	CA6	IN	—	—		
28	K5	CA7	IN	—	—		
29	K1	CA8	IN	—	—		
44	J6	CD0	BI	Hi-Z	2mA	CPU data bus	
45	K6	CD1	BI	Hi-Z	2mA		
46	L6	CD2	BI	Hi-Z	2mA		
47	H6	CD3	BI	Hi-Z	2mA		
48	J7	CD4	BI	Hi-Z	2mA		
51	K7	CD5	BI	Hi-Z	2mA		
52	H7	CD6	BI	Hi-Z	2mA		
53	J8	CD7	BI	Hi-Z	2mA		
55	L8	CD8	BI	Hi-Z	2mA		
56	K8	CD9	BI	Hi-Z	2mA		
57	J9	CD10	BI	Hi-Z	2mA		
58	L9	CD11	BI	Hi-Z	2mA		
59	K9	CD12	BI	Hi-Z	2mA		
60	H9	CD13	BI	Hi-Z	2mA		
61	K10	CD14	BI	Hi-Z	2mA		
62	L10	CD15	BI	Hi-Z	2mA		

The XINT terminal can be set to 1/0 or Hi-Z/0 mode, depending on register settings.
PD: Pull Down
PU: Pull Up

6. TERMINAL FUNCTIONS

IDE I/F

Pin	Ball	Name	I/O	RESET	Terminal type	Terminal description
103	B10	HDA2	OUT	Hi-Z	4mA	IDE register address
97	C10	HDA1	OUT	Hi-Z	4mA	
99	A10	HDA0	OUT	Hi-Z	4mA	
105	C9	XHCS1	OUT	Hi-Z	4mA	Control register access chip select
104	C6	XHCS0	OUT	Hi-Z	4mA	Command block register access chip select
93	D9	XHIOR	OUT	Hi-Z	4mA	IDE read strobe
92	D8	XHIOW	OUT	Hi-Z	4mA	IDE write strobe
91	D11	HDMARQ	IN	(PD)	(PD)	DMA transfer request
95	D6	XHDMACK	OUT	Hi-Z	4mA	DMA transfer acknowledgement
94	D7	HIORDY	IN	(PU)	(PU)	IDE register ready signal
96	C11	HINTRQ	IN	(PD)	(PD)	IDE interrupt request
68	K11	XHRESET	OUT	Hi-Z	4mA	IDE bus reset
106	D4	XHDASP	IN	(PU)	(PU)	Drive enable/slave drive available
98	B11	XHPDIAG	IN	(PU)	(PU)	Diagnostic sequence end signal
90	E7	HDD15	BI	Hi-Z	4mA(PU)	IDE data bus
87	E6	HDD14	BI	Hi-Z	4mA(PU)	
84	E11	HDD13	BI	Hi-Z	4mA(PU)	
82	E8	HDD12	BI	Hi-Z	4mA(PU)	
77	G8	HDD11	BI	Hi-Z	4mA(PU)	
75	G10	HDD10	BI	Hi-Z	4mA(PU)	
72	H11	HDD9	BI	Hi-Z	4mA(PU)	
70	H10	HDD8	BI	Hi-Z	4mA(PU)	
69	J11	HDD7	BI	(PD)	4mA(PD)	
71	J10	HDD6	BI	Hi-Z	4mA(PU)	
74	G9	HDD5	BI	Hi-Z	4mA(PU)	
76	G11	HDD4	BI	Hi-Z	4mA(PU)	
81	F7	HDD3	BI	Hi-Z	4mA(PU)	
83	E10	HDD2	BI	Hi-Z	4mA(PU)	
86	F9	HDD1	BI	Hi-Z	4mA(PU)	
88	D10	HDD0	BI	Hi-Z	4mA(PU)	

PU and PD can be turned on or off via register settings.
PD: Pull Down
PU: Pull Up

Note: The IDE I/F terminals are all 5-V tolerant.

POWER

Pin	Ball	Name	Voltage	Terminal description
8, 12, 65, 80, 89, 102, 113, 117, 123	G7, D5, F11, E1, G2, B5, A7	HVDD	3.3V	Power supply for IDE I/F I/O, USB I/O, and TEST I/O
19, 35, 49, 64	H3, L7, H8	CVDD	1.8 to 3.3 V	Power supply for CPU I/F I/O
3, 14, 17, 42, 63, 66, 78, 100, 109, 118, 127	J1, E4, F6, H1, A3, A4 , C1, A9	LVDD	1.8V	OSC I/O and internal power supply
2, 4, 6, 7, 10, 15, 18, 34, 36, 43, 50, 54, 67, 73, 79, 85, 101, 110, 112, 115, 119	F3, E3, E5, F5, C8, F8, E9, F10, H2, F2, B2, B4, B6, B8, D2, C2, B9	VSS	0V	GND
16	A1, L1, A11, L11	N.C.	0V	NC terminal (connect to GND)

7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Item	Symbol	Rating	Units
Power supply voltage	HVDD	VSS - 0.3 to 4.0	V
	CVDD	VSS - 0.3 to 4.0	V
	LVDD	VSS - 0.3 to 2.5	V
Input voltage	HVI	VSS - 0.3 to HVDD + 0.5	V
	CVI*1	VSS - 0.3 to CVDD + 0.5	V
	IVI*2	VSS - 0.3 to 5.5	V
	VVI*3	VSS - 0.3 to 6.0	V
	LVI*4	VSS - 0.3 to LVDD + 0.5	V
Output voltage	HVO	VSS - 0.3 to HVDD + 0.5	V
	CVO*1	VSS - 0.3 to CVDD + 0.5	V
Output current/terminal	IOUT	±10	mA
Storage temperature	Tstg	-65 to 150	°C

*1 CPU-I/F
*2 IDE-I/F
*3 VBUS_B
*4 XI

7.2 Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Units
Power supply voltage	HVDD	3.00	3.30	3.60	V
	CVDD	1.65	—	3.60	V
	LVDD	1.65	1.80	1.95	V
Input voltage	HVI	-0.3	—	HVDD+0.3	V
	CVI*1	-0.3	—	CVDD+0.3	V
	IVI*2	-0.3	—	5.5	V
	VVI*3	-0.3	—	6.0	V
	LVI*4	-0.3	—	LVDD+0.3	V
Ambient temperature	Ta	-40	25	85	°C

*1 CPU-I/F
*2 IDE-I/F
*3 VBUS_B
*4 XI

Power to the IC should be turned on in the sequence shown below.

LVDD (internal) → HVDD, CVDD (IO section)

Likewise, power to the IC should be turned off in the sequence shown below.

HVDD, CVDD (IO section) → LVDD (internal)

Note: Avoid leaving the HVDD or CVDD on continuously (for more than 1 second) when the LVDD is off, since doing so may affect the chip reliability.

7.3 DC Characteristics

7.3.1 Current Consumption

Item	Symbol	Condition	Min.	Typ.	Max.	Units
Power supply feed current	*1					
Power supply current	IDDH	HVDD = 3.3V(typ), HVDD = 3.6V(max)	—	41	65	mA
	IDDCH	CVDD = 3.3V(typ), CVDD = 3.6V(max)	—	1	4	mA
	IDDCL	CVDD = 1.8V(typ), CVDD = 1.95V(max)	—	0.7	2	mA
	IDDL	LVDD = 1.8V(typ), LVDD = 1.95V(max)	—	75	120	mA
Stationary current	*2					
Power supply current	IDDS	VIN = HVDD,CVDD,LVDD or VSS HVDD = 3.6V CVDD = 3.6V LVDD = 1.95V	—	—	80	μA
Input leakage						
Input leakage current	IL	HVDD = 3.6V CVDD = 3.6V LVDD = 1.95V HVIH = HVDD CVIH = CVDD LVIH = LVDD VIL = VSS	-5	—	5	μA
Input leakage						
Input leakage current (5-V tolerant)	ILIF	HVDD = 3.0V CVDD = 1.65V LVDD = 1.65V HVOH = 5.5V	-10	—	10	μA

*1: Typ values are measured with the USB-HDD connected as USB host and when transferring data between the IDE-HDD and USB-HDD (actual transfer rate 30 MB/s). Max. values are estimated from these values.
*2: Stationary current with Ta = 25°C and both terminals in input mode.

Current consumption measurements for various power management states using Seiko Epson operating conditions (Ta = 25°C)

Item	Condition	Min.	Typ.	Max.	Units
SLEEP	CPU bus operation *1 *2				
Power supply power	HVDD = 3.3V CVDD = 3.3V LVDD = 1.8V	—	0.23	—	mW
SNOOZE	CPU bus operation *1 *2				
Power supply power	HVDD = 3.3V CVDD = 3.3V LVDD = 1.8V	—	1.8	—	mW
ACTIVE60(IDE⇔CPU)	*3				
Power supply power	HVDD = 3.3V CVDD = 3.3V LVDD = 1.8V	—	41	—	mW
ACT_DEVICE(IDE⇔USB)	*4				
Power supply power	HVDD = 3.3V CVDD = 3.3V LVDD = 1.8V	—	131	—	mW
ACT_HOST(IDE⇔USB)	Copy *5				
Power supply power	HVDD = 3.3V CVDD = 3.3V LVDD = 1.8V	—	134	—	mW
ACT_HOST(IDE⇔USB)	Direct Copy *6				
Power supply power	HVDD = 3.3V CVDD = 3.3V LVDD = 1.8V	—	273	—	mW

*1: When the CPU is accessing memory (e.g., SRAM or ROM) connected to the CPU bus.
*2: Excluding current consumption due to internal S1R72C05 DP pull-up resistor (approx. 200 μA).
*3: When transferring data between the IDE-HDD and CPU (actual transfer rate 4 MB/s).
*4: When connected to the PC as a USB device and when transferring data between the IDE-HDD and USB (actual transfer rate 25 MB/s).
*5: With the USB-HDD connected as USB host and when transferring data between the IDE-HDD and USB-HDD (actual transfer rate 5.3 MB/s).
*6: With the USB-HDD connected as USB host and when transferring data between the IDE-HDD and USB-HDD (actual transfer rate 30 MB/s).

7.3.2 Input Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Units
Input characteristics (LVCMOS)	Terminal name: TEST, TDI, TCK, TRST, TMS					
H-level input voltage	VIH1	HVDD = 3.6V	2.2	—	—	V
L-level input voltage	VIL1	HVDD = 3.0V	—	—	0.8	V
Input characteristics (LVCMOS)	Terminal name: CA[8:1], CD[15:0], XCS, XRD, XWRL, XWRH, XBEL, XDACK0, XDACK1, XRESET					
H-level input voltage	VIH2	CVDD = 3.6V	2.2	—	—	V
L-level input voltage	VIL2	CVDD = 3.0V	—	—	0.8	V
H-level input voltage	VIH3	CVDD = 1.95V	1.27	—	—	V
L-level input voltage	VIL3	CVDD = 1.65V	—	—	0.57	V
Input characteristics (LVCMOS)	Terminal name: HDD[15:0], HDMARQ, HIORDY, HINTRQ, XHDASP, XHPDIAG					
H-level input voltage	VIH4	HVDD = 3.6V	2.2	—	—	V
L-level input voltage	VIL4	HVDD = 3.0V	—	—	0.8	V
Schmitt input characteristics	Terminal name: VBUSFLG_A					
H-level trigger voltage	VT+	HVDD = 3.6V	1.4	—	2.7	V
L-level trigger voltage	VT-	HVDD = 3.0V	0.6	—	1.8	V
Hysteresis voltage	ΔV	HVDD = 3.0V	0.3	—	—	V
Schmitt input characteristics (USB FS)	Terminal name: DP_A, DM_A, DP_B, DM_B					
H-level trigger voltage	VT+(USB)	HVDD = 3.6V	1.1	—	1.8	V
L-level trigger voltage	VT-(USB)	HVDD = 3.0V	1.0	—	1.5	V
Hysteresis voltage	ΔV(USB)	HVDD = 3.0V	0.1	—	—	V
Input characteristics (USB FS differential)	Terminal name: DP_A + DM_A pair, DP_B + DM_B pair					
Differential input sensitivity	VDS(USB)	HVDD = 3.0V Differential input voltage = 0.8 V to 2.5 V	—	—	0.2V	V
Input characteristics (VBUS)	Terminal name: VBUS_B					
H-level trigger voltage	VT+(VBUS)	HVDD = 3.6V	1.86	—	2.85	V
L-level trigger voltage	VT-(VBUS)	HVDD = 3.0V	1.48	—	2.23	V
Hysteresis voltage	ΔV(VBUS)	HVDD = 3.0V	0.31	—	0.64	V
Input characteristics	Terminal name: HDD[15:8], HDD[6:0], HIORDY, XHDASP, XHPDIAG, VBUSFLG_A					
Pull-up resistor	RPLU	VIL = VSS	50	100	240	kΩ
Input characteristics	Terminal name: HDD[7], HDMARQ, HINTRQ					
Pull-down resistor	RPLD	VIH = HVDD	50	100	240	kΩ
Input characteristics	Terminal name: VBUS_B					
Pull-down resistor	RPLDV	VIH = 5.0V	110	125	150	kΩ

7.3.3 Output Characteristics

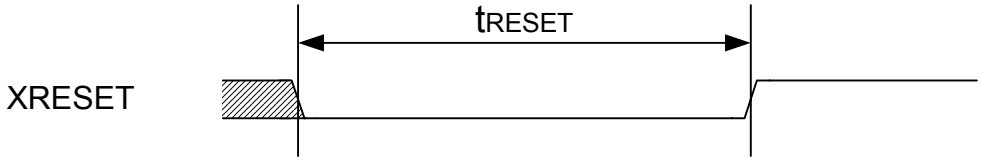
Item	Symbol	Condition	Min.	Typ.	Max.	Units
Output characteristics	Terminal name: CD[15:0], XDREQ0, XDREQ1, XINT					
H-level output voltage	VOH1	CVDD = 3.0V IOH = -2mA	CVDD-0.4	—	—	V
L-level output voltage	VOL1	CVDD = 3.0V IOL = 2mA	—	—	VSS+0.4	V
H-level output voltage	VOH2	CVDD = 1.65V IOH = -1mA	CVDD-0.4	—	—	V
L-level output voltage	VOL2	CVDD = 1.65V IOL = 1mA	—	—	VSS+0.4	V
Output characteristics	Terminal name: HDD[15:0], HDA[2:0], XHCS1, XHCS0, XHIOR, XHIOW, XHDMACK, XHRESET					
H-level output voltage	VOH3	HVDD = 3.0V IOH = -4mA	HVDD-1.0	—	—	V
L-level output voltage	VOL3	HVDD = 3.0V IOL = 4mA	—	—	VSS+0.4	V
Output characteristics	Terminal name: TDO, VBUSEN_A					
H-level output voltage	VOH4	HVDD = 3.0V IOH = -2mA	HVDD-0.4	—	—	V
L-level output voltage	VOL4	HVDD = 3.0V IOL = 2mA	—	—	VSS+0.4	V
Output characteristics (USB FS)	Terminal name: DP_A, DM_A, DP_B, DM_B					
H-level output voltage	VOH(USB)	HVDD=3.0V	2.8	—	—	V
L-level output voltage	VOL(USB)	HVDD=3.6V	—	—	0.3	V
Output characteristics (USB HS)	Terminal name: DP_A, DM_A, DP_B, DM_B					
H-level output voltage	VHSOH (USB)	HVDD = 3.0V	360	—	—	mV
L-level output voltage	VHSOL (USB)	HVDD = 3.6V	—	—	10.0	mV
Output characteristics	Terminal name: CD[15:0], XINT					
OFF-STATE leakage current	IOZ	HVDD = 3.6V CVDD = 1.95V CVOH = CVDD VOL = VSS	-5	—	5	μA
Output characteristics	Terminal name: HDD[15:0], HDA[2:0], XHCS1, XHCS0, XHIOR, XHIOW, XHDMACK, XHRESET					
OFF-STATE leakage current (5-V tolerant)	IOZHF	HVDD = 3.0V HVOH = 5.5V	-10	—	10	μA

7.3.4 Terminal Capacitance

Item	Symbol	Condition	Min.	Typ.	Max.	Units
Terminal capacitance	Terminal name: All input terminals					
Input terminal capacitance	CI	f = 10MHz HVDD = CVDD = LVDD = VSS	—	—	10	pF
Terminal capacitance	Terminal name: All output terminals					
Output terminal capacitance	CO	f = 10MHz HVDD = CVDD = LVDD = VSS	—	—	10	pF
Terminal capacitance	Terminal name: All input/output terminals (except DP_A, DM_A, DP_B, DM_B)					
Input/output terminal capacitance 1	CIO1	f = 10MHz HVDD = CVDD = LVDD = VSS	—	—	10	pF
Terminal capacitance	Terminal name: DP_A, DM_A, DP_B, DM_B					
Input/output terminal capacitance 2	CIO2	f = 10MHz HVDD = CVDD = LVDD = VSS	—	—	10	pF

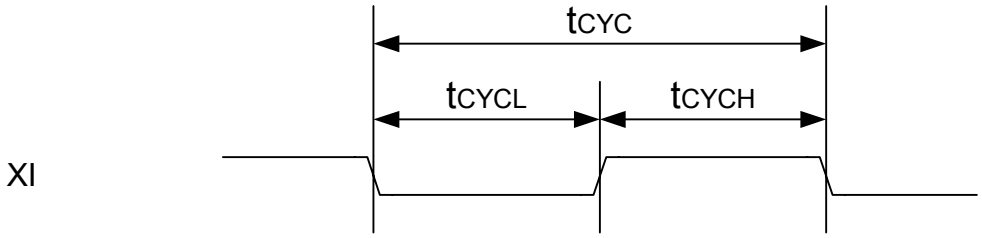
7.4 AC Characteristics

7.4.1 Reset Timing



Code	Description	Min.	Typ.	Max.	Units
t_{RESET}	Reset pulse width	40	—	—	ns

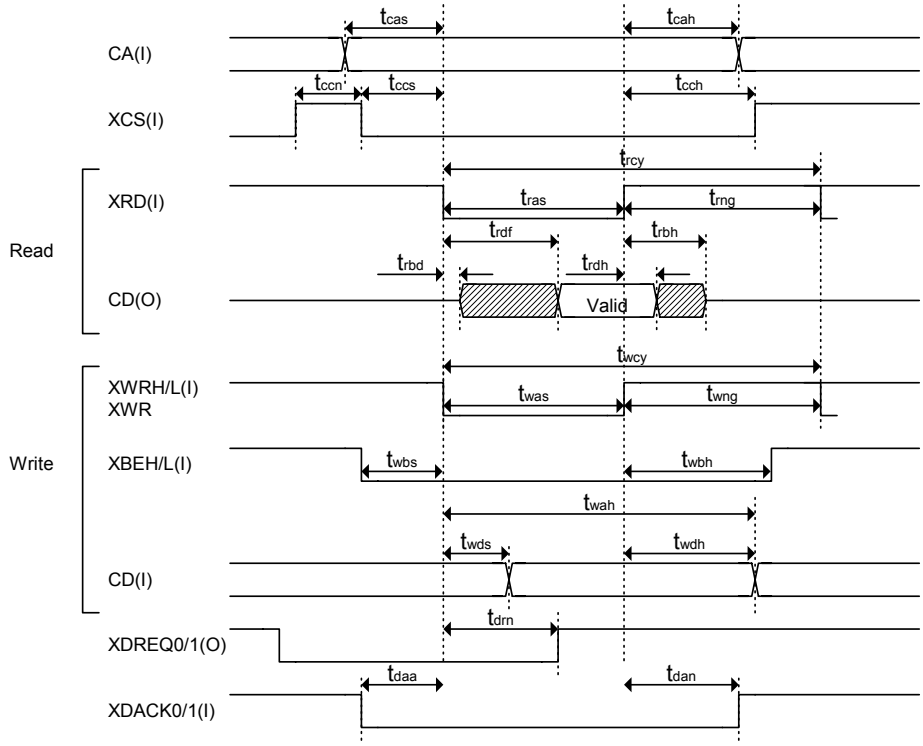
7.4.2 Clock Timing



Code	Description	Min.	Typ.	Max.	Units
t_{CYC}	Clock cycle (ClkSelect=0)	11.999	12	12.001	MHz
t_{CYC}	Clock cycle (ClkSelect=1)	23.998	24	24.002	MHz
$\frac{t_{CYCH}}{t_{CYCL}}$	Clock duty	45	—	55	%

7.4.3 CPU/DMA I/F Access Timing

7.4.3.1 Specifications for CVDD = 1.65 V to 3.6 V

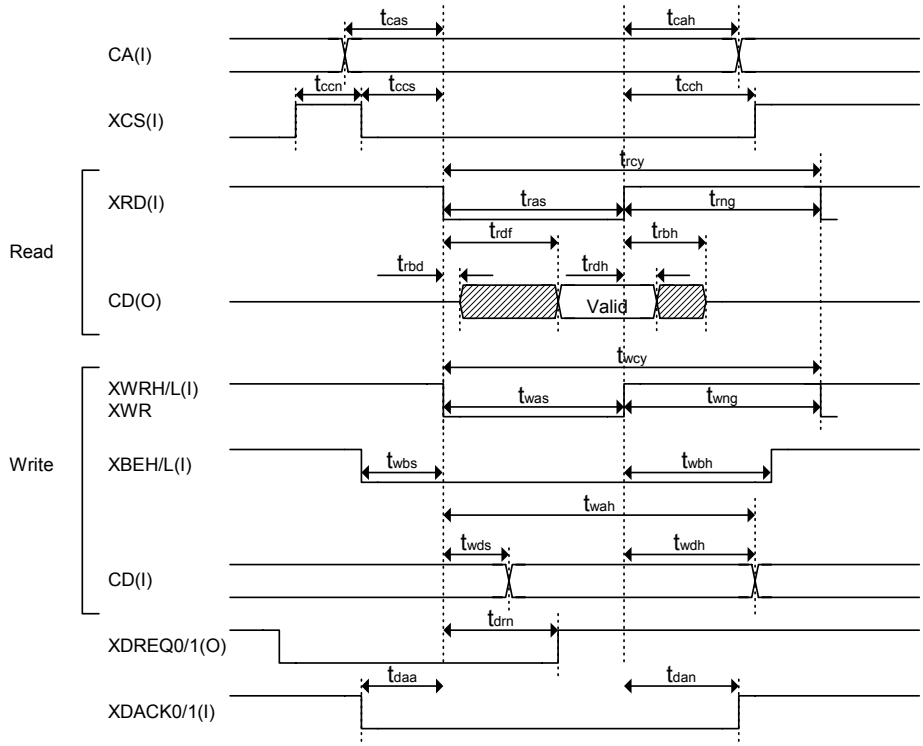


(CL=30pF)

Code	Item	Min.	Typ.	Max.	unit
t_{cas}	Address setup time	6	—	—	ns
t_{cah}	Address hold time	6	—	—	ns
t_{ccs}	XCS setup time	6	—	—	ns
t_{cch}	XCS hold time	6	—	—	ns
t_{ccn}	XCS Negate time (Only when CPUIF mode is set*)	15	—	—	ns
t_{rcy}	Read cycle	80	—	—	ns
t_{ras}	Read strobe assert time	40	—	—	ns
t_{rng}	Read strobe negate time	25	—	—	ns
t_{rbd}	Read data output start time	1	—	—	ns
t_{rdf}	Read data confirmation time	—	—	35	ns
t_{rdh}	Read data hold time	3	—	—	ns
t_{rbh}	Read data output delay time	—	—	10	ns
t_{wcy}	Write cycle	80	—	—	ns
t_{was}	Write strobe assert time	40	—	—	ns
t_{wng}	Write strobe negate time	25	—	—	ns
t_{wbs}	Write byte enable setup time	6	—	—	ns
t_{wbh}	Write byte enable hold time	6	—	—	ns
t_{wds}	Write data acknowledge delay time	—	—	10	ns
t_{wdh}	Write data hold time (after strobe negation)	6	—	—	ns
t_{wah}	Write data hold time (after strobe assertion)	50	—	—	ns
t_{drn}	XDREQ0/1 negate delay time	—	—	35	ns
t_{daa}	XDACK0/1 setup time	6	—	—	ns
t_{dan}	XDACK0/1 hold time	6	—	—	ns

* For details of CPUIF mode setting, refer to “Technical Manual.”

7.4.3.2 Specifications When Limited to CVDD = 3.0 V to 3.6 V



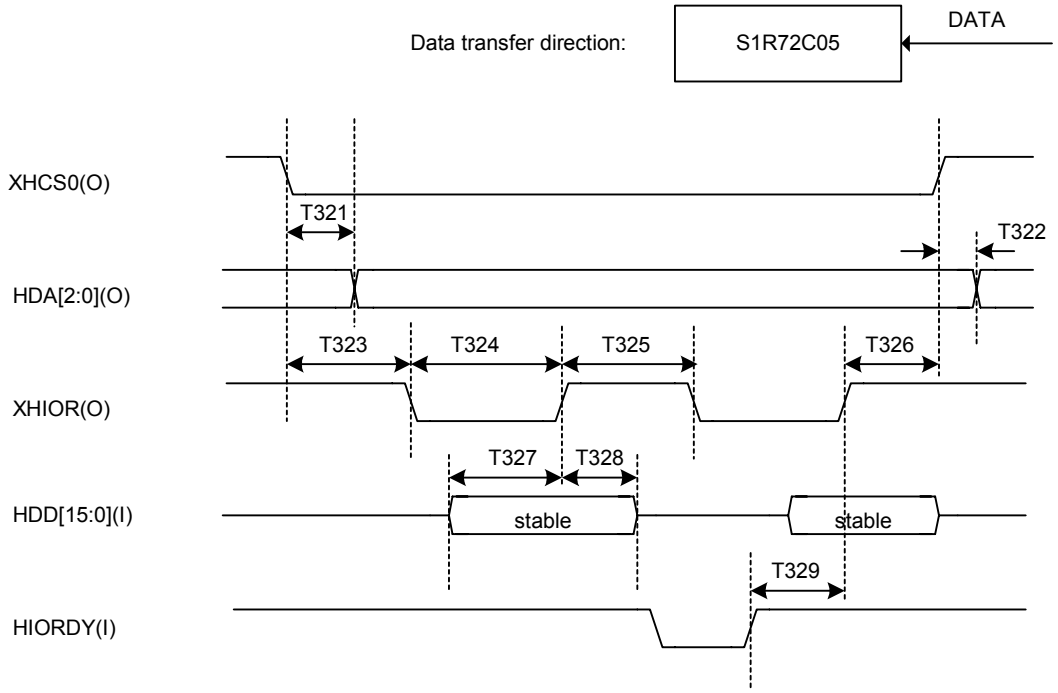
(CL=30pF)

Code	Item	Min.	Typ.	Max.	unit
t_{cas}	Address setup time	6	—	—	ns
t_{cah}	Address hold time	6	—	—	ns
t_{ccs}	XCS setup time	6	—	—	ns
t_{cch}	XCS hold time	6	—	—	ns
t_{ccn}	XCS Negate time (Only when CPUIF mode is set*)	15	—	—	ns
t_{rcy}	Read cycle	75	—	—	ns
t_{ras}	Read strobe assert time	37	—	—	ns
t_{rng}	Read strobe negate time	25	—	—	ns
t_{rbd}	Read data output start time	1	—	—	ns
t_{rdf}	Read data confirmation time	—	—	30	ns
t_{rdh}	Read data hold time	3	—	—	ns
t_{rbh}	Read data output delay time	—	—	10	ns
t_{wcy}	Write cycle	75	—	—	ns
t_{was}	Write strobe assert time	37	—	—	ns
t_{wng}	Write strobe negate time	25	—	—	ns
t_{wbs}	Write byte enable setup time	6	—	—	ns
t_{wbh}	Write byte enable hold time	6	—	—	ns
t_{wds}	Write data acknowledge delay time	—	—	10	ns
t_{wdh}	Write data hold time (after strobe negation)	6	—	—	ns
t_{wah}	Write data hold time (after strobe assertion)	50	—	—	ns
t_{drn}	XDREQ0/1 negate delay time	—	—	30	ns
t_{daa}	XDACK0/1 setup time	6	—	—	ns
t_{dan}	XDACK0/1 hold time	6	—	—	ns

* For details of CPUIF mode setting, refer to “Technical Manual.”

7.4.4 IDE I/F Timing

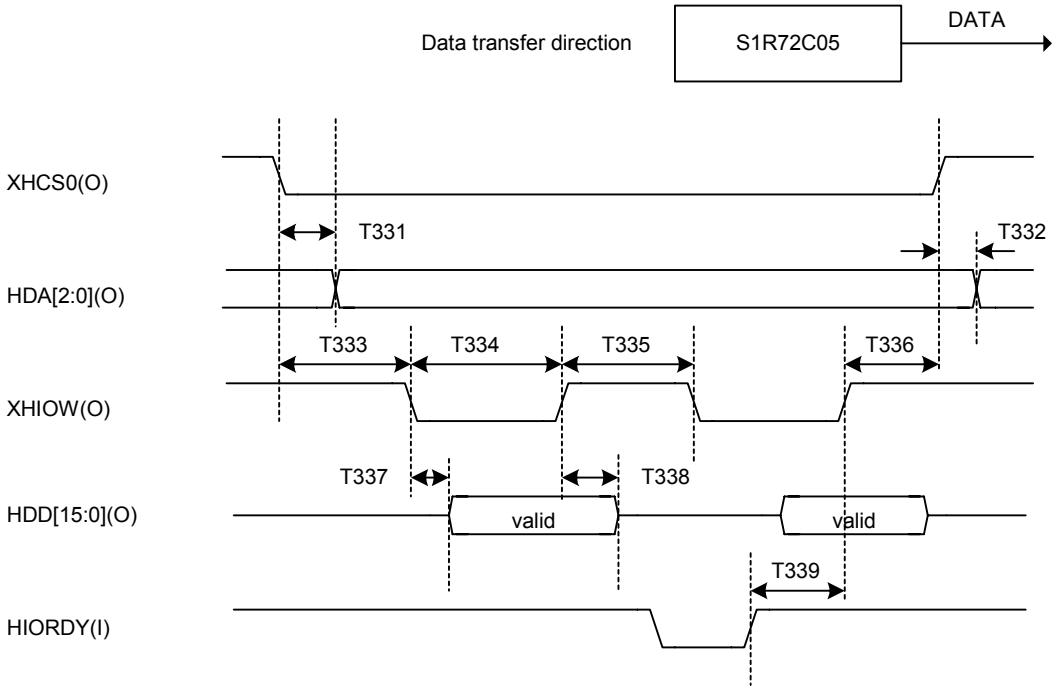
7.4.4.1 PIO Read Timing



Code	Description	Min.	Typ.	Max.	Units
T321	XHCS0 ↓ → HDA HDA output delay time	—	0	—	ns
T322	XHCS0 ↑ → HDA HDA hold time	—	0	—	ns
T323	XHCS0 ↓ → XHIOR ↓ XHCS0 setup time	80	—	—	ns
T324	XHIOR ↓ → XHIOR ↑ XHIOR assert pulse width	—	(AP+4) * 16.7 - 3	—	ns
T325	XHIOR ↑ → XHIOR ↓ XHIOR negate pulse width	—	(NP+4) * 16.7 + 3	—	ns
T326	XHIOR ↑ → XHCS0 ↑ XHCS0 hold time	50	—	—	ns
T327	HDD → XHIOR ↑ Data setup time	10	—	—	ns
T328	XHIOR ↑ → HDD Data hold time	0	—	—	ns
T329	HIORDY ↑ → XHIOR ↑ XHIOR output delay time	—	—	25	ns

*1: AP = IDE_Tmod.AssertPulseWidth, NP = IDE_Tmod.NegatePulseWidth
For detailed information, refer to “IDE Transfer Mode” in the register description.

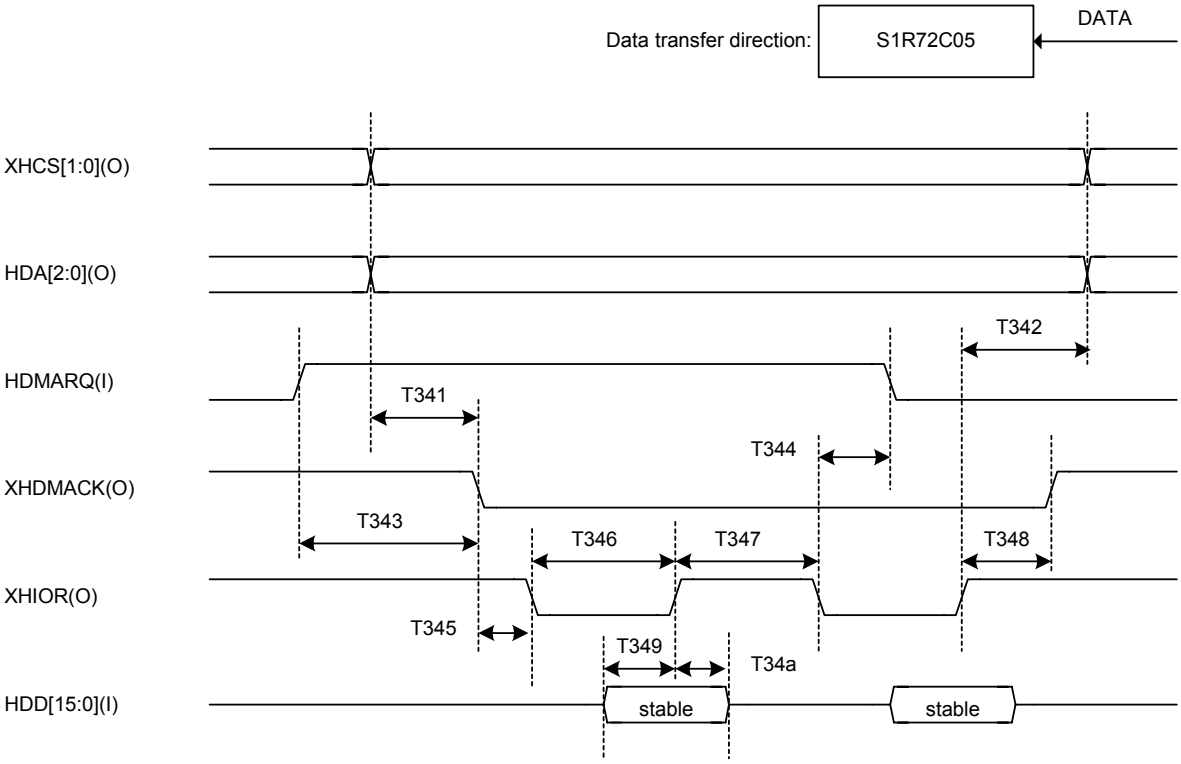
7.4.4.2 PIO Write Timing



Code	Description	Min.	Typ.	Max.	Units
T331	XHCS0 ↓ → HDA HDA output delay time	—	0	—	ns
T332	XHCS0 ↑ → HDA HDA hold time	—	0	—	ns
T333	XHCS0 ↓ → XHIOW ↓ XHCS0 setup time	80	—	—	ns
T334	XHIOW ↓ → XHIOW ↑ XHIOW assert pulse width	—	(AP+4) * 16.7 - 3	—	ns
T335	XHIOW ↑ → XHIOW ↓ XHIOW negate pulse width	—	(NP+4) * 16.7 + 3	—	ns
T336	XHIOW ↑ → XHCS0 ↑ XHCS0 hold time	50	—	—	ns
T337	XHIOW ↓ → HDD Data output delay time	0	—	10	ns
T338	XHIOW ↑ → HDD Data bus negate time	33	—	45	ns
T339	HIORDY ↑ → XHIOW ↑ XHIOW output delay time	—	—	25	ns

*1: AP = IDE_Tmod.AssertPulseWidth, NP = IDE_Tmod.NegatePulseWidth
For detailed information, refer to “IDE Transfer Mode” in the register description.

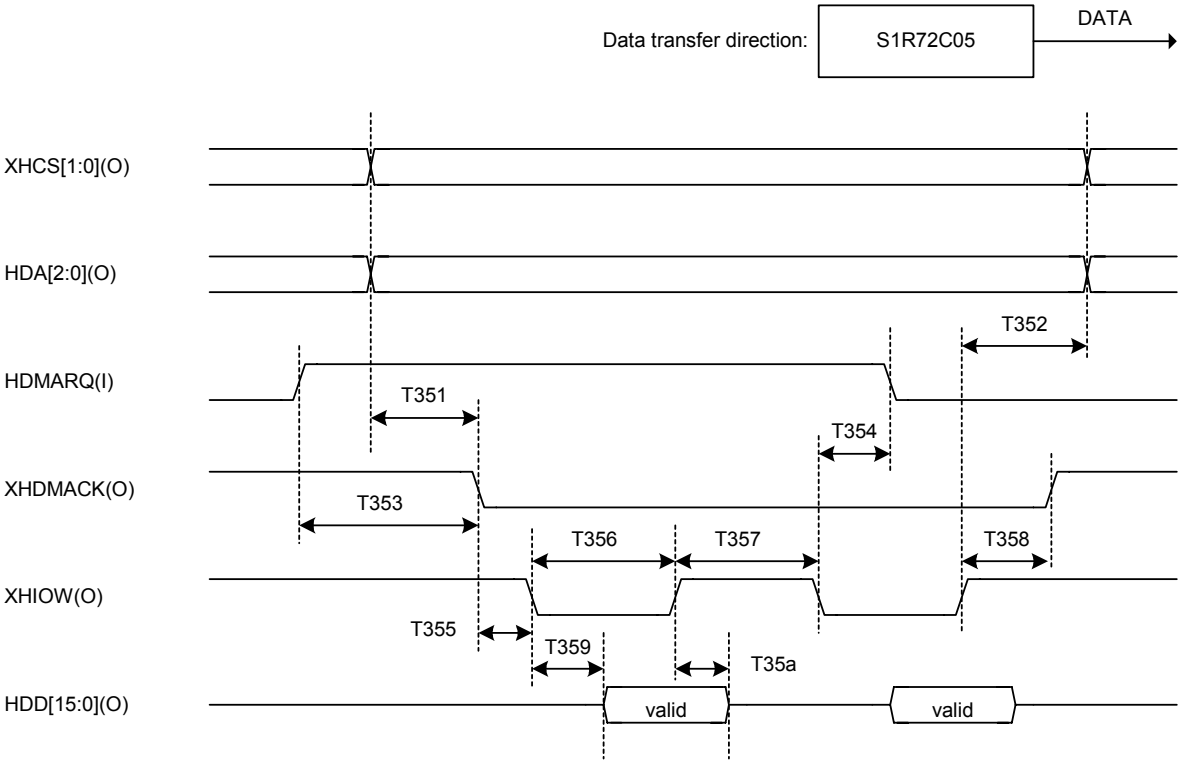
7.4.4.3 DMA Read Timing



Code	Description	Min.	Typ.	Max.	Units
T341	XHCS ↑, HDA → XHDMACK ↓ Address setup time	70	—	—	ns
T342	XHIOR ↑ → XHCS ↑, HAD Address hold time	50	—	—	ns
T343	HDMARQ ↑ → XHDMACK ↓ ↓ XHDMACK response time	17	—	—	ns
T344	XHIOR ↓ → HDMARQ negate HDMARQ hold time	0	—	—	ns
T345	XHDMACK ↓ → XHIOR ↓ XHDMACK setup time	0	—	—	ns
T346	XHIOR ↓ → XHIOR ↑ XHIOR assert pulse width	—	(AP+4) * 16.7 - 3	—	ns
T347	XHIOR ↑ → XHIOR ↓ XHIOR negate pulse width	—	(NP+4) * 16.7 + 3	—	ns
T348	XHIOR ↑ → XHDMACK ↑ XHDMACK hold time	30	—	90	ns
T349	HDD → XHIOR ↑ Data setup time	10	—	—	ns
T34a	XHIOR ↑ → HDD Data bus hold time	0	—	—	ns

*1: AP = IDE_Tmod.AssertPulseWidth, NP = IDE_Tmod.NegatePulseWidth
For detailed information, refer to “IDE Transfer Mode” in the register description.

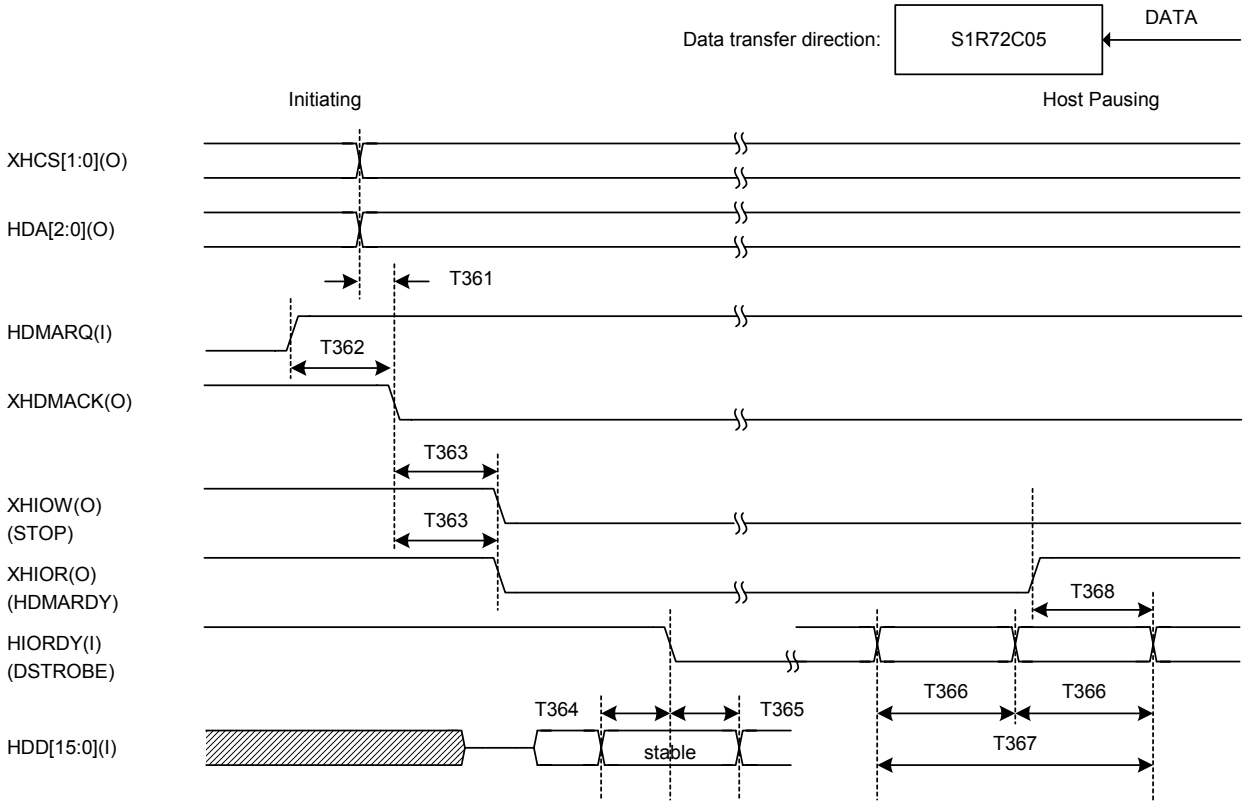
7.4.4.4 DMA Write Timing



Code	Description	Min.	Typ.	Max.	Units
T351	XHCS ↑, HDA → XHDMACK ↓ Address setup time	70	—	—	ns
T352	XHIOW ↑ → XHCS ↑, HDA Address hold time	50	—	—	ns
T353	HDMARQ ↑ → XHDMACK ↓ XHDMACK response time	17	—	—	ns
T354	XHIOW ↓ → HDMARQ negate HDMARQ hold time	0	—	—	ns
T355	XHDMACK ↓ → XHIOW ↓ XHDMACK setup time	0	—	—	ns
T356	XHIOW ↓ → XHIOW ↑ XHIOW assert pulse width	—	(AP+4) * 16.7 - 3	—	ns
T357	XHIOW ↑ → XHIOW ↓ XHIOW negate pulse width	—	(NP+4) * 16.7 + 3	—	ns
T358	XHIOW ↑ → XHDMACK ↑ XHDMACK hold time	30	—	90	ns
T359	XHIOW ↓ → HDD Data output delay time	0	—	10	ns
T35a	XHIOW ↑ → HDD Data bus hold time	33	—	45	ns

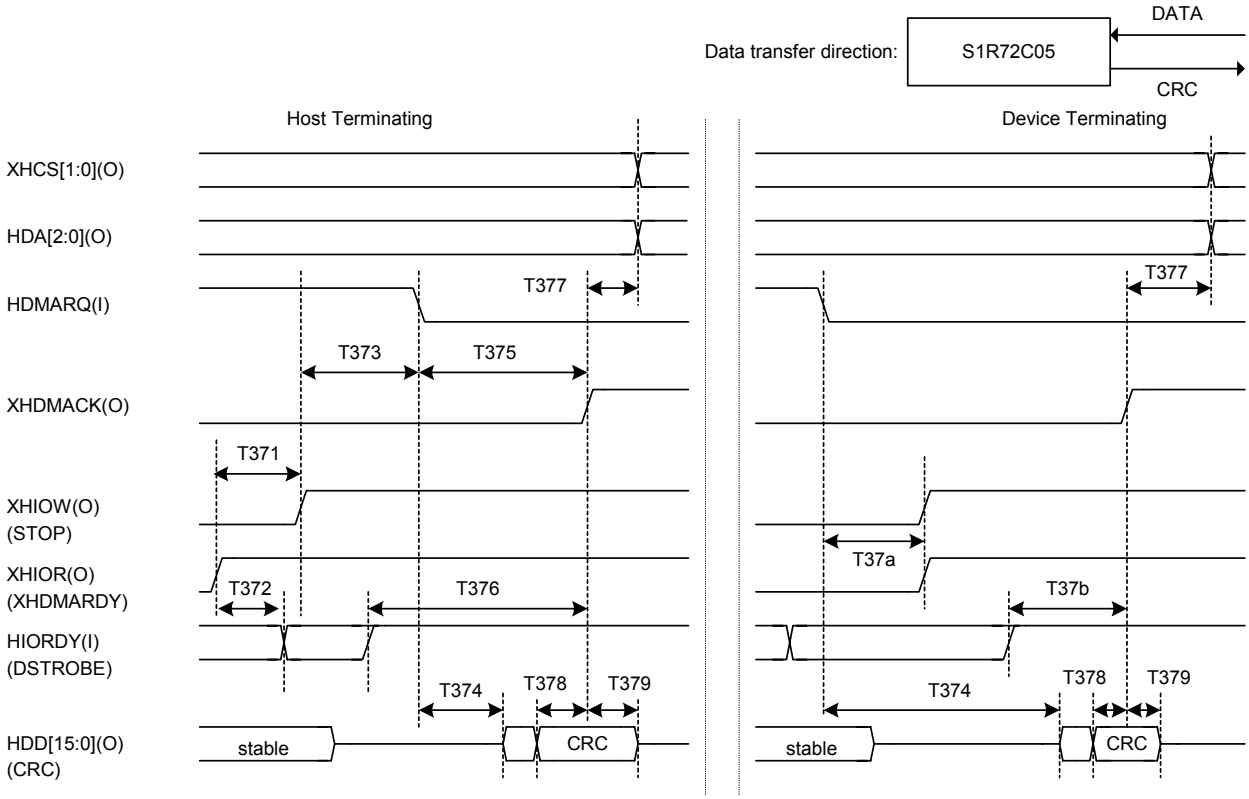
*1: AP = IDE_Tmod.AssertPulseWidth, NP = IDE_Tmod.NegatePulseWidth
For detailed information, refer to “IDE Transfer Mode” in the register description.

7.4.4.5 Ultra DMA Read Timing



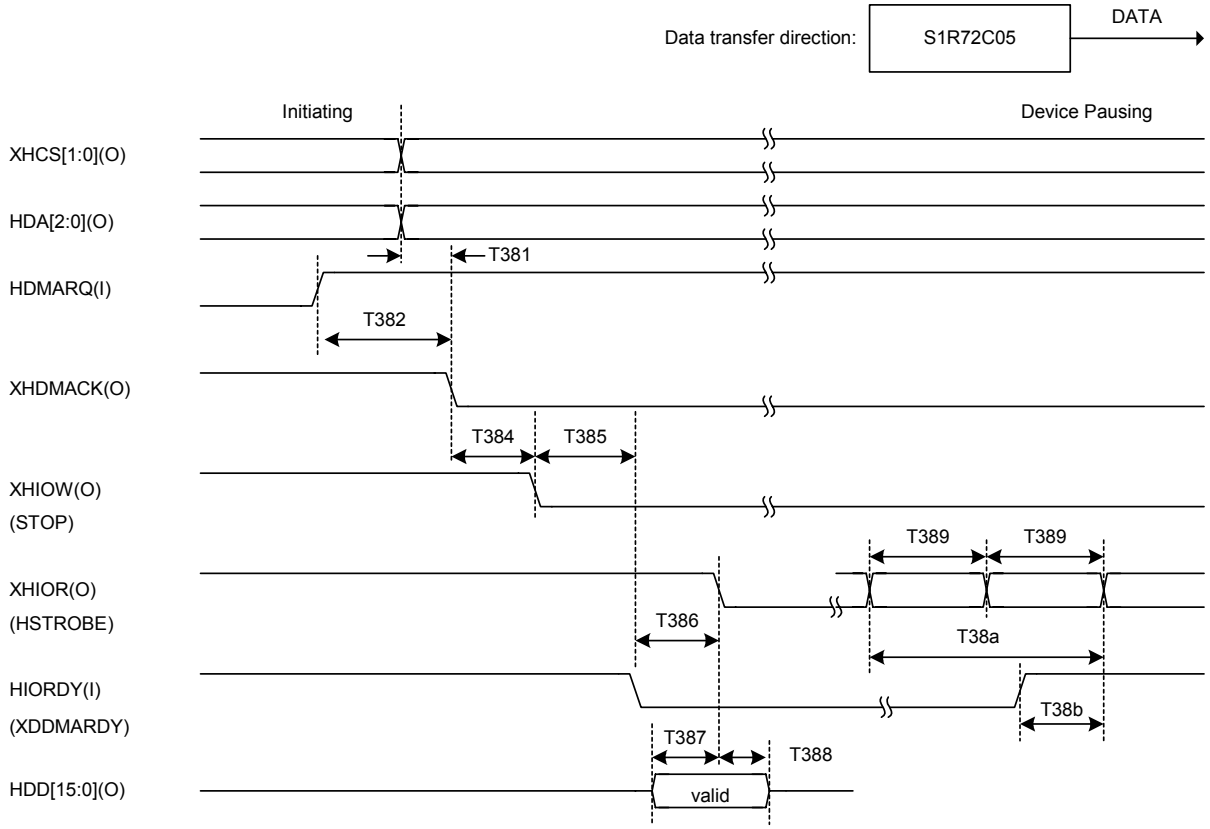
Code	Description	Min.	Typ.	Max.	Units
T361	XHCS ↑, HDA → XHDMACK ↓ Address setup time	80	—	—	ns
T362	HDMARQ ↑ → XHDMACK ↓ XHDMACK response time	65	—	—	ns
T363	XHDMACK ↓ → XHIOR(W) ↓ Envelope time	28	—	40	ns
T364	HDD → HIORDY Data setup time	4	—	—	ns
T365	HIORDY → HDD Data hold time	4	—	—	ns
T366	HIORDY → HIORDY HIORDY cycle time	15	—	—	ns
T367	HIORDY → HIORDY HIORDY cycle time x2	30	—	—	ns
T368	XHIOR ↑ → HIORDY Final STROBE time	—	—	IDE spec. t_{RFS}	ns

Ultra DMA Read Timing (continued)



Code	Description	Min.	Typ.	Max.	Units
T371	XHIOR ↑ → XHIOW ↑ Time to STOP assert	180	—	—	ns
T372	XHIOR ↑ → HIORDY Final STROBE time	—	—	IDE spec. t_{RFS}	ns
T373	XHIOW ↑ → HDMARQ ↓ Restricted interlock time	—	—	IDE spec. t_{LI}	ns
T374	HDMARQ ↓ → HDD Output delay time	70	—	—	ns
T375	HDMARQ ↓ → XHDMACK ↑ Minimum interlock time	160	—	—	ns
T376	HIORDY → XHDMACK ↑ Minimum interlock time	110	—	—	ns
T377	XHDMACK ↑ → XHCS0, 1 XHCS0, 1 hold time	35	—	—	ns
T378	HDD(CRC) → XHDMACK ↑ CRC data setup time	75	—	—	ns
T379	XHDMACK ↑ → HDD(CRC) CRC data hold time	12	—	—	ns
T37a	HDMARQ ↓ → XHIOR ↑ Restricted interlock time	20	—	38	ns
T37b	HIORDY → XHDMACK ↑ Minimum interlock time	110	—	—	ns

7.4.4.6 Ultra DMA Write Timing



Code	Description	Min.	Typ.	Max.	Units
T381	XHCS ↑, HDA → XHDMACK ↓ Address setup time	80	—	—	ns
T382	HDMARQ ↑ → XHDMACK ↓ XHDMACK response time	65	—	—	ns
T384	XHDMACK ↓ → XHIOW ↓ Envelope time	28	—	40	ns
T385	XHIOW ↓ → HIORDY ↓ Restricted interlock time	IDE spec. t_{LI}	—	IDE spec. t_{LI}	ns
T386	HIORDY ↓ → XHIOR ↓ Unrestricted interlock time	20	—	—	ns
T387	HDD → XHIOR ↓ Data setup time	—	(cyc+1) * 16.7	—	ns
T388	XHIOR ↓ → HDD Data hold time	—	(cyc+1) * 16.7	—	ns
T389	XHIOR → XHIOR XHIOR cycle time	—	(cyc+2) * 16.7	—	ns
T38a	XHIOR → XHIOR XHIOR cycle time x2	—	T389 * 2	—	ns
T38b	HIORDY ↑ → XHIOR Final STROBE time	20	—	38	ns

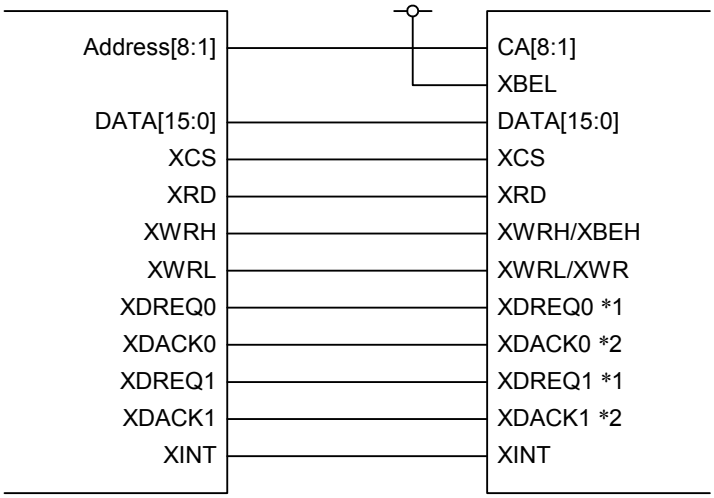
*1: cyc = UltraDMAcycle
For detailed information, refer to “IDE Ultra-DMA Transfer Mode” in the register description.

7.4.5 USB I/F Timing

Conforms to USB 2.0 standard
<Universal Serial Bus Specification Revision 2.0 Released on April 27, 2000>.

8. CONNECTION EXAMPLES

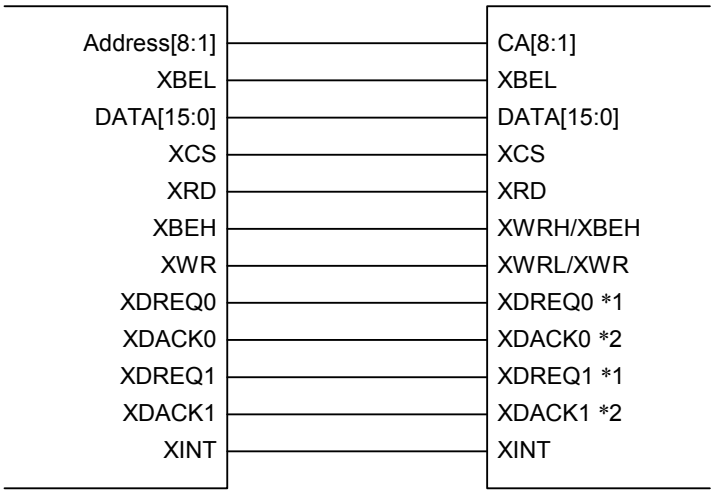
8.1 CPU I/F Connection Example



16-bit CPU (XWRH/XWRL) connection example

*1: Open when DMA is not used

*2: Fixed at inactive level when DMA is not used



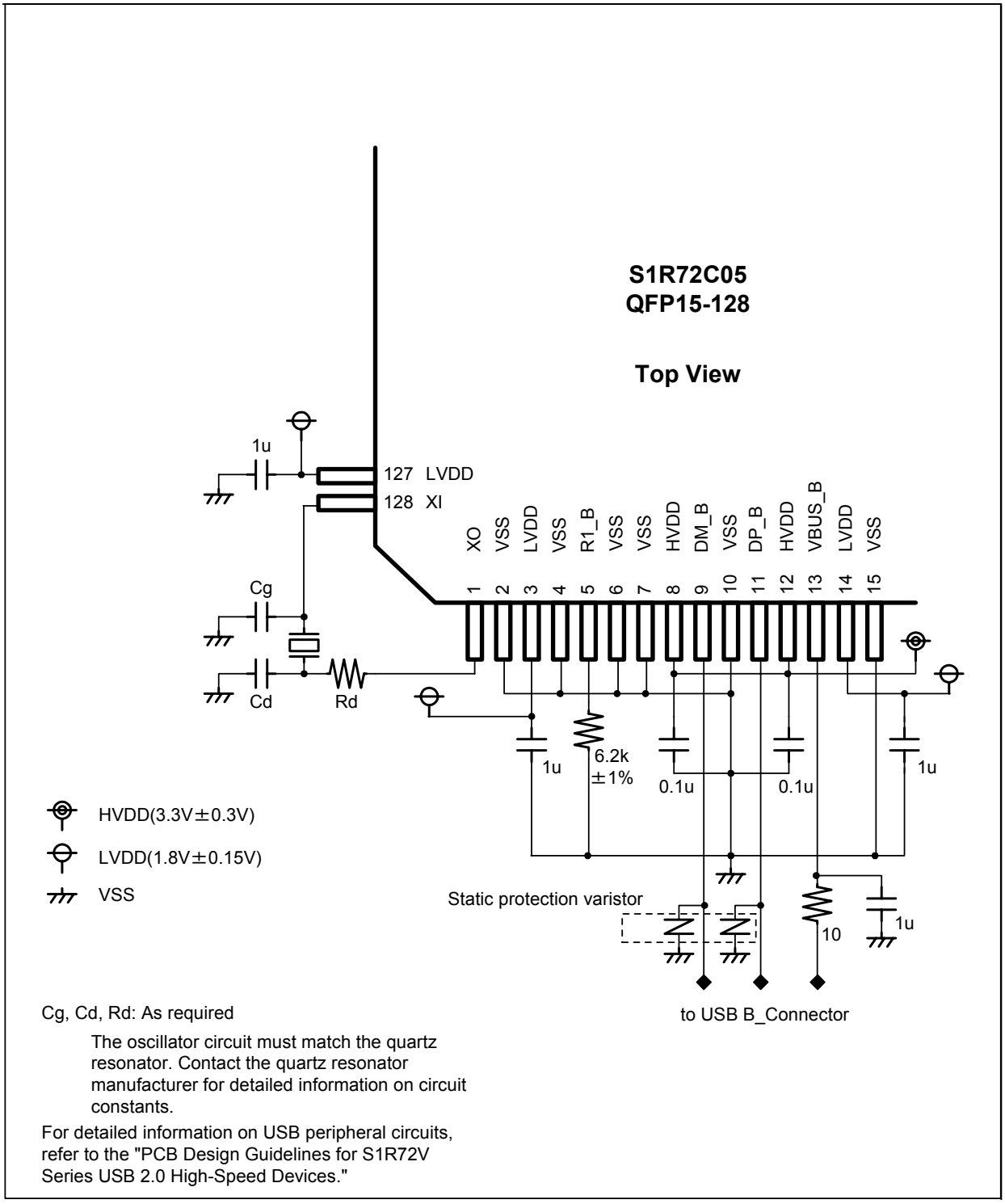
16-bit CPU (XBEH/XBEL) connection example

*1: Open when DMA is not used

*2: Fixed at inactive level when DMA is not used

8.2 USB I/F Connection Example

8.2.1 For QFP15-128 (Device Periphery)



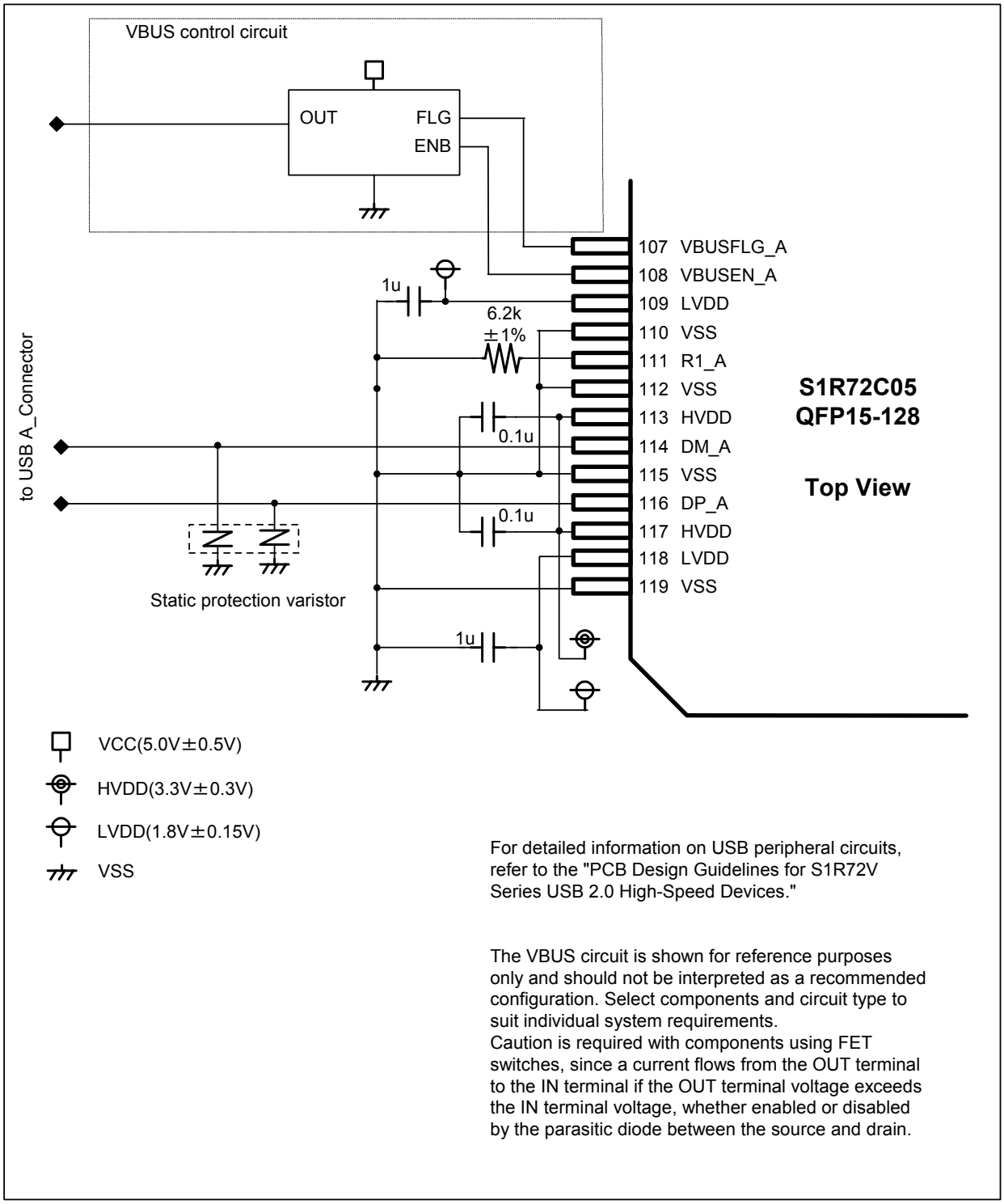
Cg, Cd, Rd: As required

The oscillator circuit must match the quartz resonator. Contact the quartz resonator manufacturer for detailed information on circuit constants.

For detailed information on USB peripheral circuits, refer to the "PCB Design Guidelines for S1R72V Series USB 2.0 High-Speed Devices."

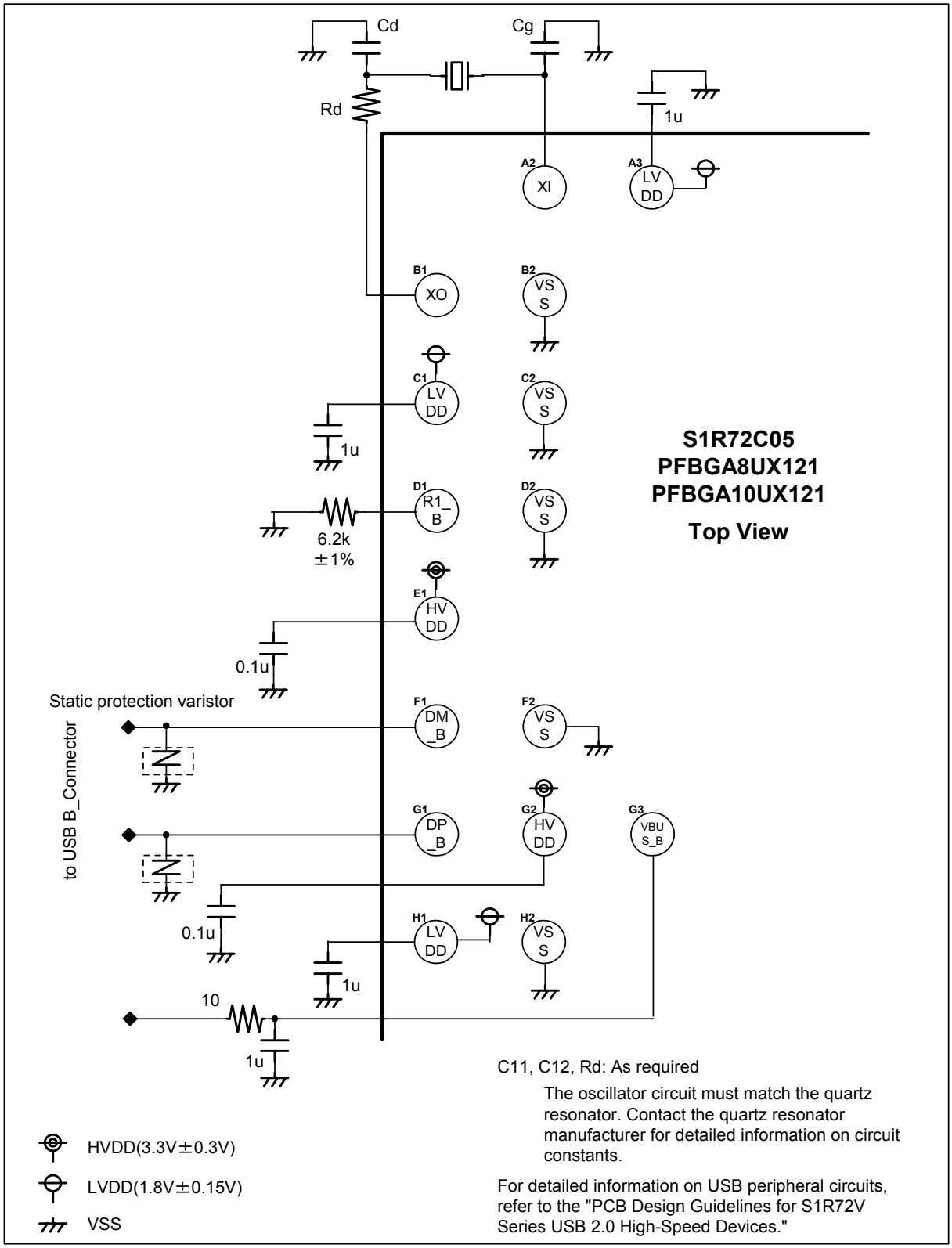
Select power supply elements carefully; their performance will affect USB signal waveform quality.

8.2.2 For QFP15-128 (Host Periphery)



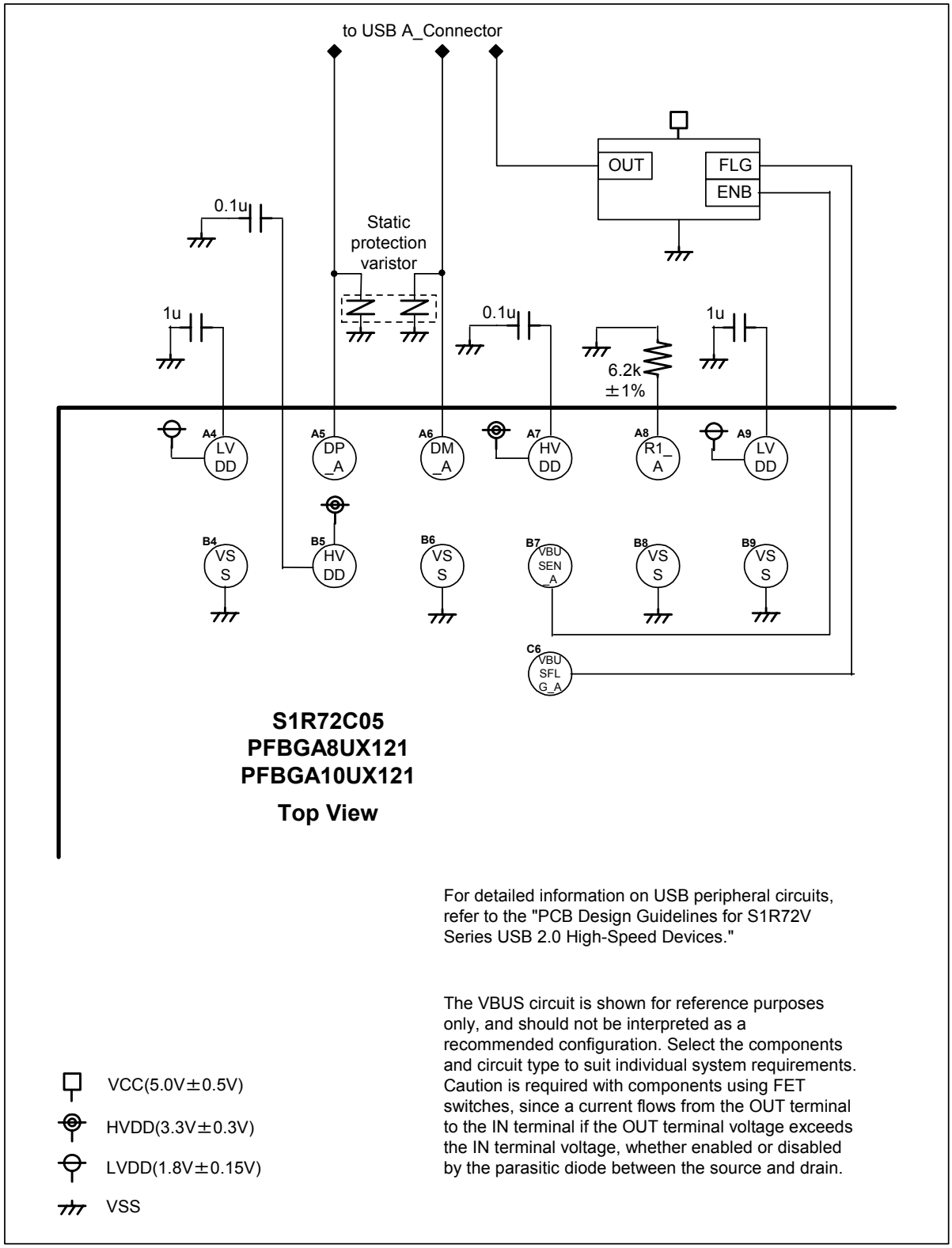
Select power supply elements carefully; their performance will affect USB signal waveform quality.

8.2.3 For PFBGA8UX121/PFBGA10UX121 (Device Periphery)



Select power supply elements carefully; their performance will affect USB signal waveform quality.

8.2.4 For PFBGA8UX121/PFBGA10UX121 (Host Periphery)



Select power supply elements carefully; their performance will affect USB signal waveform quality.

9. PRODUCT CODES

Table 9.1 Product codes

Product code	Product type
S1R72C05B08****	PFBGA8UX121 package
S1R72C05B10****	PFBGA10UX121 package
S1R72C05F15****	QFP15-128 package

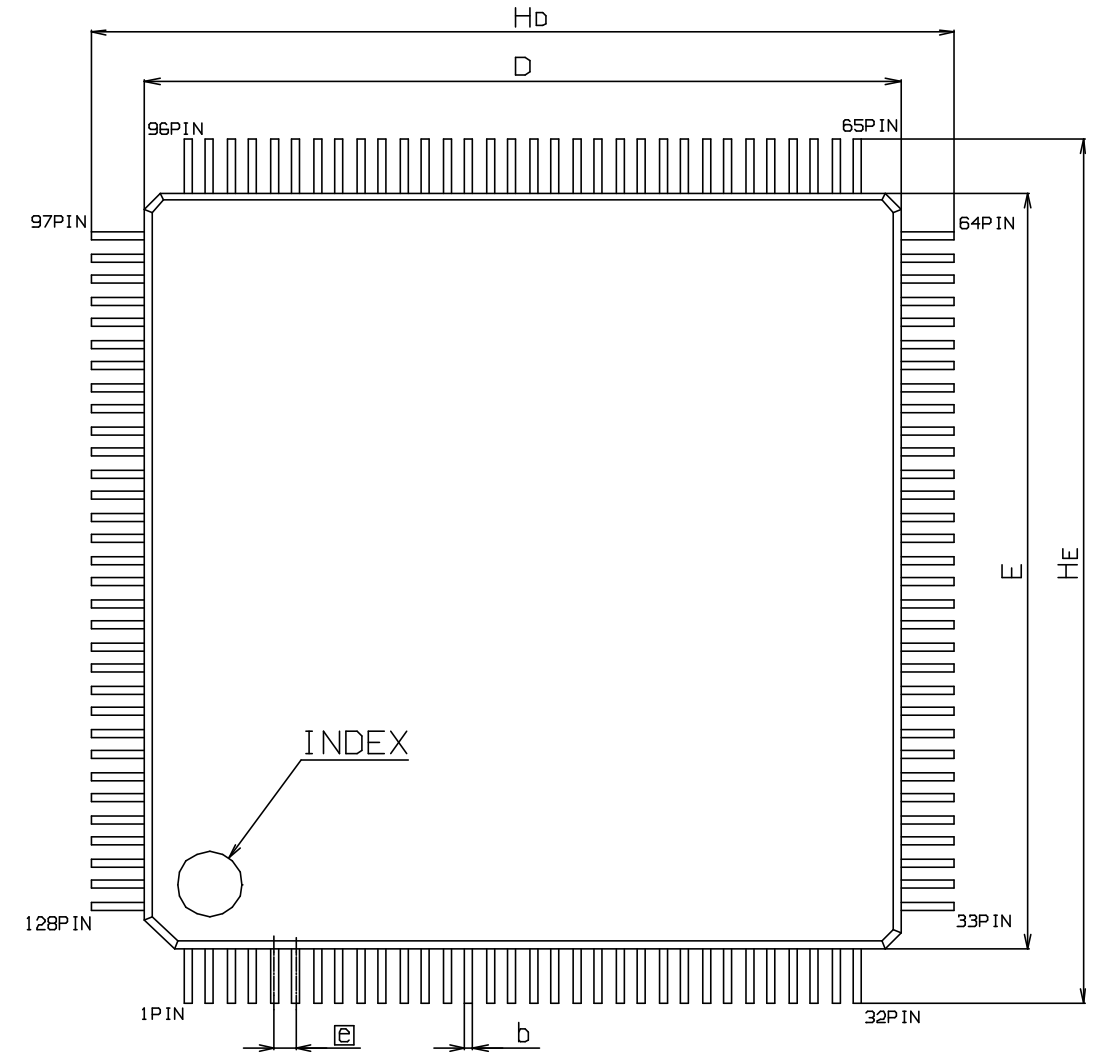
10. EXTERNAL DIMENSION DIAGRAMS

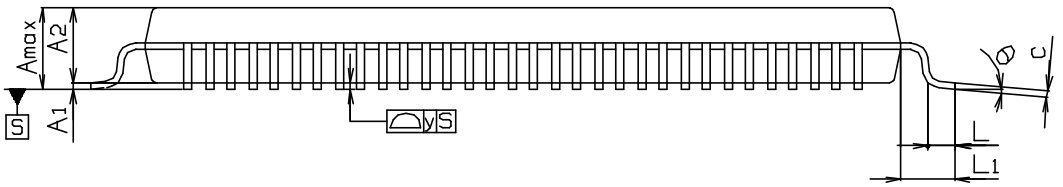
Refer the attached diagrams on the end of this document.

- QFP Package(QFP15-128)
- BGA Package (PFBGA8UX121)
- BGA Package (PFBGA10UX121)

Revision History

Date	Description of revision			
	Rev.	Page (old issue)	Classification	Description
08/21/2007	1.00	All pages	New	New issue





Symbol	Dimension in Millimeters		
	Min	Nom	Max
E	-	14	-
D	-	14	-
Amax	-	-	1.7
A1	-	0.1	-
A2	-	1.4	-
e	-	0.4	-
b	0.13	-	0.23
c	0.09	-	0.2
θ	0°	-	10°
L	0.3	-	0.75
L1	-	1	-
HE	-	16	-
HD	-	16	-
y	-	-	0.08

1 = 1mm

REV.	DATE	DRAW	CHECKED	APPROVED	CORRECTION ARTICLE
5.0	2004.08.11	C.SAITO	M.SONE	T.OTSUKI	-

TITLE
P-LQFP128-1414-0.40(QFP15-128PIN)

CAD FILE -

DWG No. 4900-0057

SCALE Free

SHEET 1 of 1

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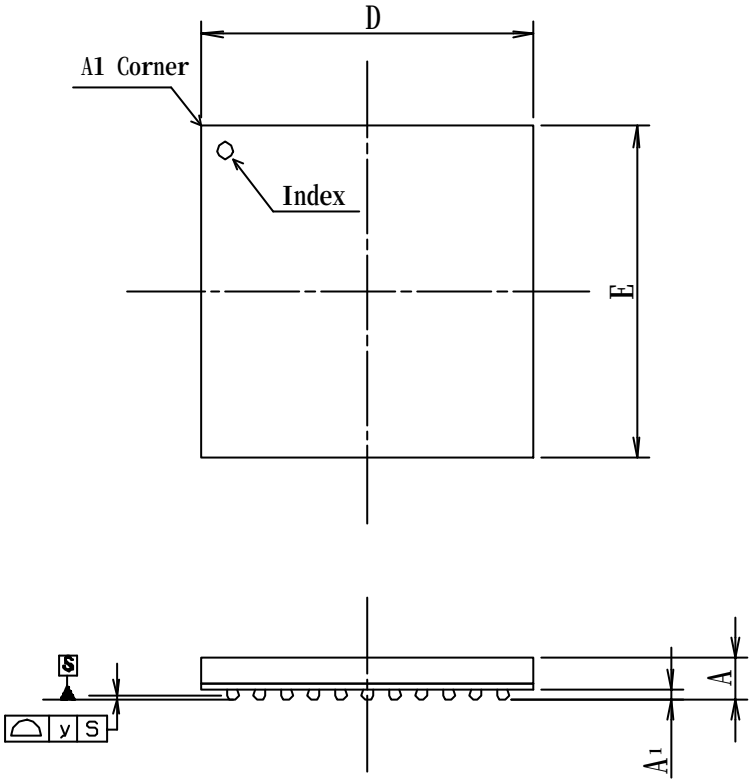
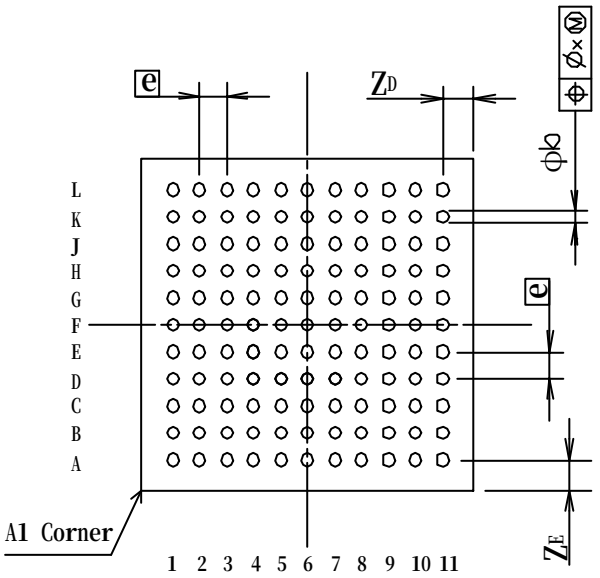
Top View



Bottom View



Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	-	8	-
E	-	8	-
A	-	-	1.2
A1	-	0.22	-
e	-	0.65	-
b	0.27	-	0.37
x	-	-	0.08
y	-	-	0.1
ZD	-	0.75	-
ZE	-	0.75	-

1 = 1mm

1.0	2005.03.25	O. SHOJI	M. SONE	T. OTSUKI	-
REV.	DATE	DRAW	CHECKED	APPROVED	CORRECTION ARTICLE
TITLE	P-TFBGA-121-0808-0.65(PFBGA8U-121)				-
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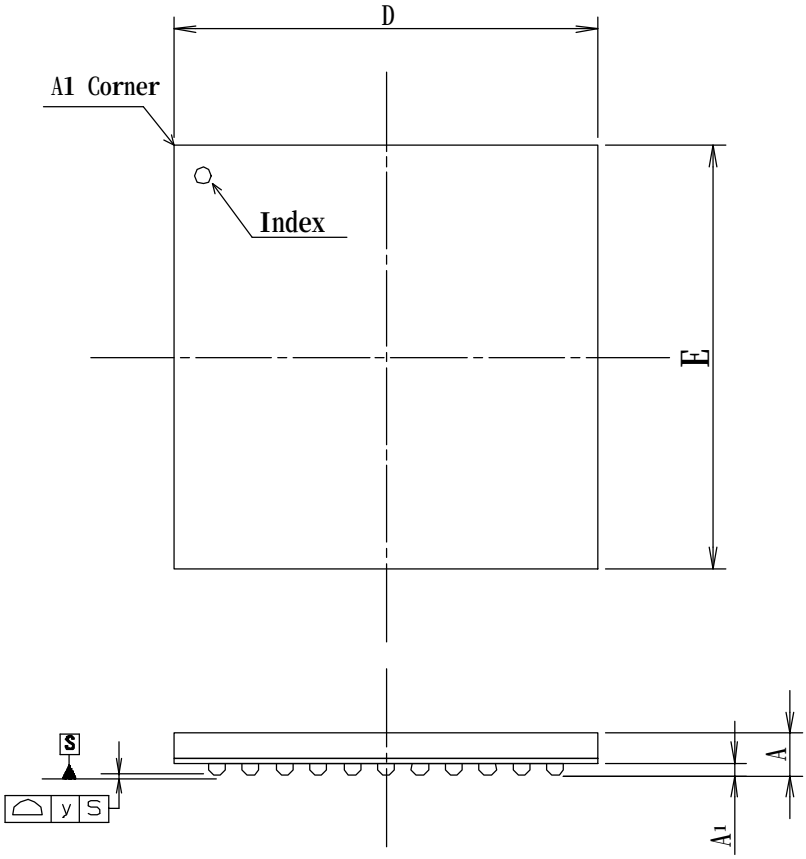
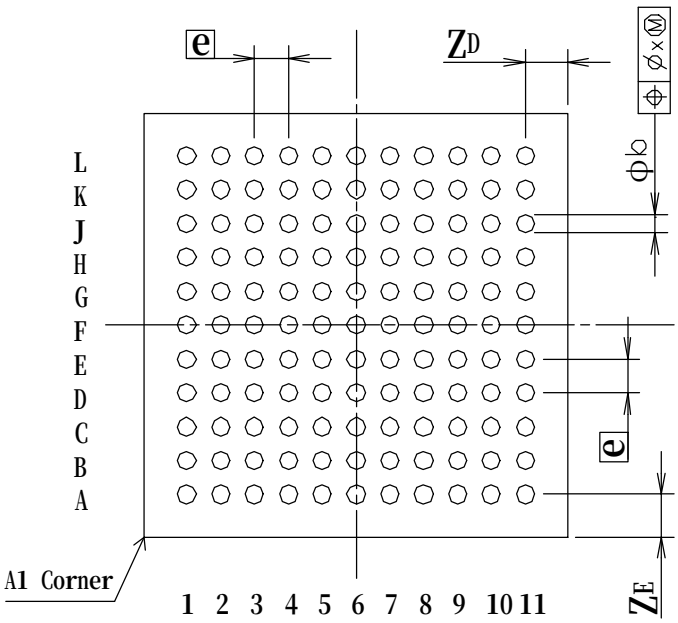
					SCALE Free SHEET 1 of 1

Top View



Bottom View



Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	-	10	-
E	-	10	-
A	-	-	1.2
A1	-	0.3	-
e	-	0.8	-
b	0.38	-	0.48
x	-	-	0.08
y	-	-	0.1
ZD	-	1	-
ZE	-	1	-

1 = 1mm

2.0	2004.10.18	C. SHOJI	M. SONE	T. OTSUKI	—
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