

N-Channel Power MOSFET

1000V, 1.85A, 8.5Ω

FEATURES

- 100% avalanche tested
- Advanced planar process
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

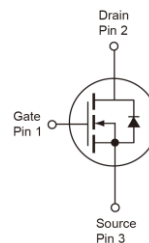
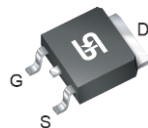
APPLICATIONS

- AC/DC LED Lighting
- Power Supply
- Power Meter

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	1000	V
$R_{DS(on)}$ (max)	8.5	Ω
Q_g	17	nC



TO-252 (DPAK)



Notes: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	Limit	UNIT
Drain-Source Voltage	V_{DS}	1000	V
Gate-Source Voltage	V_{GS}	±30	V
Continuous Drain Current ^(Note 1)	I_D	$T_C = 25^\circ\text{C}$	1.85
		$T_C = 100^\circ\text{C}$	1.16
Pulsed Drain Current ^(Note 2)	I_{DM}	7.4	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{DTOT}	77	W
Single Pulse Avalanche Energy ^(Note 3)	E_{AS}	20	mJ
Single Pulse Avalanche Current ^(Note 3)	I_{AS}	1.4	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	Limit	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	1.62	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62	°C/W

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu\text{A}$	BV_{DSS}	1000	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	3.5	4.5	5.5	V
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 1000V, V_{GS} = 0V$	I_{DSS}	--	--	1	μA
Drain-Source On-State Resistance (Note 4)	$V_{GS} = 10V, I_D = 0.9A$	$R_{DS(on)}$	--	6	8.5	Ω
Dynamic (Note 5)						
Total Gate Charge	$V_{DS} = 800V, I_D = 1.85A,$ $V_{GS} = 10V$	Q_g	--	17	--	nC
Gate-Source Charge		Q_{gs}	--	5	--	
Gate-Drain Charge		Q_{gd}	--	9	--	
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	C_{iss}	--	625	--	pF
Output Capacitance		C_{oss}	--	38	--	
Reverse Transfer Capacitance		C_{rss}	--	15	--	
Gate Resistance	$f = 1.0\text{MHz}, \text{open drain}$	R_g	--	2.2	--	Ω
Switching (Note 6)						
Turn-On Delay Time	$V_{DD} = 500V, R_G = 25\Omega,$ $I_D = 0.9A, V_{GS} = 10V$	$t_{d(on)}$	--	31	--	ns
Turn-On Rise Time		t_r	--	14	--	
Turn-Off Delay Time		$t_{d(off)}$	--	78	--	
Turn-Off Fall Time		t_f	--	44	--	
Source-Drain Diode						
Forward Voltage (Note 4)	$I_S = 1.85A, V_{GS} = 0V$	V_{SD}	--	--	1.4	V
Reverse Recovery Time	$V_R = 100V, I_S = 1.85A$ $di_f/dt = 100A/\mu\text{s}$	t_{rr}	--	359	--	ns
Reverse Recovery Charge		Q_{rr}	--	1.34	--	μC

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. $L = 20\text{mH}, I_{AS} = 1.4A, V_{DD} = 50V, R_G = 25\Omega,$ Starting $T_J = 25^\circ\text{C}$
4. Pulse test: $PW \leq 300\mu\text{s}, \text{duty cycle} \leq 2\%$
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

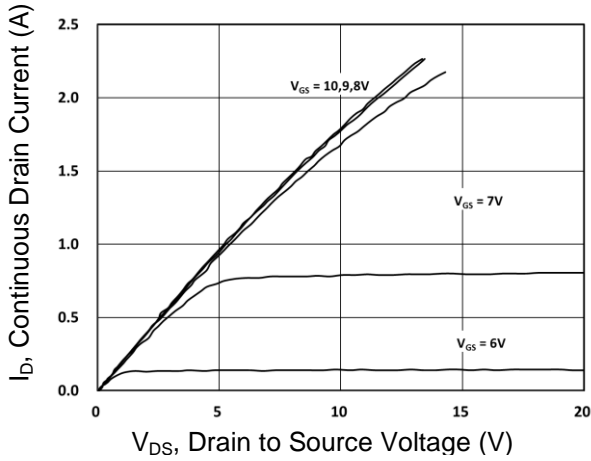
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM2N100CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

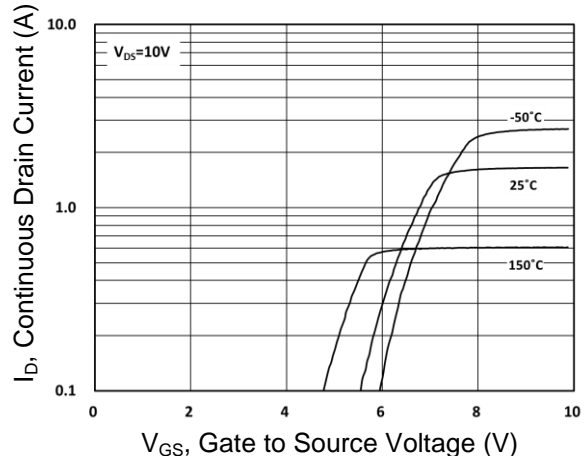
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

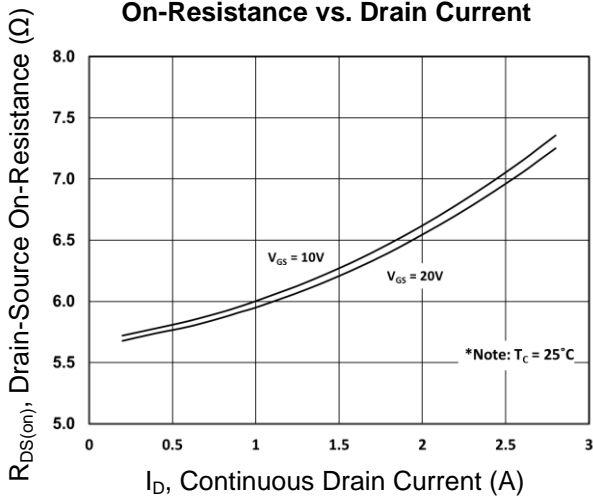
Output Characteristics



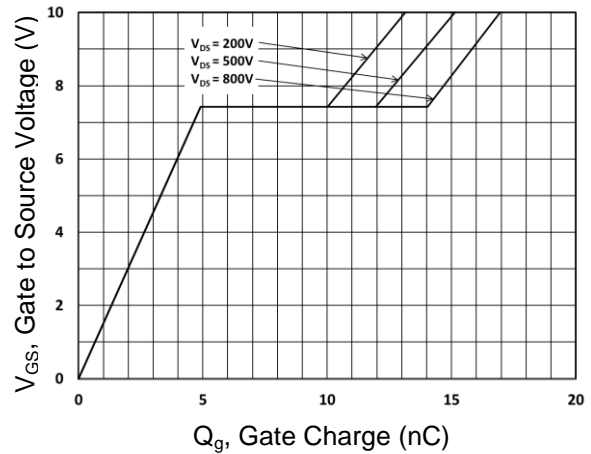
Transfer Characteristics



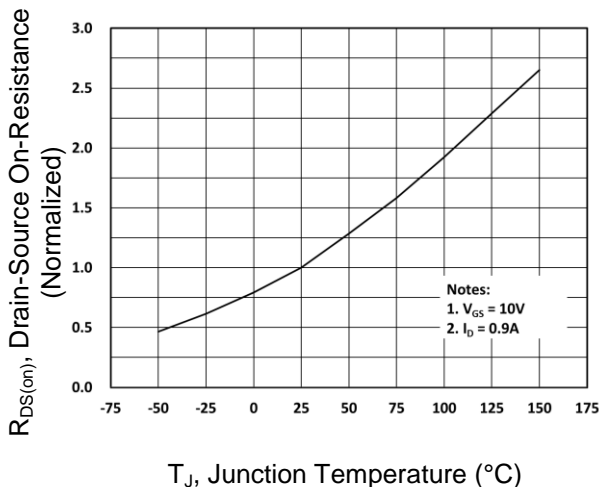
On-Resistance vs. Drain Current



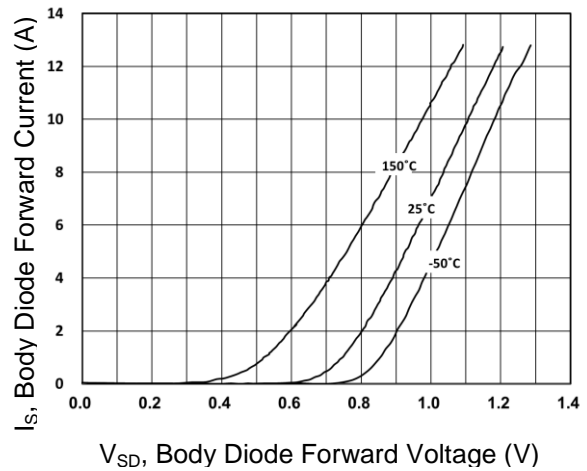
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



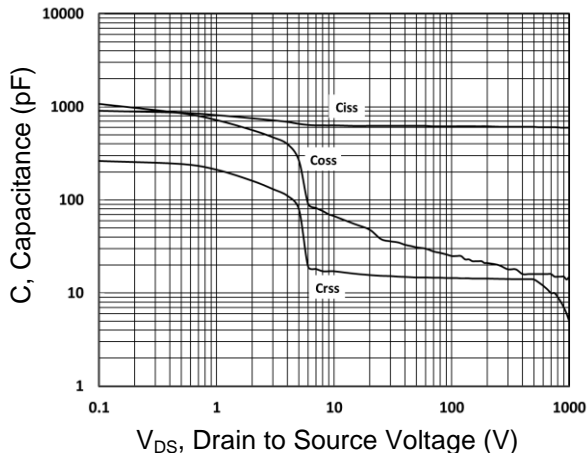
Source-Drain Diode Forward Current vs. Voltage



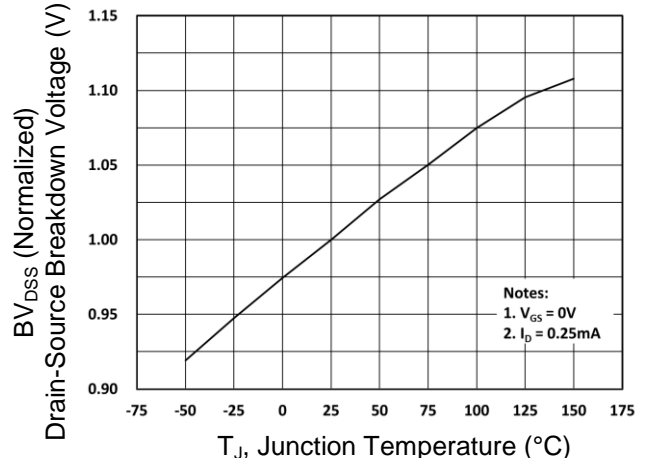
CHARACTERISTICS CURVES

($T_C = 25^\circ\text{C}$ unless otherwise noted)

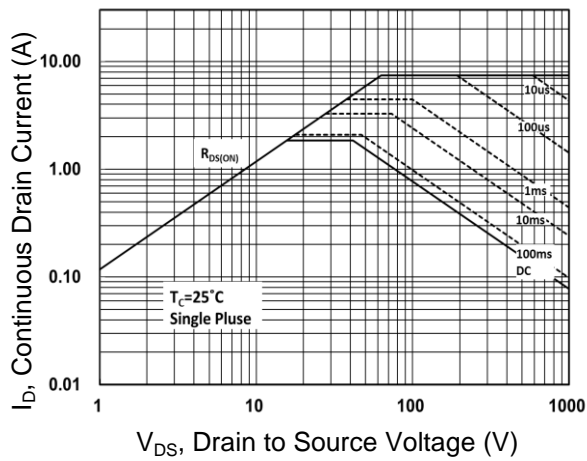
Capacitance vs. Drain-Source Voltage



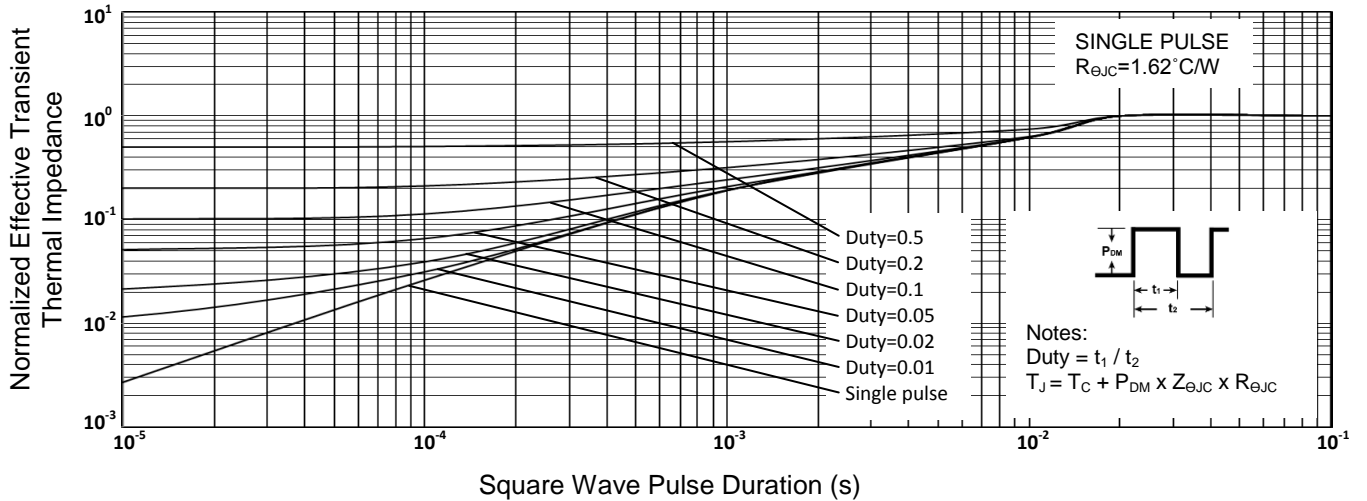
BV_{DSS} vs. Junction Temperature



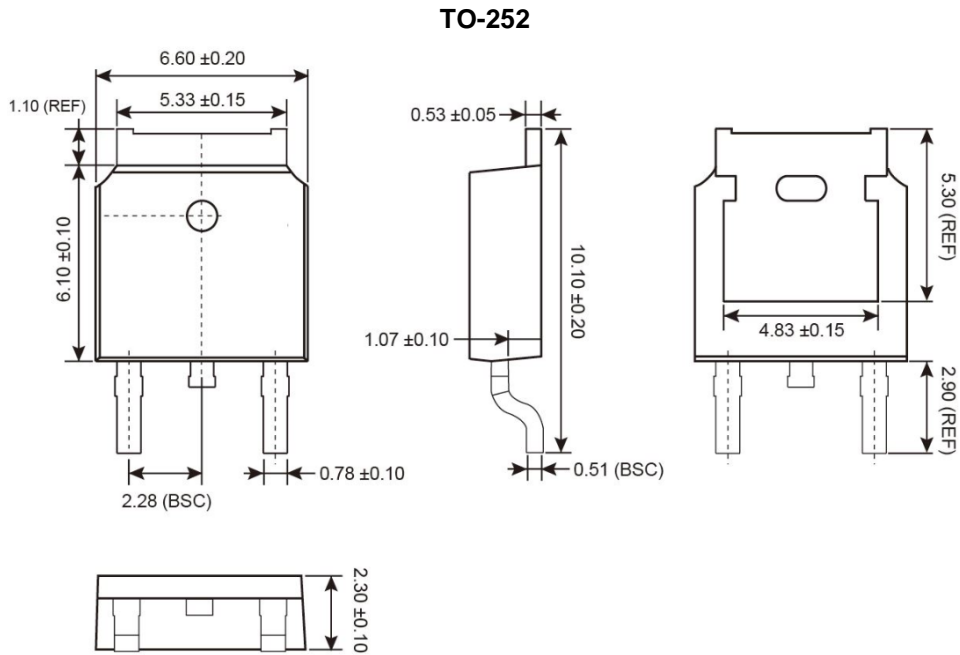
Maximum Safe Operating Area



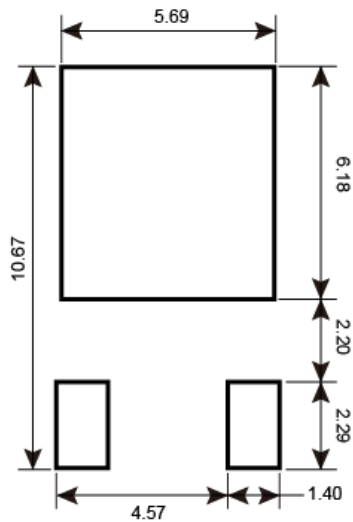
Normalized Thermal Transient Impedance, Junction-to-Case



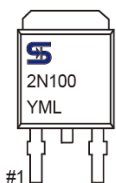
PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



SUGGESTED PAD LAYOUT



MARKING DIAGRAM



- Y** = Year Code
- M** = Month Code
- O** =Jan **P** =Feb **Q** =Mar **R** =Apr
- S** =May **T** =Jun **U** =Jul **V** =Aug
- W** =Sep **X** =Oct **Y** =Nov **Z** =Dec
- L** = Lot Code (1~9, A~Z)

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