



CMOS Analog Switches

FEATURES

- $\pm 15\text{-V}$ Input Range
- Low $r_{DS(on)}$: $30\ \Omega$
- Single Supply Operation
- Pin and Function Compatible with the JFET DG180 Family

BENEFITS

- Full Rail-to-Rail Analog Signal Range
- Minimizes Signal Error
- Low Power Dissipation

APPLICATIONS

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable and Battery Powered Systems

DESCRIPTION

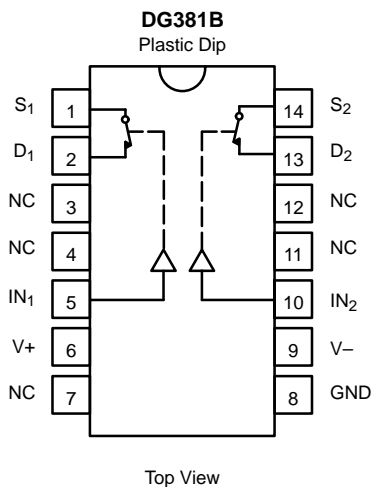
The DG381B–DG390B series of monolithic CMOS analog switches was designed for applications in instrumentation, communications, and process control. This series is suited for applications requiring fast switching and nearly flat on-resistance over the entire voltage range.

switches are ideal for battery powered applications, without sacrificing switching speed. Break-before-make switching action is guaranteed, and an epitaxial layer prevents latchup. Single supply operation is allowed by connecting the V– rail to 0 V.

Designed on Vishay Siliconix' PLUS-40 CMOS process, these devices achieve low power consumption (3.5 mW typical) and excellent on/off switch performance. These

Each switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. These switches are CMOS and quasi TTL logic compatible.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

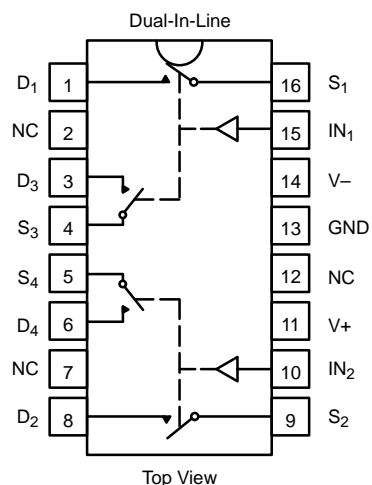


| TRUTH TABLE | |
|-------------|--------|
| Logic | Switch |
| 0 | ON |
| 1 | OFF |

Logic "0" $\leq 0.8\text{ V}$
Logic "1" $\geq 4\text{ V}$

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

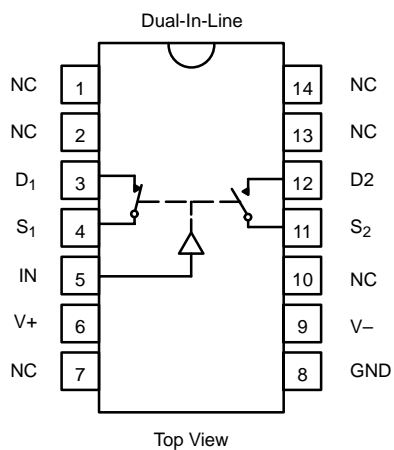
DG384B



| TRUTH TABLE | |
|-------------|--------|
| Logic | Switch |
| 0 | OFF |
| 1 | ON |

Logic "0" ≤ 0.8 V
 Logic "1" ≥ 4 V

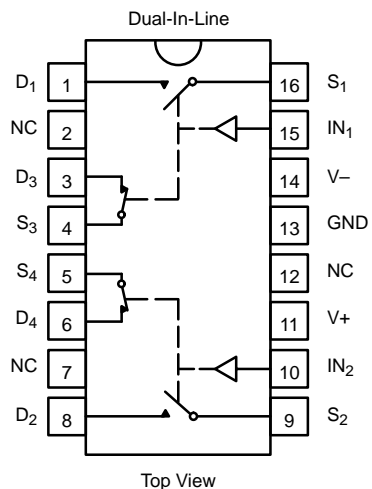
DG387B



| TRUTH TABLE | | |
|-------------|-----------------|-----------------|
| Logic | SW ₁ | SW ₂ |
| 0 | ON | OFF |
| 1 | OFF | ON |

Logic "0" ≤ 0.8 V
 Logic "1" ≥ 4 V

DG390B



| TRUTH TABLE | | |
|-------------|-----------------------------------|-----------------------------------|
| Logic | SW ₁ , SW ₂ | SW ₃ , SW ₄ |
| 0 | OFF | ON |
| 1 | ON | OFF |

Logic "0" ≤ 0.8 V
 Logic "1" ≥ 4 V

| ORDERING INFORMATION | | |
|----------------------|--------------------|-------------|
| Temp Range | Package | Part Number |
| DG381B | | |
| -40 to 85°C | 14-Pin Plastic DIP | DG381BDJ |
| DG384B | | |
| -40 to 85°C | 16-Pin Plastic DIP | DG384BDJ |
| DG387B | | |
| -40 to 85°C | 14-Pin Plastic DIP | DG387BDJ |
| DG390B | | |
| -40 to 85°C | 16-Pin Plastic DIP | DG390BDJ |

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ 44 V

GND 25 V

Digital Inputs^a, V_S, V_D (V-) -2 V to (V+) +2V or
30 mA, whichever occurs first

Current, Any Terminal Except S or D 30 mA

Continuous Current, S or D 30 mA

(Pulsed at 1 ms, 10% duty cycle max) 100 mA

Storage Temperature -65 to 150°C

Power Dissipation^b

14-Pin Plastic DIP^d 470 mW

Notes:

- Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 11 mW/°C above 75°C
- Derate 6.5 mW/°C above 25°C

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

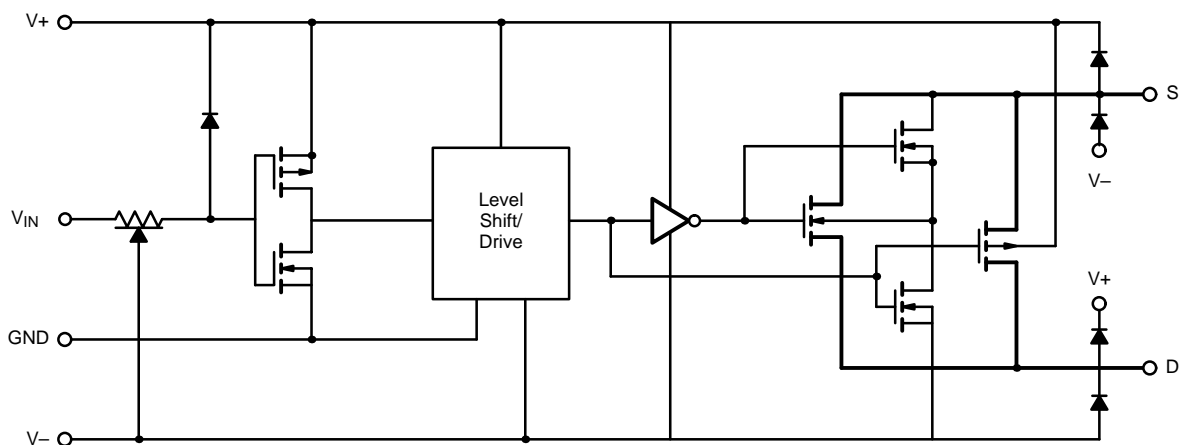


FIGURE 1.

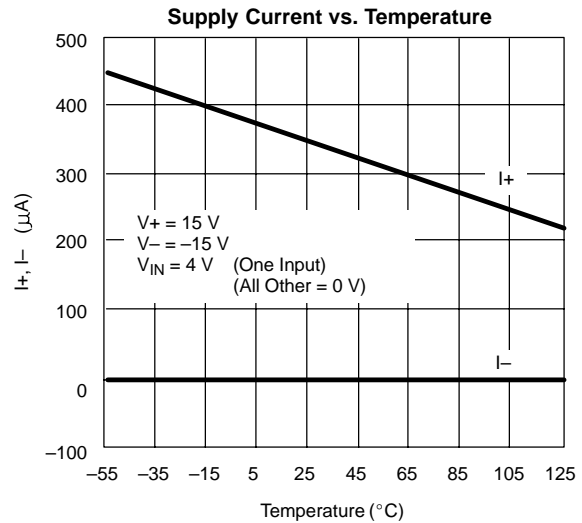
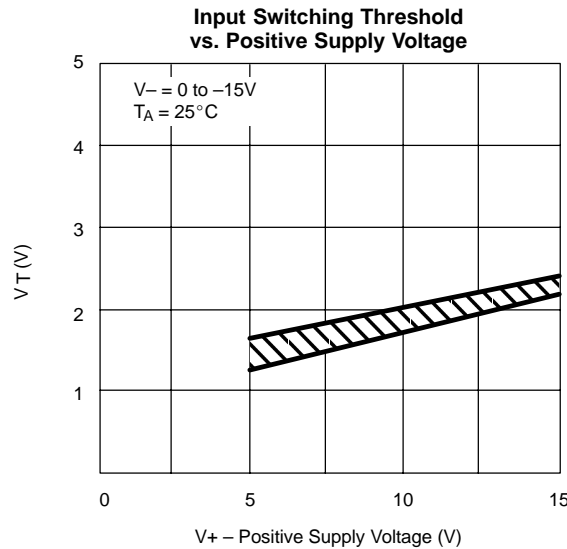
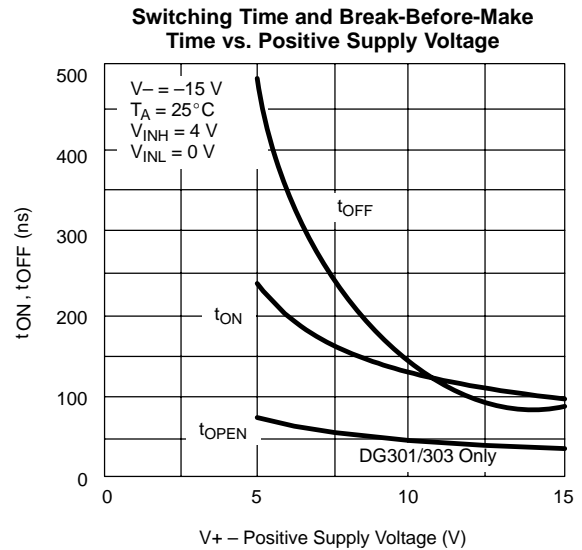
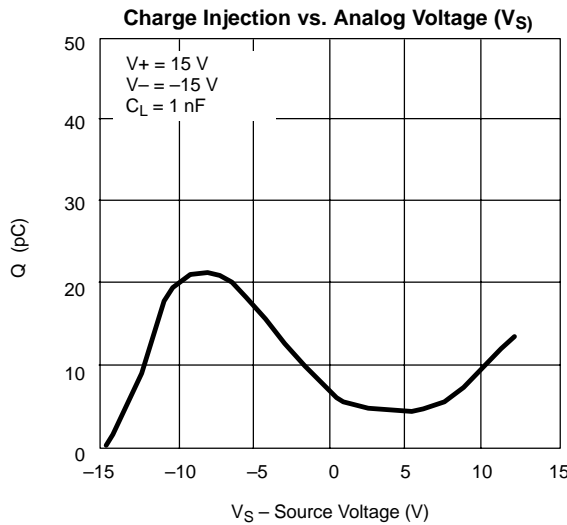
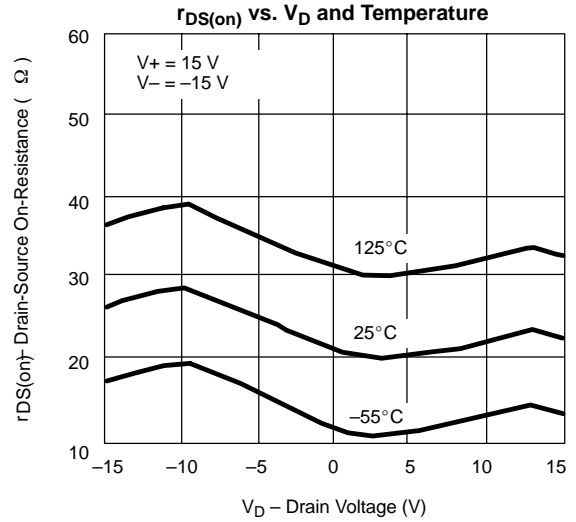
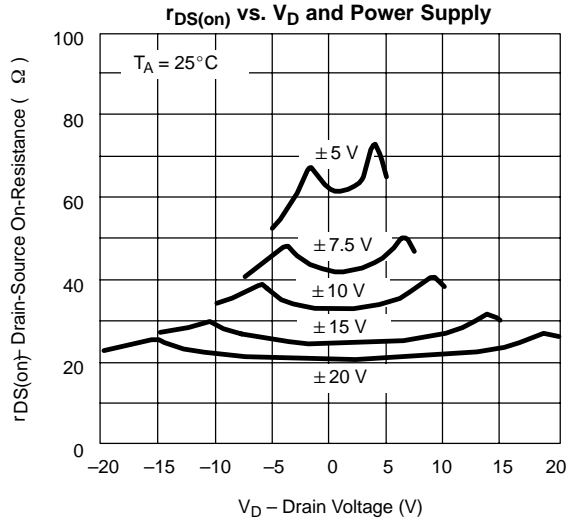
| SPECIFICATIONS ^a | | | | | | | |
|---------------------------------------|--------------|-----------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------------|------------------|------------------|---------------|
| Parameter | Symbol | Test Conditions Unless Specified $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$ $V_{IN} = 0.8\text{ V}$ or 4 V^f | Temp ^b | Limits -40 to 85°C | | | Unit |
| | | | | Min ^d | Typ ^c | Max ^d | |
| Analog Switch | | | | | | | |
| Analog Signal Range ^e | V_{ANALOG} | | Full | -15 | | 15 | V |
| Drain-Source On-Resistance | $r_{DS(on)}$ | $V_D = \pm 10\text{ V}$, $I_S = -10\text{ mA}$ | Room Full | | 30 | 50 75 | Ω |
| Source Off Leakage Current | $I_{S(off)}$ | $V_S = \pm 14\text{ V}$, $V_D = \mp 14\text{ V}$ | Room Hot | -5 -100 | ± 0.1 | 5 100 | nA |
| Drain Off Leakage Current | $I_{D(off)}$ | $V_S = \pm 14\text{ V}$, $V_D = \mp 14\text{ V}$ | Room Hot | -5 -100 | ± 0.1 | 5 100 | |
| Drain On Leakage Current | $I_{D(on)}$ | $V_D = V_S = \pm 14\text{ V}$ | Room Hot | -5 -100 | ± 0.1 | 5 100 | |
| Digital Control | | | | | | | |
| Input Current with Input Voltage High | I_{INH} | $V_{IN} = 5\text{ V}$ | Room Full | -1 | -0.001 | | μA |
| | | $V_{IN} = 15\text{ V}$ | Room Full | | 0.001 | 1 | |
| Input Current with Input Voltage Low | I_{INL} | $V_{IN} = 0\text{ V}$ | Room Full | -1 | -0.001 | | |
| Dynamic Characteristics | | | | | | | |
| Turn-On Time | t_{ON} | See Figure 2 | Room | | 150 | | ns |
| Turn-Off Time | t_{OFF} | | Room | | 130 | | |
| Break-Before-Make Time | t_{OPEN} | | Room | | 50 | | |
| Charge Injection | Q | $C_L = 0.01\ \mu\text{F}$, $R_{gen} = 0\ \Omega$, $V_{gen} = 0\text{ V}$ | Room | | 10 | | pC |
| Source-Off Capacitance | $C_{S(off)}$ | $f = 1\text{ MHz}$; V_S , $V_D = 0\text{ V}$ | Room | | 14 | | pF |
| Drain-Off Capacitance | $C_{D(off)}$ | | Room | | 14 | | |
| Channel-On Capacitance | $C_{D(on)}$ | | Room | | 40 | | |
| Input Capacitance | C_{IN} | | $f = 1\text{ MHz}$ | $V_{IN} = 0\text{ V}$ | Room | | |
| | | $V_{IN} = 15\text{ V}$ | | Room | | 7 | |
| Off-Isolation | OIRR | $V_{IN} = 0\text{ V}$, $R_L = 1\text{ k}\Omega$ $V_S = 1\text{ V}_{rms}$, $f = 500\text{ kHz}$ | Room | | 62 | | dB |
| Crosstalk (Channel-to-Channel) | X_{TALK} | | Room | | 74 | | |
| Power Supplies | | | | | | | |
| Positive Supply Current | I_+ | $V_{IN} = 4\text{ V}$ (One Input) (All Others = 0) | Room Full | | 0.23 | 1 | mA |
| Negative Supply Current | I_- | | Room Full | -100 | -0.001 | | |
| Positive Supply Current | I_+ | $V_{IN} = 0.8\text{ V}$ (All Inputs) | Room Full | | 0.001 | 100 | μA |
| Negative Supply Current | I_- | | Room Full | -100 | -0.001 | | |

Notes:

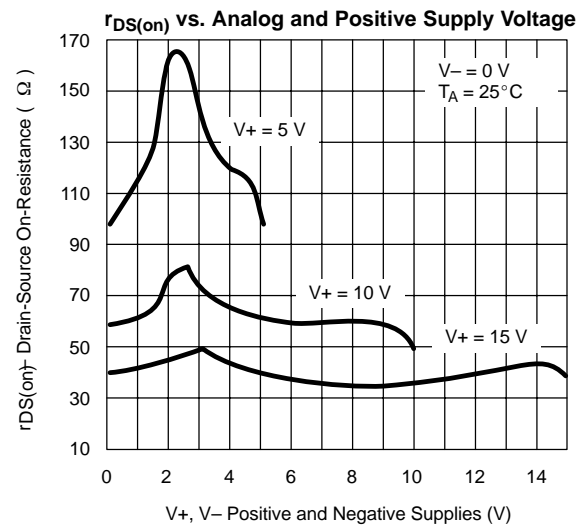
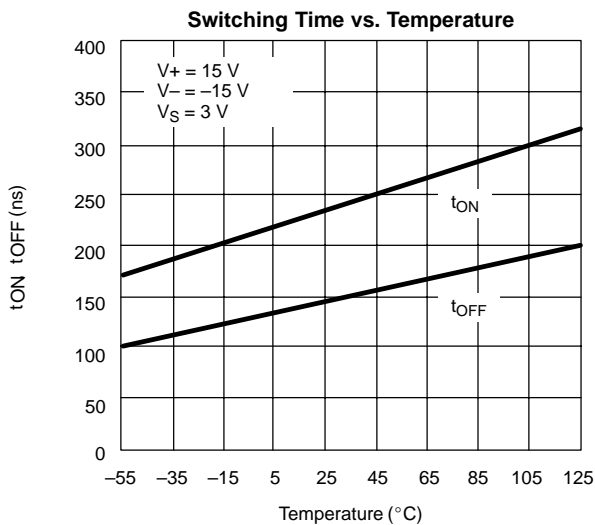
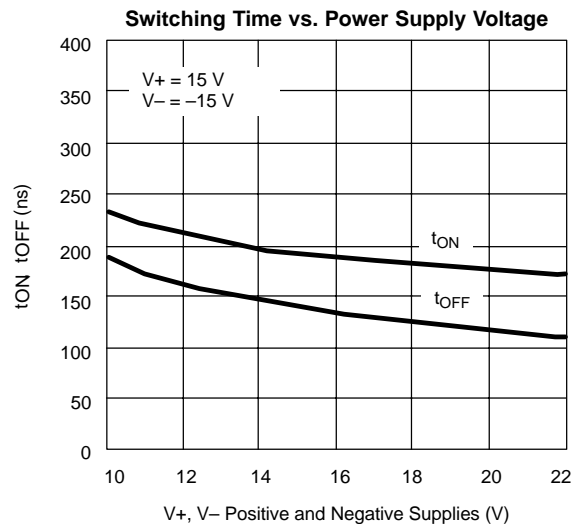
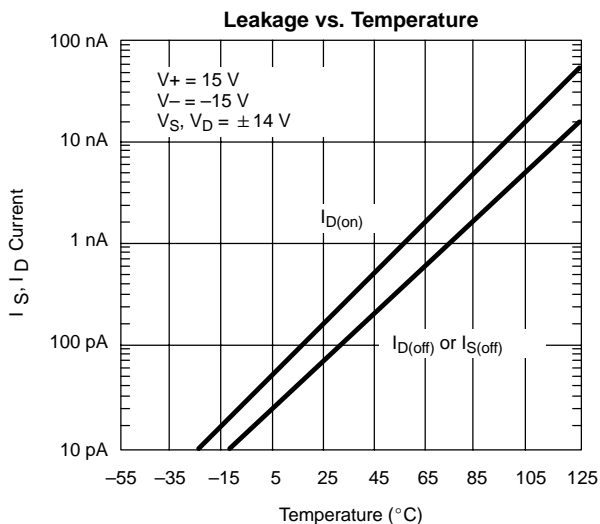
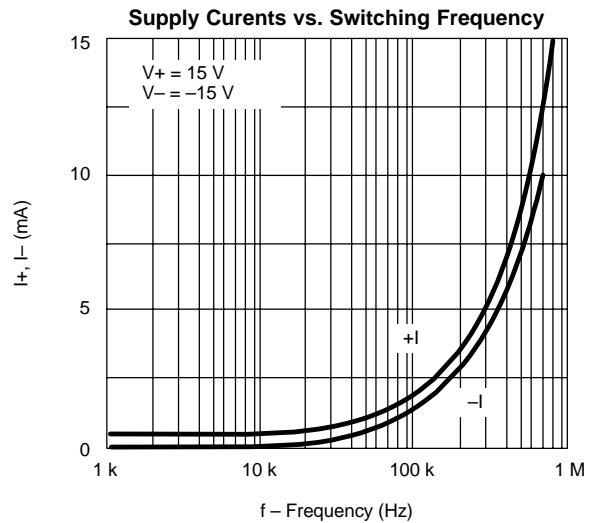
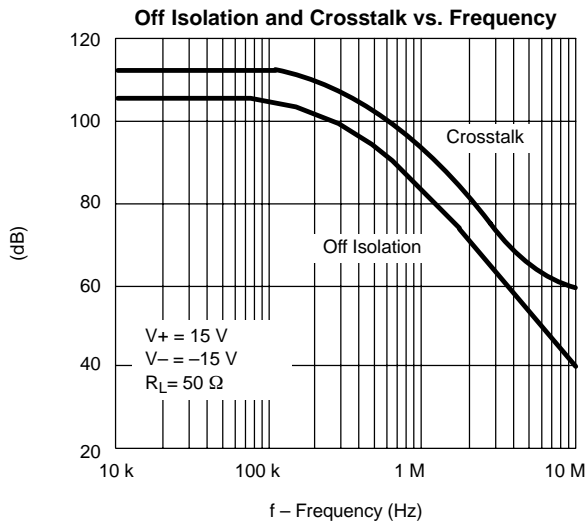
- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TEST CIRCUITS

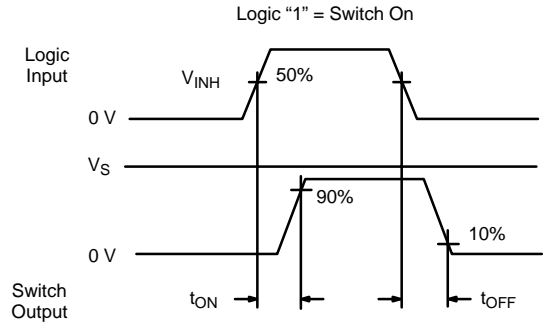
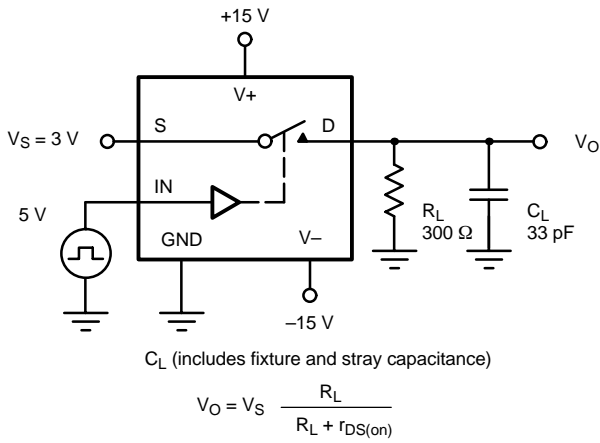


FIGURE 2. Switching Time

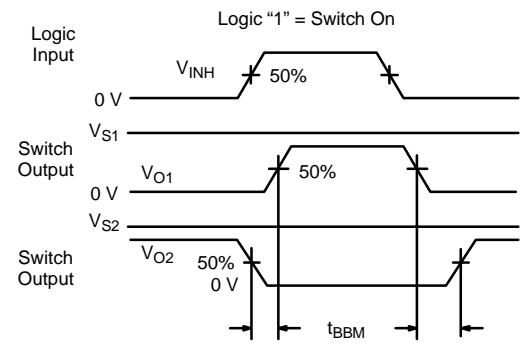
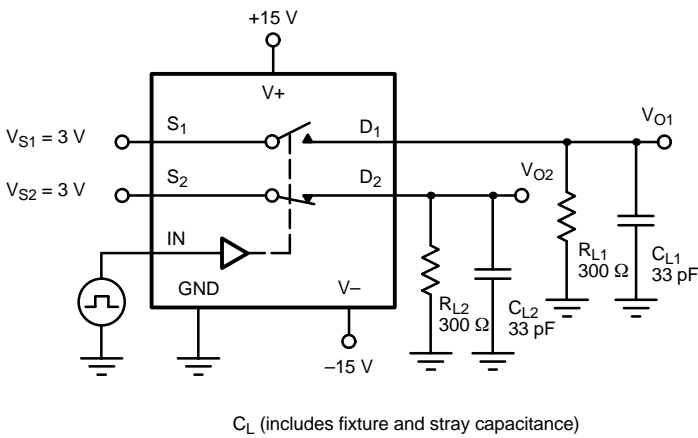


FIGURE 3. Break-Before-Make SPDT (DG387B, DG390B)

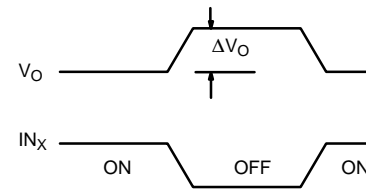
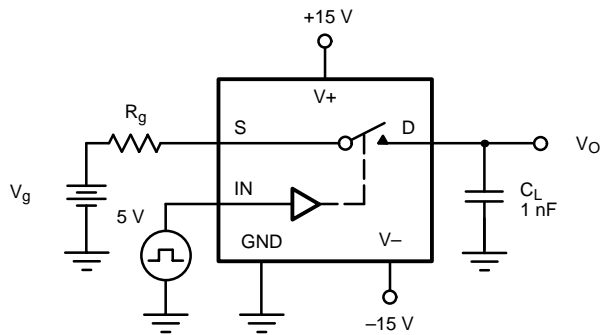


FIGURE 4. Charge Injection

APPLICATIONS

The DG381B series of analog switches will switch positive analog signals while using a single positive supply. This allows their use in applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) increased $r_{DS(on)}$, 2) slower switching speed. Typical curves for aid in designing with single supplies are supplied (see Typical Characteristics). The analog voltage should not go above or below the supply voltages which in single operation are $V+$ and 0 V.

In the integrator of Figure 4, R_D controls the discharge rate of the capacitor so that the pulsed or continuous current ratings are not exceeded. During reset SW_1 is closed and SW_2 is open. Opening SW_2 with SW_1 also open will hold the integrator output at its present value.

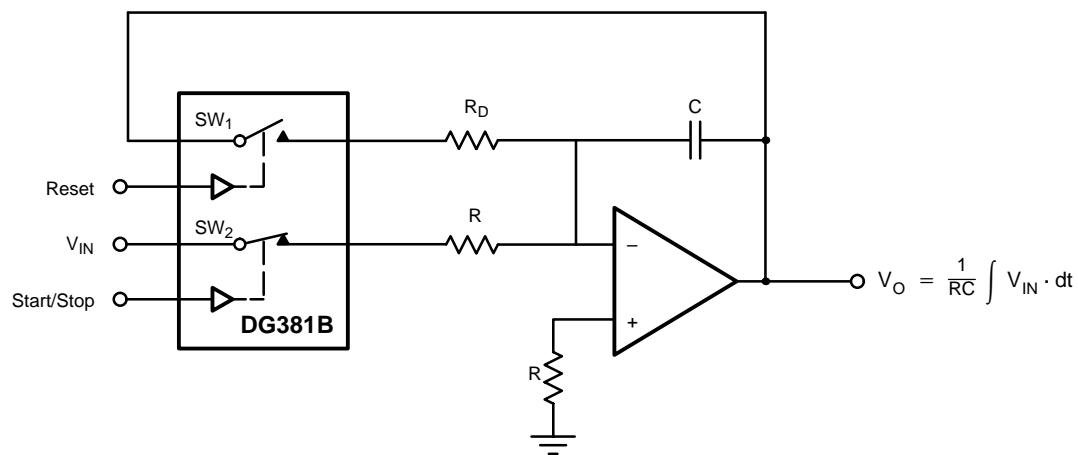


FIGURE 5. Integrator with Reset and Start/Stop



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- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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