# MIC2085/MIC2086

## Single Channel Hot Swap Controllers

## General Description

The MIC2085 and MIC2086 are single channel positive voltage hot swap controllers designed to allow the safe insertion of boards into live system backplanes. The MIC2085and MIC2086 are available in 16-pin and 20-pin QSOP packages, respectively. Using a few external components and by controlling the gate drive of an external N-Channel MOSFET device, the MIC2085/86 provide inrush current limiting and output voltage slew rate control in harsh, critical power supply environments. Additionally, a circuit breaker function will latch the output MOSFET off if the current limit threshold is exceeded for a programmed period of time. The devices' array of features provide a simplified yet robust solution for many network applications in meeting the power supply regulation requirements and affords protection of critical downstream devices and components.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

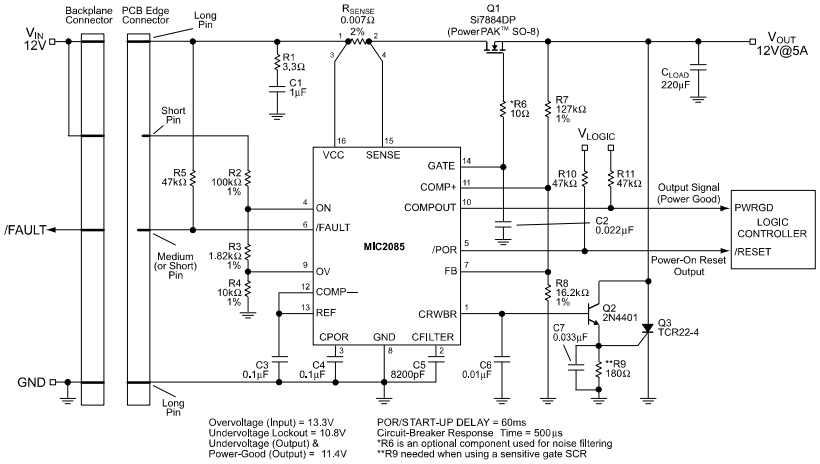
## Features

- MIC2085: Pin for pin functional equivalent to the LTC1642
- 2.3V to 16.5V supply voltage operation
- Surge voltage protection to 33V
- Operating temperature range –40°C to 85°C
- Active current regulation limits inrush current independent of load capacitance
- Programmable inrush current limiting
- Analog foldback current limiting
- Electronic circuit breaker
- Dual-level overcurrent fault sensing
- Fast response to short circuit conditions (< 1µs)
- Programmable output undervoltage detection
- Undervoltage lockout protection
- Power-on reset (MIC2085/86) and power-good (MIC2086) status outputs
- /FAULT status output
- Driver for SCR crowbar on overvoltage

## Applications

- RAID systems
- Cellular base stations
- LAN servers
- WAN servers
- InfiniBand™ Systems
- Industrial high side switching

## Typical Application

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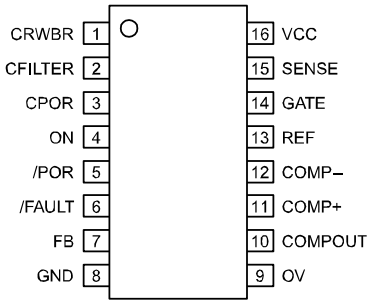
## Ordering Information

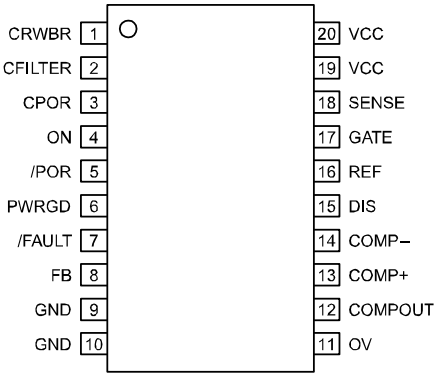
| Part Number | | Fast Circuit Breaker Threshold | Discharge Output | Package |
|---|---|---|---|---|
| Standard | Pb-Free | | | |
| MIC2085-xBQS | MIC2085-xYQS | x = J, 95mV<br>x = K, 150mV*<br>x = L, 200mV*<br>x = M, Off | NA | 16-Pin QSOP |
| MIC2086-xBQS | MIC2086-xYQS | x = J, 95mV<br>x = K, 150mV*<br>x = L, 200mV*<br>x = M, Off | Yes | 20-Pin QSOP |

* Contact factory for availability.

## Pin Configuration




**MIC2085**
**16-Pin QSOP (QS)**




**MIC2086**
**20-Pin QSOP (QS)**

## Pin Description

| Pin Number MIC2086 | Pin Number MIC2085 | Pin Name | Pin Function |
|---|---|---|---|
| 1 | 1 | CRWBR | Overvoltage Timer and Crowbar Circuit Trigger: A capacitor connected to this pin, sets the timer duration for which an overvoltage condition will trigger an external crowbar circuit. This timer begins when the OV input rises above its threshold as an internal 45µA current source charges the capacitor. Once the voltage reaches 470mV, the current increases to 1.5mA. |
| 2 | 2 | CFILTER | Current Limit Response Timer: A capacitor connected to this pin defines the period of time ($t_{OCSLOW}$) in which an overcurrent event must last to signal a fault condition and trip the circuit breaker. If no capacitor is connected, then $t_{OCSLOW}$ defaults to 5µs. |
| 3 | 3 | CPOR | Power-On Reset Timer: A capacitor connected between this pin and ground sets the start-up delay ($t_{START}$) and the power-on reset interval ($t_{POR}$). When VCC rises above the UVLO threshold, the capacitor connected to CPOR begins to charge. When the voltage at CPOR crosses 1.24V, the start-up threshold ($V_{START}$), a start cycle is initiated if ON is asserted while capacitor CPOR is immediately discharged to ground. When the voltage at FB rises above VFB, capacitor CPOR begins to charge again. When the voltage at CPOR rises above the power-on reset delay threshold (VTH), the timer resets by pulling CPOR to ground, and /POR is deasserted. If CPOR = 0, then $t_{START}$ defaults to 20µs. |

## Pin Description (Cont.)

| Pin Number MIC2086 | Pin Number MIC2085 | Pin Name | Pin Function |
|---|---|---|---|
| 4 | 4 | ON | ON Input: Active high. The ON pin, an input to a Schmitt-triggered comparator used to enable/disable the controller, is compared to a $V_{TH}$ reference with 100mV of hysteresis. Once a logic high is applied to the ON pin ($V_{ON}$ > 1.24V), a start-up sequence is initiated as the GATE pin starts ramping up towards its final operating voltage. When the ON pin receives a low logic signal ($V_{ON}$ < 1.14V), the GATE pin is grounded and /FAULT is high if VCC is above the UVLO threshold. ON must be low for at least 20µs in order to initiate a start-up sequence. Additionally, toggling the ON pin LOW to HIGH resets the circuit breaker. |
| 5 | 5 | /POR | Power-On Reset Output: Open drain N-Channel device, active low. This pin remains asserted during start-up until a time period $t_{POR}$ after the FB pin voltage rises above the power-good threshold (VFB). The timing capacitor CPOR determines $t_{POR}$. When an output undervoltage condition is detected at the FB pin, /POR is asserted for a minimum of one timing cycle, $t_{POR}$. The /POR pin has a weak pull-up to VCC |
| 6 | NA | PWRGD | Power-Good Output: Open drain N-Channel device, active high. When the voltage at the FB pin is lower than 1.24V, the PWRGD output is held low. When the voltage at the FB pin is higher than 1.24V, then PWRGD is asserted. A pull-up resistor connected to this pin and to VCC will pull the output up to VCC. The PWRGD pin has a weak pull-up to VCC. |
| 7 | 6 | /FAULT | Circuit Breaker Fault Status Output: Open drain N-Channel device, active low. The /FAULT pin is asserted when the circuit breaker trips due to an overcurrent condition. Also, this pin indicates undervoltage lockout and overvoltage fault conditions. The /FAULT pin has a weak pull-up to VCC. |
| 8 | 7 | FB | Power-Good Threshold Input: This input is internally compared to a 1.24V reference with 3mV of hysteresis. An external resistive divider may be used to set the voltage at this pin. If this input momentarily goes below 1.24V, then /POR is activated for one timing cycle, $t_{POR}$, indicating an output undervoltage condition. The /POR signal de-asserts one timing cycle after the FB pin exceeds the power-good threshold by 3mV. A 5µs filter on this pin prevents glitches from inadvertently activating this signal. |
| 9, 10 | 8 | GND | Ground Connection: Tie to analog ground |
| 11 | 9 | OV | OV Input: When the voltage on OV exceeds its trip threshold, the GATE pin is pulled low and the CRWBR timer starts. If OV remains above its threshold long enough for CRWBR to reach its trip threshold, the circuit breaker is tripped. Otherwise, the GATE pin begins to ramp up one POR timing cycle after OV drops below its trip threshold. |
| 12 | 10 | COMPOUT | Uncommitted Comparator's Open Drain Output. |
| 13 | 11 | COMP+ | Comparator's Non-Inverting Input. |
| 14 | 12 | COMP- | Comparator's Inverting Input. |
| 15 | Na | DIS | Discharge Output: When the MIC2086 is turned off, a 550Ω internal resistor at this output allows the discharging of any load capacitance to ground. |
| 16 | 13 | REF | Reference Output: 1.24V nominal. Tie a 0.1µF capacitor to ground to ensure stability. |
| 17 | 14 | GATE | Gate Drive Output: Connects to the gate of an external N-Channel MOSFET. An internal clamp ensures that no more than 13V is applied between the GATE pin and the source of the external MOSFET. The GATE pin is immediately brought low when either the circuit breaker trips or an undervoltage lockout condition occurs. |

## Pin Description (Cont.)

| Pin Number MIC2086 | Pin Number MIC2085 | Pin Name | Pin Function |
|---|---|---|---|
| 18 | 15 | SENSE | Circuit Breaker Sense Input: A resistor between this pin and VCC sets the current limit threshold. Whenever the voltage across the sense resistor exceeds the slow trip current limit threshold ($V_{TRIPSLOW}$), the GATE voltage is adjusted to ensure a constant load current. If $V_{TRIPSLOW}$ (48mV) is exceeded for longer than time period $t_{OCSLOW}$, then the circuit breaker is tripped and the GATE pin is immediately pulled low. If the voltage across the sense resistor exceeds the fast trip circuit breaker threshold, $V_{TRIPFAST}$, at any point due to fast, high amplitude power supply faults, then the GATE pin is immediately brought low without delay. To disable the circuit breaker, the SENSE and VCC pins can be tied together.<br><br>The default $V_{TRIPFAST}$ for either device is 95mV. Other fast trip thresholds are available: 150mV, 200mV, or OFF ($V_{TRIPFAST}$ disabled). Please contact factory for availability of other options. |
| 19, 20 | 16 | VCC | Positive Supply Input: 2.3V to 16.5V. The GATE pin is held low by an internal undervoltage lockout circuit until VCC exceeds a threshold of 2.18V.If VCC exceeds 16.5V, an internal shunt regulator protects the chip from VCC and SENSE pin voltages up to 33V. |

## Absolute Maximum Ratings[1]

(All voltages are referred to GND)

Supply Voltage ($V_{CC}$) ..... –0.3V to 33V
SENSE Pin ..... –0.3V to $V_{CC}$ + 0.3V
GATE Pin ..... –0.3V to 22V
ON, DIS, /POR, PWRGD, /FAULT, COMP+, COMP-, COMPOUT ..... –0.3V to 20V
CRWBR, FB, OV, REF ..... –0.3V to 6V

Maximum Currents

Digital Output Pins (/POR, /FAUTL, PWRGD, COMPOUT) ..... 10mA
DIS Pin ..... 30mA

EDS Rating

Human Body Model ..... 2kV
Machine Model ..... 200V

## Operating Ratings[2]

Supply voltage ($V_{CC}$) ..... 2.3V to +16.5V
Operating Temperature Range ..... –40°C to +85°C
Junction Temperature ($T_J$) ..... 125°C
Package Thermal Resistance $R_{\theta(JA)}$
16-pin QSOP ..... 112°C/W
20-pin QSOP ..... 91°C/W

## Electrical Characteristics[3]

$V_{CC}$ = 5.0V; $T_A$ = 25°C, unless otherwise noted. **Bold** indicates specifications over the full operating temperature range of –40°C to +85°C.

| Symbol | Parameter | Condition | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | | | **2.3** | | **16.5** | V |
| $I_{CC}$ | Supply Current | | | | | 1.6 | **2.5** | mA |
| $V_{UV}$ | Undervoltage Lockout Threshold | $V_{CC}$ rising<br>$V_{CC}$ falling | | | **2.05**<br>**1.85** | 2.18<br>2.0 | **2.28**<br>**2.10** | V<br>V |
| $V_{UVHYST}$ | UV Lockout Hysteresis | | | | | 180 | | mV |
| $V_{FB}$ | FB (Power-Good) Threshold Voltage | FB rising | | | **1.19** | 1.24 | **1.29** | V |
| $V_{FBHYST}$ | FB Hysteresis | | | | | 3 | | mV |
| $V_{OV}$ | OV Pin Threshold Voltage | OV pin rising | | | **1.19** | 1.24 | **1.29** | mV |
| $\Delta V_{OV}$ | OV Pin Threshold Voltage Line Regulation | 2.3V < $V_{CC}$ < 16.5V | | | | 5 | **15** | mV |
| $V_{OVHYST}$ | OV Pin Hysteresis | | | | | 3 | | mV |
| $I_{OV}$ | OV Pin Current | | | | | | **0.2** | µA |
| $V_{TH}$ | POR Delay and Overcurrent (CFILTER) Timer Threshold | $V_{CPOR}$, $V_{CFILTER}$ rising | | | **1.19** | 1.24 | **1.29** | V |
| $I_{CPOR}$ | Power-On Reset Timer Current | Timer on<br>Timer off | | | **–2.5** | –2.0<br>5 | **–1.5** | µA<br>mA |
| $I_{TIMER}$ | Current Limit /Overcurrent Timer Current (CFILTER) | Timer on<br>Timer off | | | **–30** | –20<br>2.5 | **–15** | µA<br>mA |
| $V_{CR}$ | CRWBR Pin Threshold Voltage | 2.3V < $V_{CC}$ < 16.5V | | | 445 | 470 | 495 | mV |
| $\Delta V_{CR}$ | CRWBR Pin Threshold Voltage Line Regulation | 2.3V < $V_{CC}$ < 16.5V | | | | 4 | **15** | µA<br>mA |
| $I_{CR}$ | CRWBR Pin Current | CRWBR On, $V_{CRWBR}$ = 0V<br>CRWBR On, $V_{CRWBR}$ = 2.1V<br>CRWBR Off, $V_{CRWBR}$ = 1.5V | | | **–60** | –45<br>–1.5<br>3.3 | **–30**<br>–1.0 | µA<br>mA<br>mA |
| $V_{TRIP}$ | Circuit Breaker Trip Voltage (Current Limit Threshold) | $V_{TRIP}$ = $V_{CC}$ = $V_{SENSE}$<br>2.3V ≤ $V_{CC}$ ≤ 16.5V | $V_{TRIPSLOW}$ | | **40** | 48 | **55** | mV |
| | | | $V_{TRIPFAST}$ | x = J<br>x = K<br>x = L | **80** | 95<br>150<br>200 | **110** | mV<br>mV<br>mV |

## Electrical Characteristics (Cont.)

| Symbol | Parameter | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{GS}$ | External Gate Drive | $V_{GATE} - V_{CC}$ | $V_{CC}$ < 3V | 4 | 8 | 9 | V |
| | | | 5V < $V_{CC}$ < 9V | 11 | 12 | 13 | V |
| | | | 9V < $V_{CC}$ <15.0V | 4.5 | 21-$V_{CC}$ | 13 | V |
| $I_{GATE}$ | GATE Pin Pull-up Current | Start cycle, $V_{GATE}$ > 0V<br>$V_{CC}$ = 16.5V<br>$V_{CC}$ = 2.3V | | **–22**<br>**–20** | –16<br>–14 | **–8**<br>**–8** | µA<br>µA |
| $I_{GATEOFF}$ | GATE Pin Sink Current | /FAULT = 0, $V_{GATE}$ > 1V<br>$V_{CC}$ = 16.5V<br>$V_{CC}$ = 2.3V | | **25**<br>**12** | 50<br>20 | | mA<br>mA |
| $V_{ON}$ | ON Pin Threshold Voltage | ON rising<br>ON falling | | **1.19**<br>**1.09** | 1.24<br>1.14 | **1.29**<br>1.19 | V<br>V |
| $V_{ONHYST}$ | ON Pin Hysteresis | | | | 100 | | mV |
| $I_{ON}$ | ON Pin Input Current | $V_{ON}$ = $V_{CC}$ | | | | **0.5** | µA |
| $V_{START}$ | Undervoltage Start-up Timer Threshold | $V_{CPOR}$ rising | | **1.19** | 1.24 | **1.29** | V |
| $V_{OL}$ | /FAULT, /POR, PWRGD Output Voltage | $I_{OUT}$ = 1.6mA<br>(PWRGD for MIC2086 only) | | | | **0.4** | V |
| $I_{PULLUP}$ | Output Signal Pull-up Current /FAULT, /POR, PWRGD, COMPOUT | /FAULT, /POR, PWRGD = GND<br>(PWRGD FOR MIC2086 only) | | | –20 | | µA |
| $V_{REF}$ | Reference Output Voltage | $I_{LOAD}$ = 0mA; $C_{REF}$ = 0.1 µF | | 1.21 | 1.24 | 1.27 | V |
| $\Delta V_{LNR}$ | Reference Line Regulation | 2.3V < $V_{CC}$ < 16.5V | | | 5 | **10** | mV |
| $\Delta V_{LDR}$ | Reference Load Regulation | $I_{OUT}$ = 1mA | | | 2.5 | **7.5** | mV |
| $I_{RSC}$ | Reference Short-Circuit Current | $V_{REF}$ = 0V | | | 3.5 | | mA |
| $V_{COS}$ | Comparator Offset Voltage | $V_{CM}$ = $V_{REF}$ | | **–5** | | **5** | mV |
| $V_{CHYST}$ | Comparator Hysteresis | $V_{CM}$ = $V_{REF}$ | | | 3 | | mV |
| $R_{DIS}$ | Discharge Pin Resistance | ON pin toggles from HI to LOW | | 100 | 550 | 1000 | Ω |

## AC Electrical Characteristics[3]

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{OCFAST}$ | Fast Overcurrent Sense to GATE Low Trip Time | $V_{CC}$ = 5V<br>$V_{CC}$ – $V_{SENSE}$ = 100mV<br>$C_{GATE}$ = 10nF, See Figure 1 | | 1 | | µs |
| $t_{OCSLOW}$ | Slow Overcurrent Sense to GATE Low Trip Time | $V_{CC}$ = 5V<br>$V_{CC}$ – $V_{SENSE}$ = 50mV<br>$C_{FILTER}$ = 0, See Figure 1 | | 5 | | µs |
| $t_{ONDLY}$ | ON Delay Filter | | | 20 | | µs |
| $t_{FBDLY}$ | FB Delay Filter | | | 20 | | µs |

**Notes:**

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Specification for packaged product only.

## Timing Diagrams

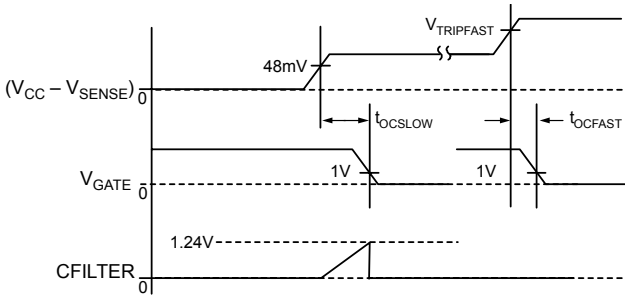



**Figure 1. Current Limit Response**

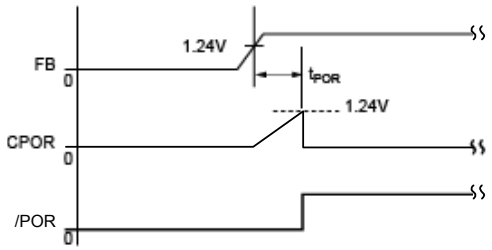



**Figure 2. Power-On Reset Response**

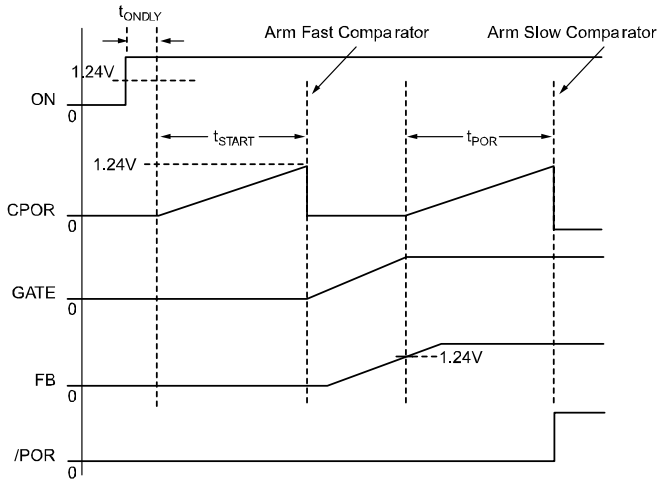



**Figure 3. Power-On Start-Up Delay Timing**

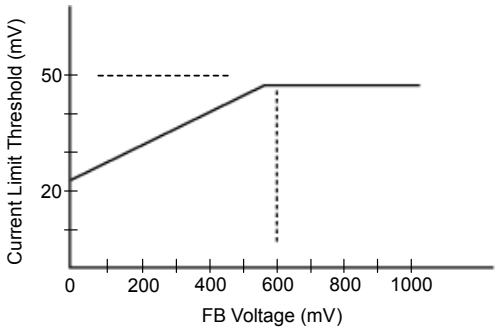
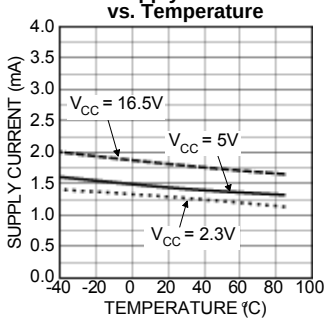


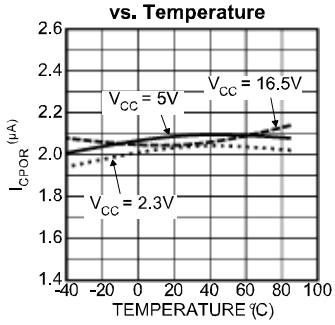

**Figure 4. Foldback Current Limit Response**

## Typical Characteristics

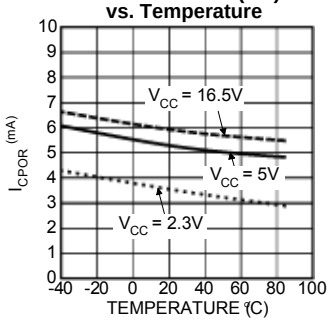
**Supply Current vs. Temperature**



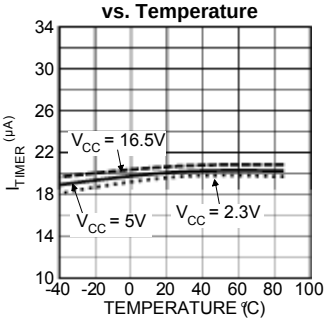

**Power-On Reset Timer Current vs. Temperature**



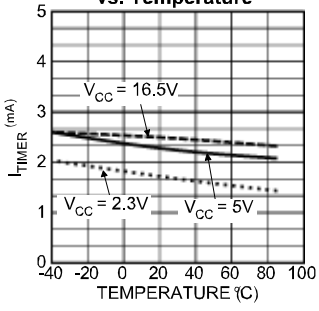

**Power-On Reset Timer (Off) Curren vs. Temperature**



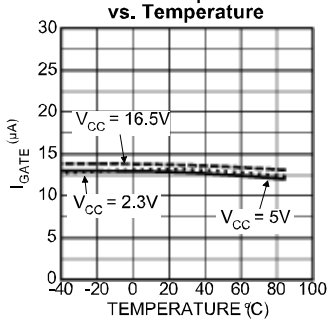

**Overcurrent Timer Current vs. Temperature**



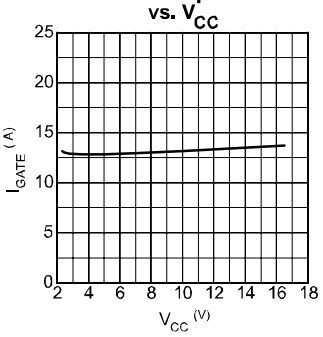

**Overcurrent Timer (Off) Current vs. Temperature**



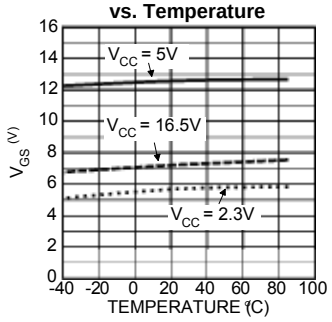

**Gate Pull-Up Current vs. Temperature**



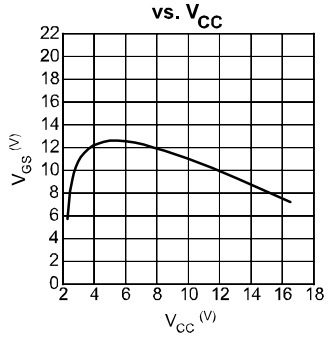

**Gate Pull-Up Current vs. $V_{CC}$**



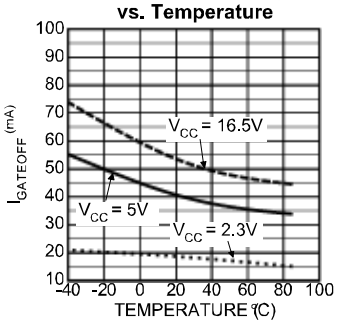

**External Gate Drive vs. Temperature**



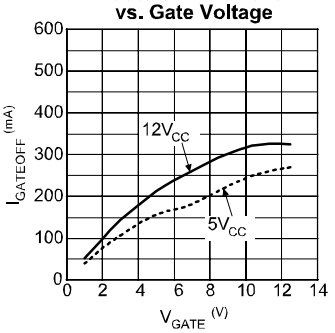

**External Gate Drive vs. $V_{CC}$**



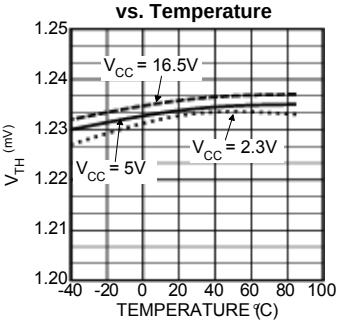

**Gate Sink Current vs. Temperature**




**Gate Sink Current vs. Gate Voltage**

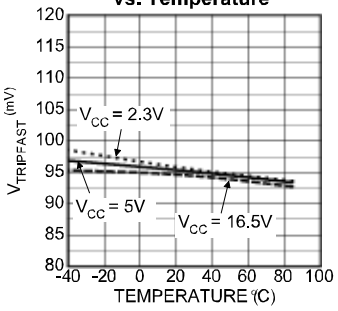



**POR Delay/Overcurrent Timer Threshold vs. Temperature**

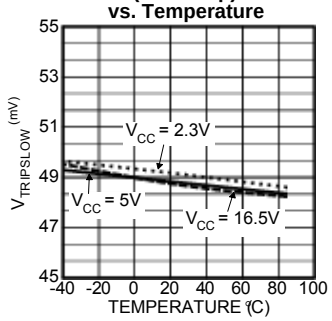


## Typical Characteristics (Cont.)

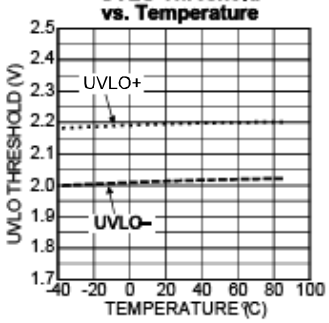
**Current Limit Threshold (Fast Trip) vs. Temperature**



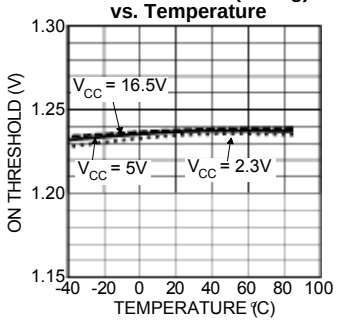

**Current Limit Threshold (Slow Trip) vs. Temperature**



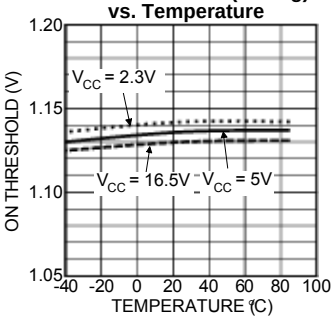

**UVLO Threshold vs. Temperature**



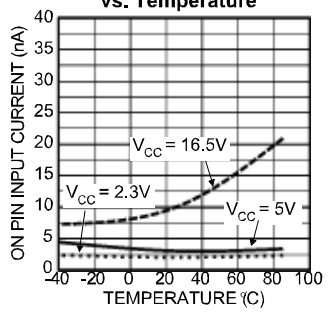

**ON Pin Threshold (Rising) vs. Temperature**



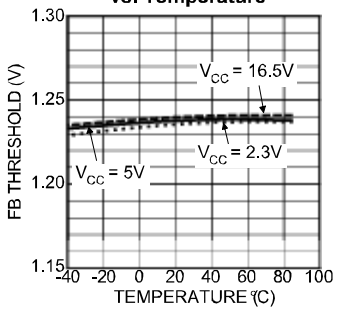

**ON Pin Threshold (Falling) vs. Temperature**



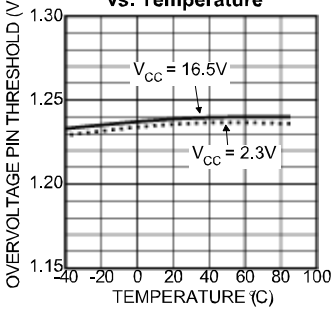

**ON Pin Input Current vs. Temperature**



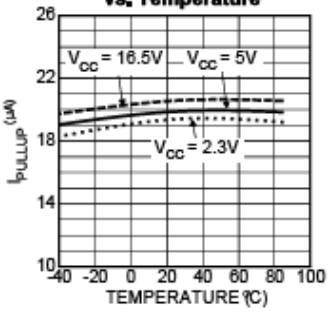

**FB (Power-Good) Threshold vs. Temperature**



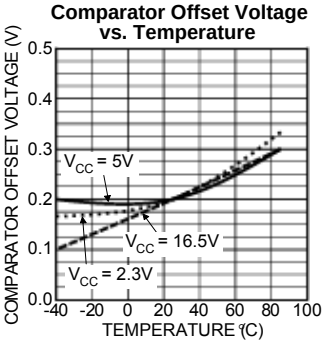

**Overvoltage Pin Threshold vs. Temperature**



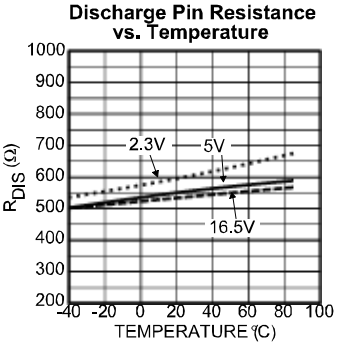

**Output Signal Pull-Up Current vs. Temperature**



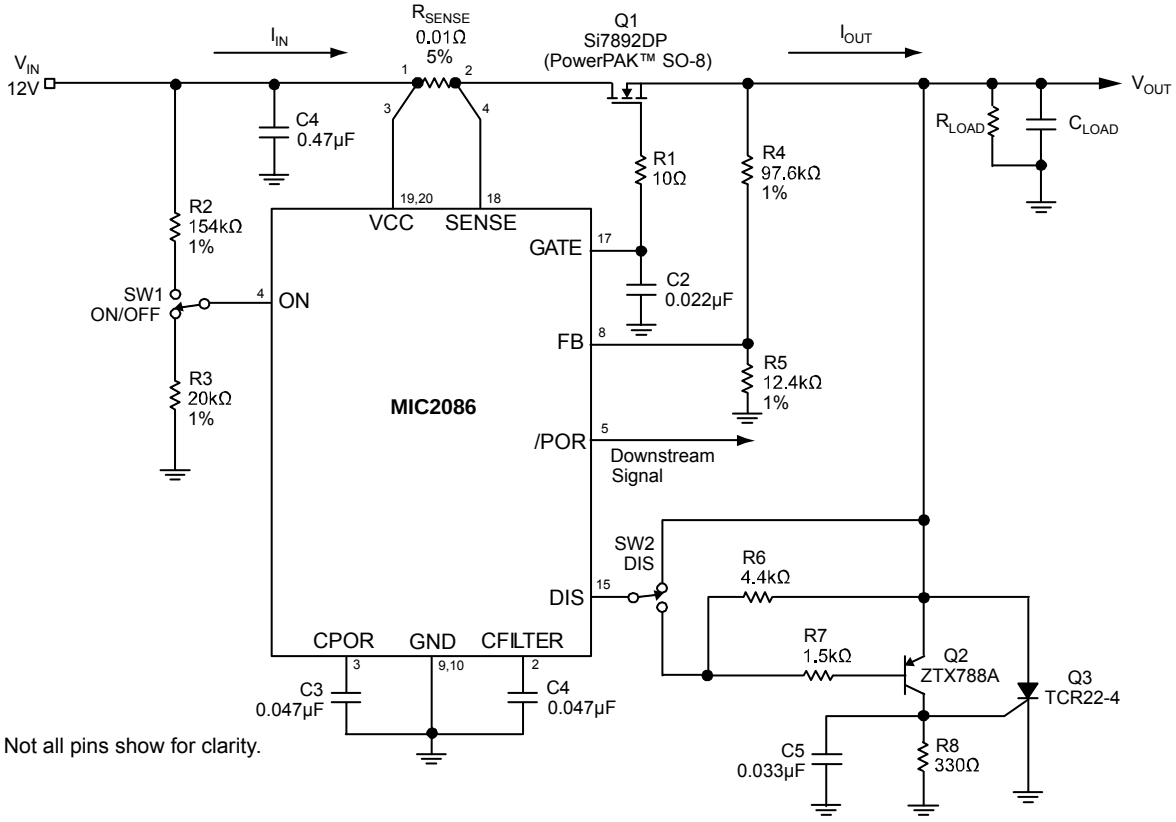

**Comparator Offset Voltage vs. Temperature**




**Discharge Pin Resistance vs. Temperature**

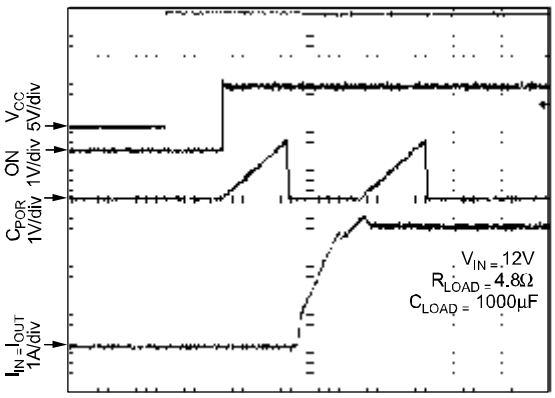


## Test Circuit

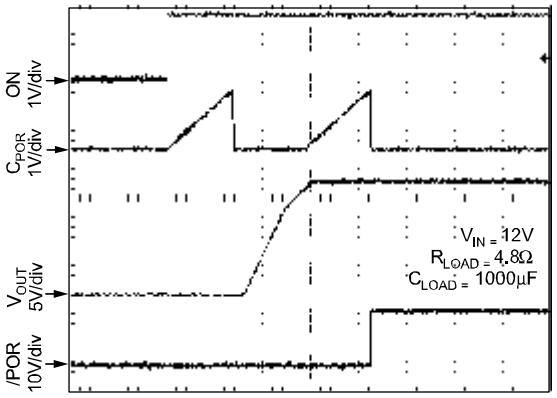


## Functional Characteristics

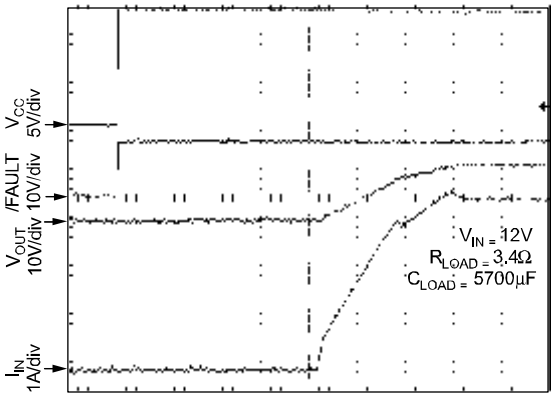
**12V Hot Insert Response**



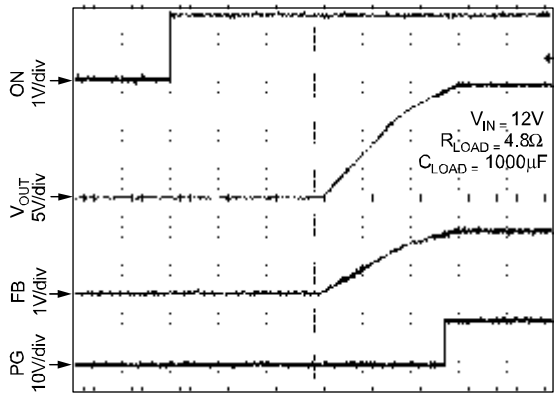

**12V Turn On Response**



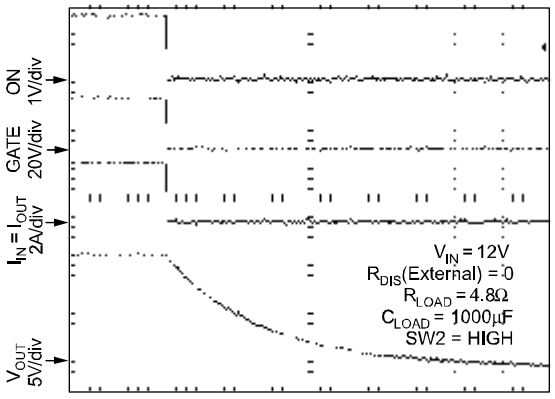

**Inrush Current Response**



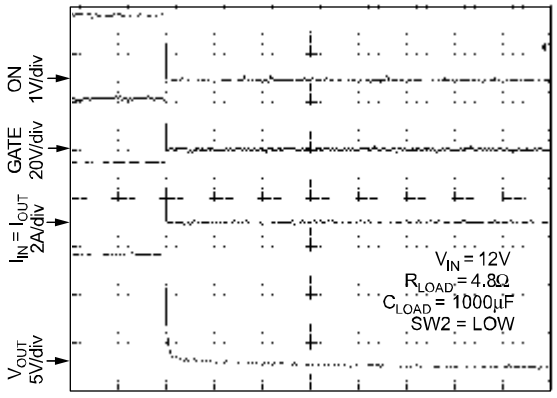

**Power-Good Response**



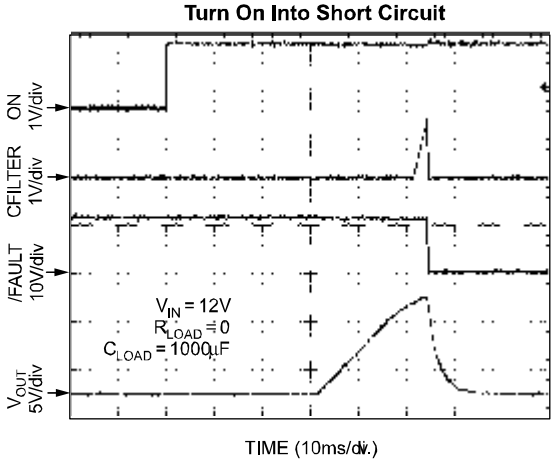

**Turn Off — Normal Discharge**



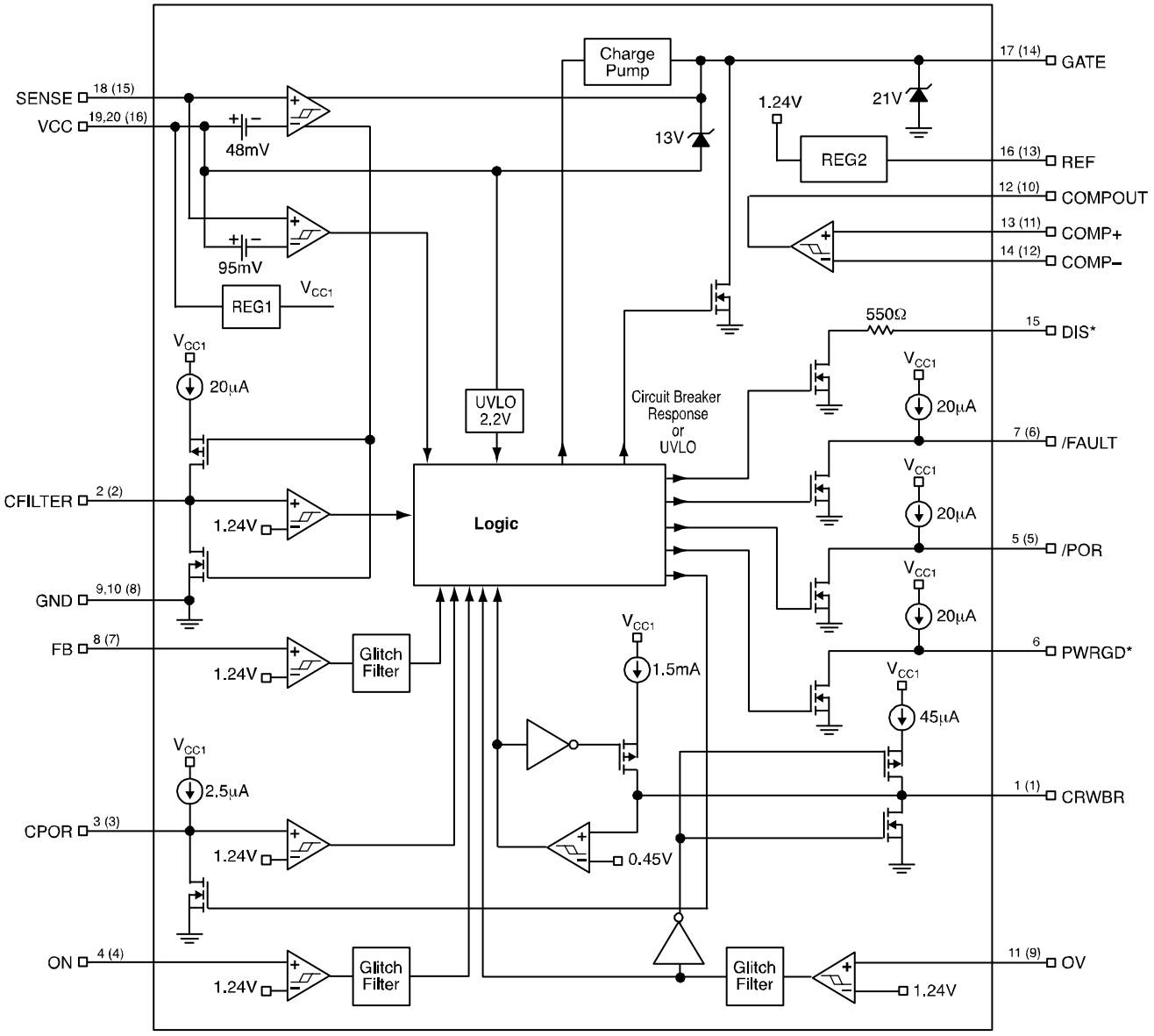

**Turn Off — Crowbar Discharge**



## Functional Characteristics (Cont.)



## Functional Diagram




*DIS and PWRGD are not available on MIC2085.
Pin numbers for MIC2085 are in parenthesis ( ) where applicable.

**MIC2086 Block Diagram**

## Functional Description

### Hot Swap Insertion

When circuit boards are inserted into live system backplanes and supply voltages, high inrush currents can result due to the charging of bulk capacitance that resides across the supply pins of the circuit board. This inrush current, although transient in nature, may be high enough to cause permanent damage to on-board components or may cause the system's supply voltages to go out of regulation during the transient period which may result in system failures. The MIC2085/86 acts as a controller for external N-Channel MOSFET devices in which the gate drive is controlled to provide inrush current limiting and output voltage slew rate control during hot plug insertions.

### Power Supply

VCC is the supply input to the MIC2085/86 controller with a voltage range of 2.3V to 16.5V. The VCC input can with stand transient spikes up to 33V. In order to help suppress transients and ensure stability of the supply voltage, a capacitor of 1.0µF to 10µF from VCC to ground is recommended. Alternatively, a low pass filter, shown in the typical application circuit, can be used to eliminate high frequency oscillations as well as help suppress transient spikes.

### Start-Up Cycle

When the voltage on the ON pin rises above its threshold of 1.24V, the MIC2085/86 first checks that its supply ($V_{CC}$) is above the UVLO threshold. If it does check above, the device is enabled and an internal 2µA current source begins charging capacitor $C_{POR}$ to 1.24V to initiate a start-up sequence (i.e., start-up delay times out). Once the start-up delay ($t_{START}$) elapses, CPOR is pulled immediately to ground and a 15µA current source begins charging the GATE output to drive the external MOSFET that switches $V_{IN}$ to $V_{OUT}$. The programmed start-up delay is calculated using the following equation:

$$t_{START} = C_{POR} \times \frac{V_{TH}}{I_{CPOR}} \cong 0.62 \times C_{POR}(\mu F) \qquad (1)$$

where $V_{TH}$, the POR delay threshold, is 1.24V, and $I_{CPOR}$, the POR timer current, is 2µA. As the GATE voltage continues ramping toward its final value (VCC + VGS) at a defined slew rate (See "Load Capacitance"/"Gate Capacitance Dominated Start-Up" sections), a second CPOR timing cycle begins if:1)/FAULT is high and 2)CFILTER is low (i.e., not an overvoltage, undervoltage lockout, or overcurrent state).This second timing cycle, $t_{POR}$, starts when the voltage at the FB pin exceeds its threshold ($V_{FB}$) indicating that the output voltage is valid. The time period $t_{POR}$ is equivalent to $t_{START}$ and sets the interval for the /POR to go Low-to-High after "power is good" (See Figure 2 of "Timing Diagrams"). Active current regulation is employed to limit the inrush current transient response during start-up by regulating the load current at the programmed current limit value (See "Current Limiting and Dual-Level Circuit Breaker" section). The following equation is used to determine the nominal current limit value:

$$I_{LIM} = \frac{V_{TRIPSLOW}}{R_{SENSE}} = \frac{48mV}{R_{SENSE}} \qquad (2)$$

where $V_{TRIPSLOW}$ is the current limit slow trip threshold found in the electrical table and $R_{SENSE}$ is the selected value that will set the desired current limit. There are two basic start-up modes for the MIC2085/86: 1)Start-up dominated by load capacitance and 2)start-up dominated by total gate capacitance. The magnitude of the inrush current delivered to the load will determine the dominant mode. If the inrush current is greater than the programmed current limit (ILIM), then load capacitance is dominant. Otherwise, gate capacitance is dominant. The expected inrush current may be calculated using the following equation:

$$INRUSH \cong I_{GATE} \times \frac{C_{LOAD}}{C_{GATE}} \cong 15\mu A \times \frac{C_{LOAD}}{C_{GATE}} \qquad (3)$$

where $I_{GATE}$ is the GATE pin pull-up current, $C_{LOAD}$ is the load capacitance, and $C_{GATE}$ is the total GATE capacitance (CISS of the external MOSFET and any external capacitor connected from the MIC2085/86 GATE pin to ground).

*Load Capacitance Dominated Start-Up*

In this case, the load capacitance, $C_{LOAD}$, is large enough to cause the inrush current to exceed the programmed current limit but is less than the fast-trip threshold (or the fast-trip threshold is disabled, 'M' option). During start-up under this condition, the load current is regulated at the programmed current limit value (ILIM) and held constant until the output voltage rises to its final value. The output slew rate and equivalent GATE voltage slew rate is computed by the following equation:

$$\text{Output Voltage Slew Rate}, dV_{OUT}/dt = \frac{I_{LIM}}{C_{LOAD}} \qquad (4)$$

where $I_{LIM}$ is the programmed current limit value. Consequently, the value of $C_{FILTER}$ must be selected to ensure that the overcurrent response time, $t_{OCSLOW}$, exceeds the time needed for the output to reach its final value. For example, given a MOSFET with an input capacitance $C_{ISS}$ = $C_{GATE}$ =4700pF, $C_{LOAD}$ is 2200µF, and $I_{LIMIT}$ is set to 6A with a 12Vinput, then the load capacitance dominates as determined by the calculated INRUSH > $I_{LIM}$. Therefore, the output voltage slew rate determined from Equation 4 is:

$$\text{Output Voltage Slew Rate, } d_{VOUT}/dt = \frac{6A}{2200\mu F} = 2.73\frac{V}{ms}$$

and the resulting $t_{OCSLOW}$ needed to achieve a 12V output is approximately 4.5ms. (See "Power-On Reset, Start-Up, and Overcurrent Timer Delays" section to calculate $t_{OCSLOW}$.)

*GATE Capacitance Dominated Start-Up*

In this case, the value of the load capacitance relative to the GATE capacitance is small enough such that the load current during start-up never exceeds the current limit threshold as determined by Equation 3. The minimum value of $C_{GATE}$ that will ensure that the current limit is never exceeded is given by the equation below:

$$C_{GATE}(min) = \frac{I_{GATE}}{I_{LIM}} \times C_{LOAD} \quad (5)$$

where $C_{GATE}$ is the summation of the MOSFET input capacitance ($C_{ISS}$) and the value of the external capacitor connected to the GATE pin of the MOSFET. Once CGATE is determined, use the following equation to determine the output slew rate for gate capacitance dominated start-up.

$$dV_{OUT}/dt(output) = \frac{I_{GATE}}{C_{GATE}} \quad (6)$$

Table 1 depicts the output slew rate for various values of $C_{GATE}$.

| $I_{GATE}$ = 15µA | |
|---|---|
| CGATE | dVOUT/dt |
| 0.001µF | 15V/ms |
| 0.01µF | 1.5V/ms |
| 0.1µF | 0.150V/ms |
| 1µF | 0.015 µF/ms |

**Table 1. Output Slew Rate Selection for GATE Capacitance Dominated Start-Up**

**Current Limiting and Dual-Level Circuit Breaker**

Many applications will require that the inrush and steady state supply current be limited at a specific value in order to protect critical components within the system. Connecting a sense resistor between the VCC and SENSE pins sets the nominal current limit value of the MIC2085/86 and the current limit is calculated using Equation 2. However, the MIC2085/86 exhibits foldback current limit response. The foldback feature allows the nominal current limit threshold to vary from 24mVup to 48mV as the FB pin voltage increases or decreases. When FB is at 0V, the current limit threshold is 24mV and for FB ≥ 0.6V, the current limit threshold is the nominal 48mV.(See Figure 4 for Foldback Current Limit Response characteristic).The MIC2085/86 also features a dual-level circuit breaker triggered via 48mV and 95mV current limit thresholds sensed across the VCC and SENSE pins. The first level of the circuit breaker functions as follows. Once the voltage sensed across these two pins exceeds 48mV, the overcurrent timer, its duration set by capacitor CFILTER, starts to ramp the voltage at CFILTER using a 2µA constant current source. If the voltage at CFILTER reaches the overcurrent timer threshold (VTH) of 1.24V, then CFILTER immediately returns to ground as the circuit breaker trips and the GATE output is immediately shut down. For the second level, if the voltage sensed across VCC and SENSE exceeds 95mV at any time, the circuit breaker trips and the GATE shuts down immediately, bypassing the overcurrent timer period. To disable current limit and circuit breaker operation, tie the SENSE and VCC pins together and the CFILTER pin to ground.

**Output Undervoltage Detection**

The MIC2085/86 employ output undervoltage detection by monitoring the output voltage through a resistive divider connected at the FB pin. During turn on, while the voltage at the FB pin is below the threshold ($V_{FB}$), the /POR pin is asserted low. Once the FB pin voltage crosses $V_{FB}$, a 2µA current source charges capacitor $C_{POR}$. Once the CPOR pin voltage reaches 1.24V, the time period $t_{POR}$ elapses as the CPOR pin is pulled to ground and the /POR pin goes HIGH. If the voltage at FB drops below $V_{FB}$ for more than 10µs, the/POR pin resets for at least one timing cycle defined by $t_{POR}$ (see Applications Information for an example).

**Input Overvoltage Protection**

The MIC2085/86 monitors and detects overvoltage conditions in the event of excessive supply transients at the input. Whenever the overvoltage threshold ($V_{OV}$) is exceeded at the OV pin, the GATE is pulled low and the output is shut off. The GATE will begin ramping one POR timing cycle after the OV pin voltage drops below its threshold. An external CRWBR circuit, as shown in the typical application diagram, provides a time period that an overvoltage condition must exceed in order to trip the circuit breaker. When the OV pin exceeds the overvoltage threshold ($V_{OV}$), the CRWBR timer begins charging the CRWBR capacitor initially with a 45µA current source.Once the voltage at CRWBR exceeds its threshold ($V_{CR}$) of 0.47V, the CRWBR current immediately increases to 1.5mA and the circuit breaker is tripped, necessitating a device reset by toggling the ON pin LOW to HIGH.

**Power-On Reset, Start-Up, and Overcurrent TimerDelays**

The Power-On Reset delay, $t_{POR}$, is the time period for the /POR pin to go HIGH once the voltage at the FB pin exceeds the power-good threshold ($V_{TH}$). A capacitor

connected to CPOR sets the interval, $t_{POR}$, and $t_{POR}$ is equivalent to the start-up delay, $t_{START}$ (see Equation 1).

A capacitor connected to CFILTER is used to set the timer which activates the circuit breaker during overcurrent conditions. When the voltage across the sense resistor exceeds the slow trip current limit threshold of 48mV, the overcurrent timer begins to charge for a period, $t_{OCSLOW}$, determined by CFILTER. If no capacitor is used at CFILTER, then $t_{OCSLOW}$ defaults to 5µs. If $t_{OCSLOW}$ elapses, then the circuit breaker is activated and the GATE output is immediately pulled to ground. The following equation is used to determine the overcurrent timer period, $t_{OCSLOW}$.

$$t_{OCSLOW} = C_{FILTER} \times \frac{V_{TH}}{I_{TIMER}} \cong 0.062 \times C_{FILTER}(\mu F) \qquad (7)$$

where $V_{TH}$, the CFILTER timer threshold, is 1.24V and $I_{TIMER}$, the overcurrent timer current, is 20µA. Tables 2 and 3 provide a quick reference for several timer calculations using select standard value capacitors.

| $C_{POR}$ | $t_{POR} = t_{START}$ |
|---|---|
| 0.01µF | 6ms |
| 0.02µF | 12ms |
| 0.033µF | 18.5ms |
| 0.05µF | 30ms |
| 0.1µF | 60ms |
| 0.33µF | 200ms |

**Table 2. Selected Power-On Reset and Start-Up Delays**

| $C_{FILTER}$ | $t_{OCSLOW}$ |
|---|---|
| 1800pF | 100µs |
| 4700pF | 290µs |
| 8200pF | 500µs |
| 0.01µF | 620µs |
| 0.02µF | 1.2ms |
| 0.033µF | 2.0ms |
| 0.05µF | 3.0ms |
| 0.1µF | 6.2ms |
| 0.33µF | 20.7ms |

**Table 3. Selected Overcurrent Timer Delays**

## Application Information

### Output Undervoltage Detection

For output undervoltage detection, the first consideration is to establish the output voltage level that indicates "power is good." For this example, the output value for which a 12V supply will signal "good" is 11V. Next, consider the tolerances of the input supply and FB threshold (VFB). For this example, the 12V supply varies ±5%, thus the resulting output voltage may be as low as 11.4V and as high as 12.6V. Additionally, the FB threshold has ±50mV tolerance and may be as low as1.19V and as high as 1.29V. Thus, to determine the values of the resistive divider network (R5 and R6) at the FB pin, shown in Figure 5, use the following iterative design procedure.

1) Choose R6 so as to limit the current through the divider to approximately 100µA or less.

$$R6 \geq \frac{V_{FB(MAX)}}{100\mu A} \geq \frac{1.29V}{100\mu A} \geq 12.9k\Omega$$

R6 is chosen as 13.3kΩ ± 1%

2) Next, determine R5 using the output "good" voltage of 11V and the following equation:

$$V_{OUT(Good)} = V_{FB}\left[\frac{(R5 + R6)}{R6}\right] \qquad (8)$$

Using some basic algebra and simplifying Equation 8 to isolate R5, yields:

$$R5 = R6\left[\left(\frac{V_{OUT(Good)}}{V_{FB(MAX)}}\right) - 1\right] \qquad (8.1)$$

where $V_{FB(MAX)}$ = 1.29V, $V_{OUT(Good)}$ = 11V, and R6 is13.3kΩ. Substituting these values into Equation 8.1 now yields R5 = 100.11kΩ. A standard 100kΩ ± 1% is selected. Now, consider the 11.4V minimum output voltage, the lower tolerance for R6 and higher tolerance for R5, 13.17kΩ and101kΩ, respectively. With only 11.4V available, the voltage sensed at the FB pin exceeds $V_{FB(MAX)}$, thus the /POR and PWRGD (MIC2086) signals will transition from LOW to HIGH, indicating "power is good" given the worse case tolerances of this example.

### Input Overvoltage Protection

The external CRWBR circuit shown in Figure 5 consists of capacitor C4, resistor R7, NPN transistor Q2, and SCR Q3.The capacitor establishes a time duration for an overvoltage condition to last before the circuit breaker trips. The CRWBR timer duration is approximated by the following equation:

$$t_{OVCR} \cong \frac{(C4 \times V_{CR})}{I_{CR}} \cong 0.01 \times C4(\mu F) \qquad (9)$$

where $V_{CR}$, the CRWBR pin threshold, is 0.47V and $I_{CR}$, the CRWBR pin current, is 45µA during the timer period (see the CRWBR timer pin description for further description). A similar design approach as the previous undervoltage detection example is recommended for the

overvoltage protection circuitry, resistors R2 and R3 in Figure 5. For input overvoltage protection, the first consideration is to establish the input voltage level that indicates an overvoltage triggering a sys-tem (output voltage) shut down. For this example, the input value for which a 12V supply will signal an “output shut down” is 13.2V (+10%). Similarly, from the previous example:

1) Choose R3 to satisfy 100µA condition.

$$R3 \geq \frac{V_{OV(MIN)}}{100\mu A} \geq \frac{1.19V}{100\mu A} \geq 11.9k\Omega$$

R3 is chosen as 13.7kΩ ± 1%.

2) Thus, following the previous example and substituting R2 and R3 for R5 and R6, respectively, and 13.2V overvoltage for 11V output “good”, the same formula yields R2 of 138.3kΩ.The next highest standard 1% value is 140kΩ.

Now, consider the 12.6V maximum input voltage ($V_{CC}$ +5%), the higher tolerance for R3 and lower tolerance for R2, 13.84k and 138.60kΩ, respectively. With a 12.6V input, the voltage sensed at the OV pin is below $V_{OV(MIN)}$, and the MIC2085/86will not indicate an overvoltage condition until VCC exceeds at least 13.2V.

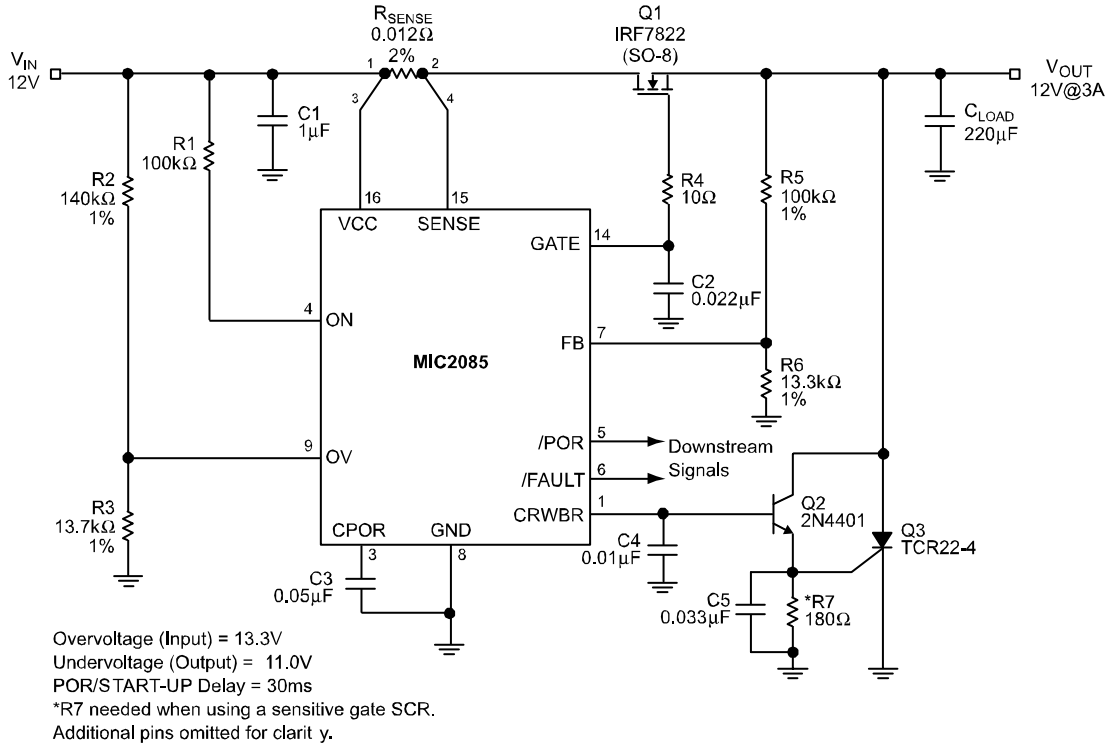



**Figure 5. Undervoltage/Overvoltage Circuit**

### PCB Connection Sense

There are several configuration options for the MIC2085/86'sON pin to detect if the PCB has been fully seated in the backplane before initiating a start-up cycle. In the typical applications circuit, the MIC2085/86 is mounted on the PCB with a resistive divider network connected to the ON pin. R2is connected to a short pin on the PCB edge connector. Until the connectors mate, the ON pin is held low which keeps the GATE output charge pump off. Once the connectors mate, the resistor network is pulled up to the input supply, 12V in this example, and the ON pin voltage exceeds its threshold ($V_{ON}$) of 1.24V and the MIC2085/86 initiates a start-up cycle. In Figure 6, the connection sense consisting of a logic-level discrete MOSFET and a few resistors allows for interrupt control from the processor or other signal controller to shut off the output of the MIC2085/86. R4 keeps the GATE of Q2 at $V_{IN}$ until the connectors are fully mated. A logic LOW at the/ON_OFF signal turns Q2 off and allows the ON pin to pull up above its threshold and initiate a start-up cycle. Applying a logic HIGH at the /ON_OFF signal will turn Q2 on and short the ON pin of the MIC2085/86 to ground which turns off the GATE output charge pump.

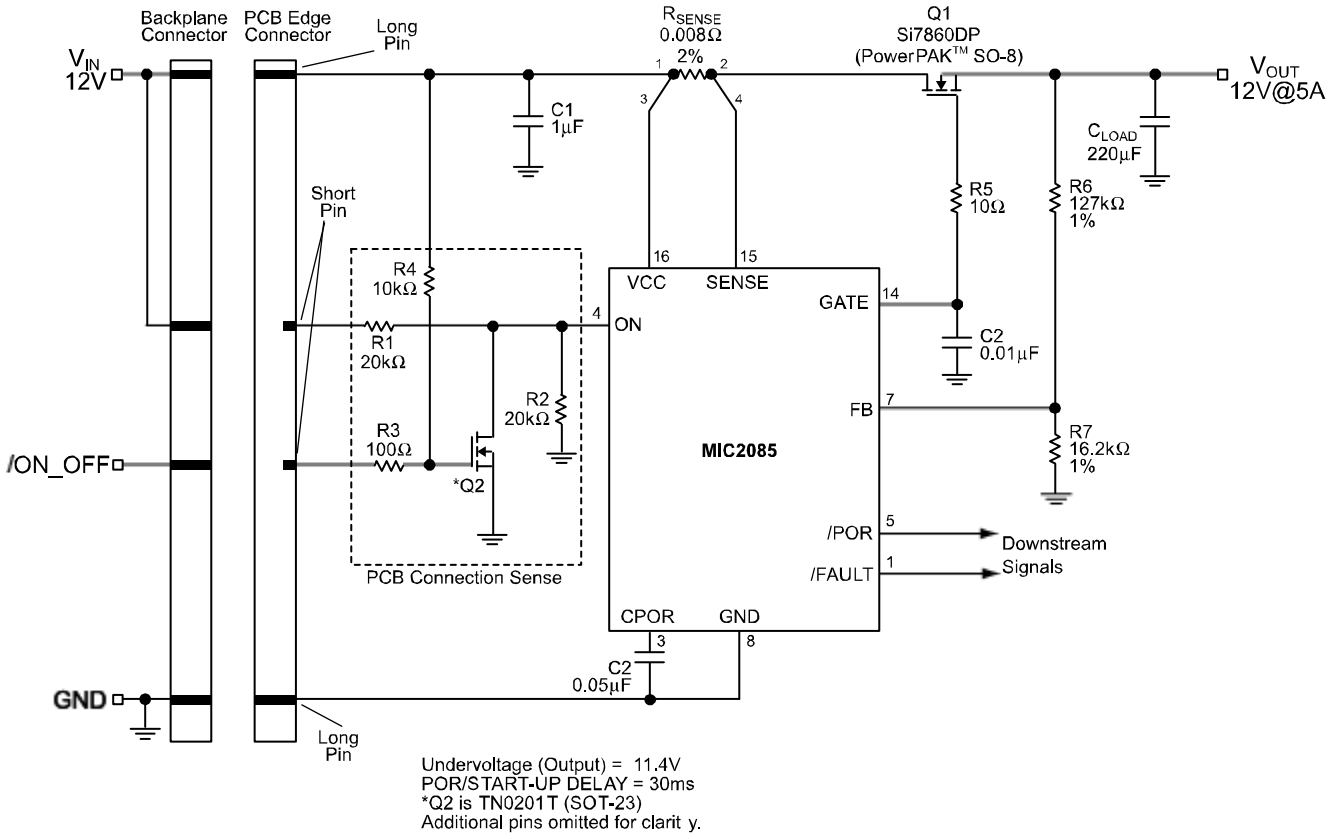



**Figure 6. PCB Connection Sense with ON/OFF Control**

### Higher UVLO Setting

Once a PCB is inserted into a backplane (power supply), the internal UVLO circuit of the MIC2085/86 holds the GATE output charge pump off until $V_{CC}$ exceeds 2.18V. If VCC falls below 2V, the UVLO circuit pulls the GATE output to ground and clears the overvoltage and/or current limit faults. For a higher UVLO threshold, the circuit in Figure 7 can be used to delay the output MOSFET from switching on until the desired input voltage is achieved. The circuit allows the charge pump to remain off until VIN exceeds $\left(1+\frac{R1}{R2}\right)\times 1.24V$. The GATE drive output will be shut down when $V_{IN}$ falls below $\left(1+\frac{R1}{R2}\right)\times 1.14V$. In the example circuit (Figure 7), the rising UVLO threshold is set at approximately 11V and the falling UVLO threshold is established as 10.1V. The circuit consists of an external resistor divider at the ON pin that keeps the GATE output charge pump off until the voltage at the ON pin exceeds its threshold ($V_{ON}$) and after the start-up time relapses.

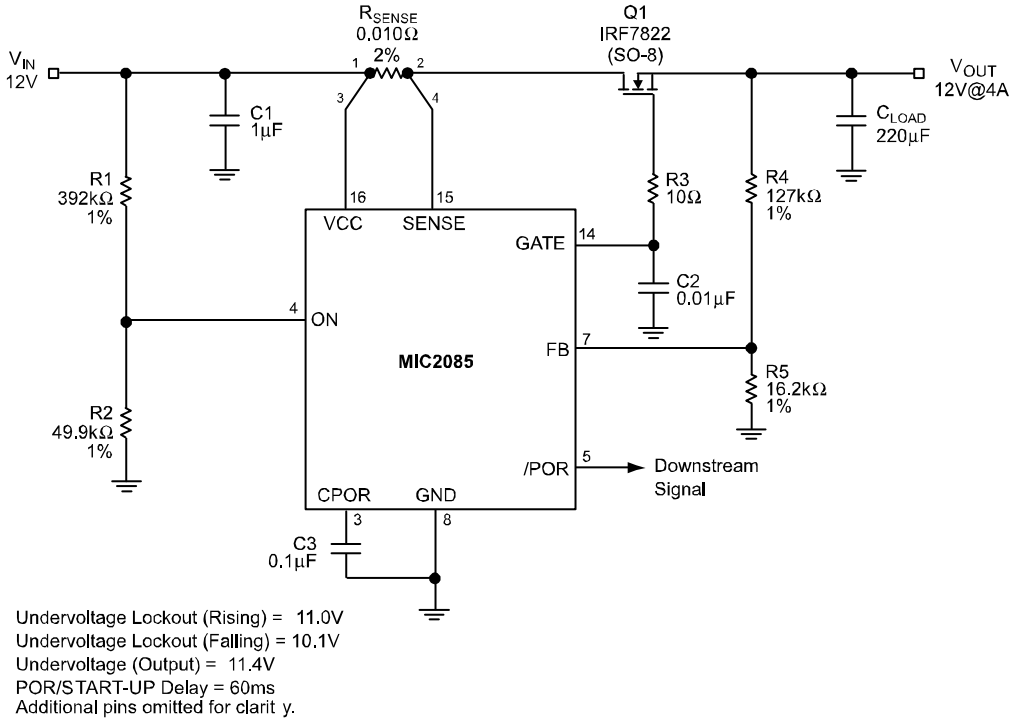



**Figure 7. Higher UVLO Setting**

### Fast Output Discharge for Capacitive Loads

In many applications where a switch controller is turned off by either removing the PCB from the backplane or the ON pin is reset, capacitive loading will cause the output to retain voltage unless a 'bleed' (low impedance) path is in place in order to discharge the capacitance. The MIC2086 is equipped with an internal MOSFET that allows the discharging of any load capacitance to ground through a 550Ω path. The discharge feature is configured by wiring the DIS pin to the output (source) of the external MOSFET and becomes active (DIS pin output is low) once the ON pin is deasserted. Figure 8(a) illustrates the use of the discharge feature with an optional resistor (R5) that can be used to provide added resistance in the output discharge path. For an even faster discharge response of capacitive loads, the configuration of Figure 8(b) can be utilized to apply a crowbar to ground through an external SCR (Q3) that is triggered when the DIS pin goes low which turns on the PNP transistor (Q2). See the different "Functional Characteristic" curves for a comparison of the discharge response configurations.

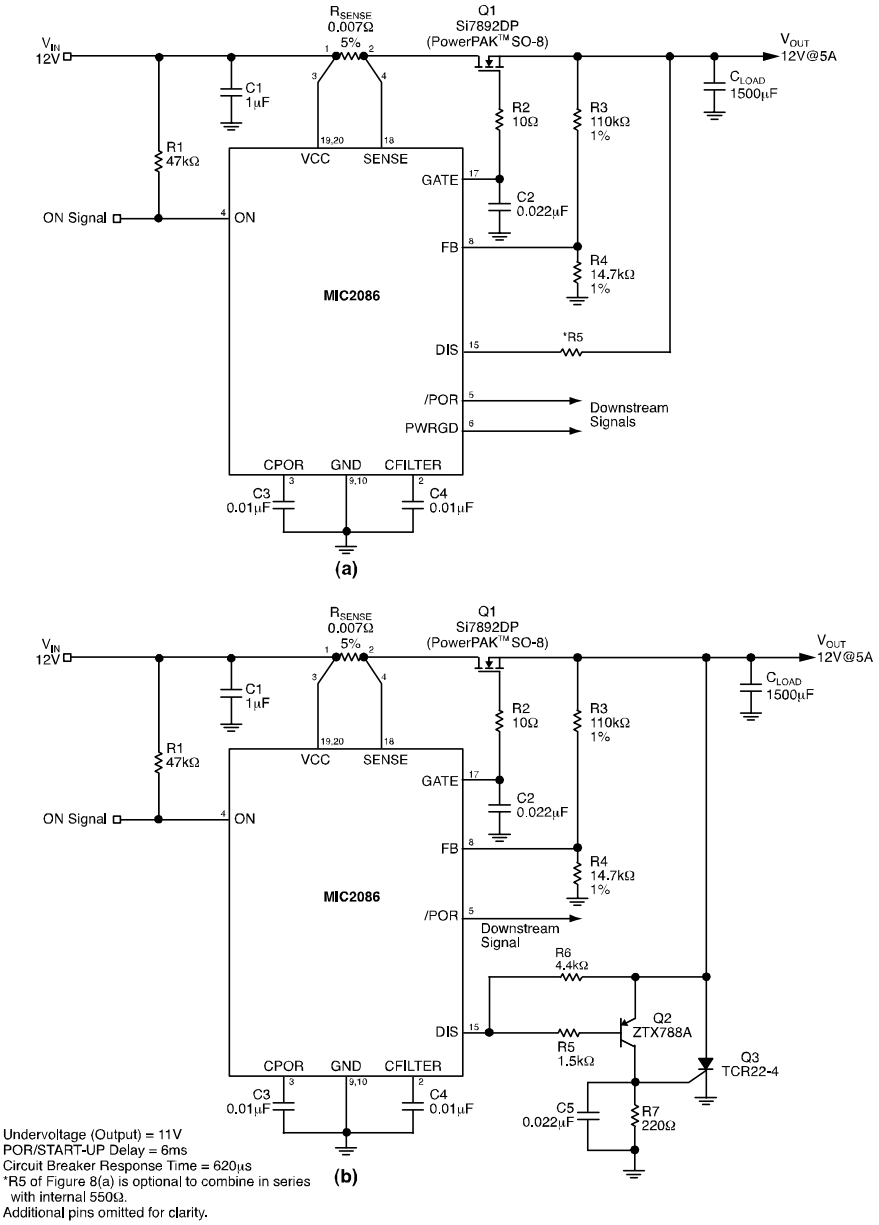



**Figure 8. MIC2086 Fast Discharge of Capacitive Load**

### Auto-Retry Upon Overcurrent Faults

The MIC2085/86 can be configured for automatic restart after a fault condition. Placing a diode between the ON and/FAULT pins, as shown in Figure 9, will enable the auto-restart capability of the controller. When an application is configured for auto-retry, the overcurrent timer should be set to minimize the duty cycle of the overcurrent response to prevent thermal runaway of the power MOSFET. See "MOSFET Transient Thermal Issues" section for further detail. A limited duty cycle is achieved when the overcurrent timer duration ($t_{OCSLOW}$) is much less than the start-up delay timer duration ($t_{START}$) and is calculated using the following equation:

$$\text{Auto} - \text{Retry Duty Cycle} = \frac{t_{OCSLOW}}{t_{START}} \times 100\% \qquad (10)$$

### An InfiniBand™ Application Circuit

The circuit in Figure 10 depicts a single 50W InfiniBand™ module using the MIC2085 controller. An InfiniBand™ backplane distributes bulk power to multiple plug-in modules that employ DC/DC converters for local supply requirements. The circuit in Figure 10 distributes 12V from the backplane to the MIC2182 DC/DC converter that steps down +12V to+3.3V for local bias. The pass transistor, Q1, isolates theMIC2182's input capacitance during module plug-in and allows the backplane to accommodate additional plug-in modules without affecting the other modules on the backplane. The two control input signals are VBxEn_L (active LOW) and a Local Power Enable (active HIGH). The MIC2085 in the circuit of Figure 10 performs a number of functions. The gate output of Q1 is enabled by the two bit input signal VBxEn_L, Local Power Enable = [0,1]. Also, the MIC2085 limits the drain current of Q1 to 7A, monitors VB_In for an overvoltage condition greater than 16V, and enables the MIC2182 DC/DC converter downstream to supply a local voltage rail. The uncommitted comparator is used to monitor VB_In for an undervoltage condition of less than 10V, indicated by a logic LOW at the comparator output (COMPOUT). COMPOUT may be used to control a downstream device such as another DC/DC converter. Additionally, the MIC2085 is configured for auto-retry upon an overcurrent fault condition by placing a diode (D1) between the /FAULT and ON pins of the controller.

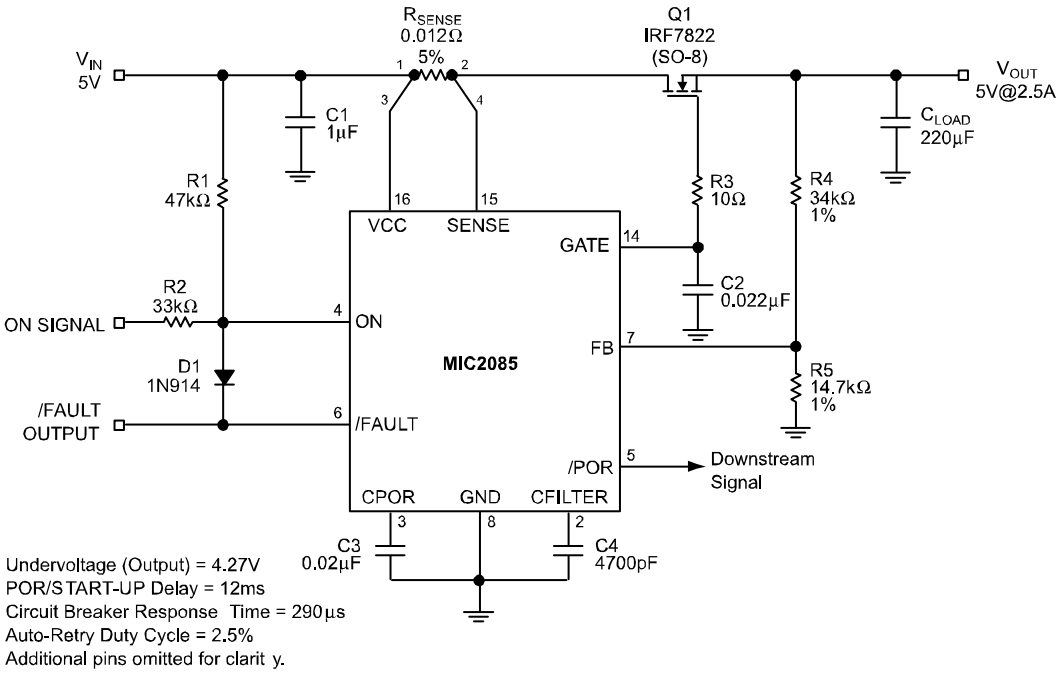



**Figure 9. Auto-Retry Configuration**

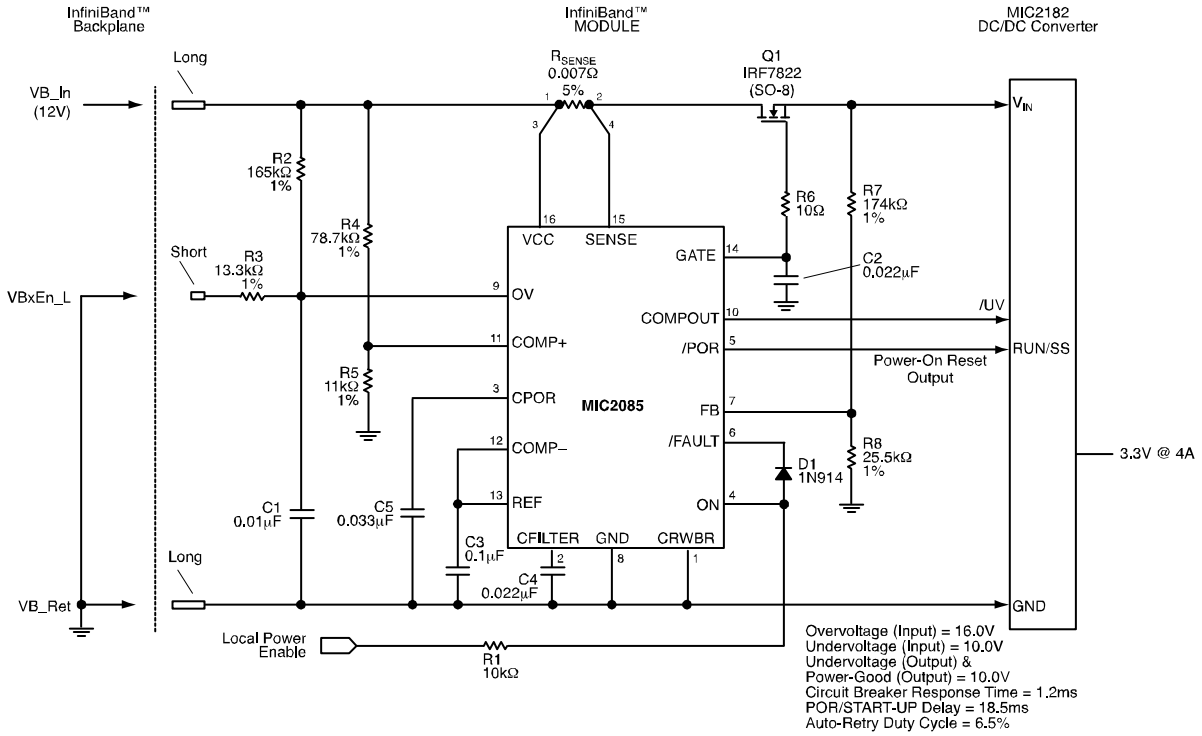



**Figure 10. A 50W InfiniBand™ Application**

### Sense Resistor Selection

The MIC2085 and MIC2086 use a low-value sense resistor to measure the current flowing through the MOSFET switch (and therefore the load). This sense resistor is nominally valued at $48mV/I_{LOAD(CONT)}$. To accommodate worst-case tolerances for both the sense resistor (allow ±3% over time and temperature for a resistor with ±1% initial tolerance) and still supply the maximum required steady-state load current, a slightly more detailed calculation must be used. The current limit threshold voltage (the "trip point") for theMIC2085/86 may be as low as 40mV, which would equate to a sense resistor value of $40mV/I_{LOAD(CONT)}$. Carrying the numbers through for the case where the value of the sense resistor is 3% high yields:

$$R_{SENSE(MAX)} = \frac{40mV}{(1.03)(I_{LOAD(CONT)})} = \frac{38.8mV}{I_{LOAD(CONT)}} \quad (11)$$

Once the value of $R_{SENSE}$ has been chosen in this manner, it is good practice to check the maximum $I_{LOAD(CONT)}$ which the circuit may let through in the case of tolerance build-up in the opposite direction. Here, the worst-case maximum cur-rent is found using a 55mV trip voltage and a sense resistor that is 3% low in value. The resulting equation is:

$$I_{LOAD(CONT,MAX)} = \frac{55mV}{(0.97)(R_{SENSE(NOM)})} = \frac{56.7mV}{R_{SENSE(NOM)}} \quad (12)$$

As an example, if an output must carry a continuous 6Awithout nuisance trips occurring, Equation 11 yields:

$$R_{SENSE(MAX)} = \frac{38.8mV}{6A} = 6.5m\Omega$$

The next lowest standard value is 6.0mW. At the other set of tolerance extremes for the output in question:

$$I_{LOAD(CONT,MAX)} = \frac{56.7mV}{6.0m\Omega} = 9.45A,$$

almost 10A. Knowing this final datum, we can determine the necessary wattage of the sense resistor, using $P = I^2R$, where I will be $I_{LOAD(CONT,\ MAX)}$, and R will be $(0.97)(R_{SENSE(NOM)})$. These numbers yield the following:

$$PMAX = (10A)^2\ (5.82m\Omega) = 0.582W.$$

In this example, a 1W sense resistor is sufficient.

### MOSFET Selection

Selecting the proper external MOSFET for use with theMIC2085/86 involves three straightforward tasks:

- Choice of a MOSFET which meets minimum voltage requirements.
- Selection of a device to handle the maximum continuous current (steady-state thermal issues).
- Verify the selected part's ability to withstand any peak currents (transient thermal issues).

**MOSFET Voltage Requirements**

The first voltage requirement for the MOSFET is that the drain-source breakdown voltage of the MOSFET must be greater than $V_{IN(MAX)}$. For instance, a 16V input may reasonably be expected to see high-frequency transients as high as 24V.Therefore, the drain-source breakdown voltage of the MOSFET must be at least 25V. For ample safety margin and standard availability, the closest minimum value should be 30V.

The second breakdown voltage criterion that must be met is a bit subtler than simple drain-source breakdown voltage. In MIC2085/86 applications, the gate of the external MOSFET is driven up to a maximum of 21V by the internal output MOSFET. At the same time, if the output of the external MOSFET (its source) is suddenly subjected to a short, the gate-source voltage will go to (21V – 0V) = 21V. Since most power MOSFETs generally have a maximum gate-source breakdown of 20V or less, the use of a Zener clamp is recommended in applications with $V_{CC} \geq 8V$. A Zener diode with 10V to 12V rating is recommended as shown in Figure11. At the present time, most power MOSFETs with a 20V gate-source voltage rating have a 30V drain-source break-down rating or higher. As a general tip, choose surface-mount devices with a drain-source rating of 30V or more as a starting point.

Finally, the external gate drive of the MIC2085/86 requires a low-voltage logic level MOSFET when operating at voltage slower than 3V. There are 2.5V logic-level MOSFETs avail-able. Please see Table 4, “MOSFET and Sense Resistor Vendors” for suggested manufacturers.

**MOSFET Steady-State Thermal Issues**

The selection of a MOSFET to meet the maximum continuous current is a fairly straightforward exercise. First, arm yourself with the following data:

- The value of $I_{LOAD(CONT,\ MAX.)}$ for the output in question (see “Sense Resistor Selection”).
- The manufacturer’s data sheet for the candidate MOSFET.
- The maximum ambient temperature in which the device will be required to operate.
- Any knowledge you can get about the heat sinking available to the device (e.g., can heat be dissipated into the ground plane or power plane, if using a surface-mount part? Is any airflow available?).

The data sheet will almost always give a value of on resistance given for the MOSFET at a gate-source voltage of 4.5V, and another value at a gate-source voltage of 10V. As a first approximation, add the two values together and divide by two to get the on-resistance of the part with 8V of enhancement. Call this value $R_{ON}$. Since a heavily enhanced MOSFET acts as an ohmic (resistive) device, almost all that’s required to determine steady-state power dissipation is to calculate I2R.The one addendum to this is that MOSFETs have a slight increase in $R_{ON}$ with increasing die temperature. A good approximation for this value is 0.5% increase in $R_{ON}$ per °C rise in junction temperature above the point at which $R_{ON}$ was initially specified by the manufacturer. For instance, if the selected MOSFET has a calculated $R_{ON}$ of 10mΩ at a $T_J$ = 25°C, and the actual junction temperature ends up at 110°C, a good first cut at the operating value for $R_{ON}$ would be:

$$R_{ON} \cong 10m\Omega[1 + (110 - 25)(0.005)] \cong 14.3m\Omega$$

The final step is to make sure that the heat sinking available to the MOSFET is capable of dissipating at least as much power (rated in °C/W) as that with which the MOSFET’s performance was specified by the manufacturer. Here are a few practical tips:

1. The heat from a surface-mount device such a san SO-8 MOSFET flows almost entirely out of the drain leads. If the drain leads can be soldered down to one square inch or more, the copper will act as the heat sink for the part. This copper must be on the same layer of the board as the MOSFET drain.

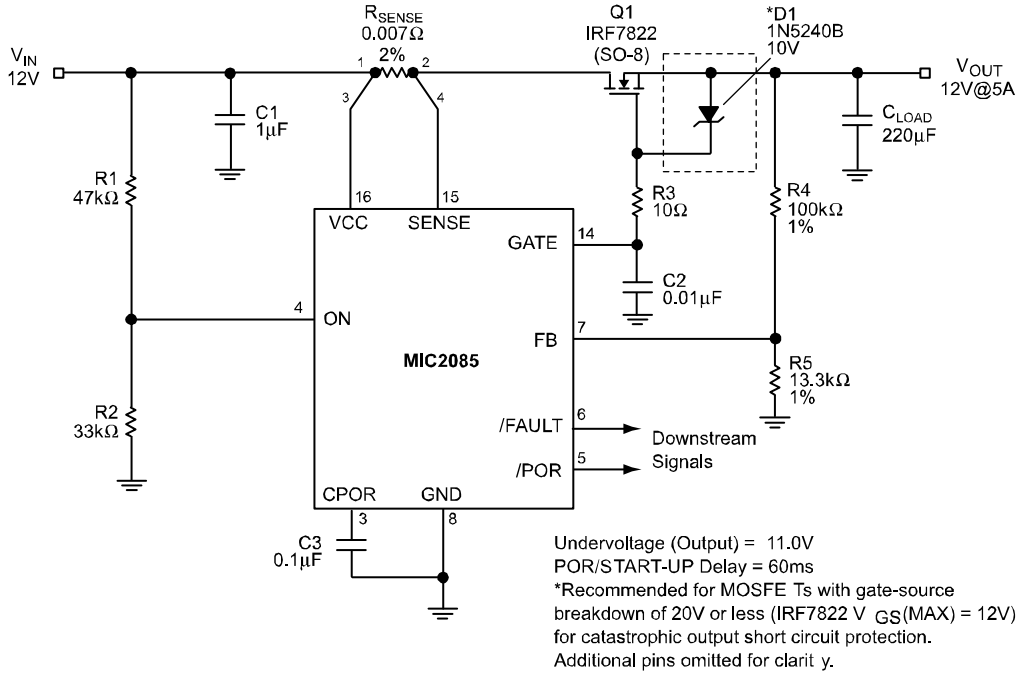



**Figure 11. Zener Clamped MOSFET GATE**

2. Airflow works. Even a few LFM (linear feet per minute) of air will cool a MOSFET down substantially. If you can, position the MOSFET(s) near the inlet of a power supply's fan, or the outlet of a processor's cooling fan.

3. The best test of a surface-mount MOSFET for an application (assuming the above tips show it to be a likely fit) is an empirical one. Check the MOSFET's temperature in the actual layout of the expected final circuit, at full operating current. The use of a thermocouple on the drain leads, or infrared pyrometer on the package, will then give a reasonable idea of the device's junction temperature.

**MOSFET Transient Thermal Issues**

Having chosen a MOSFET that will withstand the imposed voltage stresses, and the worse case continuous I2R power dissipation which it will see, it remains only to verify the MOSFET's ability to handle short-term overload power dissipation without overheating. A MOSFET can handle a much higher pulsed power without damage than its continuous dissipation ratings would imply. The reason for this is that, like everything else, thermal devices (silicon die, lead frames, etc.) have thermal inertia.

In terms related directly to the specification and use of power MOSFETs, this is known as "transient thermal impedance," or $Z_{\theta(J-A)}$. Almost all power MOSFET data sheets give a Transient Thermal Impedance Curve. For example, take the following case: VIN = 12V, $t_{OCSLOW}$ has been set to 100msec, $I_{LOAD(CONT.\ MAX)}$ is 2.5A, the slow-trip threshold is 48mVnominal, and the fast-trip threshold is 95mV. If the output is accidentally connected to a 3Ω load, the output current from the MOSFET will be regulated to 2.5A for 100ms ($t_{OCSLOW}$) before the part trips. During that time, the dissipation in the MOSFET is given by:

$$P = E \times I \qquad E_{MOSFET} = [12V-(2.5A)(3\Omega)]=4.5V$$

$$PMOSFET = (4.5V \times 2.5A) = 11.25W \text{ for } 100msec.$$

At first glance, it would appear that a really hefty MOSFET is required to withstand this sort of fault condition. This is where the transient thermal impedance curves become very useful. Figure 12 shows the curve for the Vishay (Siliconix) Si4410DY, a commonly used SO-8 power MOSFET.

Taking the simplest case first, we'll assume that once a fault event such as the one in question occurs, it will be a long time – 10 minutes or more – before the fault is isolated and the channel is reset. In such a case, we can approximate this as a "single pulse" event, that is to say, there's no significant duty cycle. Then, reading up from the X-axis at the point where "Square Wave Pulse Duration" is equal to 0.1sec (=100msec), we see that the $Z_{\theta(J-A)}$ of this MOSFET to a highly infrequent event of this duration is only 8% of its continuous $R_{\theta(J-A)}$.

This particular part is specified as having an $R_{\theta(J-A)}$ of 50°C/W for intervals of 10 seconds or less. Thus:

Assume $T_A$ = 55°C maximum, 1 square inch of copper at the drain leads, no airflow.

Recalling from our previous approximation hint, the part

has an $R_{ON}$ of (0.0335/2) = 17mΩ at 25°C.

Assume it has been carrying just about 2.5A for some time.

When performing this calculation, be sure to use the highest anticipated ambient temperature ($T_{A(MAX)}$) in which the MOSFET will be operating as the starting temperature, and find the operating junction temperature increase ($\Delta T_J$) from that point. Then, as shown next, the final junction temperature is found by adding $T_{A(MAX)}$ and $\Delta T_J$. Since this is not a closed-form equation, getting a close approximation may take one or two iterations, but it's not a hard calculation to perform, and tends to converge quickly.

Then the starting (steady-state) $T_J$ is:

$$T_J \cong T_{A(MAX)} + \Delta TJ$$
$$\cong T_{A(MAX)} + [R_{ON} + (T_{A(MAX)} - T_A)(0.005/°C)(R_{ON})] \times I^2 \times R_{\theta(J-A)}$$
$$T_J \cong 55°C + [17mΩ + (55°C-25°C)(0.005)(17mΩ)] \times (2.5A)^2 \times (50°C/W)$$
$$T_J \cong (55°C + (0.122W)(50°C/W)$$
$$\cong 61.1°C$$

Iterate the calculation once to see if this value is within a few percent of the expected final value. For this iteration we will start with $T_J$ equal to the already calculated value of 61.1°C:

$$T_J \cong T_A + [17mΩ + (61.1°C-25°C)(0.005)(17mΩ)] \times (2.5A)^2 \times (50°C/W)$$
$$T_J \cong ( 55°C + (0.125W)(50°C/W)$$
$$\cong 61.27°C$$

So our original approximation of 61.1°C was very close to the correct value. We will use TJ = 61°C.

Finally, add (11.25W)(50°C/W)(0.08) = 45°C to the steady-state $T_J$ to get $T_{J(TRANSIENT\ MAX.)}$ = 106°C. This is an acceptable maximum junction temperature for this part.

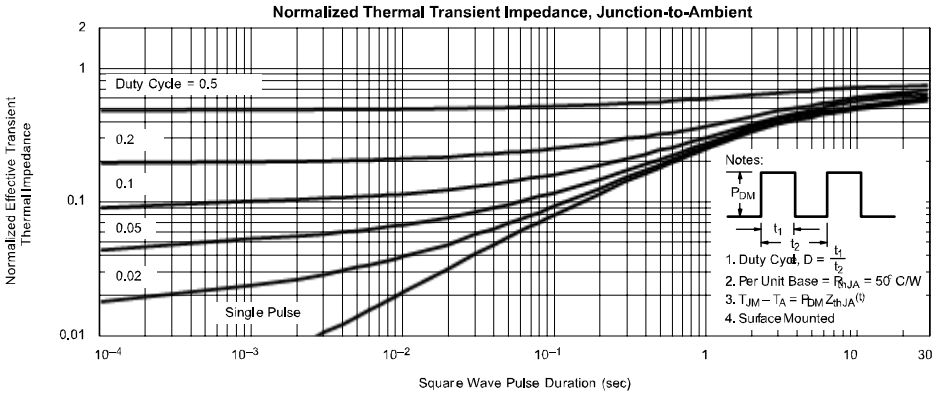



**Figure 12. Transient Thermal Impedance**

### PCB Layout Considerations

Because of the low values of the sense resistors used with theMIC2085/86 controllers, special attention to the layout must be used in order for the device's circuit breaker function to operate properly. Specifically, the use of a 4-wire Kelvin connection to measure the voltage across $R_{SENSE}$ is highly recommended. Kelvin sensing is simply a means of making sure that any voltage drops in the power traces connecting to the resistors does not get picked up by the traces themselves. Additionally, these Kelvin connections should be isolated from all other signal traces to avoid introducing noise onto these sensitive nodes. Figure 13 illustrates a recommended, multi-layer layout for the $R_{SENSE}$, Power MOSFET, timer(s), overvoltage and feedback network connections. The feed-back and overvoltage resistive networks are selected for a12V application (from Figure 5). Many hot swap applications will require load currents of several amperes. Therefore, the power (VCC and Return) trace widths (W) need to be wide enough to allow the current to flow while the rise in temperature for a given copper plate (e.g., 1 oz. or 2 oz.) is kept to a maximum of 10°C ~ 25°C. Also, these traces should be as short as possible in order to minimize the IR drops between the input and the load. For a starting point, there are many trace width calculation tools available on the web such as the following link:

http://www.aracnet.com/cgi-usr/gpatrick/trace.pl

Finally, plated-through vias are utilized to make circuit connections to the power and ground planes. The trace connections with indicated vias should follow the example shown for the GND pin connection in Figure 13.

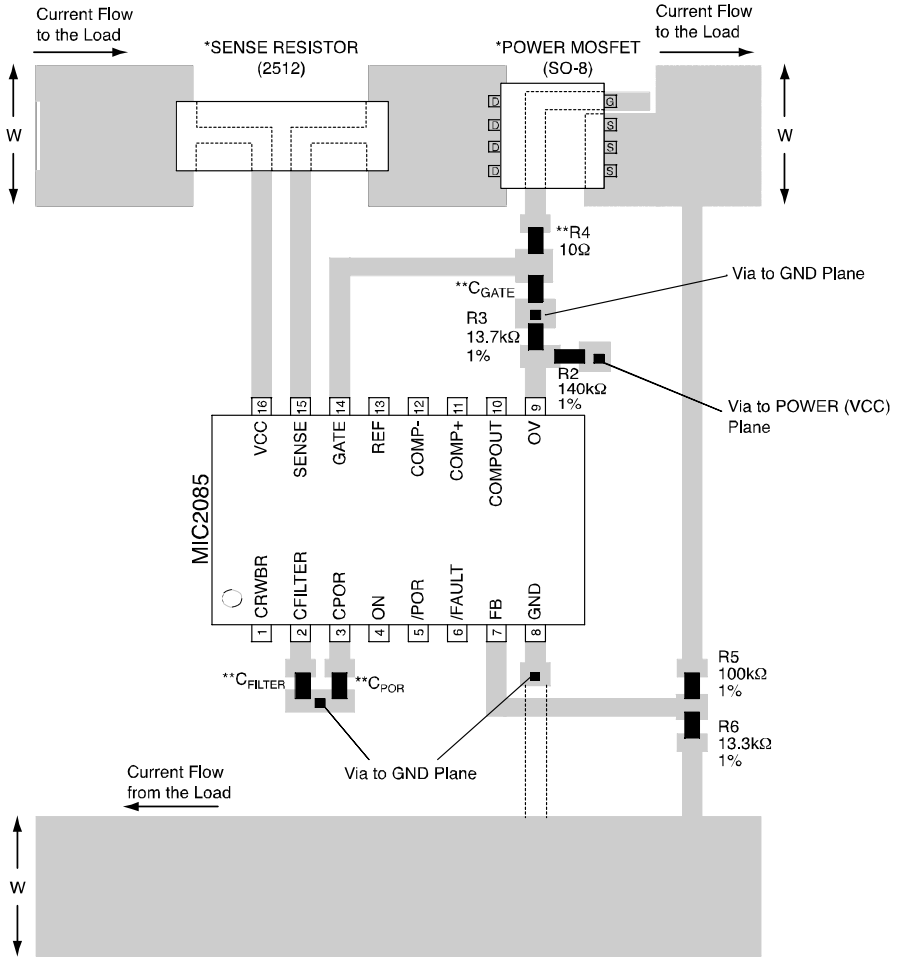



**Figure 13. Recommended PCB Layout for Sense Resistor, Power MOSFET, and Feedback/Overvoltage Network**

### MOSFET and Sense Resistor Vendors

Device types and manufacturer contact information for power MOSFETs and sense resistors is provided in Table 4. Some of the recommended MOSFETs include a metal heat sink on the bottom side of the package. The recommended trace for the MOSFET Gate of Figure 13 must be redirected when using MOSFETs packaged in this style. Contact the device manufacturer for package information.

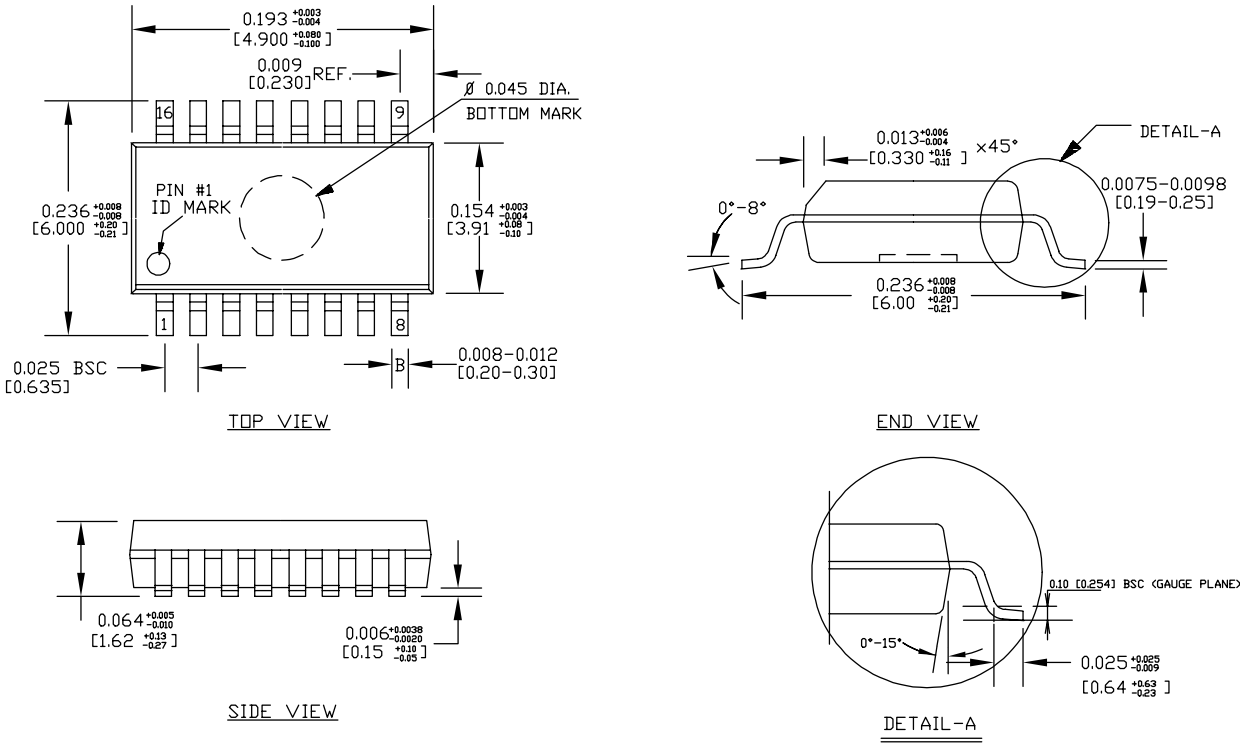
| MOSFET Vendors | Key MOSFET Type(s) | *Applications | Contact Information |
|---|---|---|---|
| Vishay (Siliconix) | Si4420DY (SO-8 package)<br>Si4442DY (SO-8 package)<br>Si3442DV (SO-8 package)<br>Si7860DP (PowerPAK™ SO-8)<br>Si7892DP (PowerPAK™ SO-8)<br>Si7884DP (PowerPAK™ SO-8)<br>SUB60N06-18 (TO-263)<br>SUB70N04-10 (TO-263) | $I_{OUT} \leq 10A$<br>$I_{OUT} = 10A – 15A, V_{CC} \leq 5V$<br>$I_{OUT} \leq 3A, V_{CC} \leq 5V$<br>$I_{OUT} \leq 12A$<br>$I_{OUT} \leq 15A$<br>$I_{OUT} \leq 15A$<br>$I_{OUT} \geq 20A, V_{CC} \geq 5V$<br>$I_{OUT} \geq 20A, V_{CC} \geq 5V$ | www.siliconix.com<br>(203) 452-5664 |
| International Rectifier | IRF7413 (SO-8 package)<br>IRF7457 (SO-8 package)<br>IRF7822 (SO-8 package)<br>IRLBA1304 (Super220™) | $I_{OUT} \leq 10A$<br>$I_{OUT} \leq 10A$<br>$I_{OUT} = 10A – 15A, V_{CC} \leq 5V$<br>$I_{OUT} \geq 20A, V_{CC} \geq 5V$ | www.irf.com<br>(310) 322-3331 |
| Fairchild Semiconductor | FDS6680A (SO-8 package)<br>FDS6690A (SO-8 package) | $I_{OUT} \leq 10A$<br>$I_{OUT} \leq 10A, V_{CC} \leq 5V$ | www.fairchildsemi.com<br>(207) 775-8100 |
| Philips | PH3230 (SOT669-LFPAK) | $I_{OUT} \geq 20A$ | www.philips.com |
| Hitachi | HAT2099H (LFPAK) | $I_{OUT} \geq 20A$ | www.halsp.hitachi.com<br>(408) 433-1990 |

* These devices are not limited to these conditions in many cases, but these conditions are provided as a helpful reference for customer applications

| Resistor Vendors | Sense Resistors | Contact Information |
|---|---|---|
| Vishay (Dale) | “WSL” Series | www.vishay.com/docswsl_30100.pdf<br>(203) 452-5664 |
| IRC | “OARS” Series<br>”LR” Series<br>(second source to “WSL”) | www.irctt.com/pdf_files/OARS.pdf<br>www.irctt.com/pdf_files/LRS.pdf<br>(828) 264-8861 |

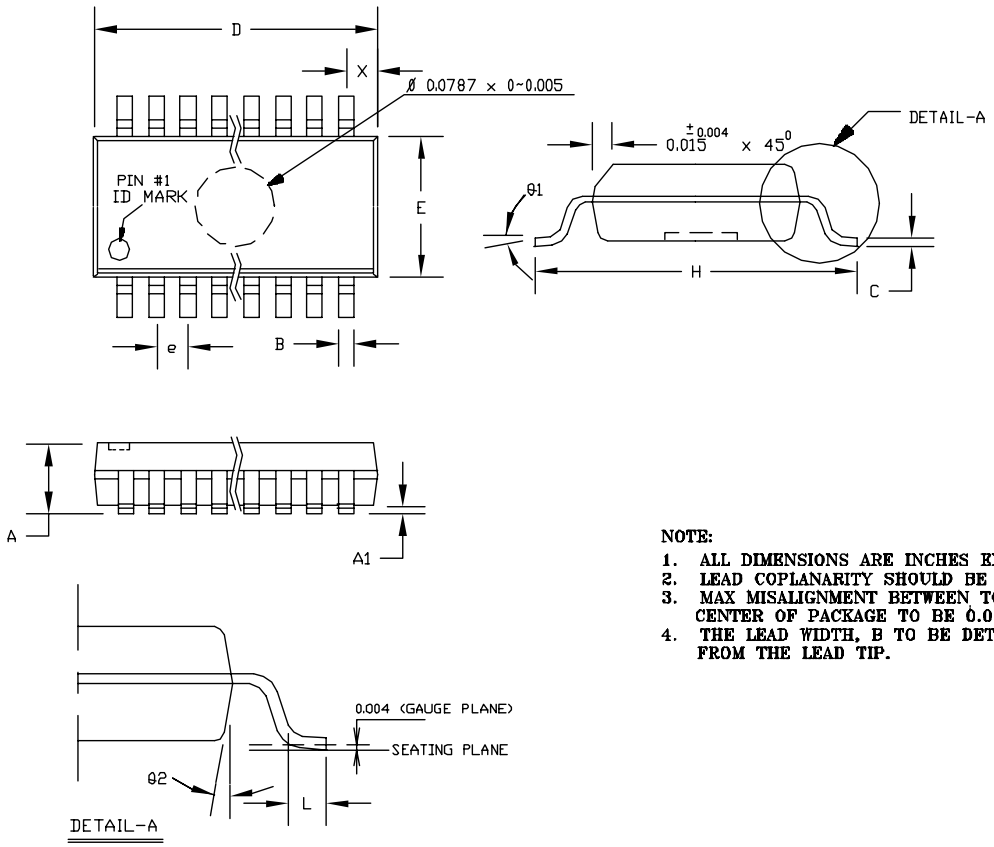
**Table 4. MOSFET and Sense Resistor Vendors**

## Package Information




NOTE:
1. ALL DIMENSIONS ARE IN INCHES [MM].
2. LEAD COPLANARITY SHOULD BE 0.004" [0.10 mm] MAX.
3. MAX MISALIGNMENT BETWEEN TOP AND BOTTOM CENTER OF PACKAGE TO BE 0.004" [0.10 mm].
4. THE LEAD WIDTH, B TO BE DETERMINED AT .0075 [0.19 mm] FROM THE LEAD TIP.
5. BOTTOM MARK IS OPTIONAL, IT MAY NOT APPEAR ON THE ACTUAL UNITS.

**16-Pin QSOP (QS)**




| | MIN | MAX |
|---|---|---|
| A | 0.053 | 0.068 |
| A1 | 0.004 | 0.010 |
| B | 0.008 | 0.012 |
| D | 0.337 | 0.344 |
| E | 0.150 | 0.157 |
| H | 0.229 | 0.244 |
| e | 0.025 BSC | |
| C | 0.007 | 0.009 |
| L | 0.016 | 0.034 |
| X | 0.0575 REF | |
| θ1 | 0° | 8° |
| θ2 | 7° BSC | |

(INCHES)

NOTE:
1. ALL DIMENSIONS ARE INCHES EXCLUDING MOLD FLASH.
2. LEAD COPLANARITY SHOULD BE 0.004" MAX.
3. MAX MISALIGNMENT BETWEEN TOP AND BOTTOM CENTER OF PACKAGE TO BE 0.004".
4. THE LEAD WIDTH, B TO BE DETERMINED AT 0.0075" FROM THE LEAD TIP.

**20-Pin QSOP (QS)**

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http:/www.micrel.com

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