ROHM's Selection Operational Amplifier/Comparator Series

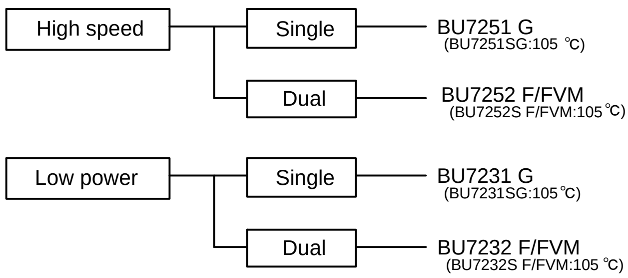
Comparators:
Low Voltage CMOS

BU7251G,BU7251SG,BU7231G,BU7231SG,
BU7252F/FVM,BU7252S F/FVM,BU7232F/FVM,BU7232S F/FVM

No.09049EAT06

●Description

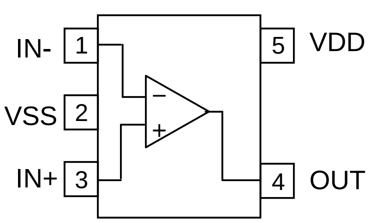
CMOS comparator BU7251/BU7231family and BU7252/BU7232 family are input full swing and push pull output comparator. These ICs integrate one op-amp or two independent op-amps and phase compensation capacitor on a single chip. The features of these ICs are low operating supplyVoltage that is +1.8V to +5.5V(single supply) and low supply current, extremely low input bias current.

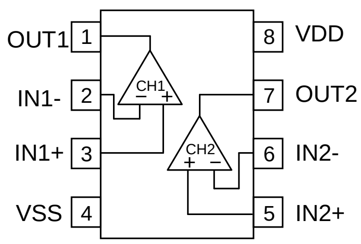


●Features

1) Low operating supply voltage (+1.8[V]～+5.5[V])
2) +1.8 [V]～+5.5[V](single supply)
   ±0.9[V]～±2.75[V](split supply)
3) Input and Output full swing
4) Push-pull output type
5) High speed operation (BU7251 family, BU7252 family)
6) Low supply current (BU7231 family, BU7232 family)
7) Internal ESD protection
   Human body model (HBM) ±4000[V](Typ.)
8) Wide temperature range
   -40[℃]～+85[℃] (BU7251G,BU7252 family, BU7231G, BU7232 family)
   -40[℃]～+105[℃] (BU7251SG,BU7252S family, BU7231SG,BU7232S family)

● Pin Assignments





SSOP5	SOP8	MSOP8
BU7251G	BU7252F	BU7252FVM
BU7251SG	BU7252SF	BU7252SFVM
BU7231G	BU7232F	BU7232FVM
BU7231SG	BU7232SF	BU7232SFVM

●Absolute maximum ratings (Ta=25[℃])

Parameter	Symbol	Rating: BU7251G,BU7252 F/FVM BU7231G,BU7232 F/FVM	Rating: BU7251SG,BU7252S F/FVM BU7231SG,BU7232S F/FVM	Unit
Supply Voltage	VDD-VSS	+7		V
Differential Input Voltage (*1)	Vid	VDD-VSS		V
Input Common-mode voltage range	Vicm	(VSS-0.3) to VDD+0.3		V
Operating Temperature	Topr	-40 to+85	-40 to+105	℃
Storage Temperature	Tstg	-55 to+125		℃
Maximum junction Temperature	Tjmax	+125		℃

Note Absolute maximum rating item indicates the condition which must not be exceeded.
Application of voltage in excess of absolute maximum rating or use out absoluted maximum rated temperature environment may cause deterioration of characteristics.
(*1) The voltage difference between inverting input and non-inverting input is the differential input voltage.Then input terminal voltage is set to more then VEE.

●Electrical characteristics

○BU7251 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature range	Guaranteed Limit BU7251G,BU7251SG Min.	Typ.	Max.	Unit	Condition
Input Offset Voltage (*2)(*4)	Vio	25℃	-	1	11	mV	-
Input Offset Current (*2)	Iio	25℃	-	1	-	pA	-
Input Bias Current (*2)	Ib	25℃	-	1	-	pA	-
Input Common-mode voltage Range	Vicm	25℃	0	-	3	V	(VDD-VSS)=3[V]
Large Signal Voltage Gain	AV	25℃	-	90	-	dB	RL=10[kΩ]
Supply current(*4)	IDD	25℃	-	15	35	μA	RL=∞
		full range	-	-	50		
Power supply rejection ratio	PSRR	25℃	-	80	-	dB	-
Common-mode rejection ratio	CMRR	25℃	-	80	-	dB	-
Output source current (*3)	IOH	25℃	1	2	-	mA	VDD-0.4
Output sink current (*3)	IOL	25℃	3	6	-	mA	VSS+0.4
High Level Output Voltage (*4)	VOH	25℃	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage (*4)	VOL	25℃	-	-	VSS+0.1	V	RL=10[kΩ]
Output rise time	Tr	25℃	-	50	-	ns	CL=15pF 100mV over drive
Output fall time	Tf	25℃	-	20	-	ns	CL=15pF 100mV over drive
Propagation delay L to H	TPLH	25℃	-	0.55	-	μs	CL=15pF 100mV over drive
Propagation delay H to L	TPHL	25℃	-	0.25	-	μs	CL=15pF 100mV over drive

(*2) Abusolute values
(*3) Reference to power dissipation under the high temperature environment and decide the output current.
Continuous short circuit is occurring the degenerate of output current characteristics.
(*4) Full range BU7251 : Ta=-40[℃] to +85[℃] BU7251S : Ta=-40[℃] to +105[℃]

○BU7252 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature range	Guaranteed Limit BU7252 F/FVM BU7252S F/FVM Min.	Typ.	Max.	Unit	Condition
Input Offset Voltage (*2)(*4)	Vio	25℃	-	1	11	mV	-
Input Offset Current (*2)	Iio	25℃	-	1	-	pA	-
Input Bias Current (*2)	Ib	25℃	-	1	-	pA	-
Input Common-mode voltage Range	Vicm	25℃	0	-	3	V	(VDD-VSS)=3[V]
Large Signal Voltage Gain	AV	25℃	-	90	-	dB	RL=10[kΩ]
Supply current(*4)	IDD	25℃	-	35	65	μA	RL=∞
		full range	-	-	80		
Power supply rejection ratio	PSRR	25℃	-	80	-	dB	-
Common-mode rejection ratio	CMRR	25℃	-	80	-	dB	-
Output source current (*3)	IOH	25℃	1	2	-	mA	VDD-0.4
Output sink current (*3)	IOL	25℃	3	6	-	mA	VSS+0.4
High Level Output Voltage (*4)	VOH	25℃	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage (*4)	VOL	25℃	-	-	VSS+0.1	V	RL=10[kΩ]
Output rise time	Tr	25℃	-	50	-	ns	CL=15pF 100mV over drive
Output fall time	Tf	25℃	-	20	-	ns	CL=15pF 100mV over drive
Propagation delay L to H	TPLH	25℃	-	0.55	-	μs	CL=15pF 100mV over drive
Propagation delay H to L	TPHL	25℃	-	0.25	-	μs	CL=15pF 100mV over drive

(*2) Abusolute values
(*3) Reference to power dissipation under the high temperature environment and decide the output current.
Continuous short circuit is occurring the degenerate of output current characteristics.
(*4) Full range BU7251,BU7252 : Ta=-40[℃] to +85[℃] BU7251S,BU7252S : Ta=-40[℃] to +105[℃]

○BU7231 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature range	Guaranteed Limit BU7231G,BU7231SG			Unit	Condition
			Min.	Typ.	Max.		
Input Offset Voltage (*5)	Vio	25℃	-	1	11	mV	-
Input Offset Current (*5)	Iio	25℃	-	1	-	pA	-
Input Bias Current (*5)	Ib	25℃	-	1	-	pA	-
Input Common-mode voltage Range	Vicm	25℃	0	-	3	V	(VDD-VSS)=3[V]
Large Signal Voltage Gain	AV	25℃	-	90	-	dB	RL=10[kΩ]
Supply current	IDD	25℃	-	5	15	μA	RL=∞
		full range	-	-	30		
Power supply rejection ratio	PSRR	25℃	-	80	-	dB	-
Common-mode rejection ratio	CMRR	25℃	-	80	-	dB	-
Output source current (*6)	IOH	25℃	1	2	-	mA	VDD-0.4
Output sink current (*6)	IOL	25℃	3	6	-	mA	VSS+0.4
High Level Output Voltage (*7)	VOH	25℃	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage (*7)	VOL	25℃	-	-	VSS+0.1	V	RL=10[kΩ]
Output rise time	Tr	25℃	-	50	-	ns	CL=15pF 100mV over drive
Output fall time	Tf	25℃	-	20	-	ns	CL=15pF 100mV over drive
Propagation delay L to H	TPLH	25℃	-	1.7	-	μs	CL=15pF 100mV over drive
Propagation delay H to L	TPHL	25℃	-	0.5	-	mV	CL=15pF 100mV over drive

(*5) Abusolute values
(*6) Reference to power dissipation under the high temperature environment and decide the output current.
Continuous short circuit is occurring the degenerate of output current characteristics.
(*7) Full range BU7231：Ta=-40[℃] to +85[℃] BU7231S,BU7232S：Ta=-40[℃] to +105[℃]

○BU7232 family (Unless otherwise specified VDD=+3[V], VSS=0[V], Ta=25[℃])

Parameter	Symbol	Temperature range	Guaranteed Limit BU7232F/FVM BU7232S F/FVM			Unit	Condition
			Min.	Typ.	Max.		
Input Offset Voltage (*5)	Vio	25℃	-	1	11	mV	-
Input Offset Current (*5)	Iio	25℃	-	1	-	pA	-
Input Bias Current (*5)	Ib	25℃	-	1	-	pA	-
Input Common-mode voltage Range	Vicm	25℃	0	-	3	V	(VDD-VSS)=3[V]
Large Signal Voltage Gain	AV	25℃	-	90	-	dB	RL=10[kΩ]
Supply current	IDD	25℃	-	10	25	μA	RL=∞
		full range	-	-	50		
Power supply rejection ratio	PSRR	25℃	-	80	-	dB	-
Common-mode rejection ratio	CMRR	25℃	-	80	-	dB	-
Output source current (*6)	IOH	25℃	1	2	-	mA	VDD-0.4
Output sink current (*6)	IOL	25℃	3	6	-	mA	VSS+0.4
High Level Output Voltage (*7)	VOH	25℃	VDD-0.1	-	-	V	RL=10[kΩ]
Low Level Output Voltage (*7)	VOL	25℃	-	-	VSS+0.1	V	RL=10[kΩ]
Output rise time	Tr	25℃	-	50	-	ns	CL=15pF 100mV over drive
Output fall time	Tf	25℃	-	20	-	ns	CL=15pF 100mV over drive
Propagation delay L to H	TPLH	25℃	-	1.7	-	μs	CL=15pF 100mV over drive
Propagation delay H to L	TPHL	25℃	-	0.5	-	mV	CL=15pF 100mV over drive

(*5) Abusolute values
(*6) Reference to power dissipation under the high temperature environment and decide the output current.
Continuous short circuit is occurring the degenerate of output current characteristics.
(*7) Full range,BU7232：Ta=-40[℃] to +85[℃] BU7232S：Ta=-40[℃] to +105[℃]

● Example of electrical characteristics

○ BU7251 family

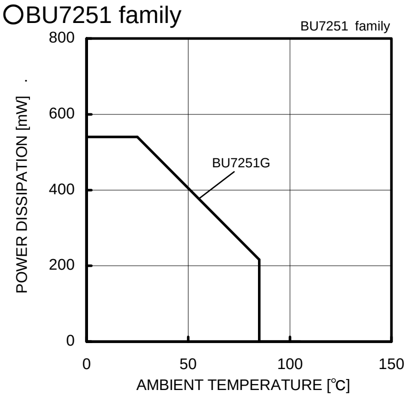


Fig. 1
Derating Curve

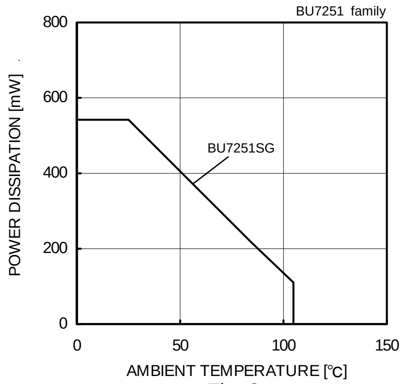


Fig. 2
Derating Curve

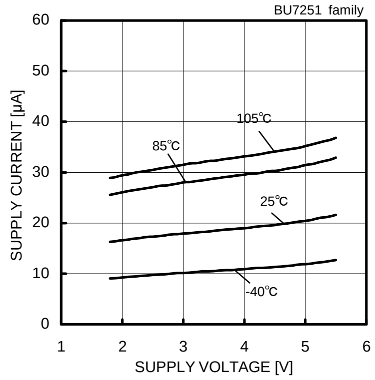


Fig. 3
Supply Current – Supply Voltage

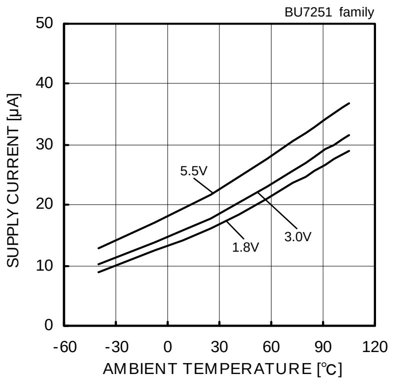


Fig. 4
Supply Current – Ambient Temperature

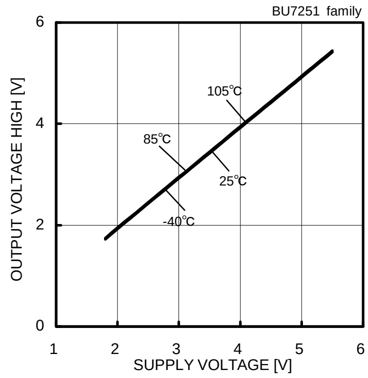


Fig. 5
Output Voltage High – Supply Voltage
(RL=10[kΩ])

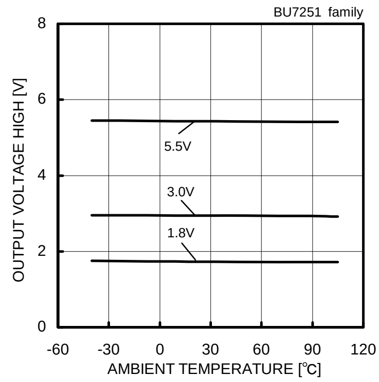


Fig. 6
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

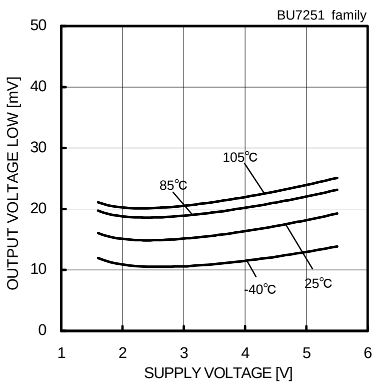


Fig. 7
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

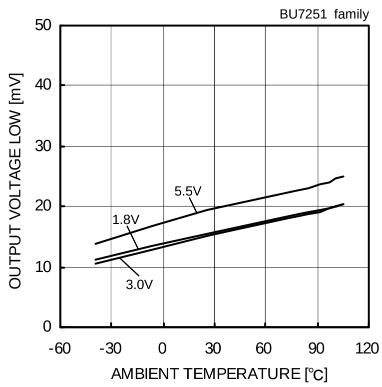


Fig. 8
Output Voltage Low – Ambient Temperature(RL=10[kΩ])

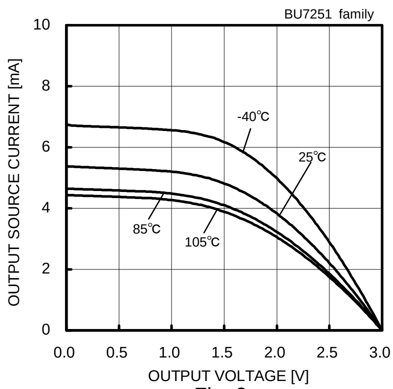


Fig. 9
Output Source Current – Supply Voltage(VDD=3[V])

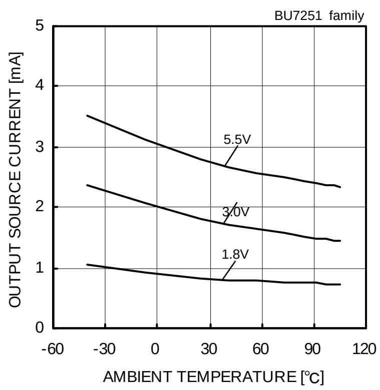


Fig. 10
Output Source Current – Ambient Temperature
(VOUT=VDD-0.4[V])

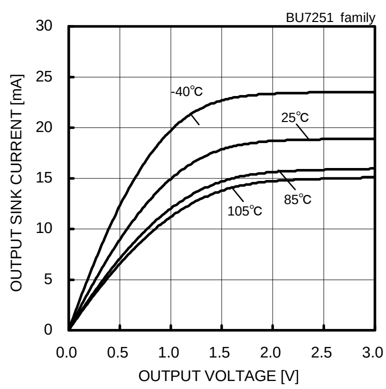


Fig. 11
Output Sink Current – Output Voltage
(VDD=3[V])

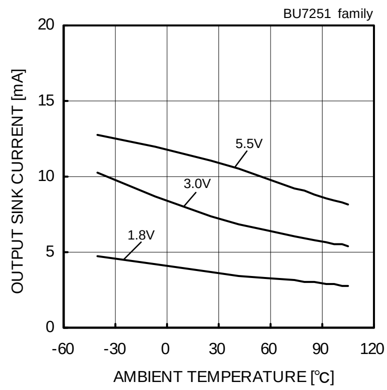


Fig. 12
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*) The above date is ability value of sample, it is not guaranteed. BU7251G : -40[℃] to+85[℃] BU7251SG : -40[℃] to+105[℃]

○BU7251 family

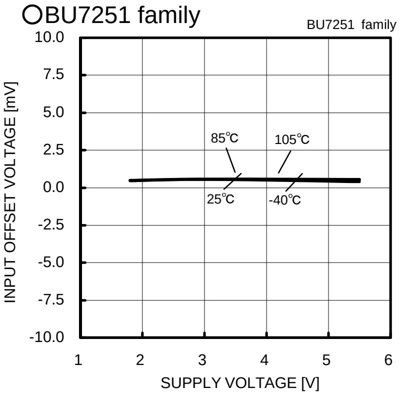


Fig. 13

Input Offset Voltage – Supply Voltage
(Vicm=VDD, Vout=0.1[V])

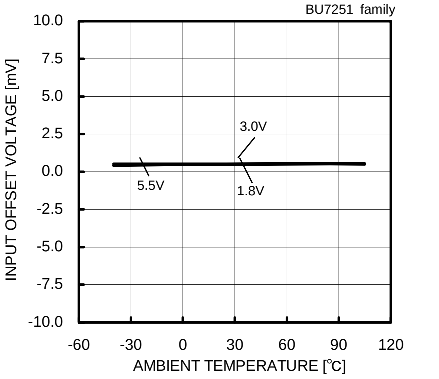


Fig. 14

Input Offset Voltage – Ambient Temperature
(Vicm=VDD, Vout=0.1[V])

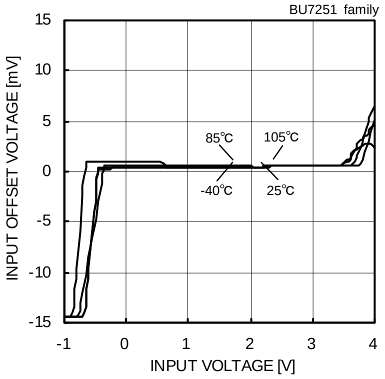


Fig. 15

Input offset voltage – Input Voltage
(VDD=3[V])

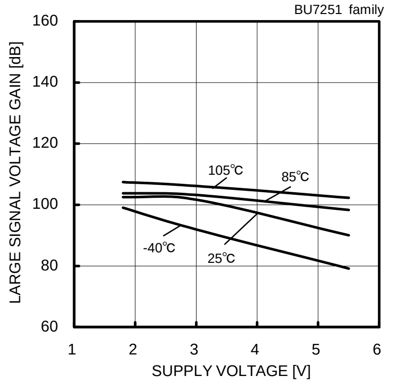


Fig. 16

Large Signal Voltage Gain – Supply Voltage

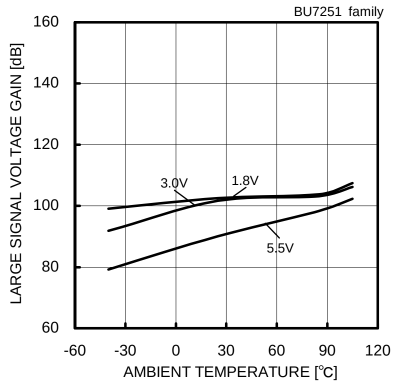


Fig. 17

Large Signal Voltage Gain
– Ambient Temperature

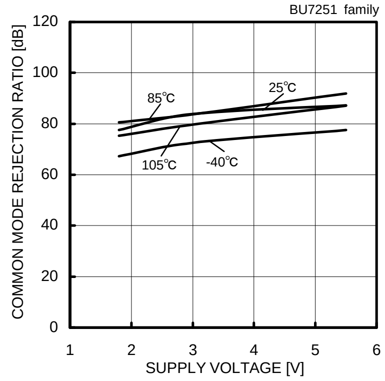


Fig. 18

Common Mode rejection Ratio
– Supply Voltage(VDD=3[V])

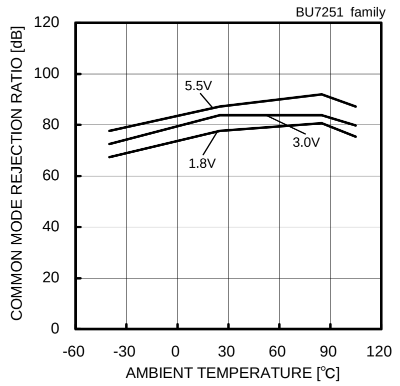


Fig. 19

Common Mode Rejection Ratio –
Ambient Temperature
(VDD=3[V])

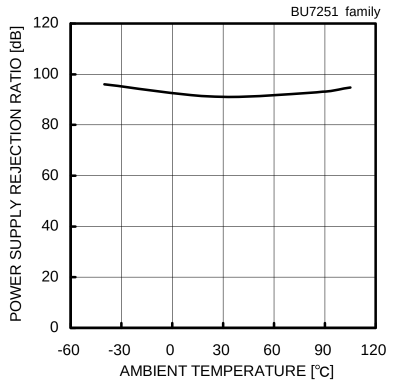


Fig. 20

Power Supply Rejection –
Ambient Temperature

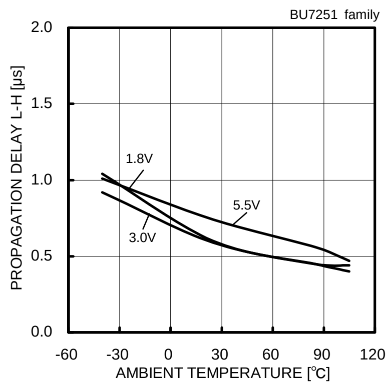


Fig. 21

Propagation Delay L-H –
Ambient Temperature

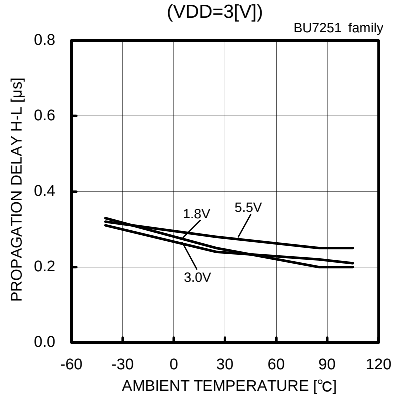


Fig. 22

Propagation Delay H-L – Ambient Temperature

(*) The above date is ability value of sample, it is not guaranteed. BU7251G：-40[℃] to+85[℃] BU7251SG：-40[℃] to+105[℃]

○BU7252 family

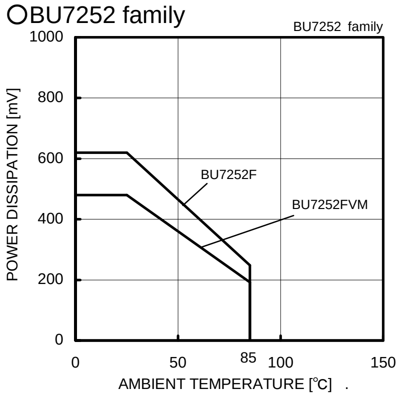


Fig. 23
Derating Curve

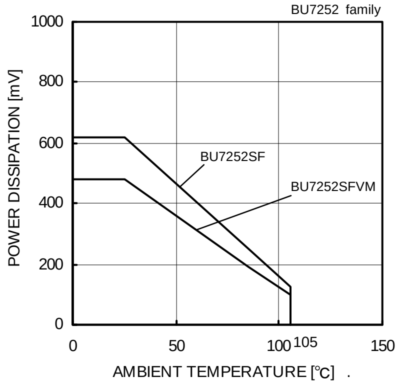


Fig. 24
Derating Curve

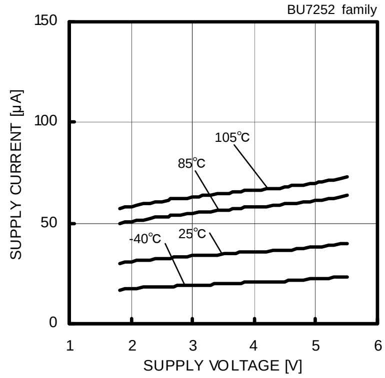


Fig. 25
Supply Current – Supply Voltage

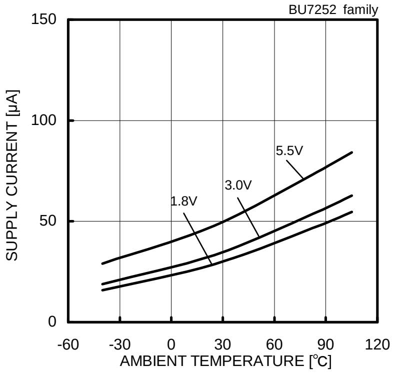


Fig. 26
Supply Curreny – Ambient Temperature

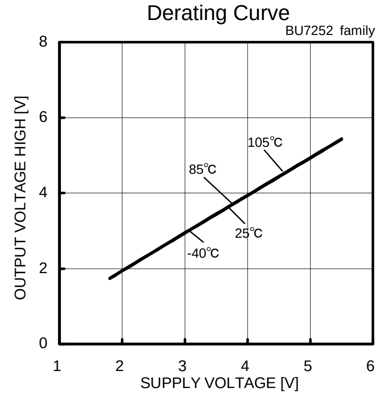


Fig. 27
Output Voltage High – Supply Voltage
(RL=10[kΩ])

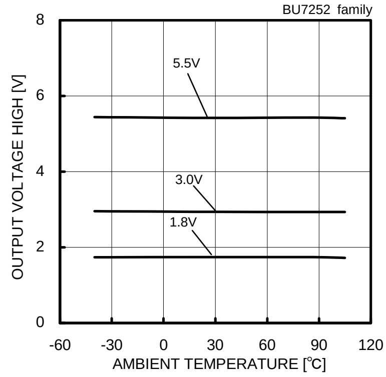


Fig. 28
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

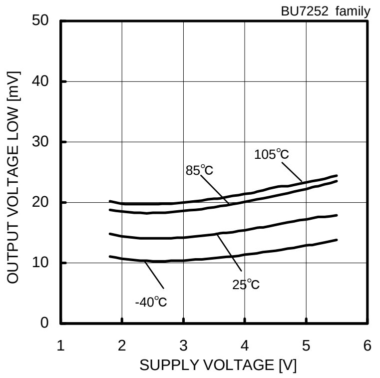


Fig. 29
Output Voltage Low – Supply Voltage(RL=10[kΩ])

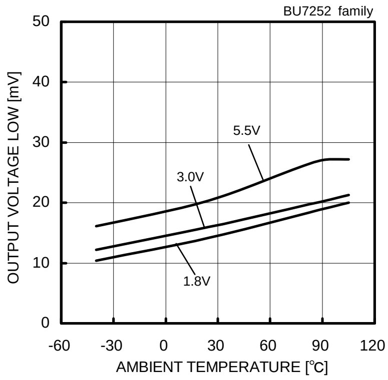


Fig. 30
Output Voltage Low – Ambient Temperature(RL=10[kΩ])

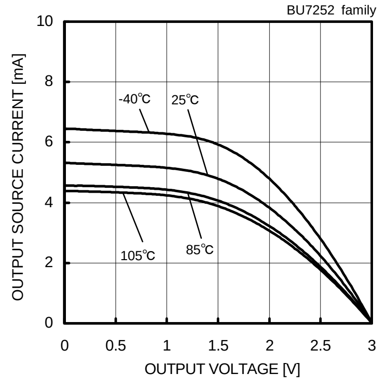


Fig. 31
Output Source Current – Output Voltage(VDD=3[V])

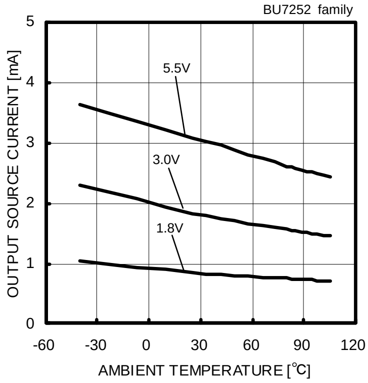


Fig. 32
Output Source Current – Ambient Temperature
(VOUT=VDD-0.4[V])

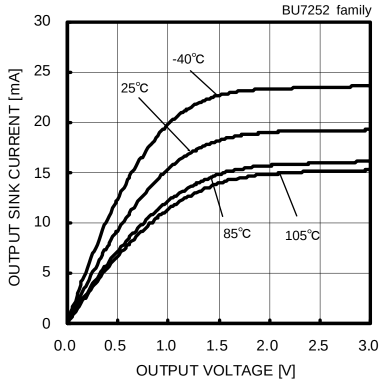


Fig. 33
Output Sink Current – Output Voltage
(VDD=3[V])

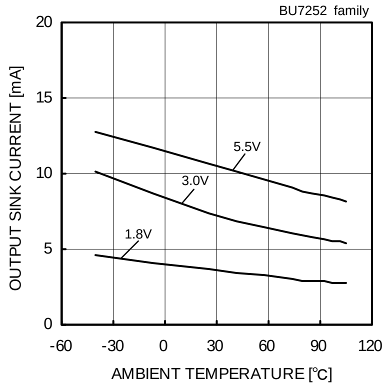


Fig. 34
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*) The above date is ability value of sample, it is not guaranteed.　BU7252 F/FVM：-40[℃] to+85[℃]　BU7252S F/FVM：-40[℃] to+105[℃]

○BU7252 family

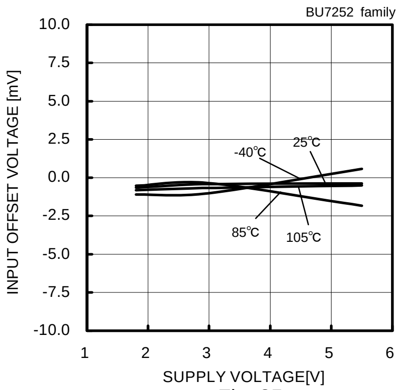


Fig. 35
Input Offset Voltage – Supply Voltage
(Vicm=VDD,VOUT=0.1[V])

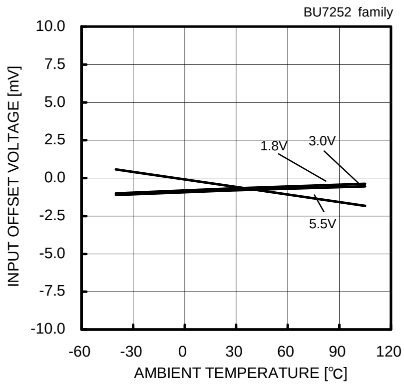


Fig. 36
Input Offset Voltage – Ambient Temperature
(Vicm=VDD,VOUT=0.1[V])

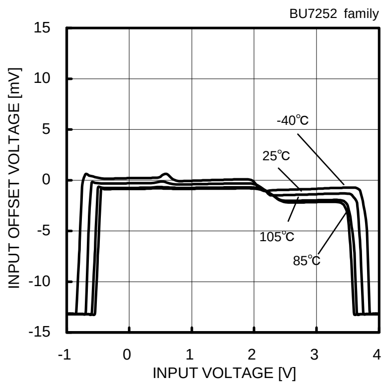


Fig. 37
Input Offset Voltage – Input Voltage
(VDD=3[V])

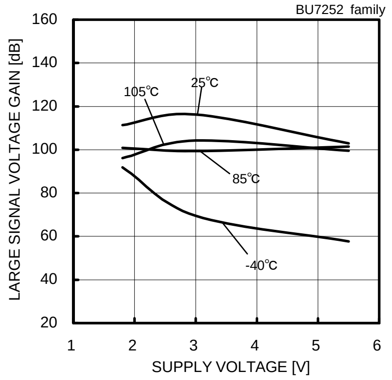


Fig. 38
Large Signal Voltage Gain – Supply Voltage

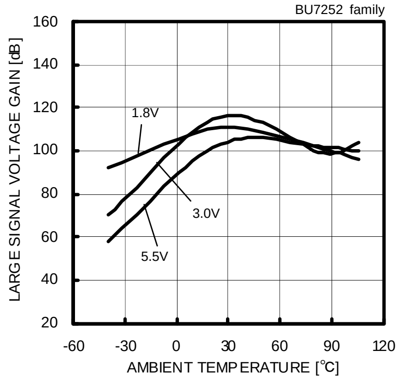


Fig. 39
Large Signal Voltage Gain
– Ambient Temperature

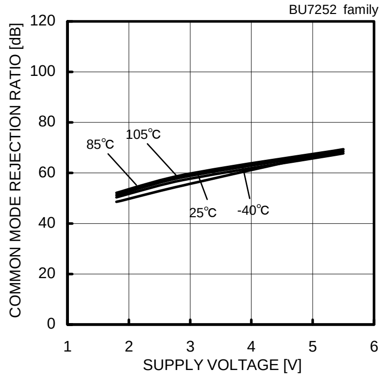


Fig. 40
Common Mode Rejection Ratio
– Supply Voltage (VDD=3[V])

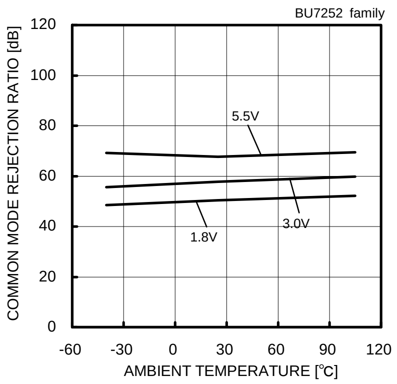


Fig. 41
Common Mode Rejection – Ambient Temperature (VDD=3[V])

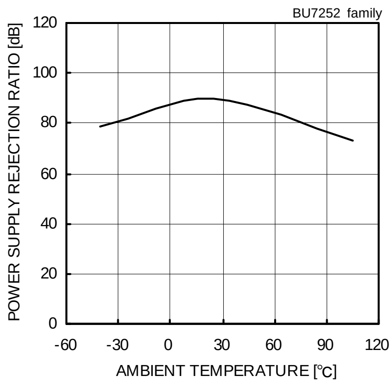


Fig. 42
Power Supply Rejection Ratio – Ambient Temperature

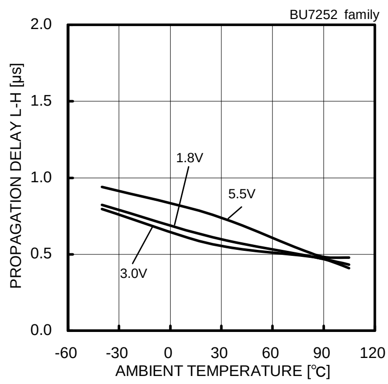


Fig. 43
Propagation Delay L-H – Ambient Temperature

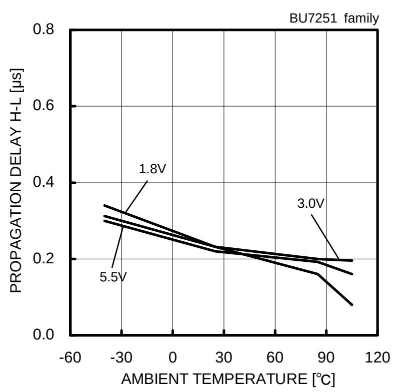


Fig. 44
Propagation Delay H-L – Ambient Temperature

(*) The above date is ability value of sample, it is not guaranteed. BU7252 F/FVM：-40[℃] to+85[℃] BU7252S F/FVM：-40[℃] to+105[℃]

5.5V

○BU7231 series

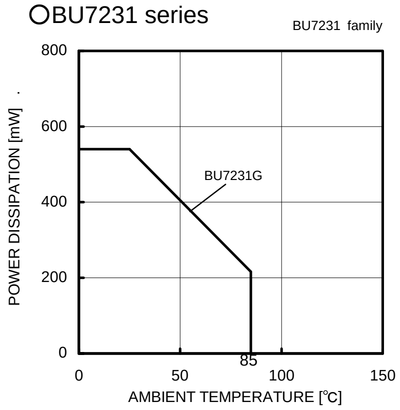


Fig. 45
Derating Curve

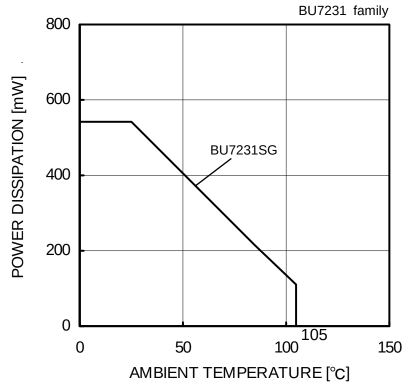


Fig. 46
Derating Curve

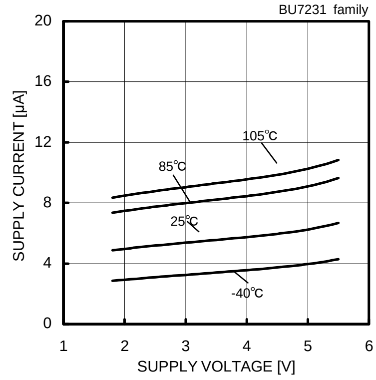


Fig. 47
Supply Current – Supply Voltage

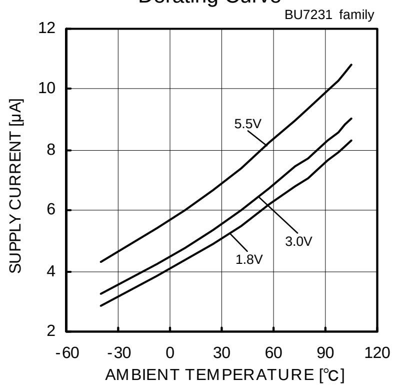


Fig. 48
Supply Current – Ambient Temperature

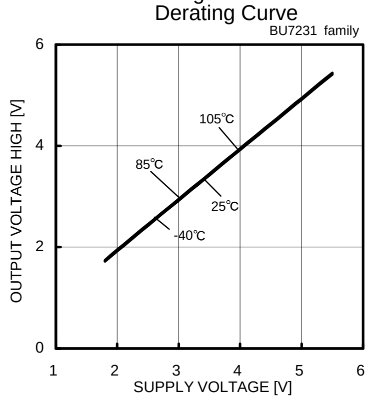


Fig. 49
Output Voltage – Supply Voltage
(RL=10[kΩ])

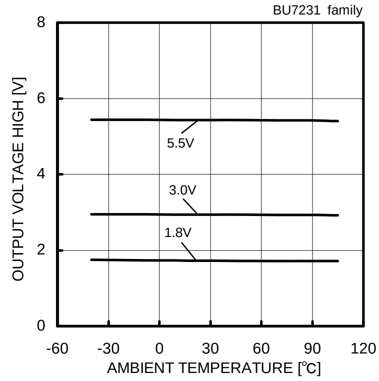


Fig. 50
Output Voltage High – Ambient Temperature
(RL=10[kΩ])

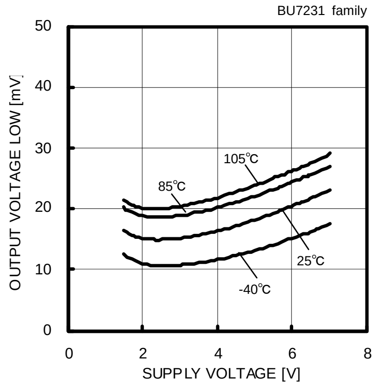


Fig. 51
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

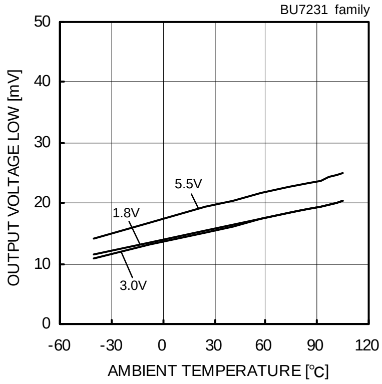


Fig. 52
Output Voltage Low – Ambient Temperature
(RL=10[kΩ])

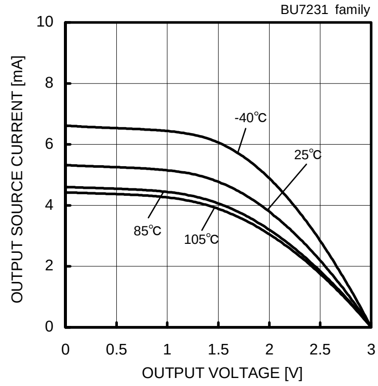


Fig. 53
Output Source Current – Output Voltage
(VDD=3[V])

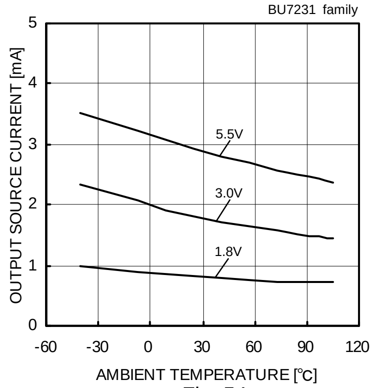


Fig. 54
Output Source Current – Ambient Temperature
(VOUT=VDD-0.4[V])

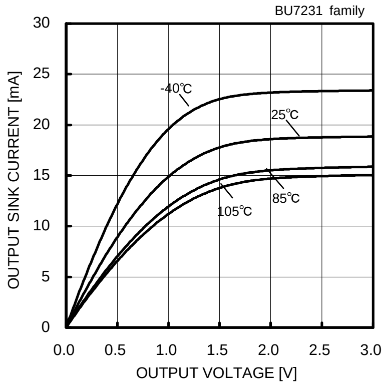


Fig. 55
Output Sink Current – Output Voltage
(VDD=3[V])

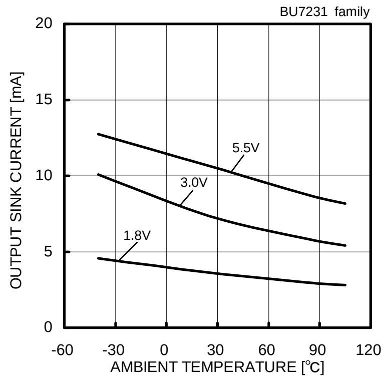


Fig. 56
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*) The above date is ability value of sample, it is not guaranteed. BU7231G：-40[℃] to+85[℃] BU7231SG：-40[℃] to+105[℃]

○BU7231 series

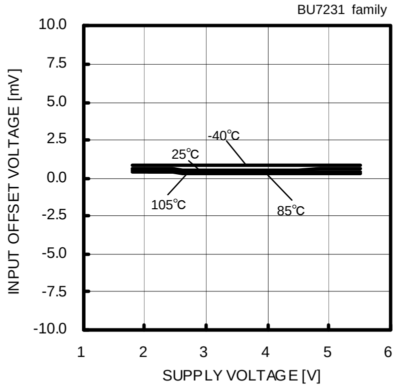


Fig. 57
Input Offset Voltage – Supply Voltage
(Vicm=VDD, Vout=0.1[V])

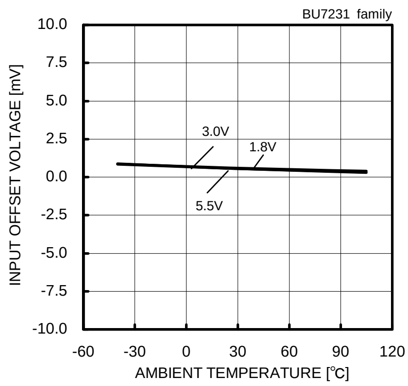


Fig. 58
Input Offset Voltage – Ambient Temperature
(Vicm=VDD, Vout=0.1[V])

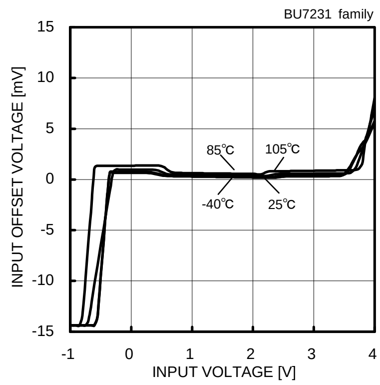


Fig. 59
Input Offset Voltage – Input Voltage
(VDD=3[V])

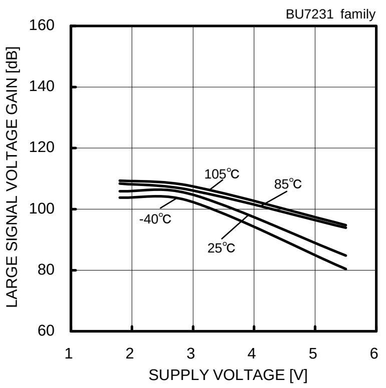


Fig. 60
Large Signal Voltage Gain – Supply Voltage

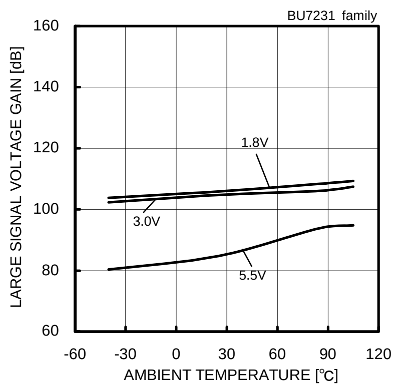


Fig. 61
Large Signal Voltage Gain
– Ambient Temperature

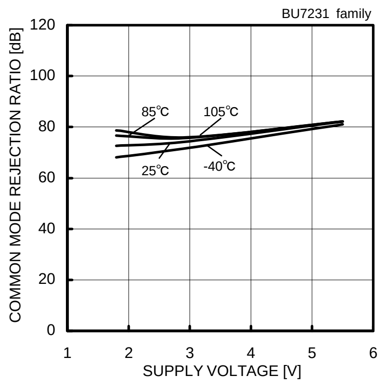


Fig. 62
Common Mode Rejection Ratio
– Supply Voltage (VDD=3[V])

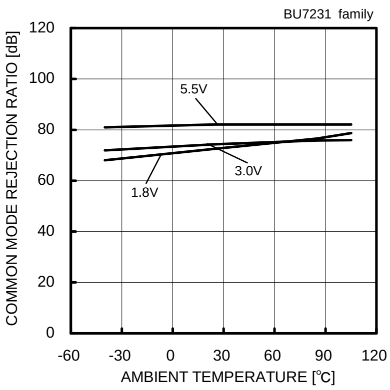


Fig. 63
Common Mode Rejection Ratio
– Ambient Temperature (VDD=3[V])

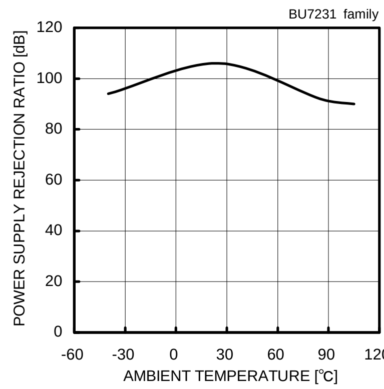


Fig. 64
Power Supply Rejection Ratio
– Ambient Temperature

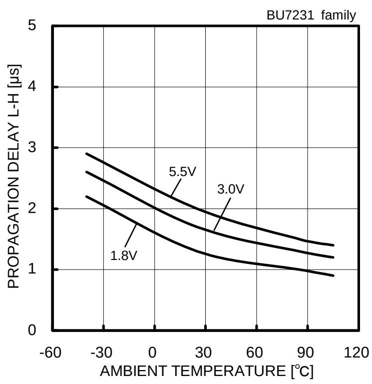


Fig. 65
Propagation Delay L-H
– Ambient Temperature

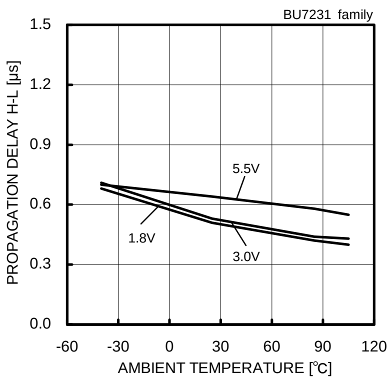


Fig. 66
Propagation Delay H-L– Ambient Temperature

(*) The above date is ability value of sample, it is not guaranteed. BU7231G：-40[℃] to+85[℃] BU7231SG：-40[℃] to+105[℃]

○BU7232 family

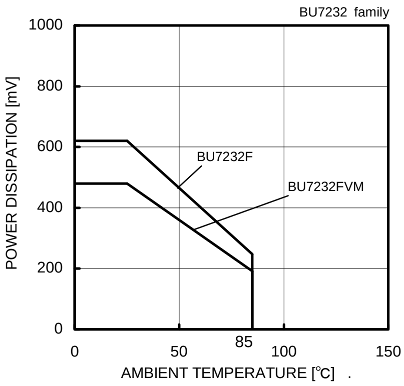


Fig. 67
Derating Curve

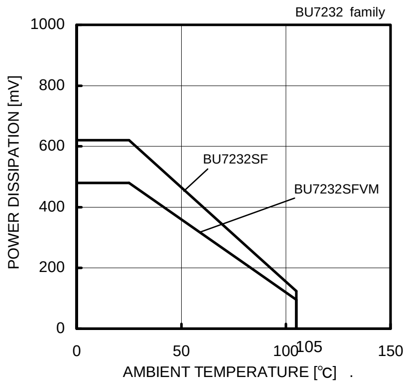


Fig. 68
Derating Curve

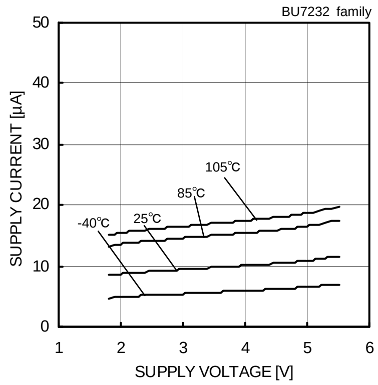


Fig. 69
Supply Current – Supply Voltage

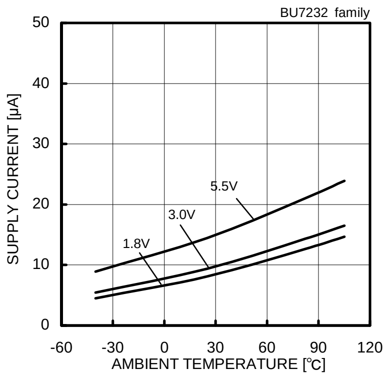


Fig. 70
Supply Current – Ambient emperature

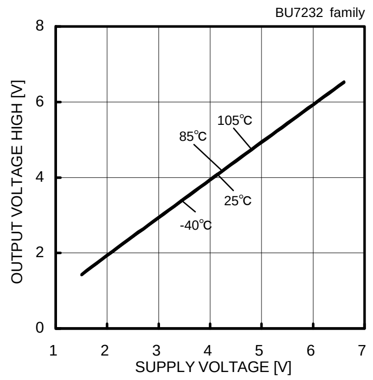


Fig. 71
Output Voltage High – Supply Voltage
(RL=10[kΩ])

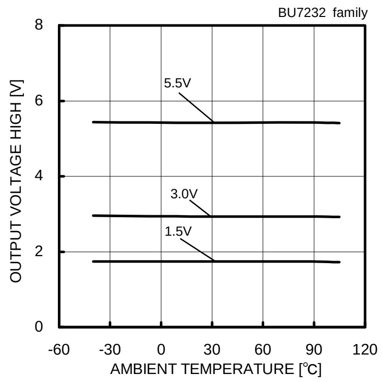


Fig. 72
Output Voltage – Ambient Temperature
(RL=10[kΩ])

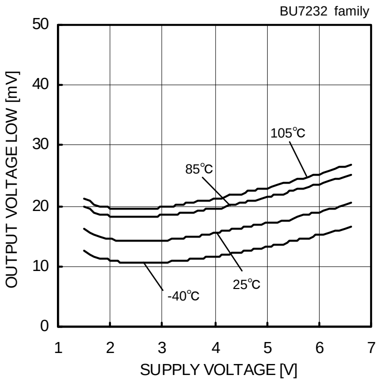


Fig. 73
Output Voltage Low – Supply Voltage
(RL=10[kΩ])

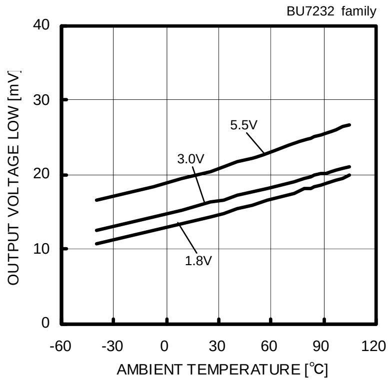


Fig. 74
Output Voltage Low – Ambient temperature
(RL=10[kΩ])

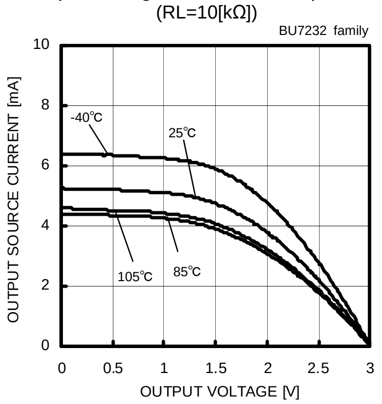


Fig. 75
Output Source Current – Output Voltage
(VDD=3[V])

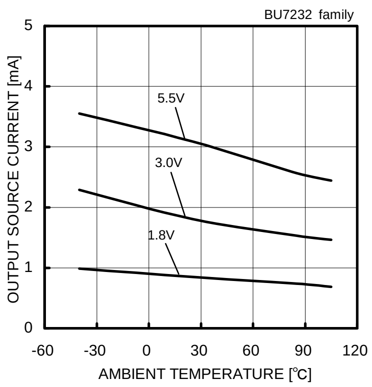


Fig. 76
Output Source Current – Ambient Temperature
(VOUT=VDD-0.4[V])

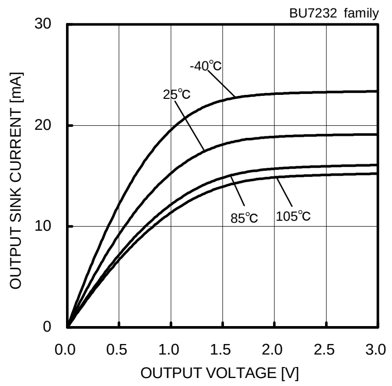


Fig. 77
Output Sink Current – Output Voltage
(VDD=3[V])

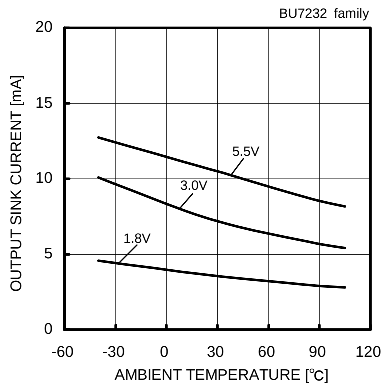


Fig. 78
Output Sink Current – Ambient Temperature
(VOUT=VSS+0.4[V])

(*) The above date is ability value of sample, it is not guaranteed. BU7232 F/FVM：-40[℃] to+85[℃] BU7232S F/FVM：-40[℃] to+105[℃]

○BU7232 family

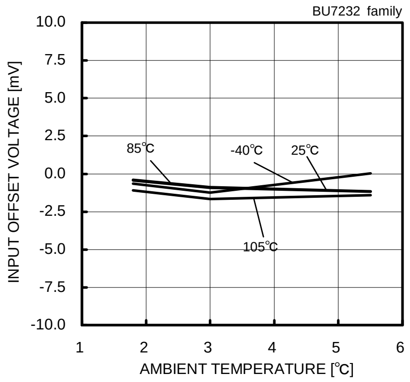


Fig. 79
Input Offset Voltage – Ambient Temperature
(Vicm=VDD, VOUT=0.1[V])

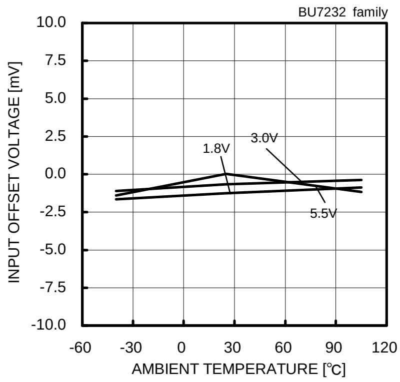


Fig. 80
Input Offset Voltage – Ambient Temperature
(Vicm=VDD, VOUT=0.1[V])

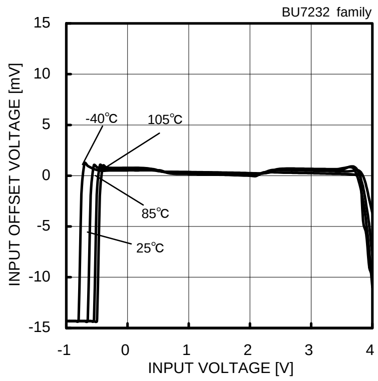


Fig. 81
Input Offset Voltage – Input Voltage
(VDD=3[V])

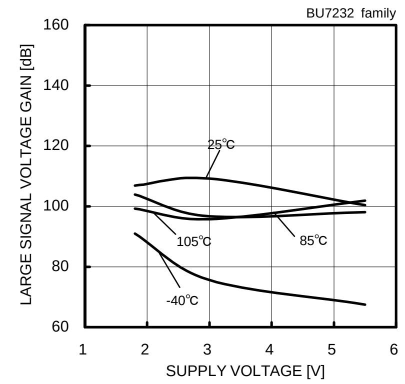


Fig. 82
Large Signal Voltage Gain - Supply Voltage

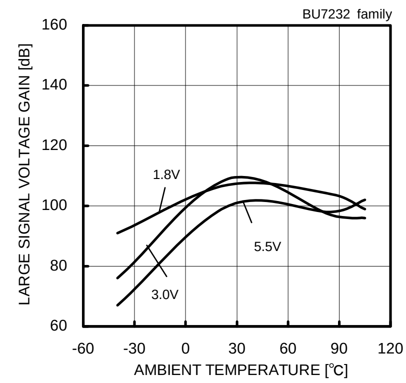


Fig. 83
Large Signal Voltage Gain
- Ambient Temperature

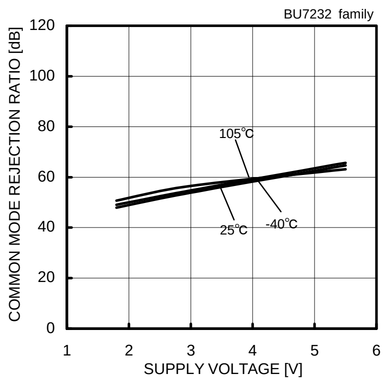


Fig. 84
Common Mode Rejection Ratio
– Supply Voltage (VDD=3[V])

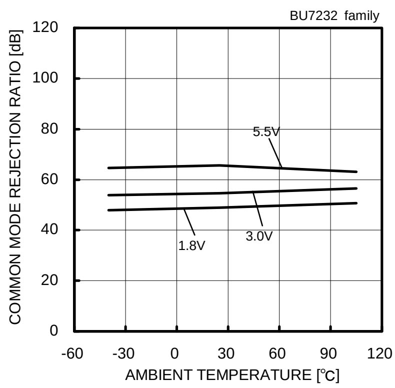


Fig. 85
Common Mode Rejection Ratio –
Ambient Temperature (VDD=3[V])

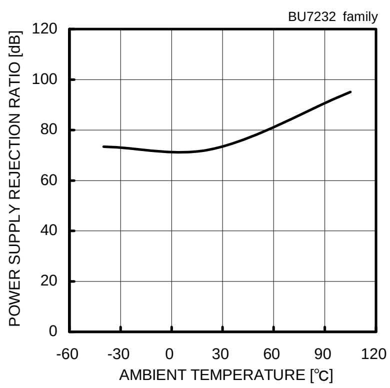


Fig. 86
Power Supply Rejection Ratio
– Ambient Temperature

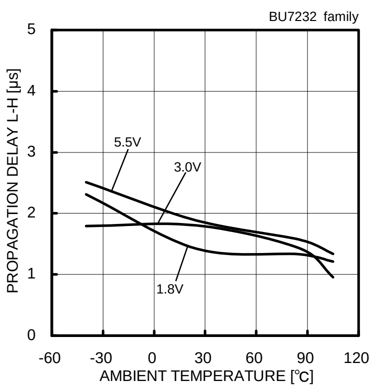


Fig. 87
Propagation Delay L-H – Ambient temperature

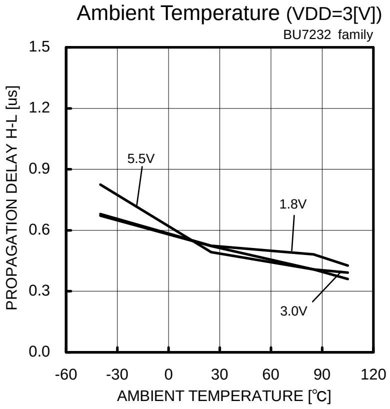


Fig. 88
Propagation Delay H-L – Ambient Temperature

(*) The above date is ability value of sample, it is not guaranteed. BU7232 F/FVM：-40[℃] to+85[℃] BU7232S F/FVM：-40[℃] to+105[℃]

●Schematic diagram

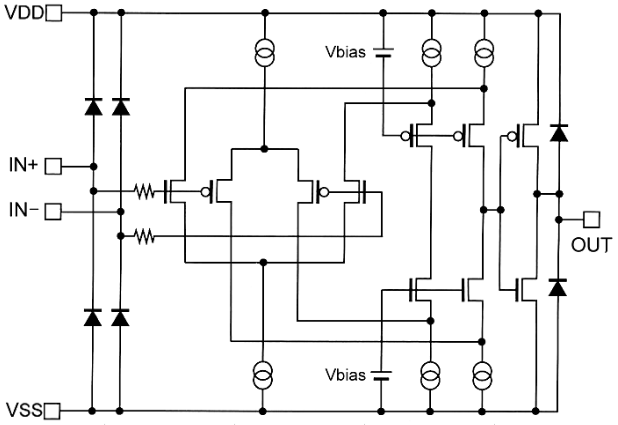


Fig. 89 Simplified schematic

●Test circuit1 NULL method

VDD,VSS,EK,Vicm, Unit : [V]

Parameter	VF	S1	S2	S3	VDD	VSS	EK	Vicm	Calculation
Input offset voltage	VF1	ON	ON	OFF	3	0	-0.1	0.3	1
Large signal voltage gain	VF2	ON	ON	ON	3	0	-0.3	0.3	2
	VF3						-2.7		
Common-mode rejection ratio (Input common-mode voltage range)	VF4	ON	ON	OFF	3	0	-0.1	0	3
	VF5							3	
Power supply rejection ratio	VF6	ON	ON	OFF	1.8	0	-0.1	0.3	4
	VF7				5.5				

-Calculation-

1. Input offset Voltage (Vio) $Vio = \frac{|VF1|}{1+Rf/Rs}$ [V]

2. Large signal voltage gain (Av) $Av = 20Log \frac{2.4\times(1+Rf/Rs)}{|VF2-VF3|}$ [dB]

3. Common-mode rejection ratio (CMRR) $CMRR = 20Log \frac{3\times(1+Rf/Rs)}{|VF4-VF5|}$ [dB]

4. Power supply rejection ratio (PSRR) $PSRR = 20Log \frac{3.7\times(1+Rf/Rs)}{|VF6-VF7|}$ [dB]

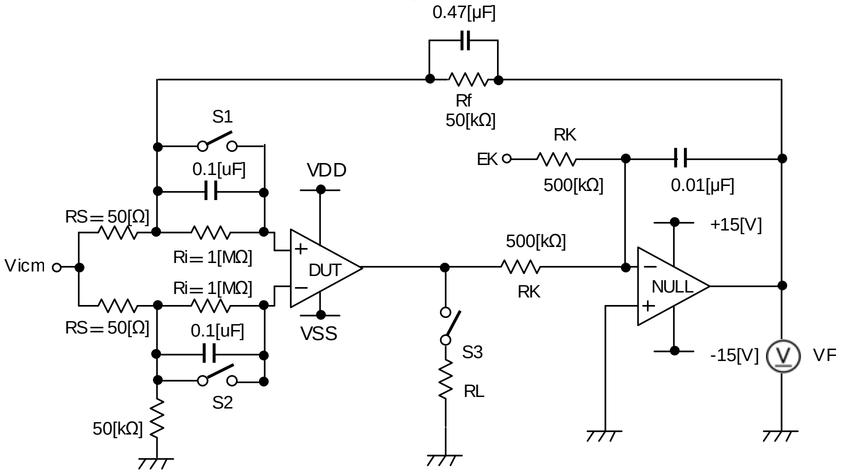


Fig. 90 Test Circuit 1 (one channel only)

●Test circuit2 switch condition

Unit : [V]

SW No.	SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	SW 8
supply current	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF
maximum output voltage RL=10 [kΩ]	OFF	ON	ON	ON	OFF	OFF	ON	OFF
output current	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
response time	ON	OFF	ON	OFF	ON	OFF	OFF	ON

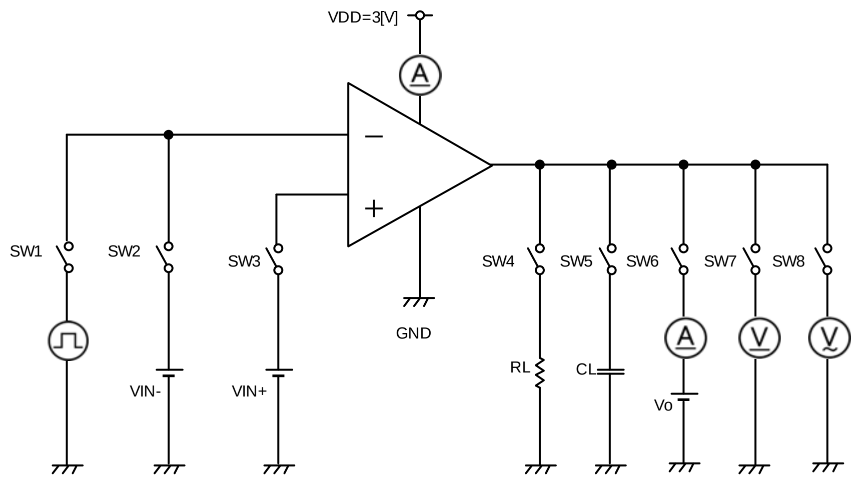


Fig. 91 Test circuit2 (one channel only)

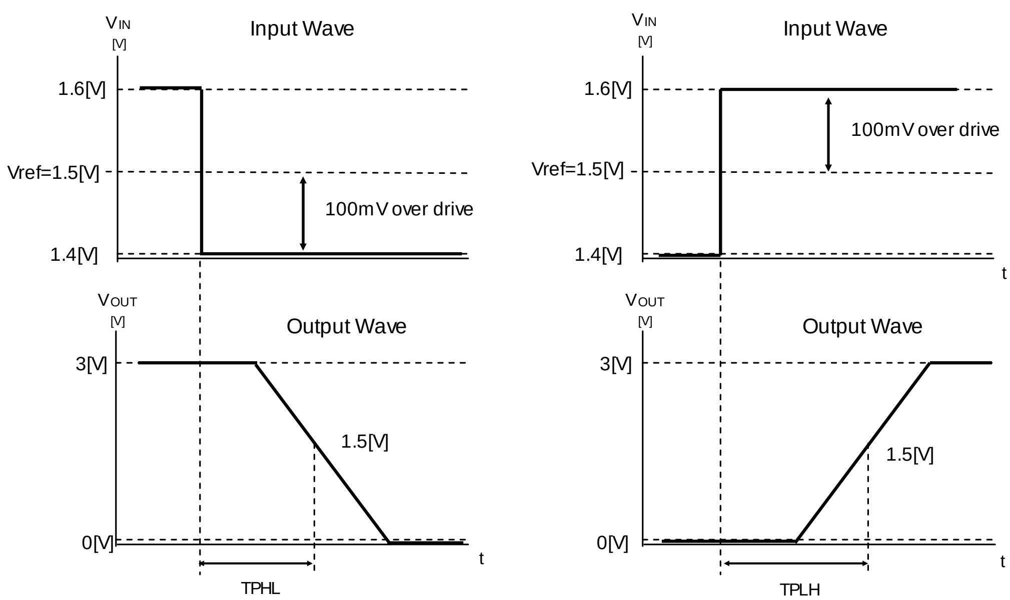


Fig. 92 Slew rate input output wave

●Description of electrical characteristics

Described here are the terms of electric characteristics used in this technical note. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacture's document or general document.

1. Absolute maximum ratings

Absolute maximum rating item indicates the condition which must not be exceeded. Application of voltage in excess of absolute Maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

1.1 Power supply voltage(VDD/VSS)

Indicates the maximum voltage that can be applied between the positive power supply terminal and negative power supply terminal without deterioration or destruction of characteristics of internal circuit.

1.2 Differential input voltage (Vid)

Indicates the maximum voltage that can be applied between non-inverting terminal and inverting terminal without deterioration and destruction of characteristics of IC.

1.3 Input common-mode voltage range (Vicm)

Indicates the maximum voltage that can be applied to non-inverting terminal and inverting terminal without deterioration or destruction of characteristics. Input common-mode voltage range of the maximum ratings not assure normal operation of IC. When normal operation of IC is desired, the input common-mode voltage of characteristics item must be followed.

1.4 Power dissipation (Pd)

Indicates the power that can be consumed by specified mounted board at the ambient temperature 25℃(normal temperature). As for package product, Pd is determined by the temperature that can be permitted by IC chip in the package(maximum junction temperature) and thermal resistance of the package

2. Electrical characteristics item

2.1 Input offset voltage (Vio)

Indicates the voltage difference between non-inverting terminal and inverting terminal.
It can be translated into the input voltage difference required for setting the output voltage at 0 [V]

2.2 Input offset current (Iio)

Indicates the difference of input bias current between non-inverting terminal and inverting terminal.

2.3 Input bias current (Ib)

Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias current at non-inverting terminal and input bias current at inverting terminal.

2.4 Input common-mode voltage range (Vicm)

Indicates the input voltage range where IC operates normally.

2.5 Large signal voltage gain (AV)

Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.
Av = (Output voltage fluctuation) / (Input offset fluctuation)

2.6 Circuit current (ICC)

Indicates the IC current that flows under specified conditions and no-load steady status.

2.7 Output sink current　(OL)

Indicates the maximum current that can be output under specified output condition (such as output voltage and load condition).

2.8 Output saturation voltage, Low level output voltage (VOL)

Indicates the voltage range that can be output under specified load conditions.

2.9 Output leakage current, High level output current(I leak)

Indicates the current that flows into IC under specified input and output conditions.

2.10 Response Time (Tre)

The interval between the application of an input and output condition.

2.11 Common-mode rejection ratio (CMRR)

Indicates the ratio of fluctuation of input offset voltage when in-phase input voltage is changed. It is normally the fluctuation of DC.
CMRR ＝(Change of Input common-mode voltage)/(Input offset fluctuation)

2.12 Power supply rejection ratio (PSRR)

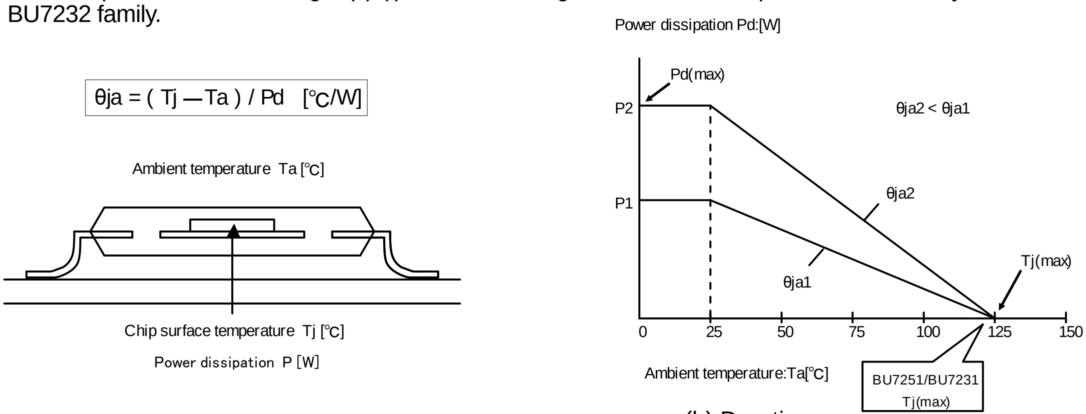
Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed. It is normally the fluctuation of DC.
PSRR＝(Change of power supply voltage)/(Input offset fluctuation)

●Derating curve

Power dissipation (total loss) indicates the power that can be consumed by IC at Ta=25℃(normal temperature).IC is heated when it consumed power, and the temperature of IC ship becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance, represented by the symbol θj-a[℃/W]. The temperature of IC inside the package can be estimated by this thermal resistance. Fig.93 (a) shows the model of thermal resistance of the package. Thermal resistance θja, ambient temperature Ta, junction temperature Tj, and power dissipation Pd can be calculated by the equation below :

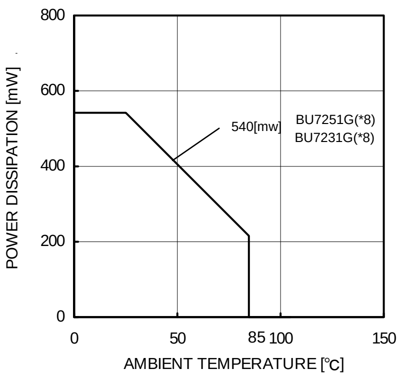
$$\theta ja = (Tj - Ta) / Pd \quad [℃/W] \quad \cdots\cdots \quad (\mathrm{I})$$

Derating curve in Fig.93 (b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θja. Thermal resistance θja depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Fig94(c)-(f) show a derating curve for an example of BU7251family, BU7252 family, BU7231 family, BU7232 family.

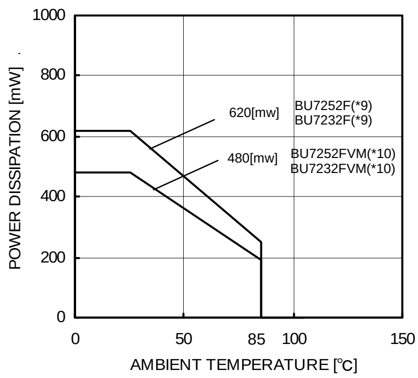


(a) Thermal resistance (b) Derating curve

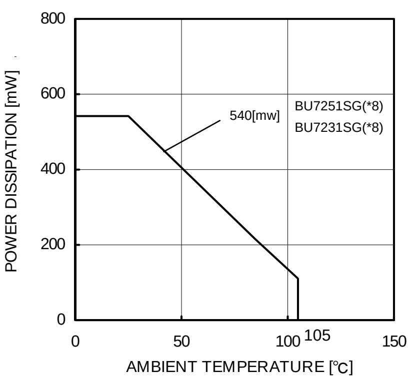
Fig. 93. Thermal resistance and power dissipation



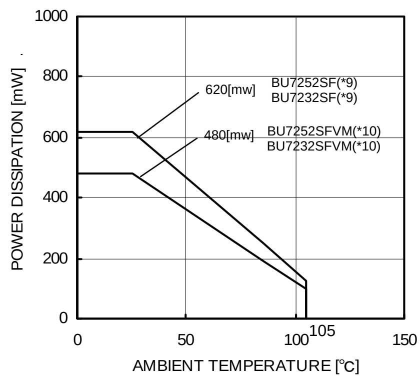
(c) BU7251G BU7231G



(d) BU7252F/FVM BU7232F/FVM



(e) BU7251SG BU7231SG



(f) BU7252S F/FVM BU72432S F/FVM

(*8)	(*9)	(*10)	Unit
5.4	6.2	4.8	[mW/℃]

When using the unit above Ta=25[℃], subtract the value above per degree[℃]. Permissible dissipation is the value when FR4 glass epoxy board 70[mm]×70[mm]×1.6[mm] (cooper foil area below 3[%]) is mounted.

Fig. 94. Derating curve

●Notes for use

1) Absolute maximum ratings
Absolute maximum ratings are the values which indicate the limits, within which the given voltage range can be safely charged to the terminal.However, it does not guarantee the circuit operation.

2) Applied voltage to the input terminal
For normal circuit operation of voltage comparator, please input voltage for its input terminal within input common mode voltage VDD+0.3[V].Then, regardless of power supply voltage,VSS-0.3[V] can be applied to inputterminals without deterioration or destruction of its characteristics.

3) Operating power supply (split power supply/single power supply)
The voltage comparator operates if a given level of voltage is applied between VDD and VSS.
Therefore, the operational amplifier can be operated under single power supply or split power supply.

4) Power dissipation (pd)
If the IC is used under excessive power dissipation. An increase in the chip temperature will cause deterioration of the radical characteristics of IC. For example, reduction of current capability.
Take consideration of the effective power dissipation and thermal design with a sufficient margin. Pd is reference to the provided power dissipation curve.

5) Short circuits between pins and incorrect mounting
Short circuits between pins and incorrect mounting when mounting the IC on a printed circuits board, take notice of the direction and positioning of the IC.
If IC is mounted erroneously, It may be damaged. Also, when a foreign object is inserted between output, between output and VDD terminal or VSS terminal which causes short circuit, the IC may be damaged.

6) Using under strong electromagnetic field
Be careful when using the IC under strong electromagnetic field because it may malfunction.

7) Usage of IC
When stress is applied to the IC through warp of the printed circuit board,
The characteristics may fluctuate due to the piezo effect. Be careful of the warp of the printed circuit board.

8) Testing IC on the set board
When testing IC on the set board, in cases where the capacitor is connected to the low impedance,make sure to discharge per fabrication because there is a possibility that IC may be damaged by stress.
When removing IC from the set board, it is essential to cut supply voltage.
As a countermeasure against the static electricity, observe proper grounding during fabrication process and take due care when carrying and storage it.

9) The IC destruction caused by capacitive load
The transistors in circuits may be damaged when VDD terminal and VSS terminal is shorted with the charged output terminal capacitor.
When IC is used as a operational amplifier or as an application circuit,where oscillation is not activated by an output capacitor,the output capacitor must be kept below 0.1[μF] in order to prevent the damage mentioned above.

10) Decupling capacitor
Insert the deculing capacitance between VDD and VSS, for stable operation of operational amplifier.

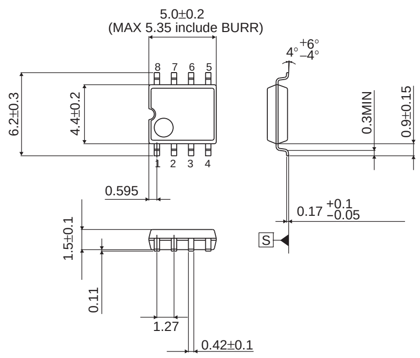
11) Latch up
Be careful of input vltage that exceed the VDD and VSS. When CMOS device have sometimes occur latch up operation.
And protect the IC from abnormaly noise

●Ordering part number

B U — 7 2 5 2 — F V M - T R

- **B U**: Part No.
- **7 2 5 2**: Part No.
  7231 , 7231S
  7251 , 7251S
  7252 , 7252S
  7232 , 7232S
- **F V M**: Package
  G: SSOP5
  F: SOP8
  FVM: MSOP8
- **T R**: Packaging and forming specification
  E2: Embossed tape and reel (SOP8)
  TR: Embossed tape and reel (SSOP5/MSOP8)

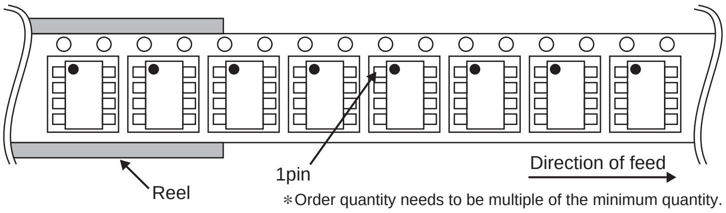
SOP8



(Unit : mm)

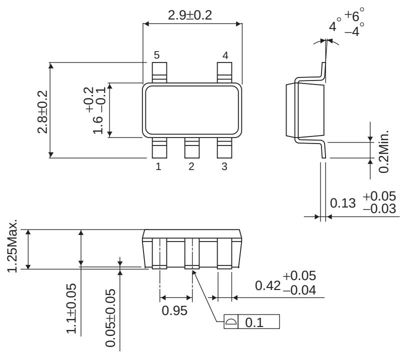
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

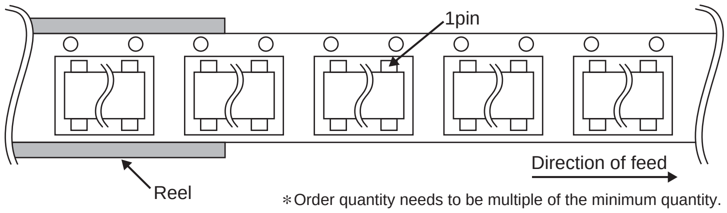
SSOP5



(Unit : mm)

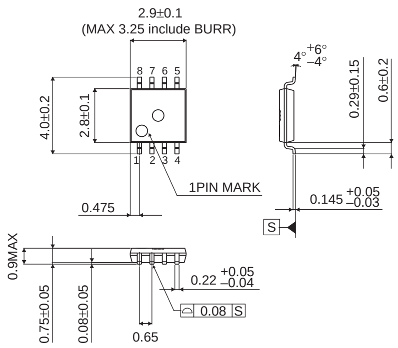
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

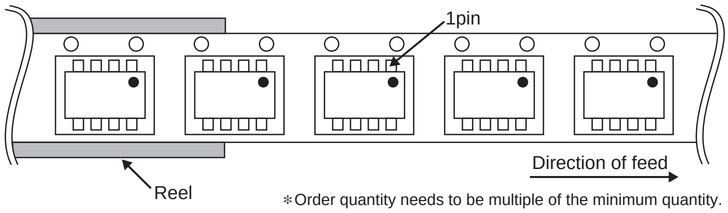
MSOP8



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

No copying or reproduction of this document, in part or in whole, is permitted without the consent of ROHM Co.,Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing ROHM's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from ROHM upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, ROHM shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM and other parties. ROHM shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While ROHM always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. ROHM shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). ROHM shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

LifeElectronics

Живое партнерство

ООО "ЛайфЭлектроникс" **"LifeElectronics" LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru