

Dual P-Channel MOSFET

-60V, -12A, 68mΩ

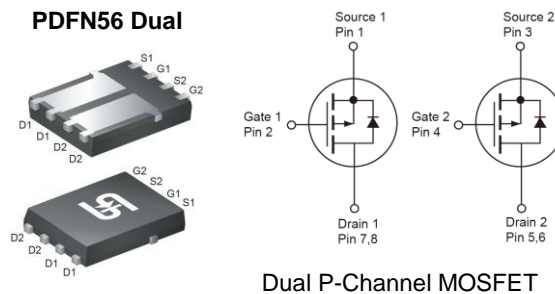
FEATURES

- Fast switching
- Low thermal resistance package
- Low profile package
- Pb-free plating
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21 definition

APPLICATION

- Power Supply
- Motor Control

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	-60	V
$R_{DS(on)}$ (max)	$V_{GS} = -10V$	68
	$V_{GS} = -4.5V$	110
Q_g	16.4	nC



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Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Note 1)	I_D	$T_C = 25^\circ\text{C}$	-12
		$T_C = 100^\circ\text{C}$	-8
Pulsed Drain Current (Note 2)	I_{DM}	-48	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{TOT}	3.5	W
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	7.2	mJ
Single Pulsed Avalanche Current (Note 3)	I_{AS}	12	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	4.5	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	85	$^\circ\text{C/W}$

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	BV_{DSS}	-60	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	$V_{GS(TH)}$	-1.2	-1.6	-2.5	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = -60V, V_{GS} = 0V$	I_{DSS}	--	--	-1	μA
	$V_{DS} = -48V, T_C = 125^\circ\text{C}$		--	--	-10	
Drain-Source On-State Resistance	$V_{GS} = -10V, I_D = -6A$	$R_{DS(on)}$	--	54	68	m Ω
	$V_{GS} = -4.5V, I_D = -3A$		--	90	110	
Forward Transconductance	$V_{DS} = -10V, I_D = -6A$	g_{fs}	--	8.5	--	S
Dynamic (Note 5)						
Total Gate Charge	$V_{DS} = -30V, I_D = -6A,$ $V_{GS} = -10V$	Q_g	--	16.4	--	nC
Gate-Source Charge		Q_{gs}	--	2.8	--	
Gate-Drain Charge		Q_{gd}	--	3.6	--	
Input Capacitance	$V_{DS} = -30V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	C_{iss}	--	870	--	pF
Output Capacitance		C_{oss}	--	70	--	
Reverse Transfer Capacitance		C_{rss}	--	42	--	
Switching (Note 6)						
Turn-On Delay Time	$V_{DD} = -30V, I_D = -1A,$ $R_{GEN} = 6\Omega$	$t_{d(on)}$	--	8.3	--	ns
Turn-On Rise Time		t_r	--	42.4	--	
Turn-Off Delay Time		$t_{d(off)}$	--	64.6	--	
Turn-Off Fall Time		t_f	--	16.4	--	
Source-Drain Diode (Note 4)						
Maximum Continuous Drain-Source Diode Forward Current	Integral reverse diode in the MOSFET	I_S	--	--	-12	A
Maximum Pulse Drain-Source Diode Forward Current		I_{SM}	--	--	-48	A
Diode-Source Forward Voltage	$V_{GS} = 0V, I_S = -1A$	V_{SD}	--	--	-1	V

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. $L = 0.1\text{mH}, I_{AS} = -12A, V_{DD} = -25V, R_G = 25\Omega, \text{Starting } T_J = 25^\circ\text{C}$
4. Pulse test: $PW \leq 300\mu s, \text{duty cycle} \leq 2\%$
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION (EXAMPLE)

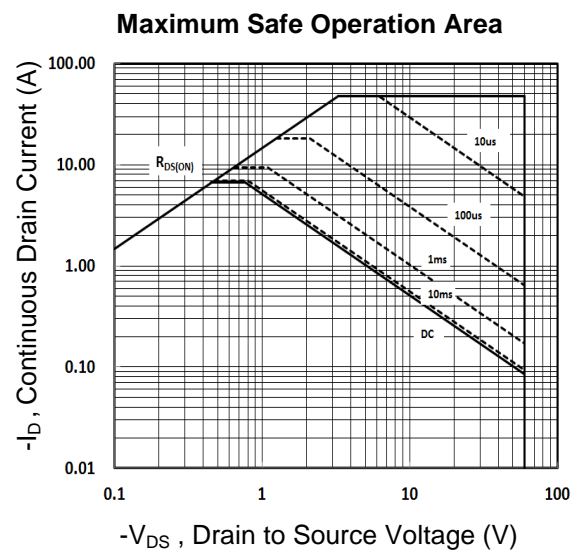
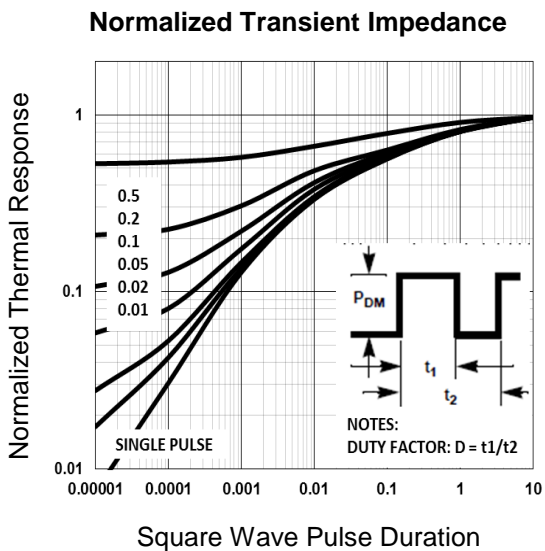
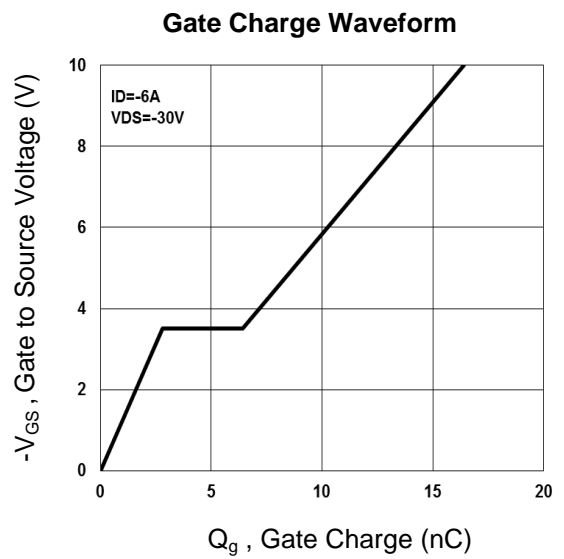
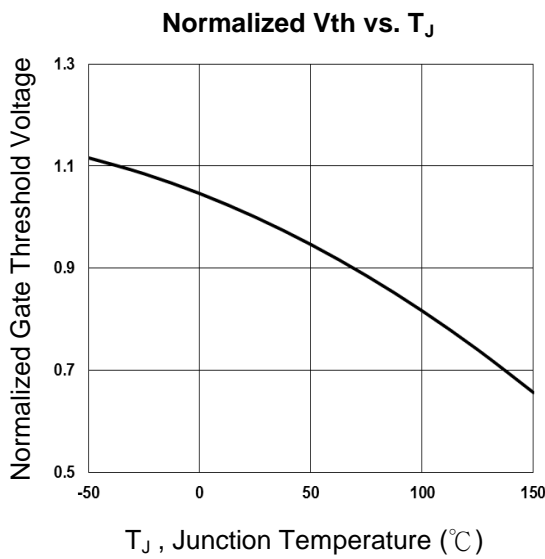
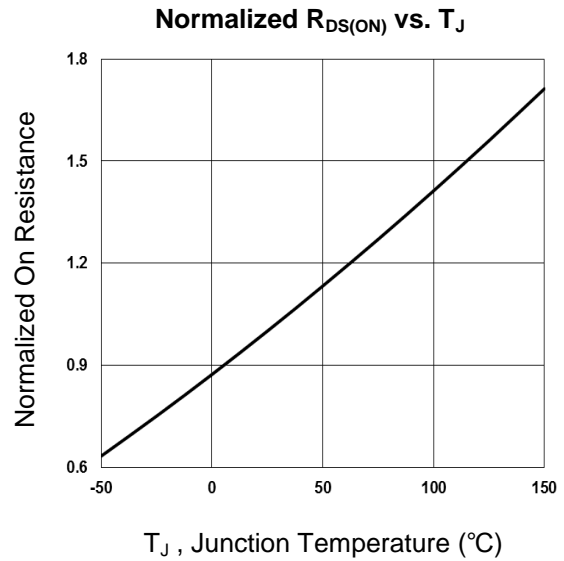
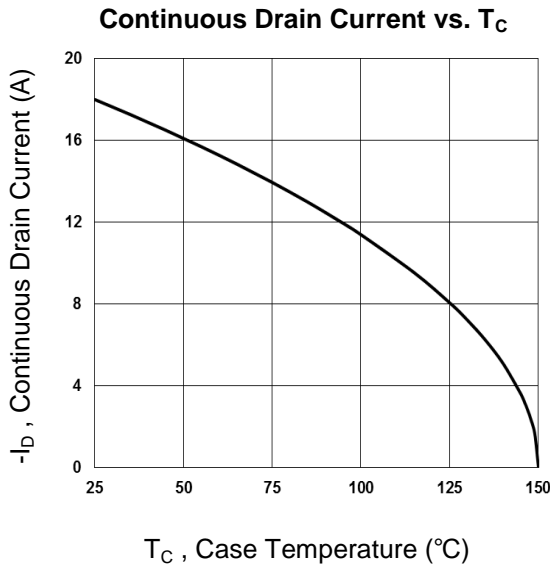
PART NO.	PACKAGE	PACKING
TSM680P06DPQ56 RLG	PDFN56 Dual	2,500pcs / 13"Reel

Note:

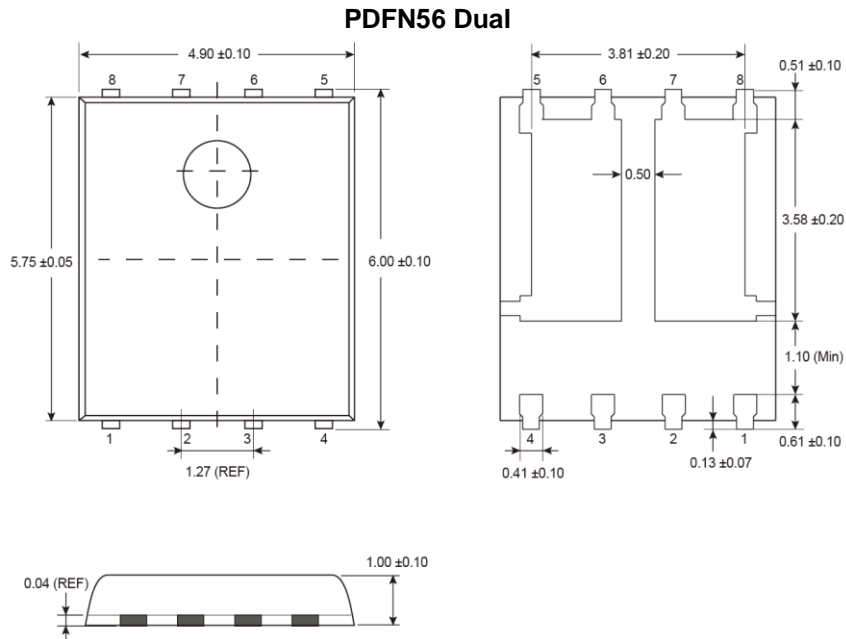
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CHARACTERISTICS CURVES

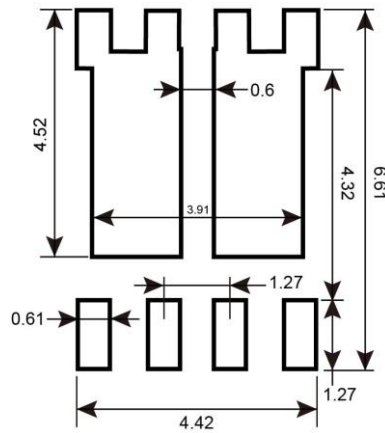
($T_C = 25^\circ\text{C}$ unless otherwise noted)



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- Y = Year Code
- M = Month Code for Halogen Free Product
 - O =Jan P =Feb Q =Mar R =Apr
 - S =May T =Jun U =Jul V =Aug
 - W =Sep X =Oct Y =Nov Z =Dec
- L = Lot Code (1~9, A~Z)

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