FAIRCHILD SEMICONDUCTOR®

July 2003

# FDD6690A

## 30V N-Channel PowerTrench® MOSFET

### General Description

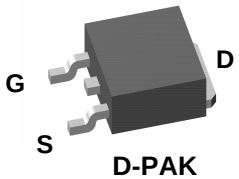
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on state resistance and yet maintain low gate charge for superior switching performance.

### Applications

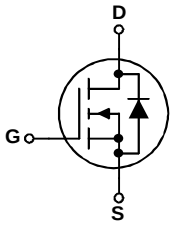
- DC/DC converter
- Motor Drives

### Features

- 46 A, 30 V $R_{DS(ON)}$ = 12 mΩ @ $V_{GS}$ = 10 V
  $R_{DS(ON)}$ = 14 mΩ @ $V_{GS}$ = 4.5 V
- Low gate charge
- Fast Switching Speed
- High performance trench technology for extremely low $R_{DS(ON)}$




D-PAK
(TO-252)




## Absolute Maximum Ratings

$T_A$=25°C unless otherwise noted

| Symbol | Parameter | | | Ratings | Units |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | | 30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | | ±20 | V |
| $I_D$ | Continuous Drain Current | @$T_C$=25°C | (Note 3) | 46 | A |
| | | @$T_A$=25°C | (Note 1a) | 12 | |
| | | Pulsed | (Note 1a) | 100 | |
| $P_D$ | Power Dissipation | @$T_C$=25°C | (Note 3) | 56 | W |
| | | @$T_A$=25°C | (Note 1a) | 3.3 | |
| | | @$T_A$=25°C | (Note 1b) | 1.5 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | | –55 to +175 | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 2.7 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 45 | |
| $R_{\theta JA}$ | | (Note 1b) | 96 | |

## Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape width | Quantity |
|---|---|---|---|---|---|
| FDD6690A | FDD6690A | D-PAK (TO-252) | 13'' | 12mm | 2500 units |

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## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Drain-Source Avalanche Ratings (Note 2)** | | | | | | |
| $E_{AS}$ | Drain-Source Avalanche Energy | Single Pulse, $V_{DD}$ = 15 V, $I_D$= 12A | | | 180 | mJ |
| $I_{AS}$ | Drain-Source Avalanche Current | | | | 12 | A |
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA,Referenced to 25°C | | 24 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSS}$ | Gate–Body Leakage | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| **On Characteristics (Note 2)** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1 | 1.9 | 3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA,Referenced to 25°C | | –5 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = 10 V, $I_D$ = 12 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 10 A<br>$V_{GS}$ = 10 V, $I_D$ = 12 A,$T_J$=125°C | | 7.7<br>9.9<br>11.4 | 12<br>14<br>19 | mΩ |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 5 V | 50 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 12 A | | 47 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 1230 | | pF |
| $C_{oss}$ | Output Capacitance | | | 325 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 150 | | pF |
| $R_G$ | Gate Resistance | $V_{GS}$ = 15 mV, f = 1.0 MHz | | 1.5 | | pF |
| **Switching Characteristics (Note 2)** | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 15 V, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 10 | 19 | ns |
| $t_r$ | Turn–On Rise Time | | | 7 | 13 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 29 | 46 | ns |
| $t_f$ | Turn–Off Fall Time | | | 12 | 21 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 15V, $I_D$ = 12 A, $V_{GS}$ = 5 V | | 13 | 18 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 3.5 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 5.1 | | nC |

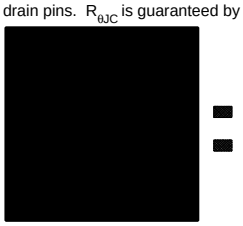
## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | 2.3 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.3 A (Note 2) | | 0.76 | 1.2 | V |
| $t_{rr}$ | Diode Reverse Recovery Time | $I_F$ = 12 A, $d_{iF}/d_t$ = 100 A/µs | | 24 | | nS |
| $Q_{rr}$ | Diode Reverse Recovery Charge | | | 13 | | nC |

**Notes:**

**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $R_{\theta JA}$ = 45°C/W when mounted on a 1in$^2$ pad of 2 oz copper

b) $R_{\theta JA}$ = 96°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

**3.** Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$

where $P_D$ is maximum power dissipation at $T_C$ = 25°C and $R_{DS(on)}$ is at $T_{J(max)}$ and $V_{GS}$ = 10V. Package current limitation is 21A

## Typical Characteristics

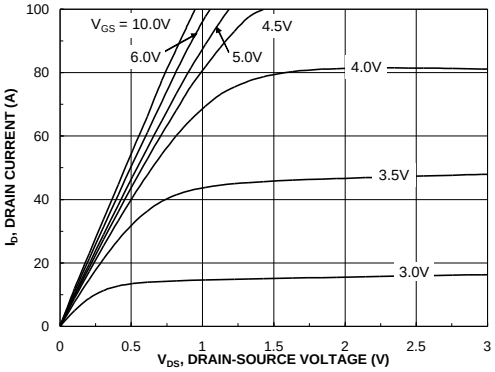



**Figure 1. On-Region Characteristics**

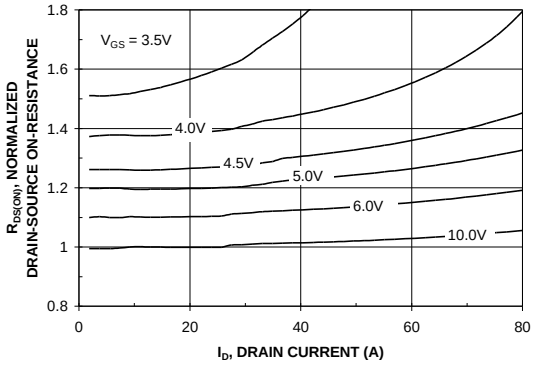



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage**

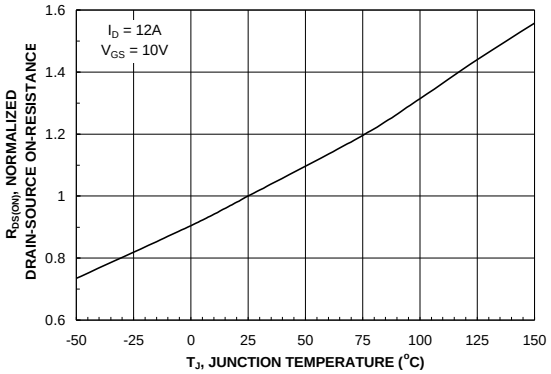



**Figure 3. On-Resistance Variation withTemperature**

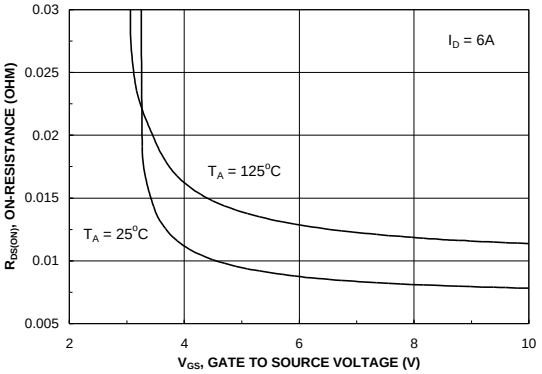



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage**

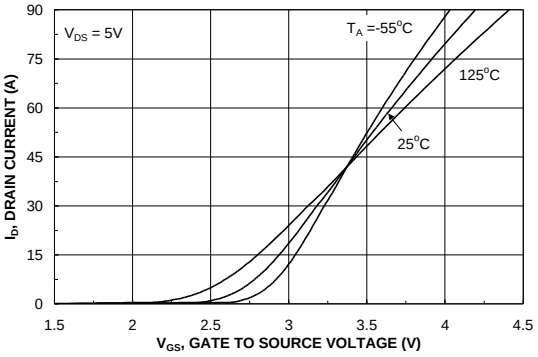



**Figure 5. Transfer Characteristics**

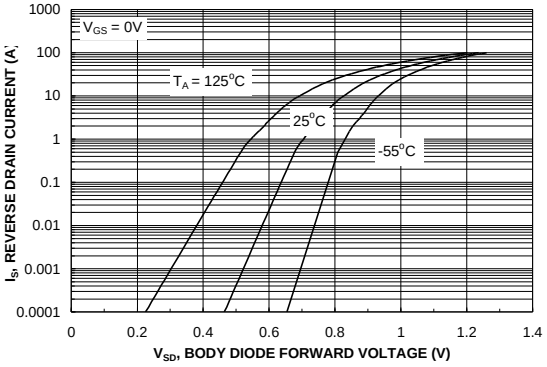



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature**

## Typical Characteristics

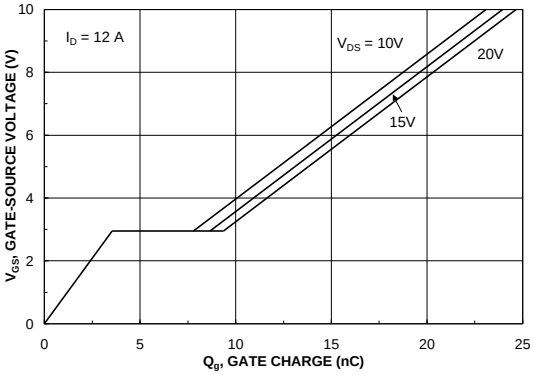



**Figure 7. Gate Charge Characteristics**

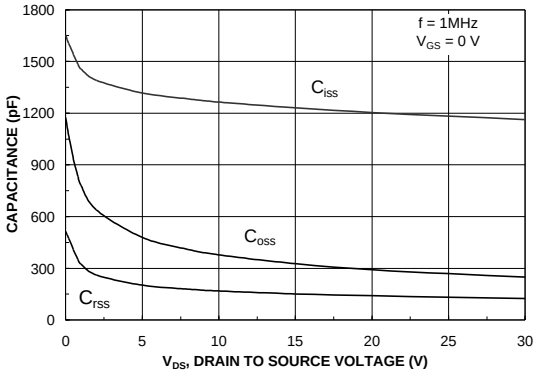



**Figure 8. Capacitance Characteristics**

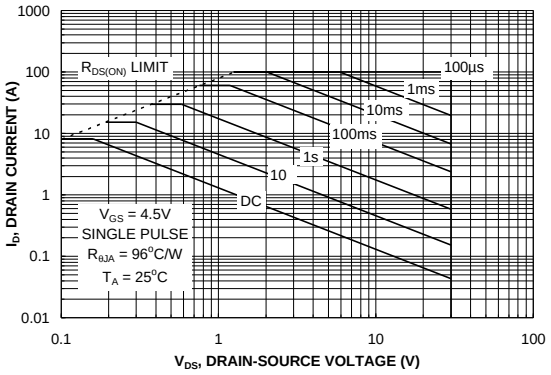



**Figure 9. Maximum Safe Operating Area**

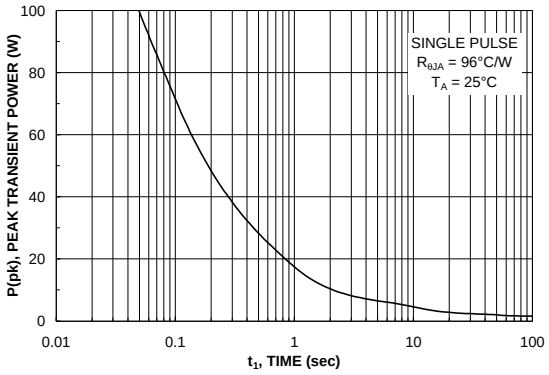



**Figure 10. Single Pulse Maximum Power Dissipation**

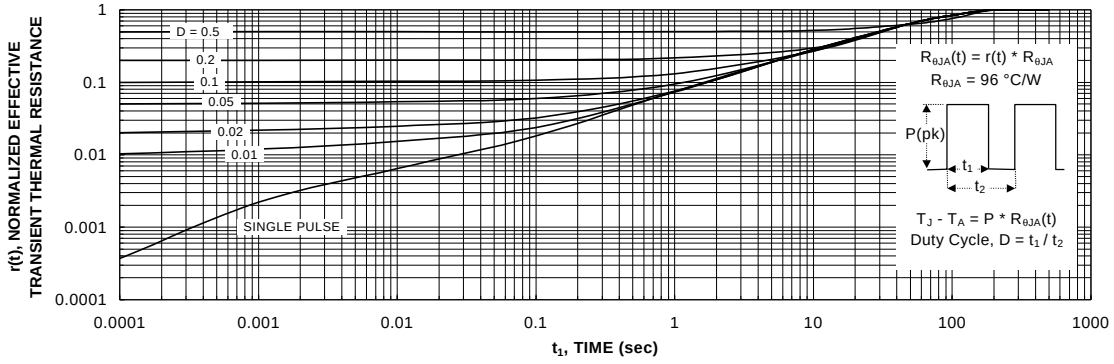



**Figure 11. Transient Thermal Response Curve**

**Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.**

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