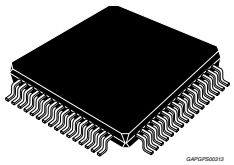
L9662

Octal squib driver and quad Manchester/PSI5 encoded sensor interface ASIC for safety application

Datasheet - production data



LQFP64 (10x10x1.4mm)

Features

- 8 deployment drivers with SPI selectable firing current and times
- Capability to deploy the squib with 1.2 A (min)/2 ms, 1.75 A (min)/1.0 ms and 1.75 A (min)/0.65 ms between VRES of 7 V to 37 V
- Capability to deploy the squib with 1.5 A (min)/2 ms between VRES of 7 V to 25 V
- Firing capability to deploy all channels simultaneously
- Independently controlled high-side and low-side MOS for diagnosis
- Analog output available for resistance measurement
- Squib short to ground, short to battery and MOS diagnostic available on SPI register
- Capability to deploy the squib the low side MOS is shorted to ground
- 4 Fire enable inputs
- Interface with 4 satellite sensors
- Programmable independent current trip points for each satellite channel
- Support Manchester 1 or 2 protocol for satellite sensors
- Support PSI5 (Parity) protocol for satellite sensors (reference PSI5 technical specification V 1.2 /14.06.07)
- Support for Sync pulse and minibus for satellites
- Supports for variable bit rate detection
- Independent current limit and fault timer shutdown protection for each satellite output
- Short to ground and short to battery detection and reporting for each satellite channel
- 2 independent SPI interfaces
- 5.5 MHz SPI interface
- Satellite message error detection
- Hall effect sensor support on satellite channels 3 and 4.
- Low voltage internal reset
- 2 kV ESD capability on all pins
- Package: LQFP64
- Technology: ST Proprietary BCD5

Description

The device is intended to deploy up to 8 squibs and to interface up to 4 satellites. 2 satellite interfaces can be used to interface Hall sensors. Squib drivers are sized to deploy 1.2 A minimum for 2 ms, 1.75 A minimum for 1 ms and 1.75 A minimum for 0.65 ms during load dump along with 1.5 A minimum for 2 ms for VRES voltages less than 25 V.

Full diagnostic capabilities of the squib interface are provided. Satellite interfaces support Manchester 1, 2 and PSI5 decoding with variable bit rate.

Table 1. Device summary

Order code	Amb. temp range, °C	Package	Packing
L9662	-40 to +85	LQFP64	Tray
L9662TR			Tape & Reel

This is information on a product in full production. www.st.com

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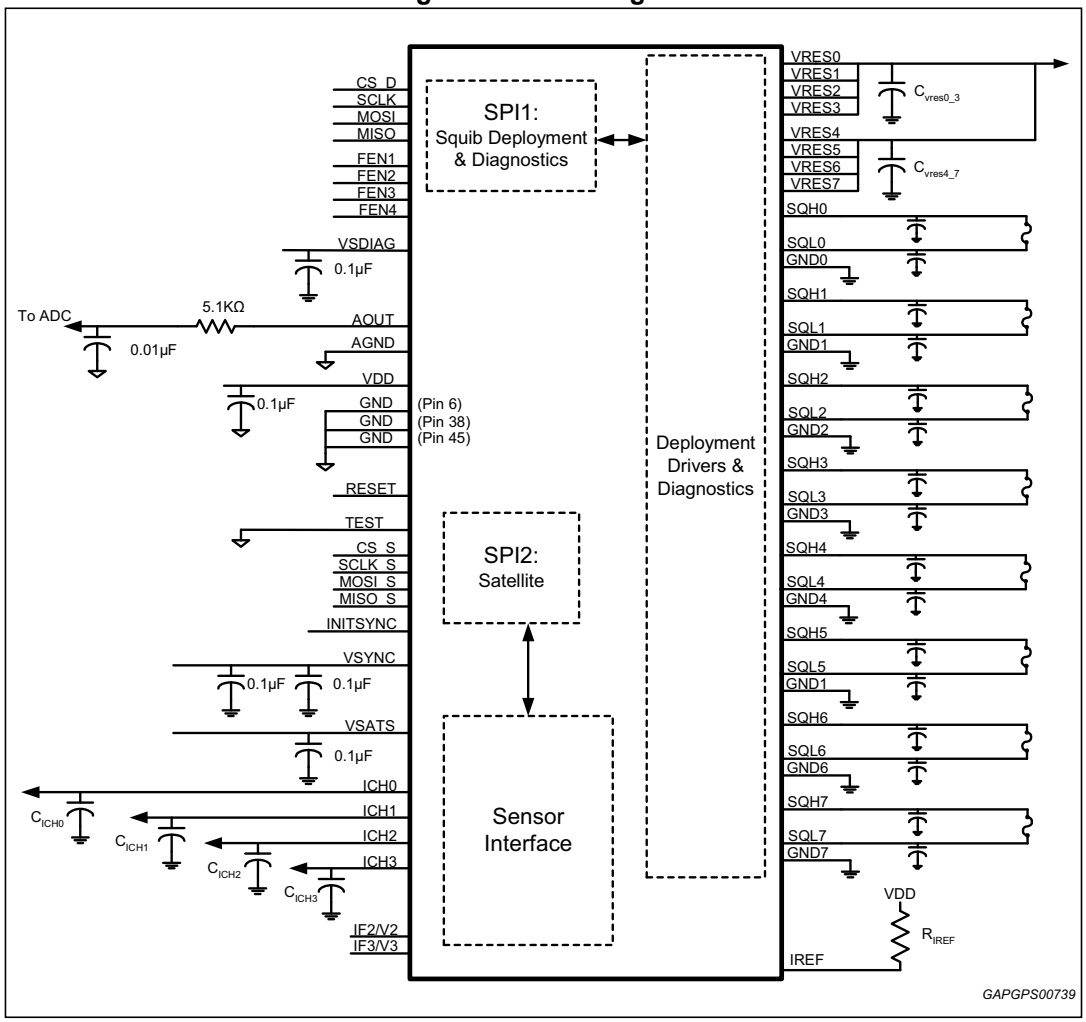
1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Table 2. Pin description

Pin Number	Pin name	Description	I/O type	Reset state
1	MISO	SPI Data Out	Output	Hi-Z
2	MISO_S	Satellite SPI Data Out	Output	Hi-Z
3	FEN1	Fire Enable for Channels 0 and 1	Input	Pulldown
4	FEN2	Fire Enable for Channels 2 and 3	Input	Pulldown
5	RESETB	Reset pin	Input	Pullup
6	GND	Ground (Analog & Digital)	-	-
7	VDD	VDD Supply Voltage	Input	-
8	FEN3	Fire Enable for Channels 4 and 5	Input	Pulldown
9	FEN4	Fire Enable for Channels 6 and 7	Input	Pulldown
10	INITSYNC	Initiate Sync Pulse	Input	Pulldown
11	CS_S	SPI Chip Select for Satellite Interface	Input	Pullup
12	CS_D	SPI Chip Select for Deployment Driver	Input	Pullup
13	MOSI	SPI Data In	Input	Hi-Z
14	MOSI_S	Satellite SPI Data In		
15	SCLK_S	Satellite SPI Clock		Hi-Z
16	SCLK	SPI Clock	Input	Hi-Z
17	GND4	Power Ground for Loop Channel 4	-	-
18	SQL4	Low Side Driver Output for Channel 4	Output	Pulldown
19	SQH4	High Side Driver Output for Channel 4	Output	Hi-Z
20	VRES4	Reserve Voltage for Loop Channel 4	Input	-
21	VRES5	Reserve Voltage for Loop Channel 5	Input	-
22	SQH5	High Side Driver Output for Channel 5	Output	Hi-Z
23	SQL5	Low Side Driver Output for Channel 5	Output	Pulldown
24	GND5	Power Ground for Loop Channel 5	-	-
25	GND6	Power Ground for Loop Channel 6	-	-
26	SQL6	Low Side Driver Output for Channel 6	Output	Pulldown
27	SQH6	High Side Driver Output for Channel 6	Output	Hi-Z
28	VRES6	Reserve Voltage for Loop Channel 6	Input	-
29	VRES7	Reserve Voltage for Loop Channel 7	Input	-
30	SQH7	High Side Driver Output for Channel 7	Output	Hi-Z
31	SQL7	Low Side Driver Output for Channel 7	Output	Pulldown
32	GND7	Power Ground for Loop Channel 7	-	-
33	TEST	Test pin	Input	Pulldown

Table 2. Pin description (continued)

Pin Number	Pin name	Description	I/O type	Reset state
34	VSDIAG	Supply for Deployment Driver Diagnostics	Input	-
35	NC	No Connect	-	-
36	IF3/V3	Current Feedback for channel 3 Raw Or Raw Data output For Channel 3	Output	Hi-Z
37	IF2/V2	Current Feedback for channel 2 Raw Or Data output For Channel 2	Output	Hi-Z
38	GND	Ground (Analog & Digital)	-	-
39	ICH3	Current Sense Output for Channel 3	Output	Hi-Z
40	ICH2	Current Sense Output for Channel 2	Output	Hi-Z
41	ICH1	Current Sense Output for Channel 1	Output	Hi-Z
42	ICH0	Current Sense Output for Channel 0	Output	Hi-Z
43	VSYNC	Supply for Satellite Sync Pulse	Input	-
44	VSATS	Supply Voltage for Satellite Interface	Input	-
45	GND	Ground (Analog & Digital)	-	-
46	IREF	External Current Reference Resistor	Output	-
47	AGND	Ground Reference for AOUT	-	-
48	AOUT	Analog Output for Loop Diagnostics	Output	Hi-Z
49	GND3	Power Ground for Loop Channel 3	-	-
50	SQL3	Low Side Driver Output for Channel 3	Output	Pulldown
51	SQH3	High Side Driver Output for Channel 3	Output	Hi-Z
52	VRES3	Reserve Voltage for Loop Channel 3	Input	-
53	VRES2	Reserve Voltage for Loop Channel 2	Input	-
54	SQH2	High Side Driver Output for Channel 2	Output	Hi-Z
55	SQL2	Low Side Driver Output for Channel 2	Output	Pulldown
56	GND2	Power Ground for Loop Channel 2	-	-
57	GND1	Power Ground for Loop Channel 1	-	-
58	SQL1	Low Side Driver Output for Channel 1	Output	Pulldown
59	SQH1	High Side Driver Output for Channel 1	Output	Hi-Z
60	VRES1	Reserve Voltage for Loop Channel 1	Input	-
61	VRES0	Reserve Voltage for Loop Channel 0	Input	-
62	SQH0	High Side Driver Output for Channel 0	Output	Hi-Z
63	SQL0	Low Side Driver Output for Channel 0	Output	Pulldown
64	GND0	Power Ground for Loop Channel 0	-	-

2 Electrical specifications

2.1 Absolute maximum ratings

The following maximum ratings are continuous absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	- 0.3 to 5.5	V
V_{SDIAG}	Supply voltage for squib diagnostics	- 0.3 to 40	V
V_{SATS}	Satellite supply voltage	- 0.3 to 40	V
V_{SYNC}	Sync supply voltage	- 0.3 to 40	V
VRESx	VRES voltage (VRES0, VRES1, VRES2, VRES3, VRES4, VRES5, VRES6, VRES7)	- 0.3 to 40	V
SQHx	Squib high side drivers (SQH0, SQH1, SQH2, SQH3, SQH4, SQH5, SQH6, SQH7)	- 0.6 to 40	V
SQLx	Squib low side drivers (SQL0, SQL1, SQL2, SQL3, SQL4, SQL5, SQL6, SQL7)	- 0.3 to 40	V
ICHx	Satellite outputs (ICH0, ICH1, ICH2, ICH3)	-1 to 40	V
TEST	Test pin	-0.3 to 40	V
V_I	Discrete input voltage (RESETB, DEPEN, CS_D, CS_S, SCLK, SCLK_S, MOSI, MOSI_S, MISO, MISO_S, FEN1, FEN2, FEN3, FEN4, INITSYNC, IREF)	- 0.3 to 5.5	V
V_O	Discrete output voltage (MISO, MISO_S, AOUT, IF2V2, IF3V3)	- 0.3 to 5.5	V
AGND	Analog output reference	-0.3 to 5.5	V
GND	Ground (GND, GND0, GND1, GND2, GND3, GND4, GND5, GND6, GND7)	-0.3 to 5.5	V
T_j	Maximum steady-state junction temperature	150	°C
T_{amb}	Ambient temperature	-40 to 95	°C
T_{stg}	Storage temperature	-65 to 150	°C
$R_{th\ j\ amb}$	Thermal resistance-junction-to-ambient	46	°C/W
The following maximum ratings are up to 48 hours; exceeding any one of these values for longer than a total time of 48 hours may cause permanent damage to the integrated circuit.			
V_{DD}	Supply voltage	- 0.3 to 6.0	V
V_I	Discrete input voltage (RESETB, DEPEN, CS_D, CS_S, SCLK, SCLK_S, MOSI, MOSI_S, MISO, MISO_S, FEN1, FEN2, FEN3, FEN4, INITSYNC, IREF)	- 0.3 to 6.0	V
V_O	Discrete output voltage (MISO, MISO_S, AOUT, IF2V2, IF3V3)	- 0.3 to 6.0	V

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
AGND	Analog output reference	-0.3 to 6.0	V
GND	Ground (GND, GND0, GND1, GND2, GND3, GND4, GND5, GND6, GND7)	-0.3 to 6.0	V
T_j	Maximum steady-state junction temperature	150	°C
T_{amb}	Ambient temperature	-40 to 95	°C
T_{stg}	Storage temperature	-65 to 150	°C
$R_{th\ j\ amb}$	Thermal resistance junction-to-ambient	46	°C/W

2.2 Absolute maximum degraded operating ratings

Under the following deviations to the ratings indicated in *Section 2.3* the device performance will be degraded and not meet the electrical characteristics outlined in *Section 2.4*. At minimum the SPI and diagnostics will function but not meet specified electrical parameters.

Table 4. Absolute maximum degraded operating ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{SDIAG}	Supply voltage for squib diagnostics	7 to 40	V
V_{SATS}	Satellite supply voltage	7 to 14	V
V_{SYNC}	Sync supply voltage	(V_{SATS}+ 5.5 V) to 40	V
V_{RES}	VRES voltage (VRES0, VRES1, VRES2, VRES3, VRES4, VRES5, VRES6, VRES7)	7 to 40	V
V_I	Discrete input voltage (RESETB, DEPEN, CS_D, CS_S, SCLK, SCLK_S, MOSI, MOSI_S, MISO, MISO_S, FEN1, FEN2, FEN3, FEN4, INITSYNC)	- 0.3 to (VDD +0.3)	V
T_j	Junction temperature	-40 to 150	°C

Note: The above is provided for informational purposes only and will result in degraded operation. Under the above conditions the SPI will be functional as well as diagnostics, though the electrical performance may not conform to the parameters outlined in Section 2.4. Firing requirements as indicated in Section 2.4 may not be met with the conditions above.

2.3 Operating ratings

Table 5. Operating ratings

Symbol	Parameter		Value	Unit
V_{DD}	Supply voltage		4.9 to 5.1	V
V_{SDIAG}	Supply voltage for squib diagnostics		7 to 37	V
V_{SATS}	Satellite supply voltage		7 to 14	V
V_{SYNC}	Sync supply voltage (1))	Continuous	(V_{SATS} + 6) to 25	V
		pulse ≤500 ms	(V_{SATS} + 6) to 40	
V_{RESx}	VRES voltage (VRES0, VRES1, VRES2, VRES3, VRES4, VRES5, VRES6, VRES7)		7 to 37	V
V_I	Discrete input voltage (RESETB, DEPEN, CS_D, CS_S, SCLK, SCLK_S, MOSI, MOSI_S, MISO, MISO_S, FEN1, FEN2, FEN3, FEN4, INITSYNC, IREF)		- 0.3 to (V_{DD} +0.3)	V
T_{amb}	Ambient temperature		-40 to 95	°C
$R_{Th\ j\text{-}amb}$	Thermal resistance junction-to-ambient		46	°C/W

1. For PSI5 the maximum operating voltage is 16.5V as called out in the PSI5 technical specification (V 1.2 /14.06.07). Depending on the sync supply voltage the sync pulse can be as high as 8 V above idle. To ensure the maximum operating voltage of 16.5 V is not exceeded then the VSATS voltage should be limited to 8.5 V.

2.4 Electrical characteristics

2.4.1 General

4.9 V ≤ V_{DD} ≤ 5.1 V; 7 V ≤ V_{RESX} ≤ 37 V; 7 V ≤ V_{SDIAG} ≤ 37 V; (V_{SATS} + 6.5 V) ≤ V_{SYNC} ≤ 25 V; 5 V ≤ V_{SATS} ≤ 14 V; FEN1 = FEN2 = FEN3 = FEN4 = V_{DD}; R_REF = 10 kΩ, ±1%, 100 PPM; -40 °C ≤ T_A ≤ +95 °C; unless other specified.

Table 6. General - DC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Osc	Internal oscillator frequency	Tested with 10K, 1%, 100ppm I_{ref} resistor	4.75	-	5.25	MHz
V_{RST1}	Internal voltage reset VDD after de-glitch time (tpor) See *Figure 6*	VDD level for device to report reset condition -deployment drivers are disabled	4.0	-	4.5	V
V_{RST2}	Internal voltage reset VDD with no de-glitch time See	Guaranteed by design	2.1	-	3.0	
t_{POR}	POR De-glitch timer	Timer for VRST1	5	-	25	µs
I_{DD}	Input current VDD	No squib diagnostics. No deployment. Satellite channels disabled.	-	-	15	mA
		Resistance measurement diagnostics with no fault condition present. Satellite channels disabled.	-	-	17	

Table 6. General - DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{DD}	Input current VDD	Resistance measurement diagnostics running with no fault condition present. Satellite channels enabled with I_ICHx=10mA and no sync pulse.	-	-	17	mA
		Resistance measurement diagnostics running with no fault condition present. Satellite channels enabled with I_ICHx = 50 mA and no sync pulse.	-	-	17	
		Resistance measurement diagnostics running with no fault condition present. Satellite channels enabled with I_ICHx = 50 mA and sync pulse at high voltage level.	-	-	17	
		Short to -0.3 V on SQHx. Satellite channels disabled.	-	-	15	
		Short to -0.3 V on SQLx. Satellite channels disabled.	-	-	15	
		Deployment. Satellite channels disabled.	-	-	15	
		Short to GND on SQL; VRCM active Satellite channels enabled with I_ICHx = 50 mA and sync pulse at high voltage level.	-	-	35	
R_{IREF_H}	Resistance threshold IREF	-	-	-	60.0	kΩ
R_{IREF_L}		-	2.0	-		kΩ
V_{IH_RESETB}	Input voltage threshold RESETB	-	-	-	2.0	V
V_{IL_RESETB}		-	0.8	-		V
V_{HYS_RST}		-	100	-	300	mV
V_{IH_TEST}	Input voltage threshold TEST	Guaranteed by design	-	3.2		V
I_{TESTPD}	Input pull-down current TEST	-	1.0	-	2.5	mA
I_{AOUT_SHRT}	AOUT pin current limit	AOUT short to ground during squib resistance diagnostics	-	-	20	mA
$I_{RESETPU}$	Input pull-up current RESETB	RESETB = VIH to GND	-10	-	-50	µA
I_{VSATS}	Current consumption VSATS	Satellite channels enabled ICH0-3 = 0 A	-	-	5	mA
I_{VSYNC}	VSYNC supply current	Satellite channels enabled ICH0-3 = 0 A	-	-	5	mA

Table 6. General - DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{RESx}	Quiescent current for VRESx during HSS test	Current per pin during HSS test excluding selected channel	-	-	10	µA
V_{IH}	Input voltage threshold (MOSI, MOSI_S, SCLK, SCLK_S, CS_S, CS_D)	Input Logic = 1	-	-	2.0	V
V_{IL}		Input Logic = 0	0.8	-	-	V
V_{HYST}	Input hysteresis	-	100	-	300	mV
I_{LKGD}	Input leakage current MOSI, MOSI_S, SCLK, SCLK_S	VIN = VDD	-	-	1	µA
		VIN = 0 to VIH	-1	-	-	µA
I_{PU_CS}	Input pull-up current CS_S, CS_D	VIN = VIH to GND	-10	-	-50	µA
I_{PD_IS}	Input pull-down current INITSYNC	VIN = VIL to VDD	10	-	50	µA
V_{OH}	Output voltage MISO, MISO_S	IOH = -800 µA	VDD–0.8	-	-	V
V_{OL}		IOL = 1.6 mA	-	-	0.4	V
I_{HI_Z}	Tri-state current MISO, MISO_S,	MISO = VDD	-	-	1	µA
		MISO = 0 V	-1	-	-	µA

2.4.2 Electrical characteristics - Squib deployment drivers and diagnostics

4.9 V ≤ V_{DD} ≤ 5. 1V; 7 V ≤ V_{RESX} ≤ 37 V; 7 V ≤ V_{SDIAG} ≤ 37 V; (V_{SATS} + 6.5 V) ≤ V_{SYNC} ≤ 25 V; 7 V ≤ V_{SATS} ≤ 14 V; FEN1 = FEN2 = FEN3 = FEN4 = V_{DD}; R_REF = 10 kΩ, ±1%, 100 PPM; C_{VRES0_3}≥ 68 nF; C_{VRES4_7} ≥ 68 nF; -40 °C ≤ T_A ≤ +95 °C; unless other specified.

Table 7. Squib deployment drivers and diagnostics - DC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
General						
I_{LKGSQH}	Leakage current SQH	VSDIAG = VDD = 0, VRES = 37 V, VSQH = 0 V	-	-	50	µA
$I_{LKGVRES}$	Bias current VRESX	VSDIAG = 18 V; VDD = 5 V; VRES = 37 V; SQH shorted to SQL	-	-	10	µA
I_{LKGSQL}	Leakage current SQL	VSDIAG = VDD = 0, VSQL = 18 V	-10	-	10	µA
I_{PD}	Pulldown current SQL	VSQL = 1.5 V to 20 V	3.3	-	4.1	mA
V_{BIAS}	Diagnostics Bias voltage	Nominal 3.6 V	-5%	VDD·0.72	+5%	V
Short to battery/ground Diagnostics - Rsqb from 0 Ω to Open						
I_{SVRCM}	Maximum Diagnostics Bias Current limit	Short to battery or ground test active VSQH = 0 V	5	-	20	mA

Table 7. Squib deployment drivers and diagnostics - DC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{STB}	Short to Battery Resistance Threshold	Vbatt = 6.5V see *Figure 9*	1.92	-	3.42	kΩ
		Vbatt = 16V see *Figure 9*	8.61	-	13.98	kΩ
		Vbatt = 20V see *Figure 9*	11.42	-	18.42	kΩ
I_{STB}	Short to battery current threshold	-	0.9	-	1.40	mA
R_{STG}	Short to Ground Threshold	-	1.2	-	1.8	kΩ
I_{STG}	Short to ground current threshold	-	2	-	3.3	mA
$t_{DIAGTIMEOUT}$	Diagnostic Delay Time	From/CS ↑ until Transistor Test Results are Valid, Output voltage change 0V to 3.5 V C_{SQHx}= 0.12 µF C_{SQLx}= 0.12 µF	-	-	1500	µs
High side safing diagnostics						
I_{SRC_HSS}	Diagnostic current into selected VRESx pin during test	Normal conditions	710	-	950	µA
I_{HSS_8}	Current during diagnostic	All 8 VRESx pins tied together	710	-	1020	µA
$R_{HSSNORM\_th}$	Normal resistance range when running high side safing diagnostics	All 8 VRESx pins tied together	1.4	-	2.5	kΩ
$V_{HSSNORM\_range}$	Normal voltage range between VSDIAG and VRESx pin) when running high side safing diagnostics	All 8 VRESx pins tied together	1.0	-	2.5	V
$V_{HSSSHORT\_th}$	Short voltage threshold between VSDIAG and VRESx pin)	All 8 VRESx pins tied together	0.5	-	1.0	V
$V_{HSSOPEN\_th}$	Open voltage threshold between VSDIAG and VRESx pin)	All 8 VRESx pins tied together	2.5	-	4.0	V
$t_{DIAGTIMEOUT}$	Diagnostic delay time	From/CS ↑ until transistor test results are valid, C_{SQHx}= 0.12 µF C_{SQLx}= 0.12 µF	-	-	500	µs
Voltage measurement diagnostics (VRESx)						
I_{RESx}	Max diagnostic current into V_{RESx} pin	Normal conditions	-	-	50	µA
$V_{VRESXLO\_th}$	Low voltage threshold for VRESx pin	-	5.0	-	7	V

Table 7. Squib deployment drivers and diagnostics - DC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{VRESXHI\_th}$	High voltage threshold for VRESx pin	-	13.7	-	18.0	V
$t_{DIAGTIMEOUT}$	Diagnostic delay time	From/CS ↑ until transistor test results are valid.	-	-	100	µs
MOS diagnostics						
$I_{\_MOS}$	MOS test max current	Normal conditions guaranteed by design	-	-	I_{SDIAG}	mA
$t_{SHUTOFF}$	LS/HS MOS turn off under fault condition	Time is measured from the valid LS/ HS MOS current > 100mA to the LS/HS turn off	-	-	4	µs
$t_{FETtimeout}$	FET timeout	Normal conditions	-	-	100	µs
High Squib resistance diagnostics						
R_{SQHIZ}	High load resistance threshold	-	1.07	-	2.1	kΩ
I_{HR}	High resistance current threshold	-	I_{STG}			mA
$t_{DIAGTIMEOUT}$	MOS diagnostic delay time	From/CS ↑ until Transistor test results are valid, C_{SQHx}= 0.12 µF C_{SQLx} = 0.12 µF	-	-	300	µs
Squib resistance diagnostics						
V_{OH}	Output voltage AOUT	High saturation voltage; I_{AOUT} = -500 µA	-	-	VDD-0.2V	V
V_{OL}		Low Saturation Voltage; I_{AOUT} = +500 µA	-	-	0.2	V
I_Z	Tri-State Current AOUT	AOUT = VDD	-	-	1	µA
		AOUT = 0 V	-1	-	-	µA
$R_{SQB\ RANGE}$	Load Resistance Range	-	3.5	-	10.0	Ω
V_{AOUT}	Resistance measurement analog output tolerance V_{AOUT} = $VDD \cdot \left[\frac{1}{10} + \left(0.08 \cdot \frac{R_{SQB}}{\Omega}\right)\right]$	0 Ω ≤ R_{SQB} < 3.5 Ω	V_{AOUT}- 0.095V	-	V_{AOUT}+ 0.095V	V
		3.5 Ω ≤ R_{SQB} ≤ 10 Ω	V_{AOUT}· 0.95V	-	V_{AOUT}· 1.05V	V
I_{SRC}	Resistance measurement current source	V_{DD} = 5.0 V; V_{SDIAG} = 7.0 V to 37 V	38	-	42	mA
I_{SINK}	Resistance measurement current sink	-	45	-	57	mA
I_{SLEW}	Rmeas current di/dt	30% - 70% of ISRC	2	-	11	mA-µs
V_{cmpr}	Voltage threshold on squib pin to shutdown ISRC	-	2.65	-	3.25	V

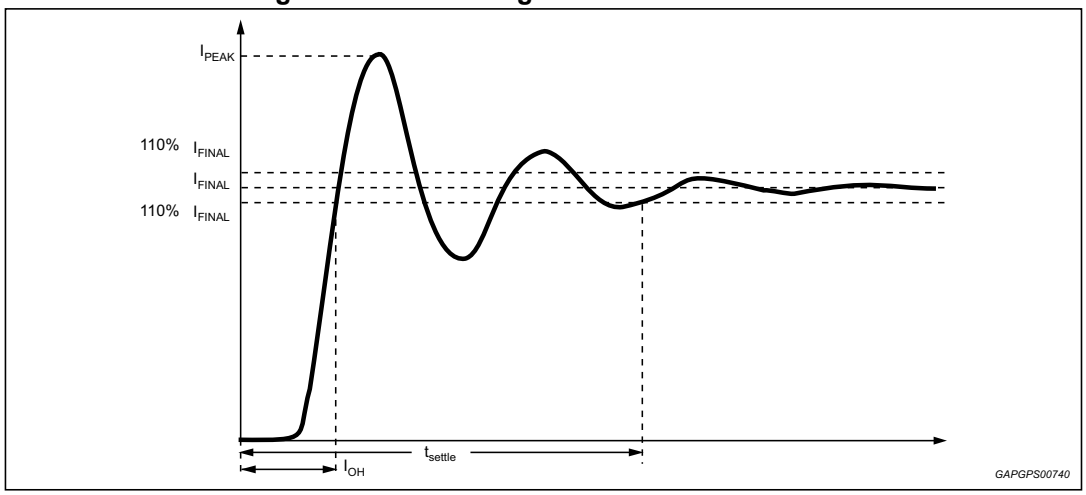
Table 7. Squib deployment drivers and diagnostics - DC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{isrcshtdwn}$	Time after voltage threshold crossed for squib pin to shutdown IISRC	Guaranteed by design	-	-	30	µs
$V_{LSDrsqb}$	Voltage threshold on squib pin to shutdown ISRC	-	0.8	-	2.2	V
t_{R_WAIT}	Rmeas wait time 6	Wait time before AOUT voltage is stable for ADC reading	-	-	300	µs
FENx Input pins						
$t_{FENfilter}$	Minimum pulse width	-	12	-	16	µs
I_{FENPD}	Internal pull-down current	VIN = VIL to VDD	20	-	50	µA
V_{FENLO}	Input low voltage threshold	-	0.8	-		V
V_{FENHI}	Input high voltage threshold	-	-	-	2.0	V
$T_{FENLATCH}$	FEN Latch timer	-	0	-	512	ms
t_{FLACC}	FEN latch timer accuracy	-	- 20%	-	20	%
Deployment drivers						
$T_{RESOLUTION}$	Diagnostic timing / resolution	Guaranteed by design, $I_{HS} \geq I_{MEAS}$, $0s \leq T_{MEASURE\_TIME} \leq 3.7$ ms $C_{SQUIB\_HI} = 0.12$ µF $C_{SQUIB\_LO} = 0.12$ µF	22.5	25	27.5	µs
$T_{ACCURACY}$	Diagnostic timing accuracy		-	-	2	LSB
I_{MEAS}	High side driver current limit detect threshold	Guaranteed by design	I_{HSX} x 0.90	-	I_{HSX} x 0.99	A
$V_{breakdown}$	HS or LS breakdown voltage	Voltage across driver = 40 V	-	-	50	µA
$R_{DSonTOTAL}$	Total high and low side MOS on resistance	High side MOS + low side MOS D9:D8="11"; V_{RES} = 7 V; I = 1.6A @95 °C	-	-	2.0	Ω
R_{DSonHS}	High side MOS on resistance	D9:D8="11"; VRES = 7 V; IVRES = 1.6 A;	-	0.3	0.8	Ω
R_{DSonLS}	Low side MOS on resistance		-	0.6	1.2	Ω

Table 7. Squib deployment drivers and diagnostics - DC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{HS_12A}	High side deployment current limit	Configuration mode 1 bits D9:D8=”00” SQHx shorted to ground; V_{RES} = 7 to 37 V	1.21	-	1.47	A
I_{HS_15A}		Configuration Mode 1 bits D9:D8=”01” SQHx shorted to ground; V_{RES} = 7 to 25 V	1.51	-	1.85	A
I_{HS_175A}		Configuration Mode 1 bits D9:D8=”11” SQHx shorted to ground; V_{RES} = 7 to 37 V	1.76	-	2.14	A
t_{ILIM}	Low side MOS shutdown under short to battery	V_{sqblo}=18 V	90	-	110	µs
I_{LS}	Low side MOS current limit		2.2	-	4.0	A
t_{settle}	Firing current settling time	Time from fire command CS_D rising edge to where firing current remains within specified limits C_{SQUIB_HI} = 0 to 0.12 µF C_{SQUIB_LO} = 0 to 0.12 µF	-	-	150	µs
$t_{DEPLOY-2ms}$	Deployment time	V_{RES} = 7 to 37 V@ I_{HS_12A} V_{RES} = 7 to 25 V@ I_{HS_15A} For I_{HS_12A} and I_{HS_15A} Firing Measured from CS_D rising edge	2.15	-	2.5	ms
$t_{DEPLOY-1ms}$		V_{RES} = 7 to 37 V For I_{HS_175A} Firing Measured from CS_D rising edge	1.15	-	1.40	ms
$t_{DEPLOY-0.65ms}$		V_{RES} = 7 to 37 V For I_{HS_175A} Firing current Measured from CS_D rising edge	0.65	-	0.85	ms

Figure 2. MOS settling time and turn-on time 2



2.4.3 Electrical characteristics - Satellite interface

4.9 V ≤ V_{DD} ≤ 5.1 V; 7 V ≤ V_{RESX} ≤ 37V; 7 V ≤ V_{SDIAG} ≤ 37 V; (V_{SATS} + 6.5V) ≤ V_{SYNC} ≤ 25 V; 5 V ≤ V_{SATS} ≤ 14 V; FEN1 = FEN2 = FEN3 = FEN4 = V_{DD}; R_REF = 10 kΩ, ±1%, 100 PPM; -40 °C ≤ T_A ≤ +95 °C; unless other specified.

Table 8. Satellite interface - DC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{ICHx\_IDLELim}$	Current limit per channel during communication voltage level	High side short to -0.3 V	-75	-	-150	mA
I_{ICHx_HVLim}	Current limit per channel during sync voltage level	High side short to -0.3 V	-100	-	-280	mA
I_{VSATS_max}	VSATS supply current excluding ICHx current	All channels with High side short to -0.3V	-	-	10	mA
$I_{VSATSLIM1}$	VSATS supply current with one channel in current limit during Sync Pulse	High side short to -0.3 V	-	-	-40	mA
$I_{VSYNCLIM1}$	VSYNC supply current per channel with channel in current limit	High side short to -0.3 V	100	-	375	mA
$I_{ICHx\_SB\_OFF}$	Short to battery current when driver is OFF.	ICHx short to battery V(ICHX)-VSATS > 50 mV 50 mV is the maximum threshold to switch OFF driver, TYP is 30 mV	-	-	5	mA
$I_{ICHx\_SB\_ON}$	Max short to battery current when driver is ON.	Guaranteed by design	-	-	25	mA
$I_{ICHxVSATS\_LK\ OFF}$	V_{SATS} leakage current per channel	V_{SATS} =18 V V_{cc} = V_{SYNC} = 0 V measured @ V_{SATS}	-	-	-1	mA

Table 8. Satellite interface - DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{ICHxVSYNC\_LK OFF}$	VSYNC leakage current per channel	V_{SYNC} = 25 V V_{cc} = V_{SATS} = 0 V measured @ V_{SYNC}	-	-	-1	mA
$I_{OUTLEAK}$	Output Leakage Current ICHX	V_{SATS} = 18 V measured @ pin under test V_{SYNC} = 25 V Analog interface OFF	-	-	1	µA
Vhdp	High side voltage drop (VSATS-VICHX) Per Channel	I = -150 mA; V_{SATS} = 7 V to 14V guaranteed by design	-	-	3.0	V
		I = -70 mA; V_{SATS} = 7 V to 14 V	-	-	1.5	V
		I = -50 mA; V_{SATS} = 7 V to 14 V	-	-	1.0	V
		I = -25 mA; V_{SATS} = 7 V to 14 V	-	-	0.5	V
IFr	IF/I_{out} CH3 & CH4	I_{out} = -5 0 mA	460	-	540	µA
		I_{out} = -5 mA	46	-	54	µA
Itr	Low to high transition current threshold	SPI channel configuration bit <2:0>=111	35.10	-	42.90	mA
		bit <2:0>=110	28.80	-	34.20	mA
		bit <2:0>=101	24.85	-	29.15	mA
		bit <2:0>=100	20.25	-	24.75	mA
		bit <2:0>=011	17.10	-	20.90	mA
		bit <2:0>=010	14.85	-	18.15	mA
		bit <2:0>=001	8.0	-	11.0	mA
		bit <2:0>=000	1.0	-	4.0	mA
V_{CLAMP}	IF/Vx CH3 & CH4 clamp voltage	R_{ext} = 33.0k, 1%; CHx is shorted to GND	0.95* Vdd	-	1.05* Vdd	V
I_{hyst}	Current Threshold hysteresis	Sink current = Ithr at the output (ICHX). Ihyst = trip point high – trip point low	0.05*Itr	-	0.15*Itr	mA
Mdf	De-glitch filter as a function of protocol speed	Manchester Protocol Excluding Osc tolerance; bit<8:7>= 00, 01, 10, 11. bit Time = the smallest bit time allowed in the selected range.	11.7% *bit-Time	-	23.5% *bit-Time	µs

Table 8. Satellite interface - DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Bitr	Minimum frequency operating range (Incoming messages fall within this operating range is guaranteed to be accepted by the IC)	Channel configurations bit<8:7> = 00 Test at frq. = 52.33 kHz Test at frq. =13.32 kHz	13.32	-	52.33	kHz
		bit<8:7> =01Test at frq =110.74 kHz Test at frq. = 26.32 kHz	26.32	-	110.74	kHz
		bit<8:7> =10 Test at frq =164.20 kHz Test at frq = 43.50 kHz	43.50	-	164.20	kHz
		bit<8:7>=11 Test at frq. = 250.63 kHz Test at frq. = 62.66 kHz	62.66	-	250.63	kHz
Bitr	Maximum frequency operating range (Incoming messages fall outside this operating range is guaranteed to be rejected by the IC)	Channel configurations bit<8:7> = 00 Test at frq. > 59.14 kHz Test at frq. <11.99 kHz	11.99	-	59.14	kHz
		bit<8:7> =01 Test at frq > 128.37 kHz Test at frq < 23.57 kHz	23.57	-	128.37	kHz
		bit<8:7> =10 Test at frq >194.93 kHz Test at frq < 38.71 kHz	38.71	-	194.93	kHz
		bit<8:7>=11 Test at frq > 309.6 kHz Test at frq < 55.37 kHz	55.37	-	309.6	kHz
Idle	Idle time	CRC disabled: The idle bit time is based on the bit time calculated using the start bits based on the last edge of previous message to 1st rising edge (start bit) of new message If an error is detected then the device shall default to 1.5 times the maximum frequency (minimum bit time). No idle time required after enabling channel	1.5*Tbit	-	-	µs
		CRC enabled:	1.5*Tbit +4µs	-	-	
Tdl & Tdh	IFx/Vx delay	Test with 10K 1% Iref resistor check response from changing between the following current levels. High = 0 to 15 mA, Low = 66 to 15 0mA	-	1	-	µs
Tdl - Tdh	IFx/Vx delay time differential	ICHX outputs with a 500 µs symmetrical pulse in and 500us out.	-	-	0.3	µs

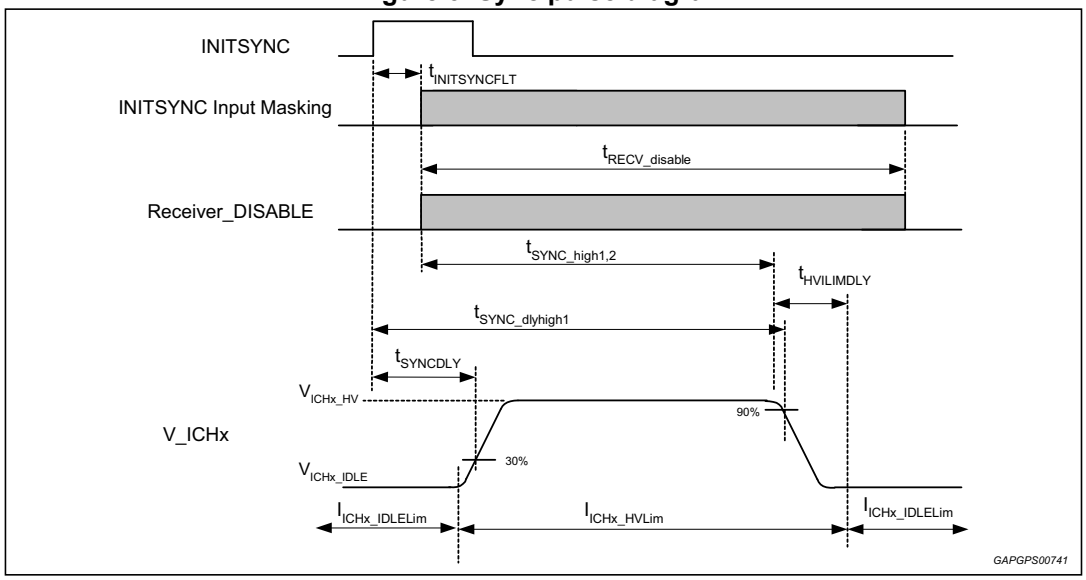
Table 8. Satellite interface - DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{Flt_BATT}	Output fault filter for short to battery	V(ICHX)-VSATS>50mV	12	-	16	µs
t_{Flt_GND}	Output fault filter for short to ground	I_sensor>I_lim	300	-	360	µs
Receive Mode						
V_{ICHx}	Output voltage on pin ICHx (x = 1…4)	I_{ICHx}= [0…50mA]; 7V ≤ V_{SATS} ≤ 14V	VSAT-1	-	VSAT	V
SYNC Mode and High Voltage mode						
V_{ICHx_HV}	Output voltage during High Voltage Mode and SYNC Mode High time	7V ≤ V_{SATS} ≤ 14V (V_{SATS}+6V) ≤ VSYNC ≤ 25V I_{ICHx} = 50mA	V_{ICHx} +4	-	V_{ICHx} +8	V
V_{REG_DO}	Regulator Drop Out voltage	I_{ICHx} = 50mA	-	-	2.5	V
$t_{SYNCDLY}$	Delay time from rising edge of INITSYNC pin to sync pulse voltage active	Measured from INITSYNC pin rising edge to 5% of V_{HV} All Channels	2.7	-	6.6	µs
t_{SYNC_high1}	SYNC pulse high time	-	-7%	20	+ 7%	µs
$t_{SYNC\_dlyhigh1}$	Total delay time from INITSYNC to sync pulse falling edge	MCR D9:D8=”00” Measured from INITSYNC pin rising edge to 90% of sync pulse falling edge (V ICHx_HV - V ICHx idle) All Channels using default slew rate	20.3	-	28	µs
t_{SYNC_high2}	SYNC pulse high time	-	-7%	30	+ 7%	µs
t_{SYNC_high3}	SYNC pulse high time data “0” pulse width (High voltage mode)	-	-7%	40	+ 7%	µs
t_{SYNC_high4}	SYNC pulse high time data “1” pulse width (High voltage mode)	-	-7%	80	+ 7%	µs
$t_{RECV\_disable}$	Receiver disable time	MCR bit D2=0	-7%	62	+ 7%	µs
		MCR bit D2=1	-7%	t_{SYNC_highx} typ + 20µs	+ 7%	µs
$t_{riseslewrate}$	High Voltage rise slew rate for ICHx	MCR bit D3=0	0.9	-	2	V/µs
		MCR bit D3=1	0.43	-	1.5	
$t_{fallslewrate}$	High Voltage fall slew rate for ICHx	MCR bit D3=0	0.9	-	2	V/µs
		MCR bit D3=1	0.43	-	1.5	

Table 8. Satellite interface - DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{HVILIMDLY}$	HV current limit active time following t_{SYNC_highx}	Guaranteed by design	-	-	12	µs
C_{ICHX}	Capacitance on satellite output for stability (per pin)	ICHx pin to $C_{ICHX} \leq$ 70nH;	10	-	47	nF
INITSYNC input						
$V_{INITSYNCLO}$	Input low voltage threshold	-	0	-	0.8	V
$V_{INITSYNCHI}$	Input high voltage threshold	-	2.0	-	1.0 x VDD	V
I_{ISPD}	Input pulldown current INITSYNC	VIN = VIL to VDD	10	-	50	µA
$T_{INITSYNCFLT}$	Minimum pulse width	-	1.7	-	2.1	µs

Figure 3. Sync pulse diagram



2.4.4 SPI timing

All SPI timing is performed with a 150 pF load on MISO unless otherwise noted

$4.9V \le V_{DD} \le 5.1V$; $7V \le V_{RESX} \le 37V$; $7V \le V_{SDIAG} \le 37V$; $(V_{SATS} + 6V) \le V_{SYNC} \le 25V$; $5V \le V_{SATS} \le 14V$; FEN1 = FEN2 = FEN3 = FEN4 = V_{DD}; R_REF = 10KΩ, ±1%, 100PPM; $-40°C \le T_A \le +95°C$; unless other specified.

Table 9. SPI timing - DC electrical characteristics

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit
-	fop	Transfer frequency	dc	-	5.50	MHz
1	tSCK	SCLK, SCLK_S period	181	-	-	ns
2	tLEAD	Enable lead time	65	-	-	ns
3	tLAG	Enable lag time	50	-	-	ns
4	tSCLKHS	SCLK, SCLK_S high time	65	-	-	ns
5	tSCLKLS	SCLK, SCLK_S low time	65	-	-	ns
6	tSUS	MOSI, MOSI_S input setup time	20	-	-	ns
7	tHS	MOSI, MOSI_S input hold time	20	-	-	ns
8	tA	MISO, MISO_S access time	-	-	60	ns
9	tDIS (1)	MISO, MISO_S disable time	-	-	100	ns
10	tVS	MISO, MISO_S output valid time	-	-	60	ns
11	tHO (1)	MISO, MISO_S output hold time	0	-	-	ns
12	tRO	Rise Time (design information)	-	-	30	ns
13	tFO	Fall Time (design information)	-	-	30	ns
14	tCSN	CS_D, CS_S negated time	640	-	-	ns
15	tCLKN	Time between CS rising edge and first transition of SCLK must be higher than tCLKN. It happens when multiple L9662 are connected to the same SCLK and MOSI but with different chip select.	500	-	-	ns

1. Parameters t_{DIS} and t_{HO} shall be measured with no additional capacitive load beyond the normal test fixture capacitance on the MISO pin. Additional capacitance during the disable time test erroneously extends the measured output disable time, and minimum capacitance on MISO is the worst case for output hold time.

Figure 4. SPI timing diagram

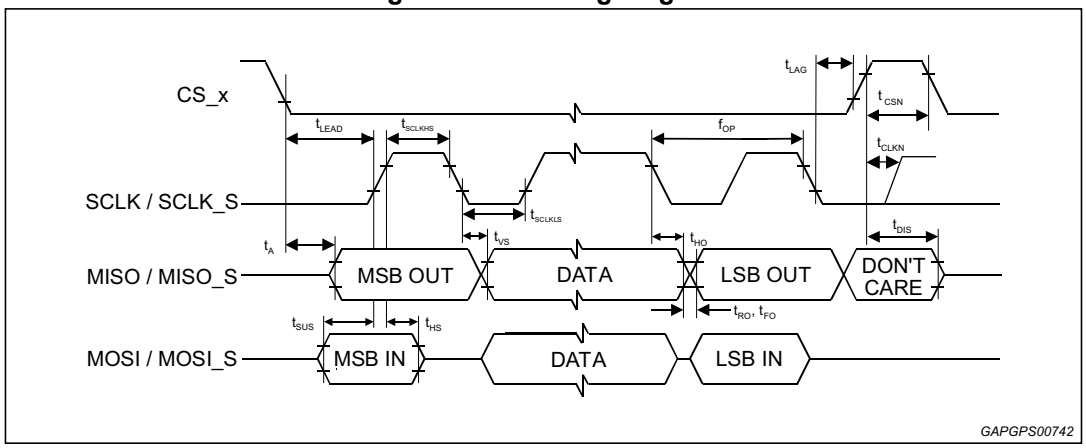
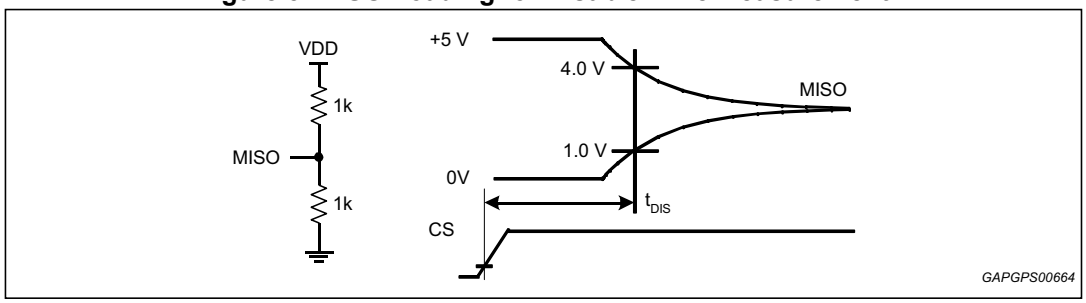


Figure 5. MISO Loading for Disable Time Measurement



3 Functional description

3.1 Overview

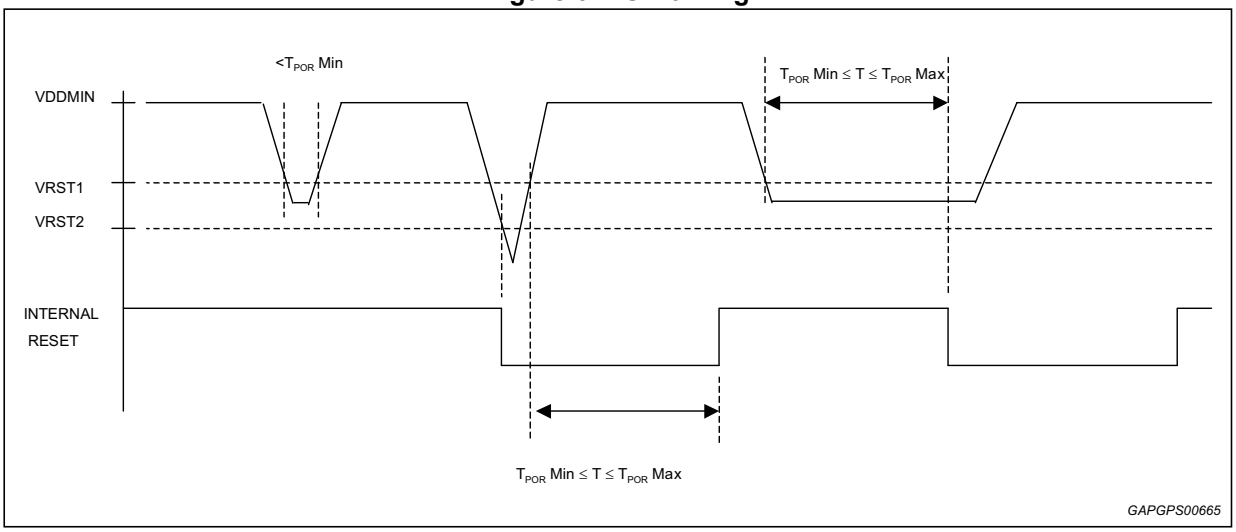
The device is an integrated circuit to be used in air bag systems. Its main functions include deployment of air bags and switched-power sources to satellite sensors. The device supports 8 deployment loops and 4 satellite-sensor interfaces.

3.2 General functions

3.2.1 Power on reset (POR)

The ASIC has a power on reset (POR) circuit, which monitors VDD voltage. When VDD voltage falls below V_{RST1} for longer than or equal to t_{POR}, all outputs are disabled and all internal registers are reset to their default condition. A second reset level, V_{RST2}, also monitors VDD but uses no filter time and will disable all outputs and all internal registers are reset to their default condition when VDD falls below the reset threshold.

Figure 6. POR timing



3.2.2 RESETB

The RESETB pin is active low. The effects of RESETB are similar to those of a POR event, except during a deployment. When a deployment is in-progress, the ASIC will ignore the RESETB signal.

However, it shall shut itself down as soon as it detects a POR condition. When the deployment is completed and RESETB signal is asserted, the device disables its outputs and reset its internal registers to their default states.

A de-glitch timer is provided for the RESETB pin. The timer protects this pin against spurious glitches. The ASIC neglects RESETB signal if it is asserted for shorter than t_{GLITCH}. RESETB has an internal pull-up in case of an open circuit.

3.2.3 Reference resistor

IREF pin shall be connected to VDD supply through a resistor, RIREF. When the device detects the resistor on IREF pin is larger than RIREF_H or smaller than RIREF_L, it goes into a reset condition. All outputs are disabled and all internal registers are reset to their default conditions.

3.2.4 Loss of ground

GND

When the GND pin is disconnected from PC-board ground, the ASIC goes in reset condition. All outputs are disabled and all internal registers are reset to their default conditions.

GND0-GND7

A loss of power-ground (GND0 – GND7) pin/s disables the respective low side driver/s on SQLx. However, the high side driver of the respective channel will still be able to be turned on. Thus under the scenario where the low side is shorted to ground the device will be able to provide the programmed firing current for the specified time.

An open GNDx connection on any channel has no affect on the other channels. An open GNDx condition will be detected using the low side MOS diagnostics.

AGND

The AGND pin is a reference for AOUT pin. When AGND loses its connection, the voltage on AOUT pin is pulled up to VDD voltage. The rest of functionality and parametric is not affected by a loss of AGND condition.

3.2.5 VRESx capacitance

To ensure all diagnostics function properly a typical capacitor of equal to or greater than 68nF is required for every 4 VRESx pins and located close to the supply pins. Thus a capacitor will be placed close to the VRES0, 1,2, and 3 pins and a second capacitor will be close to the VRES4, 5,6, and 7 pins.

3.2.6 Supply voltages

The primary current sources for the different functions of the ASIC are as follows:

- VRESx - Firing currents along with HSS and HS FET diagnostic currents
- VSDIAG - Squib resistance and HSS diagnostics
- VSATS - Voltage and current necessary for satellite operation excluding period during sync pulse
- VSYNC - Sync pulse voltage
- VDD will be used for all internal functions as well as short to battery/ground and high squib resistance diagnostics.

3.2.7 Ground connections

The GND pins (6, 38, and 45) are all common internal to the ASIC. A ground plane is needed to directly connect the GND pins together so that low impedance is maintained between the two pins. This ground plane needs to be isolated from the high current ground for the squib drivers to prevent voltage shifts.

3.3 Serial peripheral interface (SPI)

The device contains 2 serial peripheral interfaces for control of the satellite and squib functions. The 2 SPI interfaces are completely independent from each other and can be accessed simultaneously. The following table shows the distribution of features that are accessed/controlled for each of the SPIs

Table 10. Features that are accessed/controlled for each of the SPIs

Type	Function	Pin names	Features accessed
SPI1	Squib diagnostic & deployment SPI	SCLK MISO MOSI CS_D	All Squib Diagnostics Squib related status information Squib Arming and Firing Software Reset Component ID & Revision
SPI2	Satellite SPI	SCLK_S MISO_S MOSI_S CS_S	Satellite Channel Diagnostics Satellite Communication Data Channel Configuration

The software reset accessed over SPI1 will not only reset squib functions but all the satellite functions. The device has a counter to verify the number of clocks in SCLK and SCLK_S. L9662 computes SPI error length flag by counting the number of SCLK/SCLK_S rising edges occurring when CS_D/CS_S is active. If the number of clocks in SCLK is not equal to 16 clocks while CS_D is asserted, it ignores the SPI message and sends a SPI fault response. If the number of clocks in SCLK_S is not equal to 80 clocks while CS_S is asserted it ignores the entire SPI message and a fault will be reported in the SR frame. The MISO output on SPI1 shall hold the 16_{th} bit's state for SCLK rising edges greater than 16 when CS_D is active, similarly the MISO output on SPI2 shall hold the 80^{th} bit's state for SCLK_S rising edges greater than 80 when CS_S is active.

3.3.1 SPI pin descriptions

Chip select (CS_D, CS_S)

Chip-select inputs select the device for serial transfers. CS_D or CS_S can be asserted at any given time and are active low. Both CS_D and CS_S inputs can be selected simultaneously. When chip-select is asserted, the respective MISO/MISO_S pin is released from tri-state mode, and all status information is latched into the SPI shift register. While chip-select is asserted, register data is shifted into MOSI/MOSI_S pin and shifted out of MISO/MISO_S pin on each subsequent SCLK/ SCLK_S. When chip-select is negated, MISO/MISO_S pin is tri-stated. To allow sufficient time to reload the registers chip-select pin shall remain negated for at least tCSN. The chip-select inputs have current sinks which pull these pins to the negated state when there is an open circuit condition. These pins have TTL level compatible input voltages allowing proper operation with microprocessors using a 3.3 to 5.0 volt supply.

Serial clock (SCLK, SCLK_S)

SCLK/SCLK_S input is the clock signal input for synchronization of serial data transfer. This pin has TTL level compatible input voltages allowing proper operation with microprocessors

using a 3.3 to 5.0 volt supply. When chip select is asserted, both the SPI master and this device shall latch input data on the rising edge of SCLK/SCLK_S. The ASIC shifts data out on the falling edge of SCLK/SCLK_S.

Serial data output (MISO, MISO_S)

MISO/MISO_S output pins shall be in a tri-state condition when chip select is negated. When chip select is asserted, the MSB is the first bit of the word/byte transmitted on MISO/MISO_S and the LSB is the last bit of the word/byte transmitted. This pin supplies a rail to rail output, so if interfaced to a microprocessor that is using a lower VDD supply, the appropriate microprocessor input pin shall not sink more than IOH(min) and shall not clamp the MISO/MISO_S output voltage to less than VOH(min) while MISO/MISO_S pin is in a logic “1” state.

Serial data input (MOSI, MOSI_S)

MOSI/MOSI_S inputs take data from the master processor while chip select is asserted. The MSB shall be the first bit of each word/byte received on MOSI/MOSI_S and the LSB shall be the last bit of each word/byte received.

This pin has TTL level compatible input voltages allowing proper operation with microprocessors using a 3.3 to 5.0 volt supply.

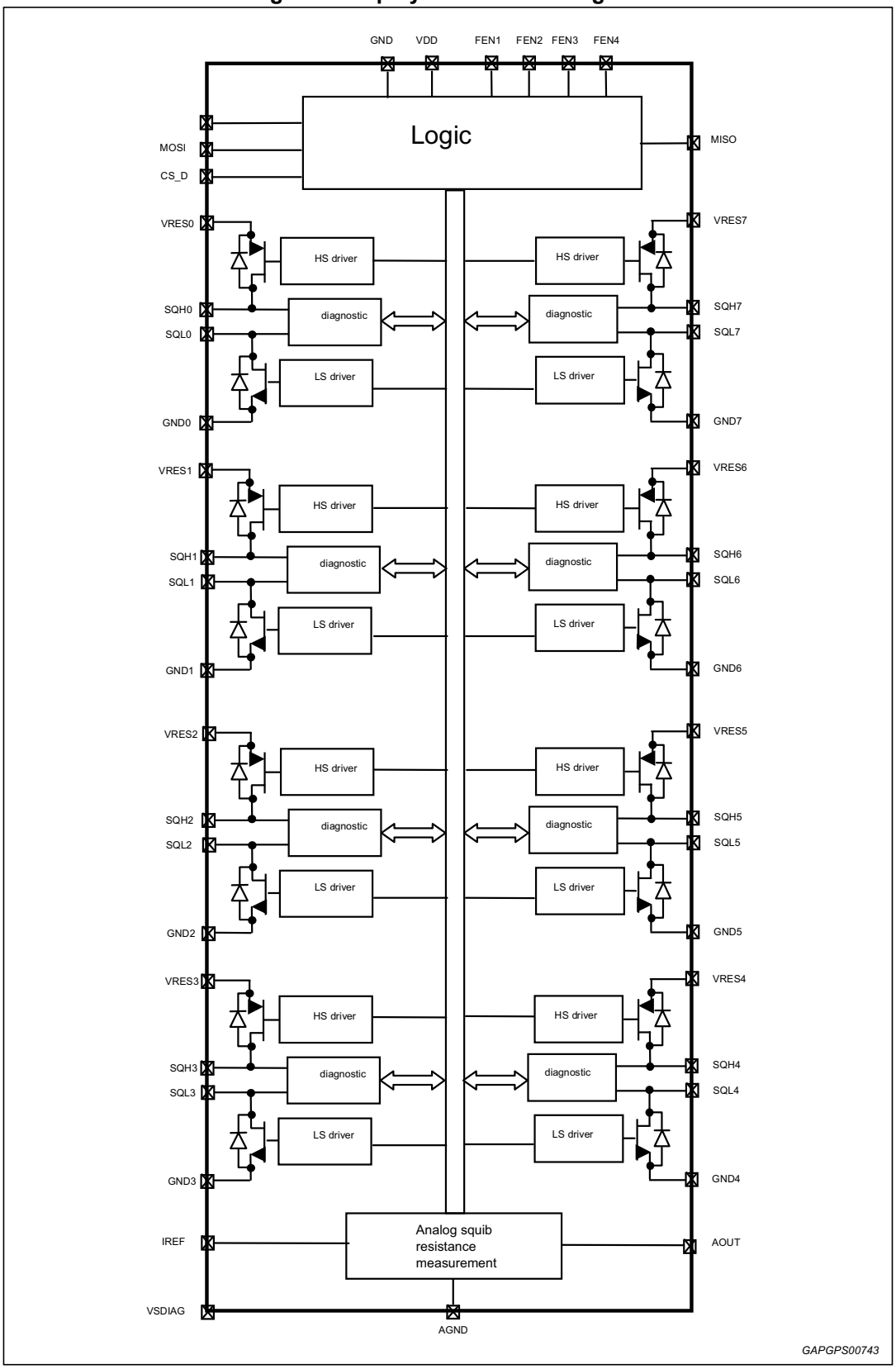
3.4 Squib drivers

3.4.1 Firing

The on-chip deployment drivers are designed to deliver 1.2 A (min) for 2 ms (min) and 1.75 A (min) for 1 ms (min) with VRESx voltages between 7 V and 37 V. In addition the device can provide 1.5 A minimum for 2 ms for VRESx voltages between 7 V and 25 V. The firing condition is selectable via the SPI. At the end of a deployment, a deploy success flag is asserted and can be read using the appropriate SPI command. Each VRESx and GNDx connection is used to accommodate 8 loops that can be deployed simultaneously.

Upon receiving a valid deployment condition, the respective SQHx and SQLx drivers are turned on. The only other activation of the SQHx and SQLx drivers is momentarily during a MOS diagnostic. Otherwise, SQHx and SQLx are inactive under any normal, fault, or transient conditions. Upon a successful deployment of the respective SQHx and SQLx drivers, a deploy command success flag is asserted via SPI. Refer to *Figure 8* for the valid conditions and the deploy success flag timing.

Figure 7. Deployment drivers diagram



The ASIC shall be protected against inadvertent turn on of the firing drivers unless the appropriate conditions are present. Non-typical conditions shall not cause driver activation. This includes the case where VRESx and/or VSDIAG pins are connected to a supply up to 40V and VDD is between 0V and VDD min. Under these conditions the device shall ensure that driver activation will not occur. No flow of current shall be allowed through the SQHx and SQLx pins.

Driver activation

The firing of a squib driver requires the appropriate FEN function to be active and two separate sixteen bit writes to be made over the SPI1. The FEN function is defined as the result of the FENx pin OR'd with the internal FENx latch. The FENx pin going high initiates the FEN function. With the FEN 1 function being active and the appropriate Arm and Fire commands sent then Squib_1 & 2 drivers would be activated. With the FEN 2 function being active and the appropriate Arm and Fire commands sent then Squib_3 & 4 drivers would be activated.

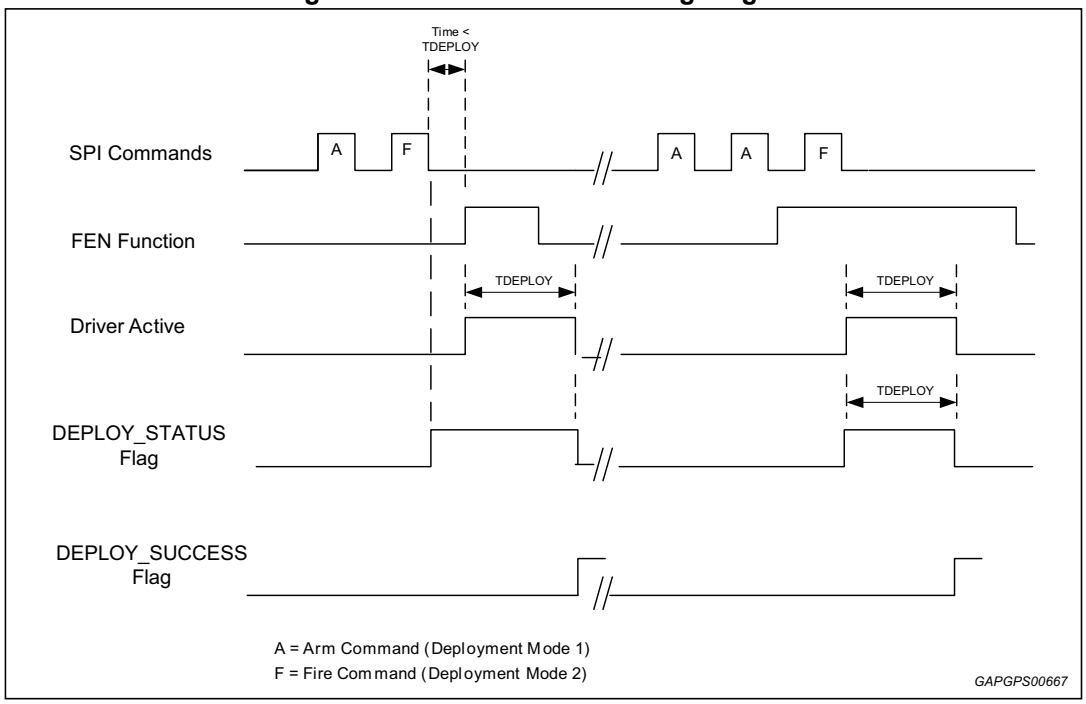
With the FEN 3 function being active and the appropriate Arm and Fire commands sent then Squib_5 & 6 drivers would be activated. With the FEN 4 function being active and the appropriate Arm and Fire commands sent then Squib_7 & 8 drivers would be activated.

The first write is to ARM the drivers in preparation of receiving the fire command. The Arm command will stop on all channels any diagnostics that are active. Any combination of squibs can be armed. The second write is to actually activate the desired driver pairs. If there is a parity mismatch the data bits will be ignored and the squib drivers will not have their status changed, and the two write sequence must then be started again. If there is a mismatch in channels selected then only those channels selected in both the Arm and Fire commands will be activated.

During the first write, when the drivers are armed, all diagnostic functions are cleared. The FIRE command must follow the ARM command along with the FEN function active in order for driver activation. If a command is between the ARM and FIRE command then the sequence must be restarted. An error response shall be received for the Fire command if the ARM/FIRE sequence is not followed.

The ARM/FIRE commands and FEN function are independent from each other. The device shall begin the t_{DEPLOY} timer once a valid ARM/FIRE sequence has been received. If a valid ARM/FIRE command has been sent and the FEN function is inactive then the drivers will not be activated but the t_{DEPLOY} timer shall start. If the FEN function becomes active before t_{DEPLOY} has expired then the drivers will become active for the full t_{DEPLOY} time. If the FEN does not become active before t_{DEPLOY} has expired then the sequence would need to be restarted. A diagram illustrating this is shown in *Figure 8*

Figure 8. Driver activation timing diagram



Only the channels selected in the ARM and, directly following, the FIRE command will be able to be activated.

By reading the appropriate registers a status of the deployment is provided. If a valid Arm/Fire sequence has been provided the status flag will become active. This flag shall remain active for as long as the T_{DEPLOY} timer is counting. Depending on the state of the FEN function the DEPLOY_STATUS flag will be active a minimum of TDEPLOY and a maximum of 2 x TDEPLOY. If driver activation did occur (both a valid Arm/Fire sequence and the appropriate FEN function active within the appropriate time) then the DEPLOY_SUCCESS flag will be active. This flag will be active until cleared by software. If a valid Arm/Fire sequence did occur but the FEN function was never activated within the T_{DEPLOY} time then the DEPLOY_SUCCESS flag will remain '0'.

During driver activation the respective high side (SQHx) and low side (SQLx) drivers will turn on for t_{DEPLOY}.

Device driver activation will not occur or, if firing is in process, will terminate under the following conditions:

- Power On Reset (POR)
- IREF resistance is larger than RIREF_H or smaller than RIREF_L
- Loss of ground condition on GND pin

The following conditions are ignored when driver activation is in-progress:

- RESETB
- Valid soft reset sequences
- SPI1 commands except as noted below Response for ignored commands will be 0xD009
- FEN function

Table 11. SPI1 MOSI/MISO response

SPI1 MOSI	SPI1 MISO	Response
Configuration Commands	SPI fault response	MOSI register mode messages shall be ignored
Deployment Commands	Command mode	Execute for channels not in deployment; no effect to deploying channel
Diagnostic Commands	SPI fault response	MOSI diagnostic mode messages shall be ignored
Monitor Commands	Status response	Execute for all channels

Note: SPI MISO sent in the next SPI transmission.

The device can only deploy a channel when the FEN function is active. Once the drivers are active the device shall keep the drivers on for the required duration regardless of the FEN state. Once completed, a status bit will be set to indicate firing is complete.

3.4.2 Firing current measurement

All channels have a 7 bit current measurement register that is used to measure the amount of time the current is above I_{MEAS} during firing. The maximum measurement for each channel is 3.175 ms nominal based on a bit weight of 25 ms. The current measurement register shall not increment outside the deployment time. The current measurement will begin incrementing once the current has exceeded 95% of the nominal target value. The count will continue to increment from the stored value until either a clear command has been issued for that channel or all ‘1’s are present in the corresponding channel measurement register. If all ‘1’s are present for a channel’s measurement register and another firing sequence has been issued the register shall remain all ‘1’s. Only if a clear command has been issued will that particular register be reset to all ‘0’s. All other channels shall keep the stored measurement count. During firing the current measurement register cannot be cleared. After a clear command has been issued for a channel then the channel is ready to count if the current exceeds the specified level. After a POR or software reset the device shall reset all 8 measurement registers to all ‘0’s.

A “real-time” current measurement status of all the channels is available. If a current limit status request is sent then the device shall report in the next SPI transfer whether the current is above or below I_{MEAS} for each of the channels. The current status results can be read at any time and shall correctly report whether current is flowing. The content of the internal current status register is captured on the falling edge of chip select during the SPI response. The internal status register is updated at a nominal sample time of 25 µs and is independent of SPI transfers.

For this circuit there is continuously being performed compensation of the comparator to remove offset errors, which is independent from SPI commands. Compensation is performed every 12.8 µs based on the internal clock.

3.4.3 Fire enable (FEN) function description

The Fire Enable (FEN) function is the result of the FENx input OR’d with the internal FEN latch. If the FEN latch is not enabled and the FENx pin is low then activation of the FET drivers are disabled except as indicated during the MOS test. All internal diagnostic

functions, and results, will be available through the serial interface. This pin must be pulled high to initiate the FEN latch function (if programmed) and enable firing of the FET drivers.

The FEN function will be considered active when the pin is active (‘1’ or high) for more than 12 microseconds. Tolerance range for the filter to be used will be 12 to 16 µs.

When the FENx input is active, ‘1’, the FEN function will be active. **When the FENx input state transitions from ‘1’ to ‘0’, the programmable latching function will hold the FEN function active until the timeout of the FEN timer.** The programmable latch and hold function will be capable of delays of 0ms, 128ms, 256ms, and 512ms. There are 4 independent timers with the timer for FEN1 associated with channels 1 & 2, timer for FEN2 associated with channels 3 & 4, timer for FEN3 associated with channels 5 & 6, and the timer for FEN4 associated with channels 7 & 8. **The timer is reset to the programmed time when the FENx pin transitions from ‘0’ to ‘1’.** The programmable counter delay will be set through a SPI command.

3.4.4 Squib diagnostics

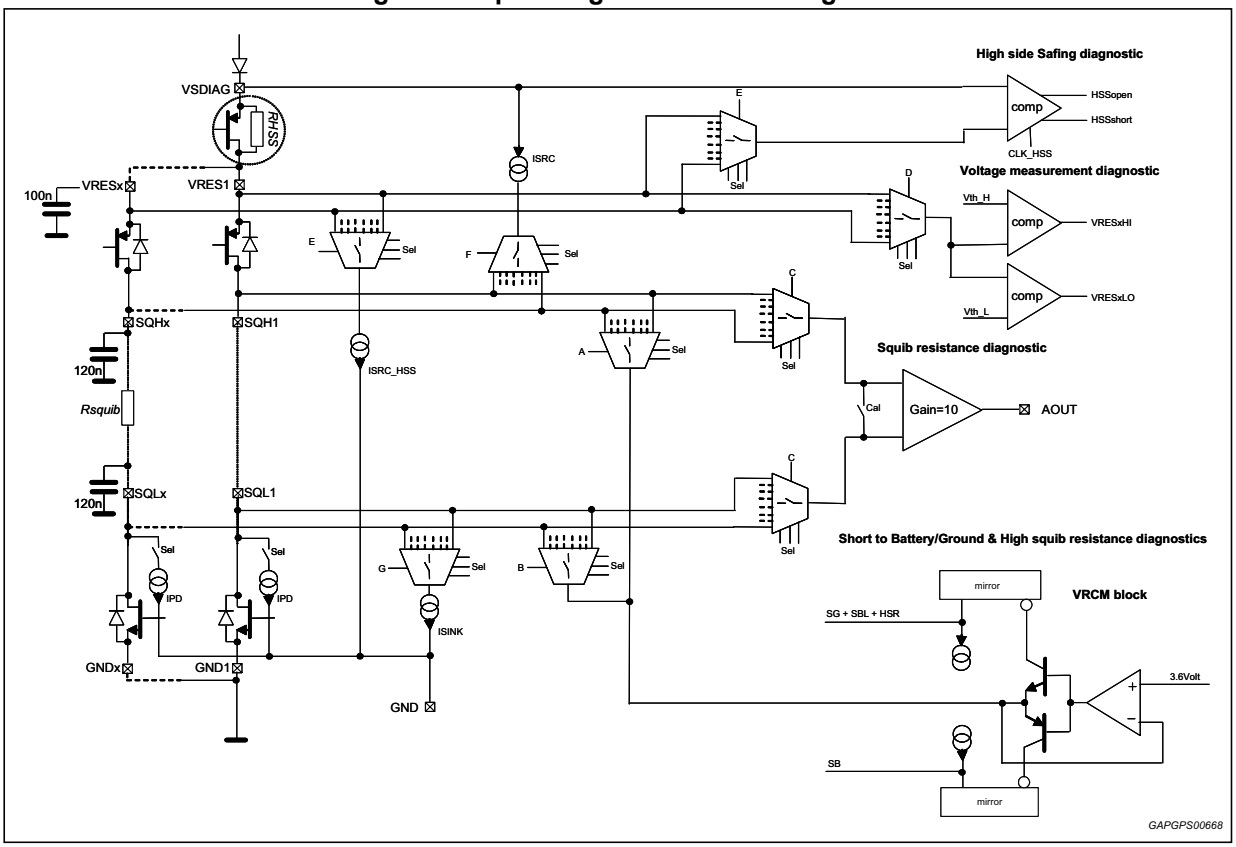
Overview

The ASIC is able to perform the following diagnostics

- Short to battery and ground on both SQHx and SQLx pins with or without a squib
- Loop to loop diagnostics
- Squib resistance measurement
- Squib High resistance
- High Side Safing FET diagnostics
- VRESx voltage status
- High and Low side FET diagnostics

Below is a block diagram showing the components involved in the squib diagnostics.

Figure 9. Squib diagnostics block diagram



Short to battery/ground and loop to loop diagnostics

The leakage diagnostic includes a short to battery, a short to ground and a short between loop tests. The test will be run for each SQHx and SQLx pin so that shorts can be detected regardless of the resistance between the squib pins.

Normal short to battery/ground diagnostics.

For the test the internal VRCM is switched on and connected to the selected pin (SQHx or SQLx). The IPD bit will be selected to be OFF which will deactivate the pulldown current on all the channels. During the test if no leakage is present the voltage on the selected SQHx or SQLx pin will be equal to VBIAS and no current is sunk or sourced by VRCM. If a leakage to ground or battery, the VRCM will sink or source a current less than ISVRCM trying to keep VBIAS. Two current comparators, ISTB and ISTG, will detect the abnormal current flow.

Loop to loop diagnostics

For this test the same procedure is followed except the pulldown current (IPD) is selected to be ON which will deactivate the pulldown current only on the channel under test with all other channel pulldown currents active. If a short to ground fault is active, assuming it was not active during normal short to battery/ground diagnostics, then that particular channel has a short to another squib loop. To detect loop to loop shorts between ASICs in the system the Stop diagnostics command with IPD enabled needs to be sent to the other ASICs before running the loop to loop diagnostics on the channel to be monitored. If the channel being monitored has a short to ground fault active, assuming it was not active

during normal short to battery/ground diagnostics, then that particular channel has a short to another squib loop in the system.

The following table indicates how faults would be interpreted.

Table 12. How faults shall be interpreted

Fault condition for channel(1)	Channel leakage diagnostics results with I_{PD} ON	Channel leakage diagnostics results with I_{PD} OFF
No Shorts	No Fault	No Fault
Short to battery	STB Fault	STB Fault
Loop to loop short	STG Fault	No Fault
Short to ground	STG Fault	STG Fault

1. Condition where 2 open channels have the SQHx pins shorted will not be detected. If one squib is open and the other has a normal squib connection then the fault will be indicated on the channel that is open. Assumes both pins are tested

Once the command is issued the state of the comparators shall be captured on the next falling edge of CS_D. The results are valid after $T_{SHORTDIAG}$ time, which is mainly dependent on the external capacitors on the squib lines.

Squib resistance measurement

During a resistance measurement, both ISRC and ISINK are switched on and connected to the selected SQHx and SQLx channel. A differential voltage is created between the SQHx and SQLx pin based in the ISRC current and resistance between the pins. The analog output pin, AOUT, will provide the resistance-measurement voltage based on the scaling factor indicated in the electrical parameters section. The tri-state output, AOUT, will be connected to an ADC input of a microprocessor. When not running squib resistance diagnostics the AOUT pin will be high impedance.

To increase accuracy of the squib resistance measurements the offset of the internal amplifier can be provided on the AOUT pin. This is done by setting the appropriate calibration bit, waiting the required time, and reading the converted AOUT voltage connected to the microprocessor ADC. In test mode, Aout pin can be used as digital/analog output for testing deployment and diagnostics comparators and thresholds. Test mode is reserved for supplier use only.

The normal measurement method for squib resistance is to take a single ended analog output measurement for a channel (V_{AOUT} with AMC bit=0) and use the tolerances and equation shown in the parametric table. The device is also capable of improving the tolerance at resistances below 3.5 Ohms by removing the offset of the differential comparator. This method involves taking the single ended analog output results for a channel (V_{AOUT} with AMC bit=0) and subtracting the internal comparator offset measurement of V_{AOUT_CAL} (V_{AOUT} with AMC bit=1). The summary of the equation for this is as follows:

$$A_{OUT\_CAL} = (V_{AOUT} - V_{AOUT\_CAL})/VDD$$

$$A_{OUT\_CAL} \text{ typical} = 0.08 \times R_{SQUIB}$$

High squib resistance diagnostics

During a high squib resistance diagnostic, VRCM and ISINK are switched ON and connected to SQHx and SQLx on the selected channel. Current flowing on SQHx will be measured and compared to IHR threshold to identify if resistance is above or below RSQHZ. The results shall be reported in the next SPI message. Once the command is issued the state of the squib resistance shall be valid after THSR captured on the next falling edge of CS_D. The voltage source for this test will be VBIAS which is based on the VDD supply.

High and low side FET diagnostics

Prior to either the HS or LS FET diagnostics being run it is required to have the VRCM switched ON. Running the leakage diagnostics with the appropriate delay time prior to either the HS or LS FET diagnostics will precondition the squib pin to the appropriate voltage level. When the FET diagnostic command is issued the flags will initially be cleared. Once this is complete there is a check to determine if the VRCM is not active or some leakage is present. If either of these conditions are present then the MOS will not be turned ON, the test will be aborted and the Fault Present (FP) bit will be set. The FEN function must be inactive for the channel under test in order to be able to run the test. The test will not start if FEN function is active on the channel under test and will result in the FP bit to be set.

If no leakage is present and FEN function is inactive, the MOS (High side or Low Side) is turned ON.

The device shall monitor the current sink or sourced by VRCM. If the MOS is working properly, this current will exceed ISTB (HS test) or ISTG (LS test) and the device shall turn off the driver under test within the specified time TSHUTOFF. If the current does not exceed ISTB or ISTG then the test will be terminated and the MOS will be switched off by the ASIC within TFETTIMEOUT. During the TFETTIMEOUT period the FET Timeout bit will be set (FT=1) and will be cleared at the expiration of the timer.

The results must be compared with the leakage diagnostic results to distinguish between a real leakage/short versus a FET fault. For high side FET diagnostics if no faults were indicated in the preceding leakage diagnostics then a normal result would be STB = 1; STG = 0 (with FT = 0; FP = 0). If the returned results for the high side FET test is not STB = 1; STG = 0 (with FT = 0; FP = 0) then either the FET is not functional, a short occurred during the test, or there is a missing VRESx connection for that channel. For low side FET diagnostics if no faults were indicated in the preceding leakage diagnostics then a normal result would be STB = 0; STG = 1 (with FT = 0; FP = 0). If the returned results for the low side FET test is not STB = 0; STG = 1 (with FT = 0; FP = 0) then either the FET is not functional, a short occurred during the test, or there is a missing GNDx connection for that channel.

On the next falling edge of CS_D, comparator results are latched and reported in the MISO response. The results will remain latched until the next test is initiated (diagnostic write command). If the test is in progress then a bit is used in the response to indicate the test completion. If the FET under test is working properly then the results shall indicate a “Short to Ground” for LS test and “Short to Battery” for HS test.

For all conditions the current on SQHx/SQLx will never exceed ISVRCM. On the squib lines there will be higher transient currents due to the presence of the filter capacitor.

High side safing diagnostics

When the command is received the ASIC will activate IHSS on the selected VRESx. The diagnostics will measure the difference between VSDIAG and VRESx. The internal comparator will detect open, short or normal condition based on the differential voltage between VSDIAG and VRESx.

The results shall be reported in the next SPI message using bits HSS1 and HSS0 as indicated in the following table. Once the command is issued the voltages shall be captured on the next falling edge of CS_D.

Table 13. High side safing diagnostics

Condition	Diagnostic Mode HSS Selection	
	HSS1	HSS0
(VSDIAG-VRESx) < $V_{HSSSHORT\_th}$	0	0
$V_{HSSSHORT\_th}$ < (VSDIAG-VRESx) < $V_{HSSOPEN\_th}$	0	1
$V_{HSSOPEN\_th}$ < (VSDIAG-VRESx)	1	1

Voltage measurement diagnostics (VRESx)

When the command is received the ASIC will activate a comparator for the selected channel. A 2 bit indication of the state of the VRESx pins shall be reported as indicated below. The results shall be reported in the next SPI message. Once the command is issued the voltages shall be captured on the next falling edge of CS_D.

Table 14. Voltage measurement diagnostics

Condition	Diagnostic mode 3 VRESx selection	
	VR1	VR0
V_{RESx} < $V_{VRESXLO\_th}$	0	0
$V_{VRESXLO\_th}$ < V_{RESx} < $V_{VRESXHI\_th}$	0	1
$V_{VRESXHI\_th}$ < V_{RESx}	1	1

Loss of ground

When any of the power grounds (GND0 – 7) are lost, no deployment can occur on the respective deployment channels because the low side driver will be inactive. The high side driver for the respective channel can still be activated.

A loss of ground condition on one or several channels will not affect the operation of the remaining channels. When a loss of ground condition occurs, the source of the low side MOS will be floating. In this case, no current will flow through the low side driver.

This condition will be detected as a fault by a low side MOS diagnostic. No additional faults will be reported from any other diagnostic due to this condition.

3.4.5 SPI register definition for squib functions

The SPI provides access to read/write to the registers internal to the device. All commands and responses sent to/from the ASIC on SPI1 shall use set D13 as required for odd parity on the 16 bit word. The responses to the commands are sent in the next valid CS_D.

The table below summarizes the MISO register mode response of various events and MOSI messages. After POR event, RESETB negated, and loss of GND, the device sends 0x0000 in MISO for the first SPI transmission.

The MISO response shown here is the one received in the next valid SPI transmission after each event or MOSI write.

Table 15. MISO responses to various events

Event/MOSI message	MISO response
MOSI Parity error or message error during a deployment	0xD000
MOSI transmission - Incorrect number of clocks/bits	0xD003
Incorrect firing sequence received (Firing Command without a valid Arm Command)	0xD005
Error due to message not allowed during deployment	0xD009
POR	0x0000
RESETB	0x0000
LOSS OF GND	0x0000
RIREF out of range	0x0000
MOSI Write Soft Reset: $AA	0x1X02
MOSI Write Soft Reset: $55 (after $AA)	0x2003

Note: X in software reset response should be interpreted as follows: D11=1;D10=0;D9:D8=CL bits

The SPI fault responses (0xD000 or 0xD003) indicate a fault in the last MOSI transmission. The device uses the parity bit to determine the integrity of the MOSI command transmission.

Squib SPI commands

The following modes are supported by the squib ASIC using SPI1.

- Configuration mode
- Deployment mode
- Diagnostic mode
- Monitor mode

The table below is a summary of the modes and the functions that are achieved by sending the particular MOSI command. The following sections will provide a full description of bit settings for each mode. All commands and responses use D13 to achieve odd parity.

Table 16. Command description summary

Command/mode	Description	Mode bits								
		D15	D14	D13	D12	D11	D10	D09	D08	D07 - D00
Configuration commands										
Config. Mode 1	Current limit programming and software reset	0	0	P	-	-	0	-	-	-
Config. Mode 2	FEN latch time Programming	0	0	P	-	-	1	-	-	-
Deployment commands										
Deployment Mode 1	Arming Command	0	1	P	1	1	0	0	1	-
Deployment Mode 2	Firing Command	0	1	P	0	0	0	0	0	-
Diagnostic commands										
Diagnostic Mode 1	Disable Diagnostic	1	0	P	-	0	0	0	-	-
Diagnostic Mode 2	Short to battery & ground diagnostics Short between loop diagnostics	1	0	P	-	0	0	1	-	-
Diagnostic Mode 3	VRESx voltage diagnostics	1	0	P	-	0	1	0	-	-
Diagnostic Mode 4	High Side Safing diagnostics	1	0	P	-	0	1	1	-	-
Diagnostic Mode 5	Squib Resistance Diagnostics	1	0	P	-	1	0	0	-	-
Diagnostic Mode 6	High Squib Resistance Diagnostics	1	0	P	-	1	0	1	-	-
Diagnostic Mode 7	LS driver diagnostics	1	0	P	-	1	1	0	-	-
Diagnostic Mode 8	HS driver diagnostics	1	0	P	-	1	1	1	-	-
Monitor commands										
Monitor Mode 1	Deployment status	1	1	P	-	0	0	-	-	-
Monitor Mode 2	Channel current limit measurement information	1	1	P	-	0	1	-	-	-
Monitor Mode 3	FENx function status and active current limit status	1	1	P	-	1	0	-	-	-
Monitor Mode 4	Revision and device ID	1	1	P	-	1	1	-	-	-
P = Parity bit – all commands and responses will use this bit to achieve odd parity										

Both the satellite and squib circuits can be reset over when sending the appropriate configuration commands via SPI1.

Configuration commands

Configuration mode 1

Configuration mode 1 main functions are as follows:

- Set Deployment current for all channels. All channels will be either set to 1.2 A/2 ms, 1.5 A/2 ms (Maximum VRESx Voltage limited to 25 V) 1.75 A/1 ms or 1.75 A/0.65 ms
- Perform a software reset

The SPI message definition for MOSI commands and MISO responses in this mode are defined below.

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MOSI Command for Configuration Mode 1															
0	0	P	R/W	SWR	0	CL Set bits	Software Reset Sequence bits								
MISO Response for Configuration Mode 1 (Except for Soft Reset/D11=1 and appropriate pattern)															
0	0	P	R/W	SWR	0	CL Set bits	0	0	0	0	0	0	1	0	

Table 17. Configuration mode 1

bit	MOSI command		MISO response
	State	Description	
D15	0	Mode bits	See above
D14	0		See above
D13		Odd Parity – Includes all 16 bits	Odd Parity – Includes all 16 bits
D12	0	Read (default) - When D12='0' bits D11 to D0 are ignored	R/W bit
	1	Write – Allows Soft reset and deployment programming	
D11	0	Sets Deployment Condition for ALL channels - When D11='0' bits D7 to D0 are ignored	See above
	1	Soft Reset Sequence (deployment circuit only) – bits D8 and D9 are ignored	
D10	0		See above
D9	-	Sets Deployment Conditions 00 = 1.2A/2ms (Default) 01 = 1.5A/2ms 10 = 1.75A/0.65ms 11 = 1.75A/1ms	Internal Stored Value CL bits
D8			-
D7 – D2	-	Software Reset-sequence	See above
D1	-		see above
D0	-		See above

Bit [D9:D8] Bits used to set the firing current/time for all channels. The default state is '00' (1.2A/2ms min.)

Bits [D7:D0] The soft reset for the ASIC, which includes deployment driver/diagnostics and satellite functions, is achieved by writing 0xAA and 0x55 within two subsequent 16-bit SPI transmissions. If the sequence is broken, the processor will be required to re-transmit the sequence. The device will not reset if the sequence is not completed within two subsequent 16- bit SPI transmissions. When soft reset command is received, the device reset its deployment driver's internal logic and timer, satellite internal logic including all internal registers. The effects of a soft reset is the same as a of POR event, except MISO response.

Bit D0 used to report the soft reset sequence status. If valid soft reset

sequences are received, bit D0 is set to ‘1.’ Otherwise, bit D0 is set to ‘0.’ When ASIC receives valid soft reset sequences, it will send a MISO register mode response containing 0x2003 in the next SPI transmission.

Configuration mode 2

Configuration mode 2 main function is as follows:

- Set the latch time for FENx input

The SPI message definition for MOSI commands and MISO responses in this mode are defined below.

MSB															**LSB**
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MOSI Command for Configuration Mode 2															
0	0	P	R/W	0	1	Latch bits		0	0	0	0	0	0	0	0
MISO Response for Configuration Mode 2															
0	0	P	R/W	0	1	Latch bits		0	0	0	0	0	0	0	0

Table 18. Configuration mode 2

Bit	**MOSI command**		**MISO response**
	State	**Description**	
D15	0	Mode bits	See above
D14	0		See above
D13		Odd Parity – Includes all 16 bits	Odd Parity – Includes all 16 bits
D12	0	Read (default) - When D12=’0’ bits D11 to D0 are ignored	R/W bit
	1	Write – FEN latch programming	
D11	0		
D10	1		
D9	00 = 0ms 01 = 128ms 10 = 256ms 11 = 512ms	FEN latch time	Internal Stored Value FEN latch bits
D8			
D7 – D0	0		See above

Bits [D9:D8] Bits are used to set the period of the FEN latch timer. The device has 4 independent timers. A valid FENx input will start the pulse stretch timer. These bits will set the timer duration. These values default to ‘00’ after a POR event.

Deployment commands

The deployment mode is used to activate the drivers. Two consecutive commands are required to activate the drivers. Any combination of channels can be fired as long as the prerequisite conditions are met as indicated in the previous section.

The SPI message definition for MOSI commands and MISO responses in Deployment Mode are defined below.

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MOSI Command for Deployment Mode 1															
0	1	P	1	1	0	0	1	Arming Channel Select							
MISO Response for Deployment Mode 1															
0	1	P	1	1	0	0	1	Armed Channels							
MOSI Command for Deployment Mode 2															
0	1	P	0	0	0	0	0	Firing Channel Select							
MISO Response for Deployment Mode 2															
0	1	P	0	0	0	0	0	Channels activated or channels waiting for FEN input							

Table 19. Deployment mode 1 bit definition

Bit	MOSI command		MISO response
	State	Description	
D15	0	Mode bits	See above
D14	1		See above
D13		Odd Parity – Includes all 16 bits	Odd Parity – Includes all 16 bits
D12 – D8		Arm pattern	See above
D7	0	Channel 7 Idle (default)	Internal Deploy Status
	1	Arm Channel 7	
D6	0	Channel 6 Idle (default)	Internal Deploy Status
	1	Arm Channel 6	
D5	0	Channel 5 Idle (default)	Internal Deploy Status
	1	Arm Channel 7	
D4	0	Channel 4 Idle (default)	Internal Deploy Status
	1	Arm Channel 4	
D3	0	Channel 3 Idle (default)	Internal Deploy Status
	1	Arm Channel 3	
D2	0	Channel 2 Idle (default)	Internal Deploy Status
	1	Arm Channel 2	
D1	0	Channel 1 Idle (default)	Internal Deploy Status
	1	Arm Channel 1	
D0	0	Channel 0 Idle (default)	Internal Deploy Status
	1	Arm Channel 0	

Table 20. Deployment mode 2 bit definition

Bit	MOSI command		MISO response
	State	Description	
D15	0	Mode bits	See above
D14	1		See above
D13		Odd Parity – Includes all 16 bits	Odd Parity – Includes all 16 bits
D12 – D8		Arm pattern	See above
D7	0	Channel 7 Idle (default)	Internal Deploy Status
	1	Arm Channel 7	
D6	0	Channel 6 Idle (default)	Internal Deploy Status
	1	Arm Channel 6	
D5	0	Channel 5 Idle (default)	Internal Deploy Status
	1	Arm Channel 7	
D4	0	Channel 4 Idle (default)	Internal Deploy Status
	1	Arm Channel 4	
D3	0	Channel 3 Idle (default)	Internal Deploy Status
	1	Arm Channel 3	
D2	0	Channel 2 Idle (default)	Internal Deploy Status
	1	Arm Channel 2	
D1	0	Channel 1 Idle (default)	Internal Deploy Status
	1	Arm Channel 1	
D0	0	Channel 0 Idle (default)	Internal Deploy Status
	1	Arm Channel 0	

The Deploy Status becomes ‘1’ when there is a valid fire sequence. Once active it will become ‘0’ when the time out has expired waiting FEN activation or when squib driver has turned off for fire completion. The same information is available when receiving a response from Monitor Mode 1.

For the drivers to be fire capable the command mode 1 (Arming) must be sent followed by command mode 2 (Firing). With this sequence valid and FEN active then firing will begin. A break in the sequence will require the process to be restarted. All other bit patterns for D12-D8 shall be ignored.

To begin a deployment 2 consecutive commands need to be sent along with the FEN active (external or internal latch). An example of a firing sequence for channel 0 would be as follows

FENx active or inactive

TX – 0x5901 – ARM Channel 0
RX – Based on previous command

TX – 0x5901 – ARM Channel 0
RX – 0x5901

TX – 0x5901 – ARM Channel 0
RX – 0x5901

TX – 0x6001 – Firing on Channel 0 is started on if FEN is active
RX – 0x5901

TX – 0x6001 – Command ignored – sequence is not allowed
RX – 0x6001

TX – 0x6001 – Command ignored
RX – 0xD005

Alternatively, if the sequence is broken the response shall be as in the following example

FENx active
TX – 0x5901 – ARM Channel 0

RX – Based on previous command
TX – 0x2000 – Read of Register Mode 1

RX – 0x5901
TX – 0x6001 – Command ignored – sequence is not allowed

RX – contents of register

TX – 0x6001 – Command ignored – sequence is not allowed
RX – 0xD005

If, for example, channel 0 and 1 bits are set in the Arm command and channel 0 and 7 bits are set in the fire command then the result will be the drivers on channel 0 will be activated (assuming FEN function is active) and there will be no effect on channel 7.

During a deployment, any commands directed to the channel that are in deployment are ignored and the response shall be 0xD009.

Diagnostic commands

Diagnostic Mode 1

Diagnostic mode main functions are as follows:

- Normal Squib Resistance Diagnostics
- High Squib Resistance Diagnostics
- Squib short to battery/ground diagnostics
- Loop to loop diagnostics
- High side safing diagnostics
- VRESx measurement
- LS and HS FET Test

The SPI message definition for MOSI commands and MISO responses in Diagnostic Mode are defined below.

Write commands definition

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MOSI Command for Diagnostic Mode Execution															
1	0	P	1	Diag. Selection bits			0	0	0	0	IPD_DIS	AMC	Channel Selection		
MISO Response for Diagnostic Mode, Stop Diagnostic Selection (MOSI D11:D9=000)															
1	0	P	1	0	0	0	0	0	0	0	IPD_DIS	0	000		
MISO Response for Short to Battery/Ground Selection (MOSI D11:D9=001)															
1	0	P	1	0	0	1	STB	STG	0	SQP	IPD_DIS	0	Channel Selection		
MISO Response for Diagnostic Mode, Vresx Selection (MOSI D11:D9=010)															
1	0	P	1	0	1	0	VR1	VR0	0	0	IPD_DIS	0	Channel Selection		
MISO Response for Diagnostic Mode, High Side Safing Selection (MOSI D11:D9=011)															
1	0	P	1	0	1	1	HSS1	HSS0	0	0	IPD_DIS	0	Channel Selection		
MISO Response for Diagnostic Mode, Squib Resistance Selection (MOSI D11:D9=100)															
1	0	P	1	1	0	0	0	0	0	0	IPD_DIS	AMC	Channel Selection		
MISO Response for Diagnostic Mode, High Squib Resistance Selection (MOSI D11:D9=101)															
1	0	P	1	1	0	1	HSR	0	0	0	IPD_DIS	0	Channel Selection		
MISO Response for Diagnostic Mode, Low Side FET Test Selection (MOSI D11:D9=110)															
1	0	P	1	1	1	0	STB	STG	FP	FT	IPD_DIS	0	Channel Selection		
MISO Response for Diagnostic Mode, High Side FET Test Selection (MOSI D11:D9=111)															
1	0	P	1	1	1	1	STB	STG	FP	FT	IPD_DIS	0	Channel Selection		

Read commands definition

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MOSI Command for Diagnostic Mode, READ command															
1	0	P	0	0	0	0	1	1	1	1	0	0	000		
MISO Response for Diagnostic Mode, READ command															
1	0	P	0	Diag. Selection bits internal state			X	X	X	X	IPD_DIS	X	Channel Selection Internal State		

Bits D13 Parity bit. Command and response will use odd parity

Bits D12 R/W
1 = Write (execute command)
0= Read

For bits D11:D09 the following table shall be used for diagnostic selection.

Table 21. Diagnostic selection

Diagnostic	Bits			Current source active	Comparator or amplifier
	D11	D10	D9		
Stop Diagnostic	0	0	0	NO	NO
Short to Battery/Ground	0	0	1	Y (VMRC)	Y (Comp ISTB/ISTG)
VRESx Diagnostic	0	1	0	N	Y (Comp VRESx)
High Side Safing Diagnostics	0	1	1	Y (IHSS)	Y (Comp HSS)
Squib Resistance Diagnostics	1	0	0	Y (ISRC/ISINK)	Y (Ampli)
High Squib Resistance Diagnostics	1	0	1	Y (VMRC)	Y (Comp IHR)
LS FET test	1	1	0	Y (VMRC)	Y (Comp ISTB/ISTG)
HS FET test	1	1	1	Y (VMRC)	Y (Comp ISTB/ISTG)

STB/STG bit Definition with MOSI D11:D9=001 (Leakage Test)

STB bit Bit used for indicating leakage to battery.

0 = No leakage to battery

1 = Short to battery / HS Driver test pass

STG bit Bit used for indicating leakage to ground.

0 = No leakage to battery

1 = Short to ground / LS Driver test pass

STB/STG bit Definition with MOSI D11:D9=110 (LS FET)

STB, STG bits see table below

Table 22. Diagnostic mode LS FET selection

Condition	STB	STG
Test in Process (FT=1); Fault (FP=1); or LS FET/GNDx open fault (FP=0,FT=0)	0	0
Short to battery occurred during test	1	0
Test Pass if leakage diagnostics did not indicate a short to GND	0	1

STB/STG bit definition with MOSI D11:D9=111 (HS FET)

STB, STG bits see table below

Table 23. Diagnostic mode HS FET selection

Condition	STB	STG
Test in Process (FT=1); Fault (FP=1); or HS FET/VRESx open fault (FP=0,FT=0)	0	0
Test Pass if leakage diagnostics did not indicate a short to battery	1	0
Short to ground occurred during test	0	1

STB/STG bit definition with MOSI D11:D9=011 (High side safing)

HSS1:HSS0 bits, see table below

Table 24. Diagnostic mode HSS selection

Condition	HSS1	HSS0
(VSDIAG-VRESx) < $V_{HSSSHORT\_th}$	0	0
$V_{HSSSHORT\_th}$ < (VSDIAG-VRESx) < $V_{HSSOPEN\_th}$	0	1
$V_{HSSOPEN\_th}$ < (VSDIAG-VRESx)	1	1

STB/STG bit definition with MOSI D11:D9=010 (VRESx supply voltage)

VR1:VR0 bits, see table below

Table 25. Diagnostic mode VRESx selection

Condition	VR1	VR0
V_{RESx} < $V_{VRESXLO\_th}$	0	0
$V_{VRESXLO\_th}$ < V_{RESx} < $V_{VRESXHI\_th}$	0	1
$V_{VRESXHI\_th}$ < V_{RESx}	1	1

STB/STG bit definition with MOSI D11:D9=101 (High squib resistance)

HSR bit — Bit used for indicating leakage to ground.

0 = Squib Resistance below R_{SQHIZ}

1 = Squib Resistance above R_{SQHIZ}

Bits D6 — Fault present prior to running LS FET or HS FET test (diagnostics aborted)

0 = Normal

1 = Test not run - Fault present (FEN in incorrect state, short to battery or ground)

Bits D5 — Bit definition based on diagnostic selection.

FT bit Read Only - Used for LS FET or HS FET diagnostics and is the status of the FET timer

0 = FET timer not active

1 = FET timer active

SQP bit: Squib Pin to be tested during short to battery/ground diagnostics

0 = SQBLx pin test

1 = SQBHx pin test

Bits D4 — Used to disable IPD on all channels

0 = IPD active as indicated;

– Active for all channels except the one under test when running Short to Battery/Ground and short between loops Diagnostics and LS/HS FET test

– Active for all channels when running Stop Diagnostic,

resistance Diagnostics, High Squib Resistance Diagnostics, HSS Diagnostic and VRESx Diagnostics
1 = IPD disabled on all channels

Bits D3 Bit used for resistance measurement amplifier calibration. Only valid when squib resistance diagnostics is selected, otherwise this bit will be ignored and a 0 will be reported in the response
0 = No calibration (Normal squib resistance measurements)
1 = Calibration

For bits D2:D0 The following table shall be used for channel selection.

Table 26. Channel selection

Channel	Bit D2	Bit D1	Bit D0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Note: Except for short to battery /ground diagnostics and loop to loop test the state of IPD (D4) will not affect the test

Monitor commands

Monitor Mode 1

Monitor mode main information:

- Deployment status

The SPI message definition for MOSI commands and MISO responses in Monitor Mode 1 are defined below.

MSB															**LSB**
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MOSI Command for Monitor Mode 1															
1	1	P	0	0	0	0	DS	Channel Selection Status Request							
MISO Response for Monitor Mode 1															
1	1	P	0	0	0	0	DS	Channel Status							

Table 27. MOSI diagnostic mode 2 bit definition

Bit	MOSI Command		MISO Response
	State	Description	
D15	1	Mode bits	See above for state
D14	1		See above for state
D13		Odd Parity – Includes all 16 bits	Odd Parity – Includes all 16 bits
D12	0		See above for state
D11	0	Monitor Mode selection bits	See above for state
D10	0	Monitor Mode selection bits	See above for state
D9	0		See above for state
D8	0	Report Deploy Success Flag (default)	Internal state of report setting
	1	Report Deploy Status	
D7	0	Keep Deploy Success Flag Channel 7 (default)	Deploy Information for channel based on bit D8 Will Either be DEPLOY_STATUS7 or DEPLOY_SUCCESS7
	1	Clear Deploy Success Flag Channel 7	
D6	0	Keep Deploy Success Flag Channel 6 (default)	Deploy Information for channel based on bit D8 Will Either be DEPLOY_STATUS6 or DEPLOY_SUCCESS6
	1	Clear Deploy Success Flag Channel 6	
D5	0	Keep Deploy Success Flag Channel 5 (default)	Deploy Information for channel based on bit D8 Will Either be DEPLOY_STATUS5 or DEPLOY_SUCCESS5
	1	Clear Deploy Success Flag Channel 5	
D4	0	Keep Deploy Success Flag Channel 4 (default)	Deploy Information for channel based on bit D8 Will Either be DEPLOY_STATUS4 or DEPLOY_SUCCESS4
	1	Clear Deploy Success Flag Channel 4	
D3	0	Keep Deploy Success Flag Channel 3 (default)	Deploy Information for channel based on bit D8 Will Either be DEPLOY_STATUS3 orDEPLOY_SUCCESS3
	1	Clear Deploy Success Flag Channel 3	
D2	0	Keep Deploy Success Flag Channel 2 (default)	Deploy Information for channel based on bit D8 Will Either be DEPLOY_STATUS2 or DEPLOY_SUCCESS62
	1	Clear Deploy Success Flag Channel 2	
D1	0	Keep Deploy Success Flag Channel 1 (default)	Deploy Information for channel based on bit D8Will Either be DEPLOY_STATUS1 or DEPLOY_SUCCESS1
	1	Clear Deploy Success Flag Channel 1	
D0	0	Keep Deploy Success Flag Channel 0 (default)	Deploy Information for channel based on bit D8 Will Either be DEPLOY_STATUS0 or DEPLOY_SUCCESS0
	1	Clear Deploy Success Flag Channel 0	

The DEPLOY_SUCCESSx flag indicates if the corresponding channel's drivers were activated and that the activation period has completed. This bit is set when the activation period has expired. The DEPLOY_SUCCESSx flag will be '1' until it is cleared by writing a '1' to the appropriate channel(s) (bits D7-D0).

The DEPLOY_STATUSx bit will become '1' when there is a valid Arm and Fire sequence for the corresponding channel. The DEPLOY_STATUSx bit transitioning from a '0' to a '1' does not depend on the state of the FEN function. It will become '0' when time out has expired.

Depending on the state of FEN the DEPLOY_STATUSx flag could be '1' for a minimum of 1x t_{DEPLOY} and a maximum of up to 2 x t_{DEPLOY} (see *Figure 8*). The Deployment status is captured on the falling edge of CS_D.

Bit D8 is used to select the meaning of bit D7 through bit D0 in the status response message. When this bit is set to '1,' bits D7 through D0 in the status response message will report the state of the DEPLOY_STATUSx flag.

When this bit is '0,' bit D7 through bit D0 in the status response message will report the DEPLOY_SUCCESSx flag. The following table 16 shows the conditions for the DEPLOY_STATUSx flag and the DEPLOY_SUCCESSx flag.

Table 28. DEPLOY_STATUSx flag and the DEPLOY_SUCCESSx flag conditions

DEPLOY_STATUSx flag	DEPLOY_SUCCESSx flag	Description
0	0	No Deployment in process or has been initiated since POR or since last Clear of Success flag
0	1	Deployment has successfully completed
1	0	Deployment in process
1	1	Deployment terminated / LSD shutdown

Once the Deploy Success Flag is set, it will inhibit the subsequent deployment command until a SPI command to clear this deployment success flag is received. Bits D7 through bit D0 are used to clear/keep the deploy success flag. When these bits are set to '1,' the flag can be cleared. Otherwise, the state of these flags is not affected. **The Success flag must be cleared to allow re-activation of the drivers**

Monitor mode 2

Monitor mode main information:

- Current limit measurement of channels

The SPI message definition for MOSI commands and MISO responses in Monitor Mode 2 are defined below.

MSB															**LSB**
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MOSI Command for Monitor Mode 2															
1	1	P	CLR	0	1	Current Measurement Channel Select			0	0	0	0	0	0	0
MISO Response for Monitor Mode 2															
1	1	P	0	0	1	Current Measurement Channel			Current Measurement Data						

Table 29. MOSI monitor mode 2 Bit definition

Bit	MOSI command		MISO response
	State	Description	
D15	1	Mode Bits	See above for state
D14	1		See above for state
D13		Odd Parity – Includes all 16 bits	Odd Parity – Includes all 16 bits
D12	0	Keep timer measurements	See above for state
	1	Clear “current measurement time” stored on the register of channel selected by D9:D7	See above for state
D11	0	Monitor Mode selection bits	See above for state
D10	1	Monitor Mode selection bits	See above for state
D9		Channel selected for current measurement See *Table 30*	Internal Stored channel selections bits
D8			
D7			
D6:D0	0	-	Current measurement of selected channel

Bits [D9:D7]. Used when sending the MOSI command to select the channel to be measured. The MISO response shall echo the MOSI command.

Table 30. Current measurement channel selections

Channel	Bit D9	Bit D08	Bit D07
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Bits [D6:D0]. Current measurement data of selected squib channel. Bit weight is nominally 25 µs for a total measurement time 3.175 ms.

Monitor mode 3

Monitor mode main information:

- Status of FENx Function - FENx pin OR’d with Internal FENx latch
- Status of current for each channel

The SPI message definition for MOSI commands and MISO responses in Monitor Mode 3 are defined below.

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MOSI Command for Monitor Mode 3															
1	1	P	0	1	0	CFS	0	0	0	0	0	0	0	0	0
MISO Response for Monitor Mode 3															
1	1	P	0	1	0	CFS	POR STAT	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0

Table 31. MOSI monitor mode 3 bit definition

Bit	MOSI command		MISO response
	State	Description	
D15	1	Mode Bits	See above for state
D14	1		See above for state
D13		Odd Parity – Includes all 16 bits	Odd Parity – Includes all 16 bits
D12	0		See above for state
D11	1		See above for state
D10	0		See above for state
D09		Status Type 0 = Current limit status 1 = FEN function status	0 = current measurement status reported in bit D7:D0 1 = FEN function status reported in D7:D0
D08	0		POR status
D7:D0	0		Current measurement status of channels or FEN status as indicated below

Bit [D10] POR status

0= Reset occurred. Bit cleared when read

1= Normal

With Bit D9 = 1

Bit D7:D4 ‘0000’

Bit D3: 0 = FEN4 input or FEN4 latch timer inactive

1 = FEN4 input or FEN4 latch timer active

Bit D2 0 = FEN3 input or FEN3 latch timer inactive

1 = FEN3 input or FEN3 latch timer active

Bit D1: 0 = FEN2 input or FEN2 latch timer inactive

1 = FEN2 input or FEN2 latch timer active

Bit D0: 0 = FEN1 input or FEN1 latch timer inactive

1 = FEN1 input or FEN1 latch timer active

Note: The FEN status is the result of the state of the FEN input pin OR'd with the FEN latch timer. The FEN latch timer will remain inactive until a transition of '1' to '0' on the FEN input (assuming the pin was high for a minimum of 16µs). At that time the FEN latch timer will be active and keep the internal FEN signal active based on the programmed time (0ms, 128ms, 256ms or 512ms) for that particular FEN function.

With Bit D9 = 2

Bit D7: 0 = Current through channel 7 is below I_{MEAS}

1 = Current through channel 7 is above I_{MEAS}

Bit D6: 0 = Current through channel 6 is below I_{MEAS}

1 = Current through channel 6 is above I_{MEAS}

Bit D5: 0 = Current through channel 5 is below I_{MEAS}

1 = Current through channel 5 is above I_{MEAS}

Bit D4: 0 = Current through channel 4 is below I_{MEAS}

1 = Current through channel 4 is above I_{MEAS}

Bit D3: 0 = Current through channel 3 is below I_{MEAS}

1 = Current through channel 3 is above I_{MEAS}

Bit D2: 0 = Current through channel 2 is below I_{MEAS}

1 = Current through channel 2 is above I_{MEAS}

Bit D1: 0 = Current through channel 1 is below I_{MEAS}

1 = Current through channel 1 is above I_{MEAS}

Bit D0: 0 = Current through channel 0 is below I_{MEAS}

1 = Current through channel 0 is above I_{MEAS}

Note: current status for channel is captured on the falling edge of chip select

Monitor mode 4

Monitor mode main information:

- Revision
- Device ID

The SPI message definition for MOSI commands and MISO responses in Monitor Mode 4 are defined below

MSB															**LSB**
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MOSI Command for Monitor Mode 4															
1	1	P	0	1	1	0	0	0	0	0	0	0	0	0	0
MISO Response for Monitor Mode 4															
1	1	P	0	1	1	ID3	ID2	ID1	ID0	R5	R4	R3	R2	R1	R0

Table 32. MOSI monitor mode 3 bit definition

Bit	MOSI command		MISO response
	State	Description	
D15	1	Mode Bits	See above for state
D14	1		See above for state
D13		Odd Parity – Includes all 16 bits	Odd Parity – Includes all 16 bits
D12	0		See above for state
D11	1	Mode selection	See above for state
D10	1	Mode selection	See above for state
D9-D6			‘0001’ shall be device L9662
D5:D0	0		Revision Information: Upper 3 bits will reflect full pass Lower 3 bits will reflect metal/minor change First pass device will be indicated as “001 000”

3.4.6 Satellite sensor interface

The device provides four currents limited to I_Lim each through outputs ICH1, ICH2, ICH3 and ICH4. The voltage at these four channels is supplied by the VSATS input. Channels 1, 2, 3 and 4 serve as switched power sources to remote mounted satellite sensors. The device will monitor the current flow from its output pin and “demodulate” the current to be decoded using Manchester protocol. Decoded satellite message is communicated to an external microprocessor via SPI2. Both the satellite and squib circuits can be reset over when sending the appropriate configuration commands via SPI1 (16 bit SPI).

For operation using a sync pulse a capacitor between 10 nF to 47 nF is required to be within 70 nH of the respective ASIC pin for signal stability.

In case of loss of VCC all outputs will remain off.

Satellite operation modes

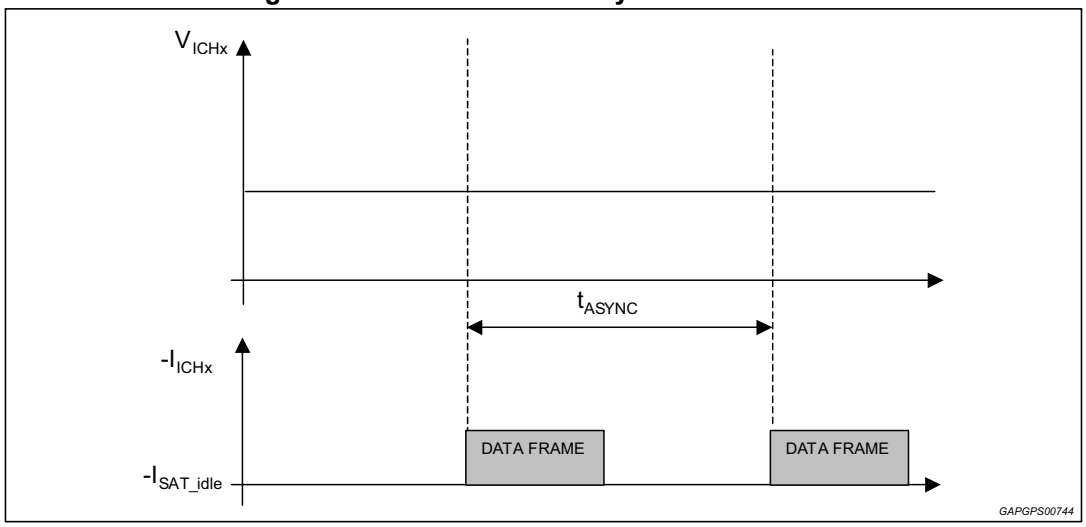
Each receiver channel provides different modes of operation that can be programmed by SPI command.

Receive mode (asynchronous data transfer)

In Receive Mode the sensor interface operates in asynchronous mode. The specified data messages from each channel will be continuously received every t_{async}. (Design Information only).

The Sensor Interface supplies satellites and receives current modulated data. In this mode, the channels are supplied via pin VSATS. A voltage $\geq V_{ICHxmin}+V_{hdp\_max(I=75mA@105°C)}$ at this input pin is required to provide the regulated voltage of $V_{ICHxmin}$ at the satellite outputs [ICH0]...[ICH3].

Figure 10. Transmission in asynchronous mode



High voltage mode and satellite SYNC mode

In High Voltage Mode and SYNC Mode the ICHx outputs are regulated to a higher output voltage (V_{ICHx_HV}) than in Receive mode. In this case, the channel power supply is taken from a separate input pin (VSYNC). Both modes are activated and deactivated by the same SPI command. The start of the SYNC impulse is arbitrary and is created by a signal from the µC using the INITSYNC input pin. The Sync pulse shall be initiated for all satellites based on the rising edge of the INITSYNC input after a $t_{SYNCDLY}$ delay. The duration of the sync pulse shall be based on the programmed sync pulse high time based on [D9:D8] in the MCR. If the sync timing register has not been written the default pulse high time shall be t_{SYNC_high1}. The absence of an INITSYNC input rising edge does not prevent processing of incoming messages when in HV or SYNC mode.

For Sync mode the valid sync time selections would be tSYNC_high1 and t_{SYNC_high2}. For High Voltage Mode the valid sync time selections would be t_{SYNC_high3} and t_{SYNC_high4}. The time selections of t_{SYNC_high3} and t_{SYNC_high4} cannot be used in normal operation because the time duration will be longer than the receive disable time, resulting in improper communication with the satellites. For HV mode (used only in the manufacturing or supplier facility) if there is a short to battery flag is set then the message must be ignored.

At the start of a sync pulse there is a short period before the actual start of the sync pulse for a channel where the current is limited to 20mA typical. This low current limit will start after the $t_{INITSYNCFLT}$ time and last for 200 ns. The satellite current requirements in conjunction with the capacitance on the pins should be verified so that the minimum satellite voltage can be maintained.

SYNC mode

During the receiver disable time a sync pulse cannot be initiated and any change on the INITSYNC pin will be ignored by the ASIC.The satellite SYNC mode is used to generate automatic sync pulses for synchronous data transmission. In this mode, the output operates in Receive Mode, but is periodically switched to a higher output voltage V_{ICHx_HV}. Thus, the receiver decoder blocks are deactivated for the duration of the Sync pulse. To avoid disturbance in the data flow during re-settling of the output voltage to the receive-mode level, the receiver decoder block is deactivated for time $t_{RECV\_disable}$.

The receiver disable time, $t_{RECV\_disable}$, is started from the rising edge of the INITSYNC input. When operating in sync mode the valid sync time selections would be t_{SYNC_high1} and t_{SYNC_high2}.

In synchronous communication mode it is possible to communicate with a maximum of two (2) satellites on one channel. This is done using a simple form of time division multiplexing where each device transmit its data during a known time slot.

The figure below shows examples for 1 or 2 satellites on a channel.

Figure 11. Synchronization pulse timing (single device)

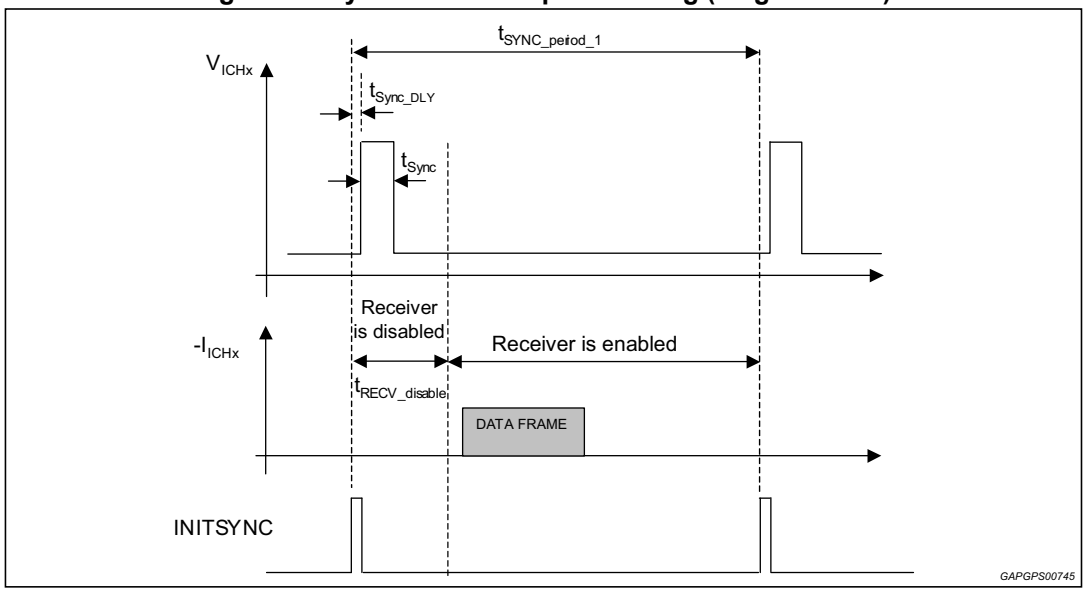
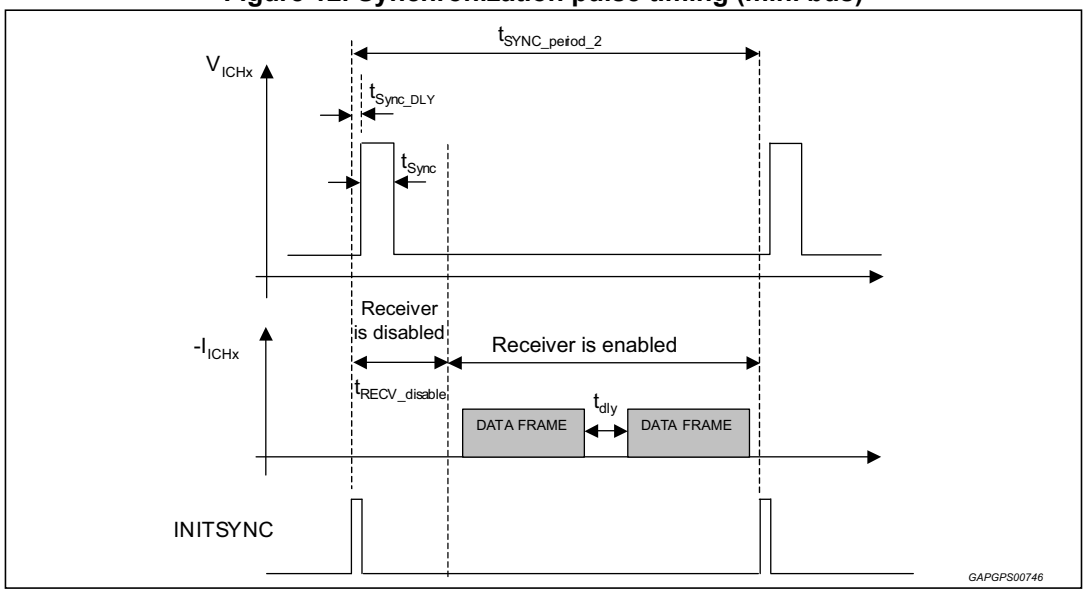


Figure 12. Synchronization pulse timing (mini bus)

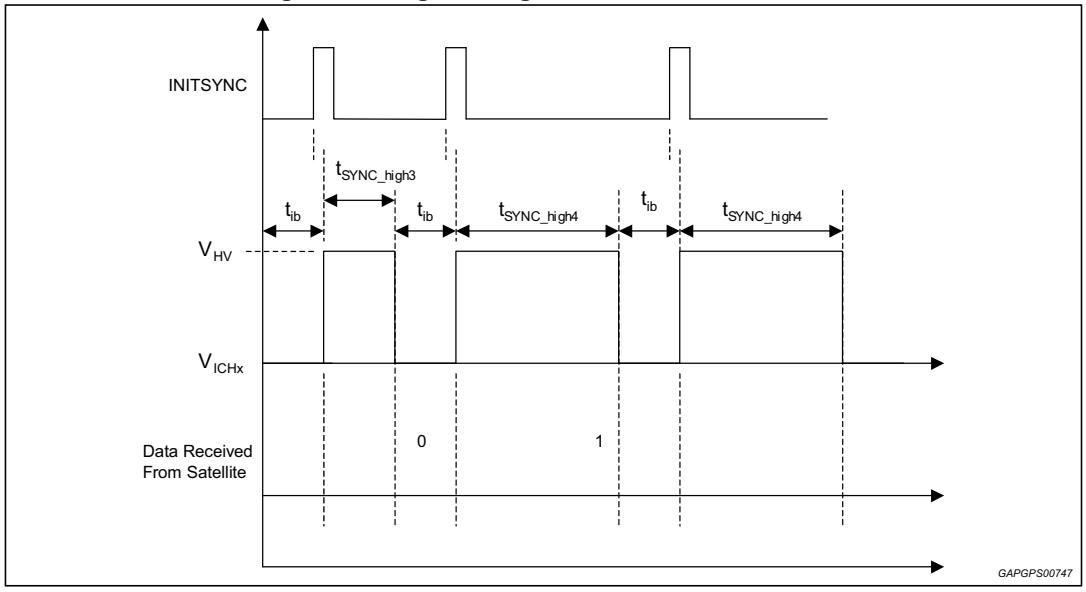


High voltage mode

The High Voltage Mode is based on the SYNC Mode and will be used to communicate with the external satellites via voltage modulation. When in this mode the valid sync time selections would be tSYNC_high3 and tSYNC_high4.

During the High Voltage Mode it is necessary to disable the receiver of the sensor interface until a complete data frame is sent. After sending a data frame the receiver must be enabled again to receive the expected answer from the satellites. The microcontroller will control the enabling and disabling of the receiver along with Sync pulse high time (tSYNC_highx) the over SPI2 for each bit of the data frame.

Figure 13. High voltage mode communication

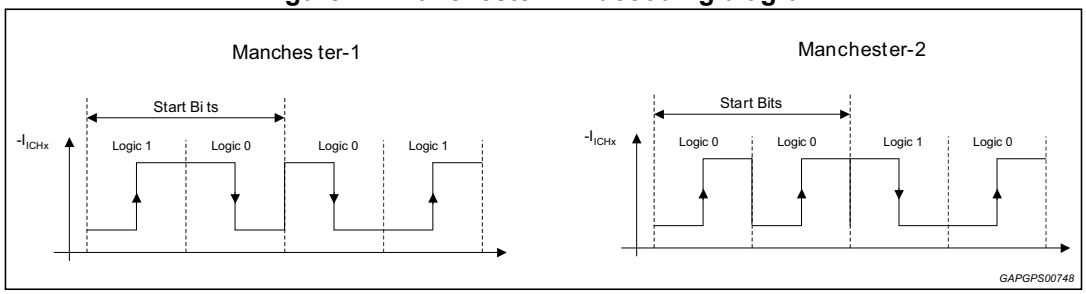


Satellite message decoding

The device is configurable for decoding of satellite messages based on either Manchester-1 or Manchester-2 decoding. Each of the four satellite channels has a Manchester decoder that can be enabled or disabled through the CCR register.

For Manchester-1 decoding a logic 0 is defined as a signal transition from 1 to 0 at 50% Duty cycle, logic 1 is defined as a signal transition from 0 to 1 at 50% Duty cycle. For Manchester-2 decoding a logic 0 is defined as a signal transition from 0 to 1 at 50% Duty cycle, logic 1 is defined as a signal transition from 1 to 0 at 50% Duty cycle. An example of Manchester-1 and Manchester-2 decoding is given below.

Figure 14. Manchester-1/2 decoding diagram



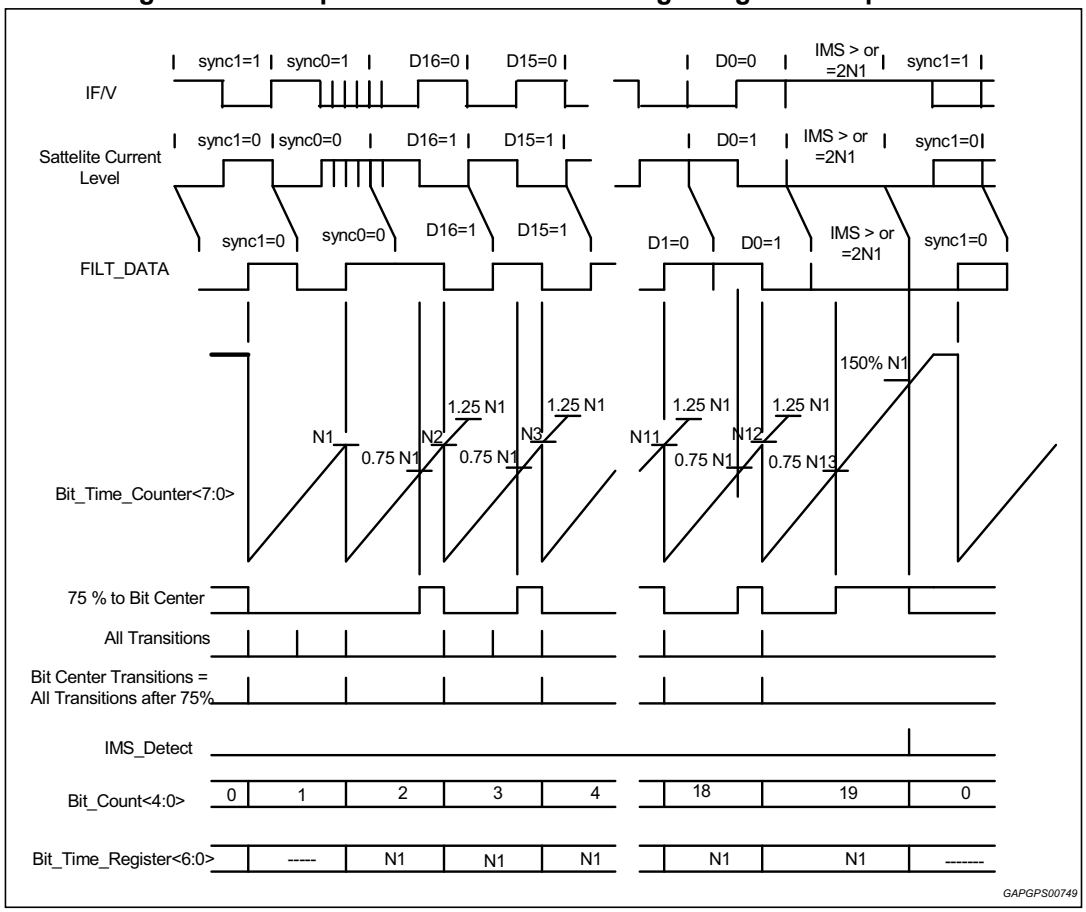
The device is capable of different bit rates, which can be programmed via SPI2 based on the operating frequency of the satellite bus. For the first message and all subsequent messages the ASIC uses the Start Bits' time to decode the rest of the bits in the message. In case the measured bit rate obtained using the 2 Start bits doesn't fall within the range selected by the SPI as defined the device declares a bit time error and waits for idle. The idle time between messages is 1.5 times the measured start bits time of the previous message unless a message error is detected. If an error is detected then the device shall default to 1.5 times the maximum frequency (minimum bit time). The initial idle time (after a POR or reset) is 0 bit times.

The decoder uses a counter to track the high to low and low to high transitions at the bit center. *Figure 15* is an example that illustrates how the ASIC performs the decoding.

A transition is considered a bit center only when an edge is detected 75% to 125% of the reference bit time after de-glitch filter. The de-glitch filter can modify bit time if the noise on is not symmetric on each transition. When a single edge occurs below 75% of the reference bit time it is considered to be a bit edge but it is ignored. When the decoder detects a second edge below 75% of the reference bit time the device declares a bit time error via SPI, revert to the minimum bit time of the selected range, and wait for idle. When a valid bit center is detected the counter will reset and start counting again until another edge is detected. If the message is not complete and no edge is detected in the range of 75% to 125% of measured bit time, the device declares a bit time error via SPI, revert to the minimum bit time of the selected range, and wait for idle. The idle time is defined as 150% of the minimum bit time of the selected protocol speed range. If there is no bit transition detected for that period of time and the correct number of bits was received, the message is considered complete. Bit time error and too many bits faults are stored directly into the data register once they are selected without the need to wait till an idle time. Since a bit time error is reported directly once it is detected before Idle time, too few bits error may never be reported since bit time error is detected first.

Bit time errors and too many bits errors will cause the decoder to revert to the minimum bit time of the selected range, and discard the message. In case of a message containing multiple errors only one error code is reported per message, errors detected in the decoding phase have the following reporting priority; bit time errors, too many bits errors then communication errors (CRC/Parity).

Figure 15. Example of Manchester decoding using satellite protocol



Communication protocols

In order to support the various satellite sensors, the device supports two different communication standards (MS and PSI5 Mode). The Manchester standard consists of two protocols (CRC / Even Parity), while the PSI5 standard consists of one protocol (Even Parity) for a total of three communication protocols. The three protocols which are described in this section are: 1) Protocol A - CRC. 2) Protocol B Generic – Parity: to support Bosch PAS3 and PAS4 sensors. 3) Protocol C: PSI5 – Parity: support for various sensors. Bit D3 of the MCR configures the device for either MS or PSI5 communication standard. Bits D10 to D13 in the MCR register are used to configure the specific device channel (Ch. 0,1,2,3) to use any of these specified protocols.

This version of the device supports the following PSI5 Operational Modes.

PSI5-A8P-250/1L

PSI5-A10P-250/1L

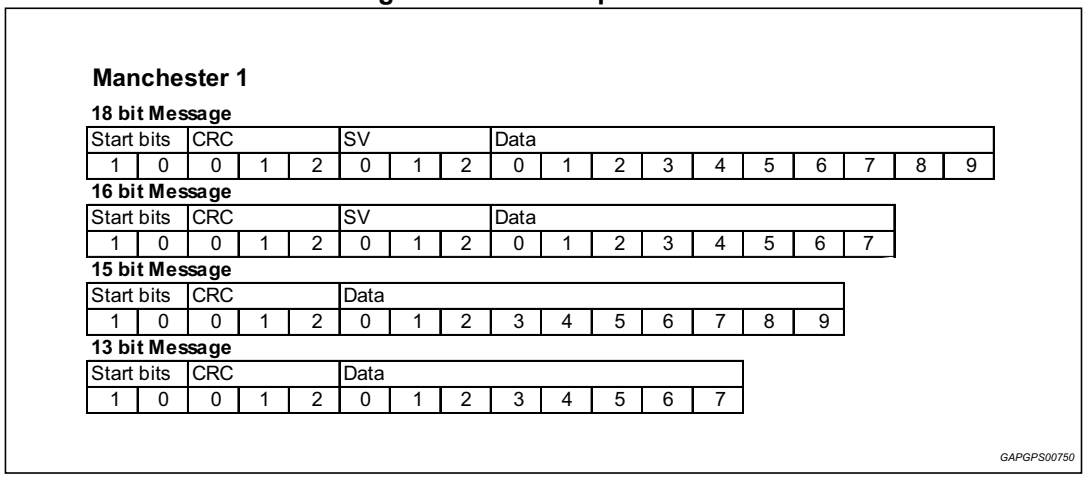
PSI5-P10P-250/1L

PSI5-P10P-500/2L

Protocol A

The data received from satellite receiver block has to be decoded in the digital block. The data is received LSB first. The protocol format is defined below for the 4 different message lengths.

Figure 16. Satellite protocol-A



The default for the device is to perform CRC decoding on all messages. The device has the option not to perform the CRC decoding and pass the satellite message, excluding the 2 start bits, over the MISO. CRC decoding can be disabled/enabled by writing to the appropriate bit in the CCR register.

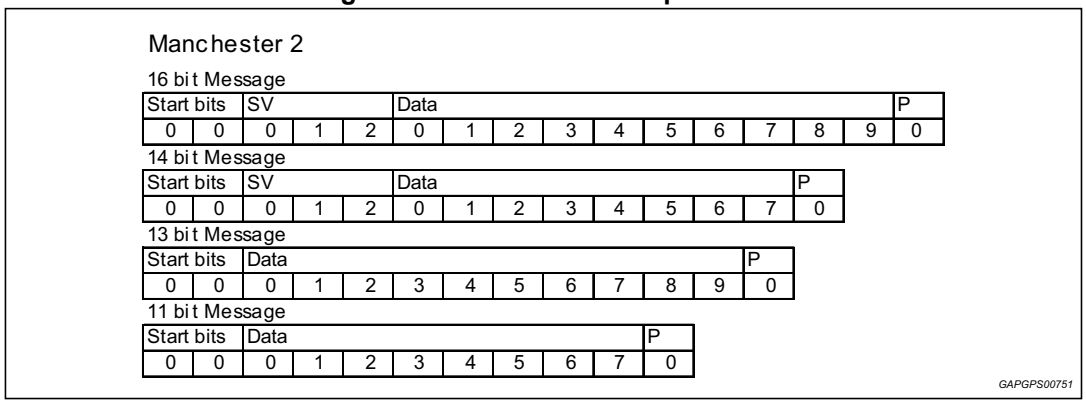
For the CRC mode the error detection code used for processing the message is based on the polynomial $x^3 + x^1 + x^0$. If the device is in CRC mode it will process all incoming messages and report an error via SPI2 in case of a CRC mismatch. The CRC is performed after a complete message is received and, in case of CRC error, the device sets a fault code in the SR word.

The message data sent over SPI2 is MSB first.

Protocol B: generic variable length protocol

The data received from satellite receiver block has to be decoded in the digital block. The data is received LSB first. The protocol format is defined below for the 4 different message lengths.

Figure 17. Generic satellite protocol



The ASIC shall supports a Satellite Protocol-B, which is based on Bosch sensors PAS3/PAS4 protocols. The default for the device is to perform parity decoding on all messages. The device has the option not to perform the CRC decoding and pass the satellite message, excluding the 2 start bits, over the MISO. Parity decoding can be disabled/enabled by writing to the appropriate bit in the CCR register.

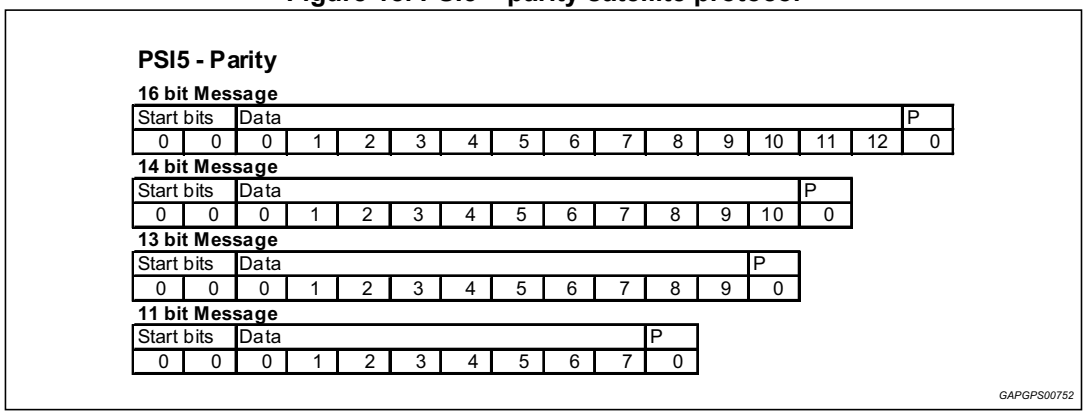
For the parity mode the error detection code used for processing the message is even. If the device is in CRC mode it will process all incoming messages and report an error via SPI2 in case of a parity mismatch. The parity check is performed after a complete message is received and, in case of an error, the device sets a fault code in the SR word.

The message data sent over SPI2 is MSB first.

Protocol C: PSI5 mode - parity protocol

The data received from satellite receiver block has to be decoded in the digital block. The data received from the satellite is LSB first followed by the Parity bit. The protocol format is defined below for the 4 different message lengths.

Figure 18. PSI5 – parity satellite protocol



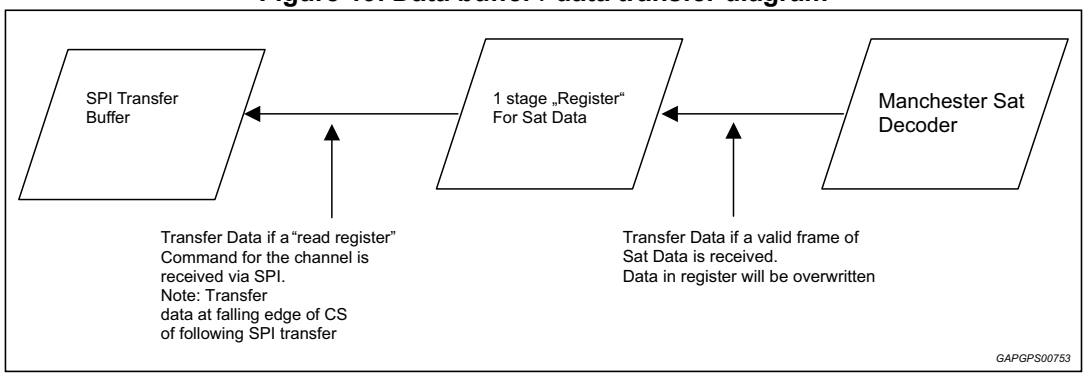
When the PSI5 parity protocol is selected, the ASIC performs a parity check then passes the satellite message, excluding the 2 start bits and parity bit over the MISO on SPI2. For parity protocol, the error detection code used for processing the message is even. The parity check is performed and in case of an error, the device sets a fault code in the SR word.

When commanded, the message data excluding the start bits and parity bit is sent over SPI2 MSB first.

DATA buffer/DATA transfer

The IC includes 4 internal DATA registers; one for each output channel, each one is 16 bits and one deep.

Figure 19. Data buffer / data transfer diagram



Once the data is transferred to the SPI transfer buffer the satellite data register is cleared.

If there is no incoming satellite message before the next SPI data read a register empty flag will be indicated assuming no other fault conditions exist.

Current sensor description

Each output channel senses the current drawn by the remote satellite sensor. The circuit modulates the load current into logic voltage levels for post processing by a Manchester decoder. Each channel has an internal comparator with a programmable currents trip points selectable through the appropriate setting in the CCR Register for each of the 4 satellite channels. For determining the appropriate current threshold setting the total current, idle plus signal, must be taken into account. The current sense comparator also provides hysteresis, which can be enabled through appropriate setting in the CCR Register. Each comparator output have a de-glitch filter as a function of the protocol speed.

Satellite short conditions

Each channel has a short circuit protection by independent current limit. When a short to ground occurs the output becomes current limited to 150 mA maximum when the voltage is at idle and 280 mA maximum during the sync pulse for a total period of t_{Flt_GND}. After time t_{Flt_GND} the output will shut off and a leakage to ground fault shall be reported in the SR word. The output will remain off until re-enabled via SPI and if the short is not present then the outputs shall return to normal operation. All channels that do not have a short condition shall not be affected.

When the output is shorted to battery, an internal comparator senses the output voltage level then turns off an internal series transistor to provide blocking diode for the current going through the output channel. The output will be OFF only when fault condition is present. As soon as the fault disappears, the interface will become ON again. A leakage to battery fault will be set and reported in the SR word after it has been present for t_{Flt_BATT}. Once read it shall be cleared and if the condition is still present the flag will be set. The comparators have 20 to 50 mV input offset to prevent turning off the output under an open circuit condition.

IFx/Vx output configuration

The IFx/Vx pins are high impedance by writing to D7 and D6 of the MCR and setting the bits to 0. When the pins are enabled and if the pin is shorted to ground then the device can source up to 100mA from VDD.

Analog output

Channels 2 and 3 of the device can by used to provide an analog feed back current as a $1/100^{th}$ ratio of the sense current in this mode internal data register and decoder are bypassed. This will allow the IF2/V2 and IF3/V3 pins to be connected to a resistor to ground and provide an analog voltage equivalent to the sense current to be read by an A/D port. These two pins have an internal clamp as protection. This feature is available for Channels 2 and 3.

Digital output

Channels 2 and 3 can be configured as a logic level output with the level reflecting if the current is above or below the selected internal current threshold. See *Table 33* for MCR and CCR bit settings for this mode. The output voltage has a reversed polarity to the satellite current such that when the current drawn by the satellite is below the current detection threshold, the IFx/Vx signal level transitions into a high state, on the other hand if the current drawn by the satellite exceeds the current detection threshold, IFx/Vx signal transitions into a low state.

Channel 2 and 3 mode selection

These channels can be configured to decode satellite messages or Hall Effect sensors and provide results through the SPI and/or the IFx/Vx pins. The following *Table 33* shows the settings for the MCR and CCR based on the interfacing to a sensor or satellite.

Table 33. MCR and CCR settings based on the interfacing to a sensor or satellite

Register settings			Functions active		Information available	
MCR D7/D6 Bits	MCR D5/D4 Bits	CCR D5:D4 Bits	Channel (ICHx)	Decoder	SPI DATA register	IFx/Vx pin
0	0	00	OFF (ICHx HiZ)	OFF	Empty	OFF (HiZ)
0	1	00	OFF (ICHx HiZ)	OFF	Empty	OFF (HiZ)
1	0	00	OFF (ICHx HiZ)	OFF	Empty	ON (1)
1	1	00	OFF (ICHx HiZ)	OFF	Empty	VDD
0	0	01	ON	OFF	Empty	OFF (HiZ)
0	1	01	ON	OFF	Data will reflect if ICHx current is above/below threshold setting (1) D0 = 0 (above thres.) D0 = 1 (below thres.)	OFF (HiZ)
1	0	01	ON	OFF	Empty	Analog Output (I_Sat/100)

Table 33. MCR and CCR settings based on the interfacing to a sensor or satellite (continued)

Register settings			Functions active		Information available	
MCR D7/D6 Bits	MCR D5/D4 Bits	CCR D5:D4 Bits	Channel (ICHx)	Decoder	SPI DATA register	IFx/Vx pin
1	1	01	ON	OFF	Data will reflect if ICHx current is above/below threshold setting (1) D0 = 0 (above thres.) D0 = 1 (below thres.)	Digital Output
0	0	10	ON	ON	Satellite Data	OFF (HiZ)
0	1	10	ON	ON	Satellite Data	OFF (HiZ)
1	0	10	ON	ON	Empty	Analog Output (I_Sat/100)
1	1	10	ON	ON	Satellite Data	Digital Output
0	0	11	ON	OFF	Empty	OFF (HiZ)
0	1	11	ON	OFF	Empty	OFF (HiZ)
1	0	11	ON	OFF	Empty	Analog Output (I_Sat/100)
1	1	11	ON	OFF	Empty	Digital Output

1. IFx/Vx Pin is set as Analog Output (I_Sat/100) but since ICHx is off (HiZ) the IFx/Vx output will look like it is HiZ

3.4.7 SPI register definition for satellite functions

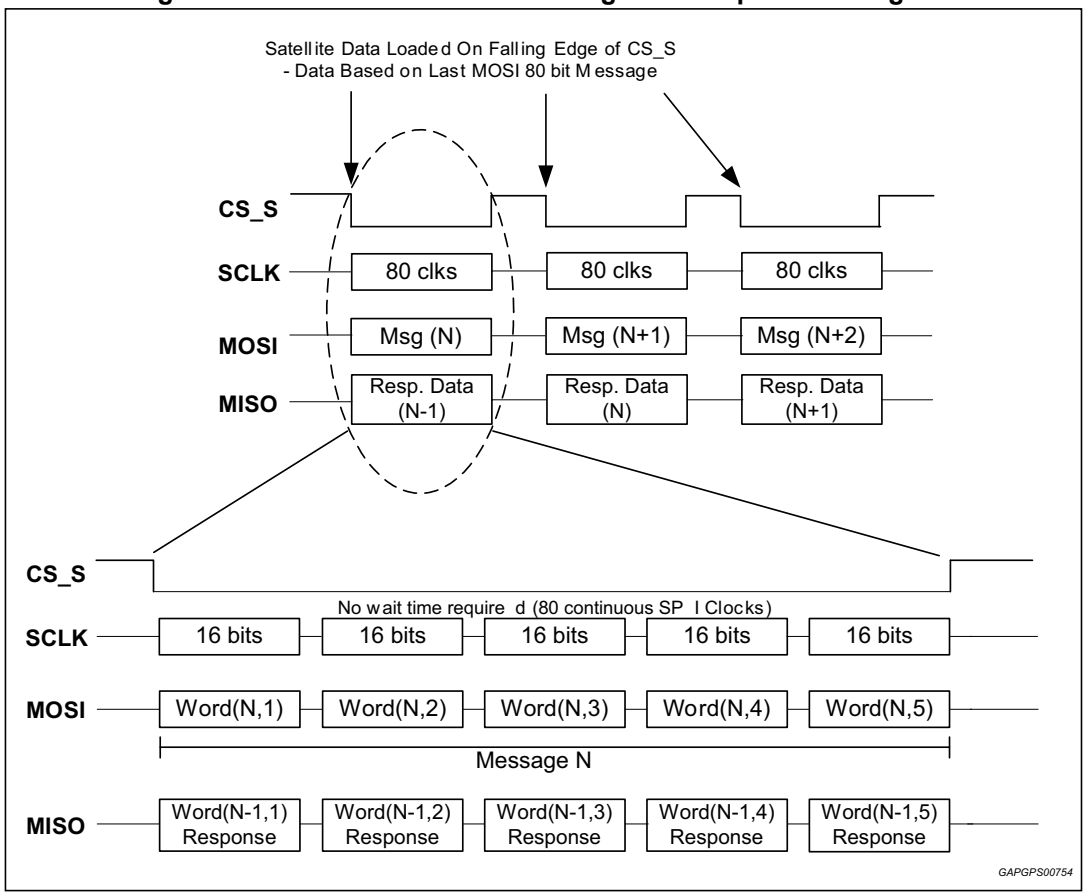
The SPI provides access to read/write to the registers internal to the device. All commands sent to the ASIC shall use set D15 as required for odd parity on the 16 bit word. The total message length when CS_S is active is 80 bits. The response to the command is sent in the next valid CS_S.

Table 34. SPI register definition

Registers for satellite communication		Description
Module Configuration Register	MCR	Global configuration for all channels
Channel Configuration Registers	CCR1 CCR2 CCR3 CCR4	Used to configure individual channels and receive satellite information Internal pointer incremented to each channel register
Status Register	SR	Status of channels Channel leakage to ground/battery/open faults Message faults (Start bits, Other)

The following diagram shows the satellite SPI transfer during normal operation. The satellite data is uploaded based on CS_S going active. All the register data for the channels will be loaded at the same time.

Figure 20. Satellite SPI transfer during normal operation diagram



Based on the above format the micro must send the commands in a specific order. The following table represents the allowable commands/positions sent out on MOSI along with responses.

Table 35. Commands/positions sent out on MOSI along with responses

Word position	Allowable MOSI	Commands MISO reponses
Word (N,1)	MCR	MCR(1) or SR
Word (N,2)	CCR1	CCR1 or Data
Word (N,3)	CCR2	CCR2 or Data
Word (N,4)	CCR3	CCR3 or Data
Word (N,5)	CCR4	CCR4 or Data

1. Only allowed if Words 2-5 are CCRs.

When the device is set to report the MCR in the MISO response it must be done only when reporting all CCRs. If Data is reported with the MCR in the MISO response then the data status information is lost. When the MCR is in MISO word 1 then there is no indicator whether a response in words 2 to 5 are CCR or Data.

If the SR is returned in the MISO response with a CCR then the status information for that word will not change until the next SR with Data. The SR bits will indicate which words are CCR and Data.

The MOSI input takes data from the master microprocessor while CS_S is asserted. The MSB is the first bit of each word received on MOSI and the LSB is the last bit of each word received on MOSI. This pin has TTL level compatible input voltages allowing proper operation with microprocessors using a 3.3 to 5.0 volt supply.

When data is transmitted for any of the first 4 words on MISO then the SR will be the 5th word. This is required to identify good vs. bad data since, depending on the data mode, all 16 bits from a satellite can be data.

Satellite module configuration register (MCR)

This register defines the global configuration to the satellite module.

The MCR will be the 1st word in the message of the MOSI transfer. The micro MUST never write the MCR in the wrong position because it will be recognized by the ASIC as a CCR.

The SPI message definition for MOSI commands and MISO responses for the MCR are defined below.

Command/ Mode	MOSI Bit Definition															
	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
MOSI Command																
MCR	0	0	CH4P	CH3P	CH2P	CH1P	SPL1	SPL0	IV4EN	IV3EN	IV4SEL	IV3SEL	SW	RD	0	odd
MISO Response																
MCR	0	0	CH4P	CH3P	CH2P	CH1P	SPL	SPL	IV4EN	IV3EN	IV4SEL	IV3SEL	SW	RD	0	odd

Table 36. MOSI MCR bit definition

Bit	MOSI Command MS – Mode‘D3’=0		MOSI Command PSI5 – Mode‘D3’=1
	State	Description	
D15	0		
D14	0	Register Selection (SR/MCR)	
D13	0 1	CH3 Protocol A Mode (default) CH3 Protocol B Mode	Not valid PSI5 Parity
D12	0 1	CH2 Protocol A Mode (default) CH2 Protocol B Mode	Not valid PSI5 Parity
D11	0 1	CH1 Protocol A Mode (default) CH1 Protocol B Mode	Not valid PSI5 Parity
D10	0 1	CH0 Protocol A Mode (default) CH0 Protocol B Mode	Not valid PSI5 Parity
D9	0	Sync Pulse length	Sync Pulse length
D8	0		
D7	0	Disable IF3/V3 pin (default)	Disable IF3/V3 pin (default) Enable IF3/V3 pin
	1	Enable IF3/V3 pin	
D6	0	Disable IF2/V2 pin (default)	Disable IF3/V3 pin (default) Enable IF3/V3 pin
D5		IF3/V3 Output Selection	IF3/V3 Output Selection

Table 36. MOSI MCR bit definition (continued)

Bit	MOSI Command MS – Mode'D3'=0		MOSI Command PSI5 – Mode'D3'=1
	State	Description	
D4		IF2/V2 Output Selection	IF2/V2 Output Selection
D3	0 1	MS Mode (Prot a\Prot B) Default PSI5 Mode	MS Mode (Prot a\Prot B) Default PSI5 Mode
D2		Receiver Disable Time Selection	Receiver Disable Time Selection
D1	X		
D0		Odd Parity – Includes all 16 bits	Odd Parity – Includes all 16 bits

The following describes the bit usage for both MS & PSI5 Satellite Modes:

Bit [D15] If during the previous received request a SPI communication error occurred or invalid message was received, the device shall set bit D15 indicating that the whole data frame of 80 bit is not valid.

Bits [D13:D10] These bits are used to configure the output channels for either CRC or Parity sensor protocols.

When in MS Mode the default configuration is the protocol A. For PSI5 mode these bits must be set to 1's.

Bits [D09:D08] Sync Pulse high time

Table 37. Sync pulse high time selections

SPL1	SPL0	Description
0	0	20µs (default)
0	1	30µs
1	0	40µs
1	1	80µs

Bit [D7:D5] These bits control the configuration of the IF3/V3 pin.

Table 38. Configuration of the IF3/V3 pin

D7/D6	D5/D4	Description
0	0	IFx/Vx pin is HiZ
0	1	IFx/Vx pin is HiZ
1	0	IFx/Vx pin will source an analog current that is 1/100 of the sensor current
1	1	IFx/Vx pin will be a digital output indicating if the current is above or below the selected threshold. When a channel (ICHx) is off this pin will be high (~VDD).

Bit [D3] Satellite Communication Protocol Selection
0 = MS Protocol
1 = PSI5 Protocol

Bit [D2]. Receiver disable time selection

0 = Receiver disable time is 62µs typical

1 = Receiver disable time is (Tsynchighx time + 20µs)

Channel configuration registers (CCR1, CCR2, CCR3, CCR4)

The SPI message definition for MOSI commands and MISO responses for the CCR/Data are defined below.

Command/ Mode from Master	MOSI Bit Definition															
	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
MOSI Command																
CCR	odd	RS	R/W	MAN	CRC	PC1	PC0	SYNC	BT1	BT0	EN1	EN0	IHYS	I_Threshold		
MISO Response (CCR)																
CCR (D14=1 in MOSI)	odd	1	R/W	MAN	CRC	PC1	PC0	SYNC	BT1	BT0	EN1	EN0	IHYS	I_Threshold		
MISO Response (Data)																
CCR (D14=1 in MOSI)	See *Table 40* for MISO Responses															

Table 39. MOSI CCR bit definition

Bit	State	MS Mode	PSI5 Mode (1)	MS / PSI5 Mode	MS / PSI5 Mode
		MOSI Command	MOSI Command	MISO Response for CCR Mode	MISO Response for Data Mode
		Description			
D15		Odd Parity – Includes all 16 bits	Same as MS Mode	Odd Parity – Includes all 16 bits	See *Table 40*
D14	0 1	Register Selection: CCR (1) / DATA (0)	Same as MS Mode	1= CCR response	
D13	0	Read	Same as MS Mode	R/W	
	1	WRITE (only valid if CCR request)			

Table 39. MOSI CCR bit definition (continued)

Bit	State	MS Mode	PSI5 Mode (1)	MS / PSI5 Mode	MS / PSI5 Mode
		MOSI Command	MOSI Command	MISO Response for CCR Mode	MISO Response for Data Mode
		Description			
D12	0	Manchester 2	Not Used	Manchester Selection PSI5 mode – don't care	See *Table 40*
	1	Manchester 1			
D11	0	Checksum calculation enabled (default) – Target is to use checksum calculated by ASIC	Not Used	Checksum calculation Status PSI5 mode – don't care	
	1	Checksum calculation disabled Note: Checksum for MS only not PSI5			
D10	1	MS Message Length See *Table 40*	PSI5 Message Length See *Table 40*		
	0			Data length Status	
D9	1				
	0				
D8	0	Sync pulse disabled (default)	Same as MS Mode	Sync pulse Status	
	1	Sync pulse enabled			
D7		Bit time selection	Same as MS Mode	Bit time selection	
D6					
D5		Satellite/Decoder Control	Same as MS Mode	Satellite/Decoder Control	
D4					
D3	0	Current Trip Point Hysteresis Disabled (default)	Same as MS Mode	Current Trip Point Hysteresis Status	
	1	Current Trip Point Hysteresis Enabled			
D2		Current Trip Point threshold	Same as MS Mode	Current Trip Point threshold	
D1					
D0					

1. MISO Response shown in *Table 40*.

Table 40. MISO responses with D14=0 (Data register selection)

MOSI Bit Setting			MISO Bit Definition															
D11	D10	D09	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
MISO Data Response in MS Mode: MERAS Protocol																		
0	0	0	odd	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	SV2	SV1	SV0	0	0
0	0	1	odd	D7	D6	D5	D4	D3	D2	D1	D0	SV2	SV1	SV0	0	0	0	0

Table 40. MISO responses with D14=0 (Data register selection) (continued)

MOSI Bit Setting			MISO Bit Definition															
D11	**D10**	**D09**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D09**	**D08**	**D07**	**D06**	**D05**	**D04**	**D03**	**D02**	**D01**	**D00**
0	1	0	odd	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		0	0	0	0
0	1	1	odd	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0	0	0	0
1	0	0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	SV2	SV1	SV0	CRC2	CRC1	CRC0
1	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0	SV2	SV1	SV0	CRC2	CRC1	CRC0	0
1	1	0	0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	CRC2	CRC1	CRC0	0	0
1	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0	CRC2	CRC1	CRC0	0	0	0	0
MISO Data Response in MS Mode: Generic Protocol																		
0	0	0	odd	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	SV2	SV1	SV0	0	0
0	0	1	odd	D7	D6	D5	D4	D3	D2	D1	D0	SV2	SV1	SV0	0	0	0	0
0	1	0	odd	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0	0
0	1	1	odd	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0	0	0	0
1	0	0	P	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	SV2	SV1	SV0	0	0
1	0	1	P	D7	D6	D5	D4	D3	D2	D1	D0	SV2	SV1	SV0	0	0	0	0
1	1	0	P	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0	0
1	1	1	P	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0	0	0	0
MISO Data Response in PSI5 Mode: Parity Protocol																		
X	0	0	odd	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0
X	0	1	odd	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0
X	1	0	odd	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0	0
X	1	1	odd	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0	0	0	0
MISO Data Response in Raw Data Mode																		
0	X	X	odd	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Data
1	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Data
MISO Data Response in Hall Effect Mode																		
0	X	X	odd	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: With CHxSF2:CHxSF0 = '000', '001, or '101'

When transferring data if the CRC check is disabled on the ASIC then there is no parity bit and the CRC bits will be present along with the data bits on the MISO line.

The following describes the bit usage for the CCR command

Bits [D11]. Used to enable/disable checksum calculations in MS satellite mode (D11 is ignored in PSI5).

0 = Checksum performed by ASIC
1 = Checksum calculation disabled

Bits [D10:D09]. These bits are used to configure the number of bits in the MS and PSI5 Modes.
MS Mode: For these bits to execute on any given channel, the channel has to be configured for generic protocol B / protocol A through bits <D13:D10> in the MCR register. If the checksum calculation is disabled the ASIC does not perform a parity check on the incoming message and will be included in the data field.

Table 41. Protocol A/B mode configuration

D10	D09	Protocol-A Mode (Set in MCR – D13:D10)			Protocol -B Mode (Set in MCR – D13:D10)		
		Message Length	Data Report Length		Message Length	Data Report Length	
			D11=0	D11=1		D11=0	D11=1
0	0	18 bits	13 bits (default)	16 bits	16 bits	13 bits (default)	14 bits)
0	1	16 bits	11 bits	14 bits	14 bits	11 bits	12 bits
1	0	15 bits	10 bits	13 bits	13 bits	10 bits	11 bits
1	1	13 bits	8 bits	11 bits	11 bits	8 bits	9 bits

PSI5 Mode: For these bits to execute on any given channel, the channel has to be configured for PSI5 - Parity protocol through bits <D13:D10> in the MCR register. In PSI5 mode, the checksum calculation is always done by the ASIC, thus, bit D11 is ignored and parity bits are not included in the MISO response.

Table 42. PSI5 – parity protocol (Set in MCR D13:D10)

D10	D09	Message Length	Data Report
0	0	16 bits	13 bits (default)
0	1	14 bits	11 bits
1	0	13 bits	10 bits
1	1	11 bits	8 bits

Bits [D7:D6]. These bits shall configure speed selection for any of the satellite channels. Upon power up or reset the protocol configuration shall initialize to the default speed as shown in the table below.

Table 43. Default speed

D7	D6	Guaranteed frequency operating range (kHz)
0	0	62.66 to 238.66 (default)
0	1	43.50 to 158.97
1	0	26.32 to 106.04
1	1	13.3 to 51.25

Bits [D5:D4]. These bits are used to enable the satellite channels and the internal decoders to be commanded on or off according to the following table. If both the satellite and decoder are to be enabled then the channel needs to be enabled first and in a following command the decoder would be enabled. This is to prevent erroneous/spurious data to be read.

Table 44. On/off condition for satellite and decoder

D5	D4	Definition		SPI DATA Register (For appropriate wordx)	
		Satellite	Decoder	ICH0/ICH1	ICH2/ICH3
0	0	OFF (default)	OFF (default)	Empty	See *Table 33*
0	1	ON	OFF	Data will reflect if ICHx current is above/below threshold setting (1) D0 = 0 (above thres.) D0 = 1 (below thres.)	
1	0	ON	ON	Sat. Data	
1	1	ON	OFF	Empty	

Bit D3 All incoming satellite signals are processed through deglitch filter before reaching the decoder. D3 enables a hysteresis around the current threshold for added noise immunity.

Bits [D2:D0] These bits program the threshold for the current demodulation affecting each individual channel. The current ranges supported are showed in table below.

Table 45. Current range supported

D2	D1	D0	Current Threshold (mA) min/max
0	0	0	1.0/4.0(default)
0	0	1	8.0/11.0
0	1	0	14.85/18.15

Table 45. Current range supported

D2	D1	D0	Current Threshold (mA) min/max
0	1	1	17.10/20.90
1	0	0	20.25/24.75
1	0	1	24.85/29.15
1	1	0	28.80/34.20
1	1	1	35.10/42.90

Status registers (SR)

The definition for the Status Register is valid for all four protocols.

The SR will always be the 1st word in the message of the MOSI frame

The message faults and data/channel information are indicated using 3 bits per channel (SF2, SF1 and SF0). These bits represent the actual highest priority state of the ICHx-receiver, i.e. any change in a state will overwrite the previous value with the highest priority fault being reported if more than one fault exists.

Command/ Mode from Master	MOSI Bit Definition															
	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
MOSI Command																
	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	odd
MISO Response																
SR	SPI ERR	1	CH4 SF2	CH4 SF1	CH4 SF0	CH3 SF2	CH3 SF1	CH3 SF0	CH2S SF2	CH2S SF1	CH2S SF0	CH1S SF2	CH1 SF1	CH1 SF0	POR STAT	odd

The following describes the bit usage

Bit [D15] If during the previous received request a SPI communication error occurred or invalid message was received, the device shall set bit D15 and this means that the whole data frame of 80 bit is not valid.

Bits [D13:D02] Fault Codes Definition Supporting Satellite Interface, Hall Effect, and raw data modes

Table 46. CCR D14 definition

Priority	CHxSF2	CHxSF1	CHxSF0	Description
CCR D14=0				
7	0	0	0	Good Data from satellite on word ‘x’
6	0	0	1	Two or more good data received from satellite, i.e. there are some data lost.

Table 46. CCR D14 definition (continued)

Priority	CHxSF2	CHxSF1	CHxSF0	Description
5	0	1	0	Register empty. No data received from satellite
4	0	1	1	Not valid data received i.e. – Start bit time outside valid range – Frame length – Bit time error – CRC/Parity error on sat received message (in this case there should be “register empty”)
3	1	0	0	Leakage to Supply Voltage at ICHx port and Not Good Data (data lost or register empty or not valid data)
2	1	0	1	Leakage to Supply at ICHx port & Good Data
1	1	1	0	Leakage to ground at ICHx port; (Over current detected switched OFF ICHx analog port, it can be still OFF if micro never wrote on CCR.D5:D4 to switch ON port)
CCR D14=1				
NA	1	1	1	CCR report is present on word ‘x’: Channel status is the response selected with bit D14 on CCR command

Codes are prioritized with the highest being 1 and the lowest being 7.

Error code 011 is an “or-ed”combination of the following errors:

- Start bit error outside of selected operating range
- Data length error or stop bit error
- CRC/Parity Error of received Satellite Message
- Bit time error outside 75% 125% of start bit

If in Hall Effect mode the status register under normal conditions will report a Register Empty (CHxSF2:CHxSF0='010'). If a fault is on the channel then either a Leakage to supply and no good data (CHxSF2:CHxSF0='101') or Leakage to ground (CHxSF2:CHxSF0='110') would be present.

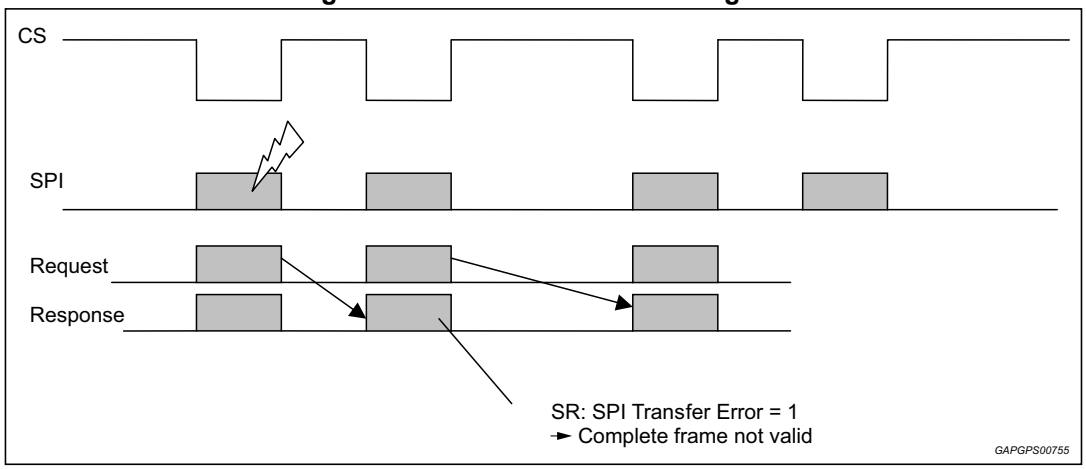
If in Raw data mode the status resister under normal conditions will report Register Empty (CHxSF2:CHxSF0='010').

- If decoder is on then satellite data will be present (See *Table 40* under protocol A or Protocol B)
- If decoder is off then D0 will contain data

If a fault is on the channel then either a Leakage to supply and no good data (CHxSF2: CHxSF0='101') or Leakage to ground (CHxSF2:CHxSF0='110') would be present.

Bit [D00] POR status
0 = Reset occurred. Bit cleared when read
1 = Normal

Figure 21. Combination errors diagram



This error is an”or-ed” combination of the following errors:

- Parity
- Length

If a SPI error is detected by the ASIC the response shall be a SR followed by all Data Words.

Following a POR the first response from the ASIC over SPI2 shall be as follows:

Table 47. First response from the ASIC over SPI2e

Word Position	Register Type	Data
Word 1	SR	$5248
Word 2	Data	$8000
Word 3	Data	$8000
Word 4	Data	$8000
Word 5	Data	$8000

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 LQFP64 (10x10x1.4 mm) package information

Figure 22. LQFP64 (10x10x1.4 mm) package outline

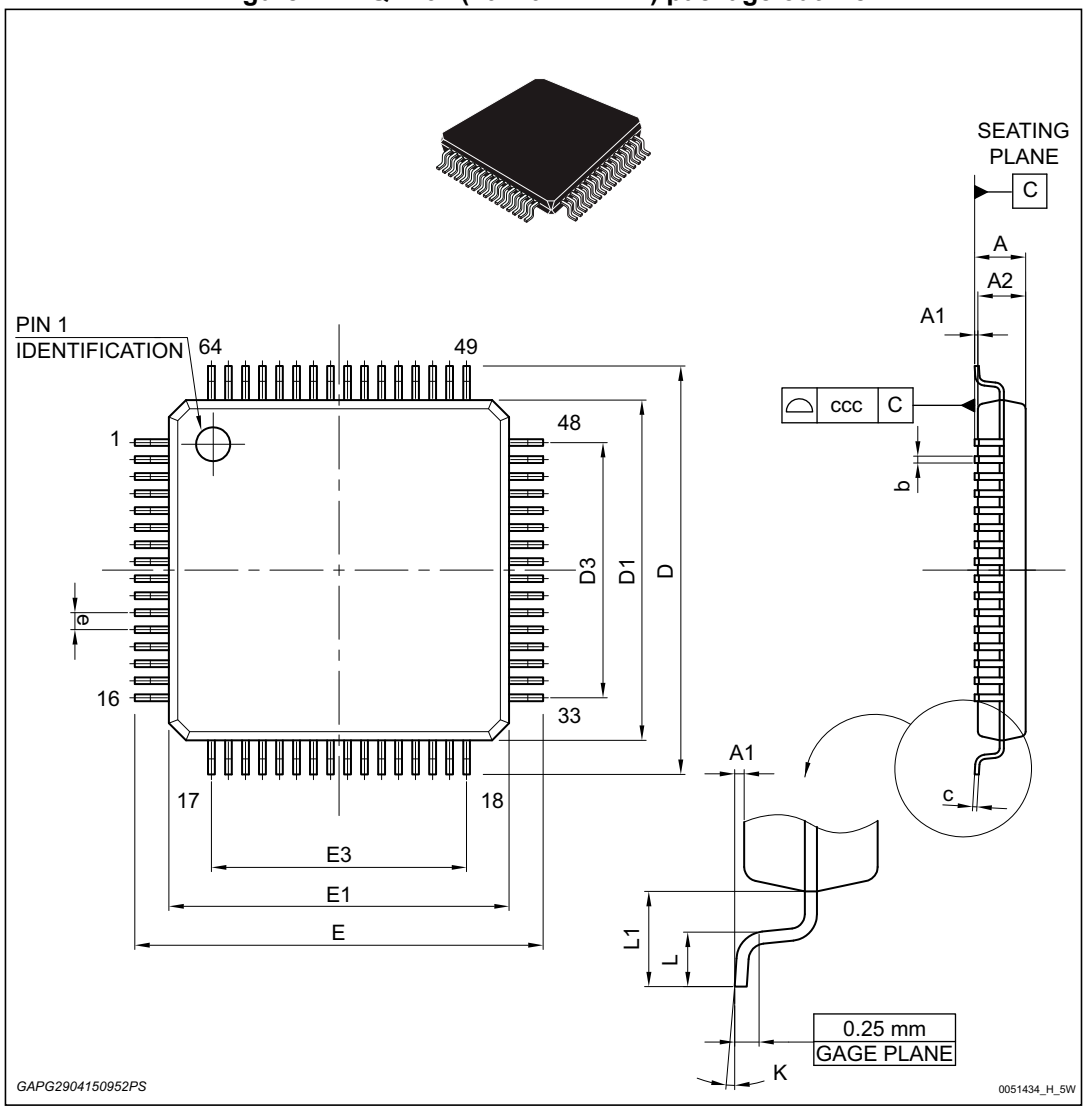


Table 48. LQFP64 (10x10x1.4 mm) package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.60	-	-	0.0630
A1	0.05	-	0.15	0.0020	-	0.0059
A2	1.350	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09	-	0.20	0.0035	-	0.0079
D	11.80	12.00	12.20	0.4646	0.4724	0.4803
D1	9.80	10.00	10.20	0.3858	0.3937	0.4016
D3	-	7.50	-	-	0.2953	-
E	11.80	12.00	12.20	0.4646	0.4724	0.4803
E1	9.80	10.00	10.20	0.3858	0.3937	0.4016
E3	-	7.50	-	-	0.2953	-
e	-	0.50	-	-	0.0197	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
K	0° (min.), 3.5° (typ.) 7° (max.)					
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

5 Revision history

Table 49. Document revision history

Date	Revision	Changes
08-Sep-2015	1	Initial release.

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