

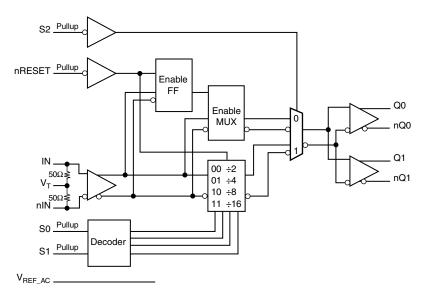
General Description

The 8S89874 is a high speed 1:2 Differential-to- LVPECL Buffer/ Divider. The 8S89874 has a selectable $\div 1$, $\div 2$, $\div 4$, $\div 8$, $\div 16$ output divider, which allows the device to be used as either a 1:2 fanout buffer or frequency divider. The clock input has internal termination resistors, allowing it to interface with several differential signal types while minimizing the number of required external components. The device is packaged in a small, 3mm x 3mm VFQFN package, making it ideal for use on space-constrained boards.

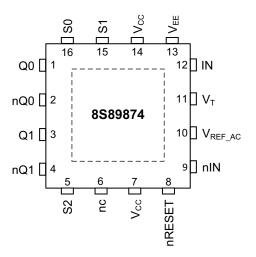
Features

- Two LVPECL/ECL output pairs
- Frequency divide select options: ÷1 (pass through), ÷2, ÷4, ÷8, ÷16
- IN, nIN input can accept the following differential input levels: LVPECL, LVDS, CML
- Output frequency: 2GHz (maximum)
- Output skew: 15ps (maximum)
- Part-to-part skew: 250ps (maximum)
- · Additive phase jitter, RMS: 0.20ps (typical)
- LVPECL supply voltage range: 2.375V to 3.63V
- ECL supply voltage range: -3.63V to -2.375V
- -40°C to 85°C ambient operating temperature
- · Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



16-pin, 3mm x 3mm VFQFN Package



Table 1. Pin Descriptions

Number	Name	Ту	ре	Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL/ECL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVPECL/ECL interface levels.
5, 15, 16	S2, S1, S0	Input	Pullup	Select pins. LVCMOS/LVTTL interface levels.
6	nc	Unused		No connect.
7, 14	V _{cc}	Power		Positive supply pins.
8	nRESET	Input	Pullup	When LOW, resets the divider. Pulled HIGH when left unconnected. Input threshold is $V_{CC}/2$. Includes a 37k Ω pullup resistor. LVTTL/LVCMOS interface levels.
9	nIN	Input		Inverting differential LVPECL clock input. $R_T = 50\Omega$ termination to V_T .
10	V _{REF_AC}	Output		Reference voltage for AC-coupled applications.
11	V _T	Input		Termination input.
12	IN	Input		Non-inverting LVPECL differential clock input. $R_T = 50\Omega$ termination to V_T .
13	V _{EE}	Power		Negative supply pin.

NOTE: Pullup refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R _{PULLUP}	Input Pullup Resistor			37		kΩ



Function Tables

Table 3A. Control Input Function Table

	Inputs	Outputs		
nRESET Selected Source		Q0, Q1	nQ0, nQ1	
0	IN/nIN	Disabled; LOW	Disabled; HIGH	
1	IN/nIN	Enabled	Enabled	

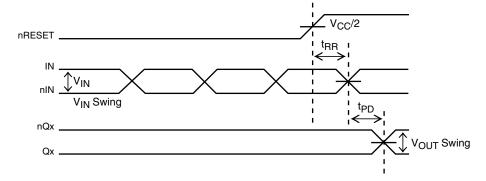


Figure 1. nRESET Timing Diagram

Table 3B. Truth Table

	Inputs			
nRESET	S2	S1	S0	Outputs
1	0	Х	Х	Reference Clock ÷1 (pass through)
1	1	0	0	Reference Clock ÷2
1	1	0	1	Reference Clock ÷4
1	1	1	0	Reference Clock ÷8
1	1	1	1	Reference Clock ÷16
0	1	Х	Х	Q = LOW, nQ = HIGH; Clock Disabled
0	0	Х	Х	Q = LOW, nQ = HIGH; Clock Disabled



Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V _{CC}	-0.5V to + 4.6V
Inputs, V _I	-0.5V to V _{CC} + 0.5V
Outputs, I _O Continuous Current Surge Current	50mA 100mA
Input Current, IN, nIN	±50mA
V _T Current, I _{VT}	±100mA
V _{REF_AC} Input Sink/Source, I _{REF_AC}	±2mA
Operating Temperature Range, T _A	-40°C to +85°C
Package Thermal Impedance, θ_{JA} , (Junction-to-Ambient)	74.7°C/W (0 mps)
Storage Temperature, T _{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = 3.3V \pm 10\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V _{CC}	Positive Supply Voltage		2.375	3.3	3.63	V
I _{EE}	Power Supply Current				45	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = 3.3V \pm 10\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V _{IH}	Input High Voltage		2.2		V _{CC} + 0.3	V
V _{IL}	Input Low Voltage		0		0.8	V
I _{IH}	Input High Current	V _{CC} = V _{IN} = 3.63V or 2.625V			10	μΑ
I _{IL}	Input Low Current	V _{CC} = 3.63V or 2.625V, V _{IN} = 0V	-150			μΑ



Table 4C. Differential DC Characteristics, V_{CC} = 3.3V \pm 10% or 2.5V \pm 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R _{IN}	Differential Input Resistance	(IN, nIN)		40	50	60	Ω
V _{IH}	Input High Voltage	(IN, nIN)		1.2		V _{CC}	V
V _{IL}	Input Low Voltage	(IN, nIN)		0		V _{IH} – 0.15	V
V _{IN}	Input Voltage Swing			0.15		1.2	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3			V
I _{IN}	Input Current; NOTE 1	(IN, nIN)				35	mA
V _{REF_AC}	Bias Voltage			V _{CC} - 1.45	V _{CC} – 1.37	V _{CC} - 1.32	V

NOTE 1: Guaranteed by design.

Table 4D. LVPECL DC Characteristics, V_{CC} = 3.3V \pm 10% or 2.5V \pm 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V _{OH}	Output High Voltage; NOTE 1		V _{CC} – 1.175		V _{CC} – 0.82	V
V_{OL}	Output Low Voltage; NOTE 1		V _{CC} – 2.0		V _{CC} – 1.575	V
V _{OUT}	Output Voltage Swing		0.6		1.0	V
V _{DIFF_OUT}	Differential Output Voltage Swing		1.2		2.0	V

NOTE: Input and output parameters vary 1:1 with V $_{CC}.$ NOTE 1: Outputs terminated with 50 $\!\Omega$ to V $_{CC}$ – 2V.



AC Electrical Characteristics

Table 5. AC Characteristics, $V_{CC} = 3.3V \pm 10\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f _{OUT}	Output Frequency	Output Swing ≥ 450mV			2	GHz
f _{IN}	Input Frequency	÷2, ÷4, ÷8, ÷16			2.5	GHz
IDD	Propagation Delay; (Differential);	Input Swing: <400mV	460	640	840	ps
	NOTE 1	Input Swing: ≥ 400mV	430	615	810	ps
tsk(o)	Output Skew; NOTE 2, 4				15	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4				250	ps
<i>t</i> jit	Buffer Additive Jitter; RMS; refer to Additive Phase Jitter Section; NOTE 5	155.52MHz, Integration Range: 12kHz – 20MHz		0.20		ps
t _{RR}	Reset Recovery time		600			ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	70		250	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters characterized at ≤ 1GHz, 800mV input signal, unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

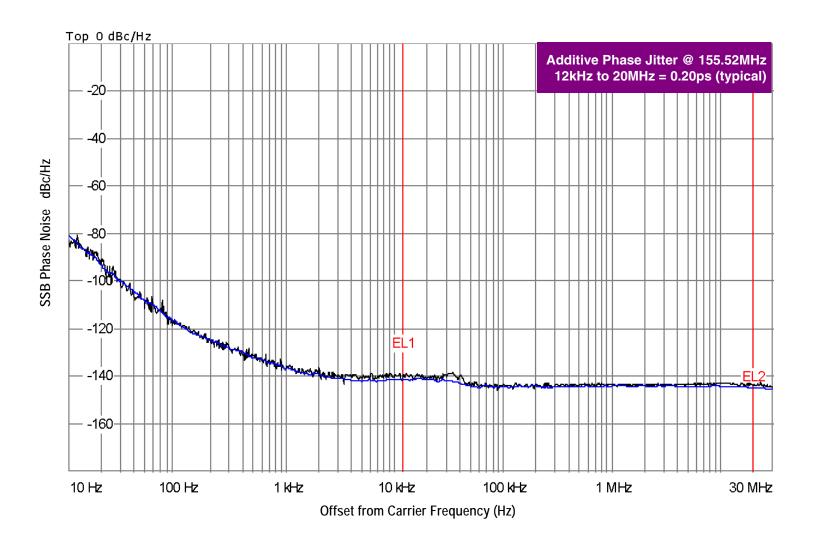
NOTE 5: Pass through, ÷1 mode.



Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise*. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the

fundamental. When the required offset is specified, the phase noise is called a *dBc* value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

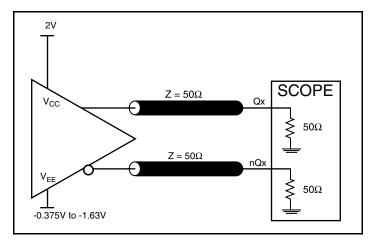


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

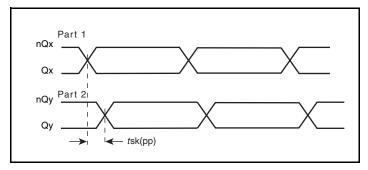
The source generator IFR2042 and Agilent 8133 were the external input to drive the input clock, IN, nIN.



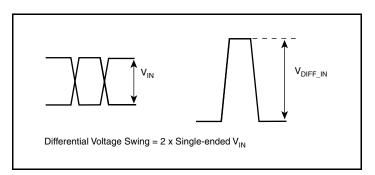
Parameter Measurement Information



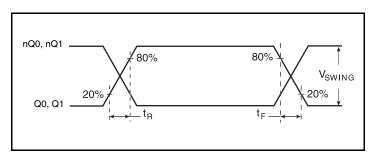
Output Load AC Test Circuit



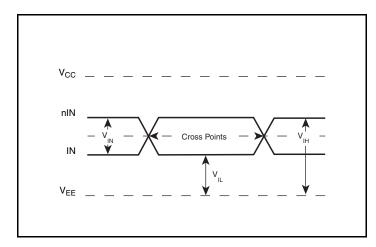
Part-to-Part Skew



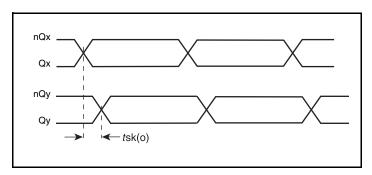
Single-ended & Differential Input Voltage Swing



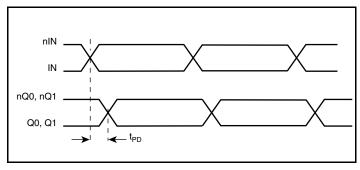
Output Rise/Fall Time



Differential Input Level



Output Skew



Propagation Delay



Applications Information

3.3V Differential Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 2A to 2D* show interface examples for the IN/nIN input with built-in 50Ω terminations driven by

the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

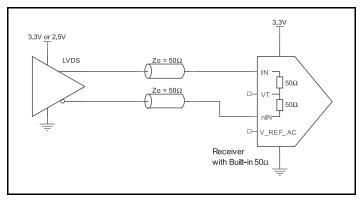


Figure 2A. N/nlN Input with Built-In 50Ω Driven by an LVDS Driver

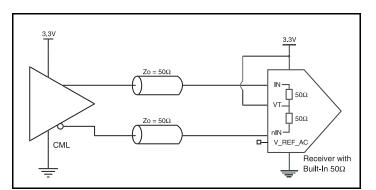


Figure 2C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver

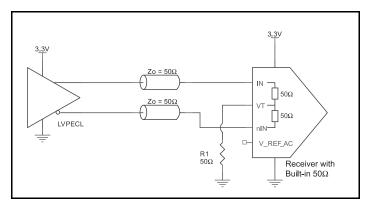


Figure 2B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

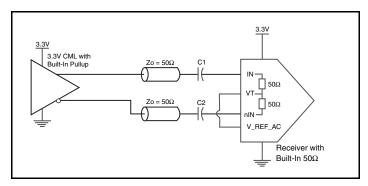


Figure 2D. IN/nIN Input with Built-In 50 Ω Driven by a CML Driver with Built-In 50 Ω Pullup



2.5V LVPECL Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 3A to 3D* show interface examples for the IN/nIN with built-in 50Ω termination input driven by

the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

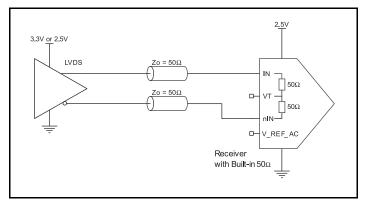


Figure 3A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

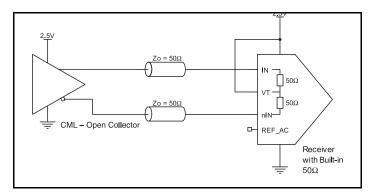


Figure 3C. IN/nIN Input with Built-In 50 Ω Driven by a CML Driver

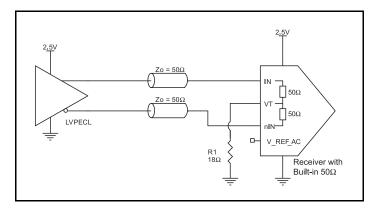


Figure 3B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

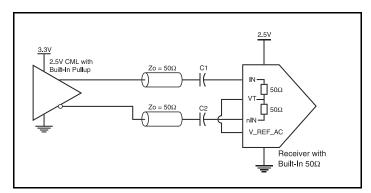


Figure 3D. IN/nIN Input with Built-In 50 Ω Driven by a CML Driver with Built-In 50 Ω Pullup



Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins has internal pullups; additional resistance is not required but can be added for additional protection. A $1k\Omega$ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

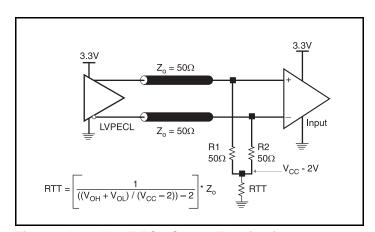


Figure 4A. 3.3V LVPECL Output Termination

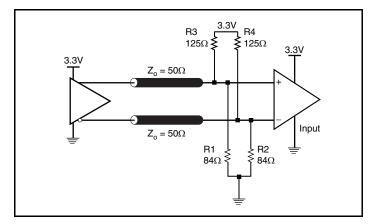


Figure 4B. 3.3V LVPECL Output Termination



Termination for 2.5V LVPECL Outputs

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground

level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C*.

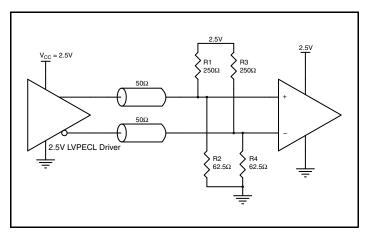


Figure 5A. 2.5V LVPECL Driver Termination Example

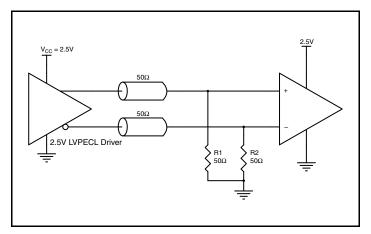


Figure 5C. 2.5V LVPECL Driver Termination Example

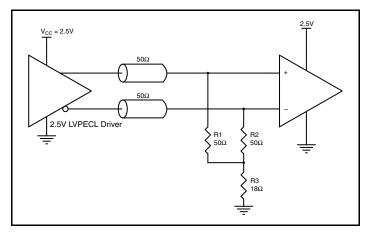


Figure 5B. 2.5V LVPECL Driver Termination Example



VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a quideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

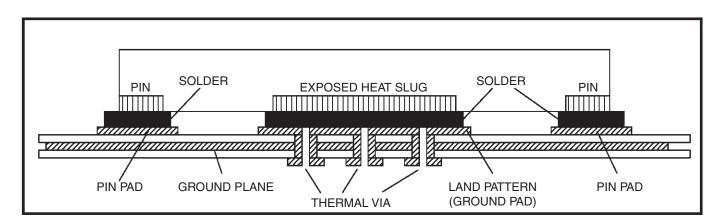


Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)



Power Considerations

This section provides information on power dissipation and junction temperature for the 8S89874. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8S89874 is the sum of the core power plus the power dissipated in the load(s).

The following is the power dissipation for $V_{CC} = 3.63V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = V_{CC MAX} * I_{EE MAX} = 3.63V * 45mA = 163.35mW
- Power (outputs)_{MAX} = 32.62mW/Loaded Output pair
 If all outputs are loaded, the total power is 2 * 32.62mW = 65.24mW
- Power Dissipation for internal termination R_T Power $(R_T)_{MAX} = (V_{IN\ MAX})^2/R_{T\ MIN} = (1.2V)^2/80\Omega = 18mW$

Total Power_MAX = (3.63V, with all outputs switching) = 163.35mW + 65.24mW + 18mW = 246.59mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

 θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

 $85^{\circ}\text{C} + 0.247\text{W} * 74.7^{\circ}\text{C/W} = 103.5^{\circ}\text{C}$. This is well below the limit of 125°C .

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead VFQFN, Forced Convection

$ heta_{\sf JA}$ vs. Air Flow					
Meters per Second	0	1	2.5		
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W		



3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in Figure 7.

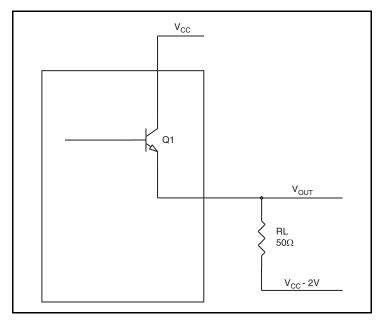


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} 0.82V$ $(V_{CC_MAX} V_{OH_MAX}) = 0.82V$
- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} 1.58V$ $(V_{CC_MAX} - V_{OL_MAX}) = 1.58V$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - 0.82V)/50\Omega] * 0.82V = \textbf{19.35mW}$$

$$Pd_{L} = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_{L}] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_{L}] * (V_{CO_MAX} - V_{OL_MAX}) = [(2V - 1.58V)/50\Omega] * 1.58V = 13.27mW$$

Total Power Dissipation per output pair = Pd_H + Pd_L = 32.62mW



Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ _{JA} by Velocity						
Meters per Second	0	1	2.5			
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W			

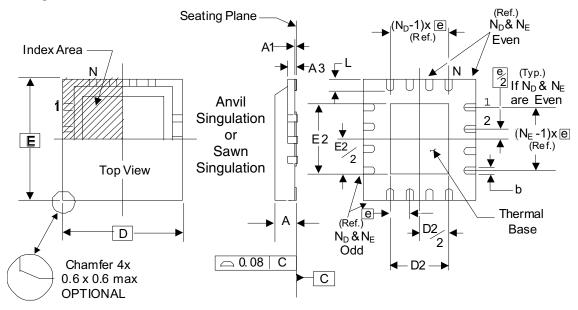
Transistor Count

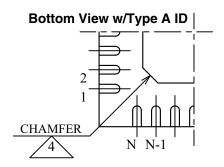
The transistor count for 8S89874 is: 489 Pin compatible with 889874

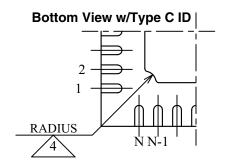


Package Outline and Package Dimensions

Package Outline - K Suffix for 16 Lead VFQFN







There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

- 1. Type A: Chamfer on the paddle (near pin 1)
- 2. Type C: Mouse bite on the paddle (near pin 1)

Table 8. Package Dimensions

JEDEC Variation: VEED-2/-4 All Dimensions in Millimeters					
Symbol	Minimum	Maximum			
N	16				
Α	0.80	1.00			
A1	0	0.05			
А3	0.25 Ref.				
b	0.18	0.30			
N _D & N _E	4				
D&E	3.00 Basic				
D2 & E2	1.00	1.80			
е	0.50 Basic				
L	0.30	0.50			

Reference Document: JEDEC Publication 95, MO-220



Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8S89874BKILF	874B	16 Lead VFQFN, Lead-Free	Tube	-40°C to 85°C
8S89874BKILFT	874B	16 Lead VFQFN, Lead-Free	Tape & Reel Pin 1 Orientation: EIA-481-C	-40°C to 85°C
8S89874BKILF/W	874B	16 Lead VFQFN, Lead-Free	Tape & Reel Pin 1 Orientation: EIA-481-D	-40°C to 85°C

Table 10. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
LFT	Quadrant 1 (EIA-481-C)	Correct Pin 1 ORIENTATION CARRIER TAPE TOPSIDE (Round Sprocket Holes) USER DIRECTION OF FEED
LF/W	Quadrant 2 (EIA-481-D)	Correct Pin 1 ORIENTATION CARRIER TAPE TOPSIDE (Round Sprocket Holes) USER DIRECTION OF FEED



Revision History Sheet

Rev	Table	Page	Description of Change	Date
В	T9 T10	18 18	Ordering information Table - added additional row. Added Pin 1 Orientation in Tape & Reel Packaging Table. Updated header/footer throughout the datasheet.	2/25/2015
В	Т9	18	Ordering Information - removed LF note below table. Updated header and footer.	2/9/16

19





Corporate Headquarters 6024 Silver Creek Valley Road San Jose, CA 95138 USA www.IDT.com Sales 1-800-345-7015 or 408-284-8200

Fax: 408-284-2775 www.IDT.com/go/sales Tech Support www.idt.com/go/support

DISCLAIMER Integrated Device Technology, Inc. (IDT) reserves the right to modify the products and/or specifications described herein at any time, without notice, at IDT's sole discretion. Performance specifications and operating parameters of the described products are determined in an independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are trademarks or registered trademarks of IDT and its subsidiaries in the United States and other countries. Other trademarks used herein are the property of IDT or their respective third party owners.

For datasheet type definitions and a glossary of common terms, visit www.idt.com/go/glossary.



OOO «ЛайфЭлектроникс" "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 P/C 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 3010181090000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



Тел: +7 (812) 336 43 04 (многоканальный) Email: org@lifeelectronics.ru