

User Guide

M.2 Development Kit (DVK-SU60-2230C)

Version 1.0

REVISION HISTORY

| Version | Date | Notes | Approver |
|---------|--------------|-----------------|-----------|
| 1.0 | 29 July 2017 | Initial Release | Jay White |

CONTENTS

| | |
|--|----|
| 1. Overview..... | 4 |
| 1.1 Introduction..... | 4 |
| 1.2 Package Contents | 4 |
| 2. M.2 Development Kit – Main Development Board..... | 4 |
| 1.3 Key Features | 5 |
| 1.4 Understanding the Development Board | 6 |
| 3. Functional Blocks..... | 7 |
| 1.5 Pin Definitions | 7 |
| 1.5.1 M.2 Key-E Socket..... | 7 |
| 1.5.2 SDIO-Pin Header | 9 |
| 1.5.3 PCIe Golden Finger | 10 |
| 1.6 Power Supply..... | 11 |
| 1.7 Tact Switch..... | 12 |
| 1.7.1 PCIE_W_DISABLE_N (SW5)..... | 13 |
| 1.7.2 PDn (SW6)..... | 13 |
| 1.7.3 PMU_EN (SW7)..... | 14 |
| 1.8 4-wire UART Serial Interface | 14 |
| 1.8.1 UART Mapping..... | 14 |
| 1.8.2 UART Interface Driven by USB..... | 14 |
| 1.8.3 UART Interface Driven by External Source | 15 |
| 1.9 32.768 KHz Oscillator..... | 15 |
| 1.10 PCM | 16 |
| 1.11 LTE Coexistence | 16 |
| 1.12 LED Indicator | 17 |
| 4. Additional Documentation | 17 |
| 5. Appendix..... | 17 |

1 OVERVIEW

The Laird M.2 development kit provides a platform for rapid wireless connectivity prototyping, providing multiple options for the development of Wi-Fi applications.

This manual is for Rev. 01 of the development PCB and relates to DVK-SU60-2230C-B0 on the PCB itself. The complete functionality of the development kit hardware requires the use of Laird 50- and 60-series firmware version **v xx.xx.xx** or greater.

Part number: **DVK-SU60-2230C**

Applicable to the following Wi-Fi module part numbers:

| | |
|------------|--|
| SU60-2230C | Dual-Band 802.11ac Wi-Fi + Bluetooth v4.2 combo module |
| M2SD50NBT | Dual-Band 802.11ac Wi-Fi + Bluetooth v4.0 combo module |
| M2US50NBT | Dual-Band 802.11ac Wi-Fi + Bluetooth v4.0 combo module |

1.1 Introduction

The Laird M.2 development kit is designed to support the rapid development of applications and software for the 50- and 60-series of Wi-Fi modules featuring Laird's innovative event driven programming language – **xxxxxx**. More information regarding this product series including a detailed module user guide are available from the 60 Series product page of the Laird website.

1.2 Package Contents

Each kit contains the following:

| | |
|----------------------|---|
| Development board | The development board has the required SU60-2230C module installed onto it and exposes all the various hardware interfaces available. |
| Power options | <ul style="list-style-type: none">USB cable – Type A to micro B. The cable also provides serial communications via the FTDI USB – RS232 converter chip on the development boardDC barrel plug with clips for connection to external power supply |
| IDC cable x? | Supplied to allow simple connection to the ? x ? way pin headers into J20, J21, and J23. The IDC cables are 2.54 mm pitch. |
| SDIO extension cable | Supplied to allow a simple connection to the SDIO socket |
| Web link card | Provides links to additional information including the 50- and 60-series user guide, schematics, quick start guides, and firmware release notes. |

2 M.2 DEVELOPMENT KIT – MAIN DEVELOPMENT BOARD

This section describes the M.2 development board hardware. The M.2 development board is delivered with the 50- and 60-series modules but no onboard firmware applications.

The M.2 development board is a universal development tool to highlight the capabilities of the 50- and 60-series modules. The development kit is supplied in a default configuration which should be suitable for multiple experimentation options. It also offers a number of pin headers that help to create different configurations for 50- and 60-series modules. This allows you to test different operating scenarios.

The development board allows the 50- and 60-series modules to physically connect to a SDIO host via the supplied SDIO extension cable for development purposes. The development board also provides USB-to-Virtual

COM port conversion through a FTDI chip – part number [FT232R](#). Any Windows PC (XP or later) and Linux PC (Ubuntu xx.xx or Fedora xx.xx) should auto-install the necessary drivers; if your PC cannot locate the drivers, you can download them from <http://www.ftdichip.com/Drivers/VCP.htm>

2.1 Key Features

The M.2 development board has the following features:

- 50- or 60-series module installed on-board
- Power supply options for powering development board from:
 - USB
 - External DC supply
 - SDIO interface
- Regulated 3.3 V for powering the 50- or 60-series modules. Optional regulated 1.8 V for powering the VCCIO for FTDI chip
- USB-to-UART bridge (FTDI chip)
- USB interface for Wifi or BT
- M.2 UART can be interfaced to:
 - USB (PC) using the USB-UART bridge
 - External UART source (using IO break-out connector when development board powered from DC jack or SDIO interface)
- Current measuring options:
 - Pin header (Ammeter)
- IO break-out (2.54 mm pitch headers) connectors interface for plugging-in external modules and accessing all interfaces of the 50- or 60-series modules [UART, LTE coexistence, PCM, GPIO].
- Three buttons and LEDs for user interaction.
- External 32 KHz oscillator for the sleep clock.

2.2 Understanding the Development Board

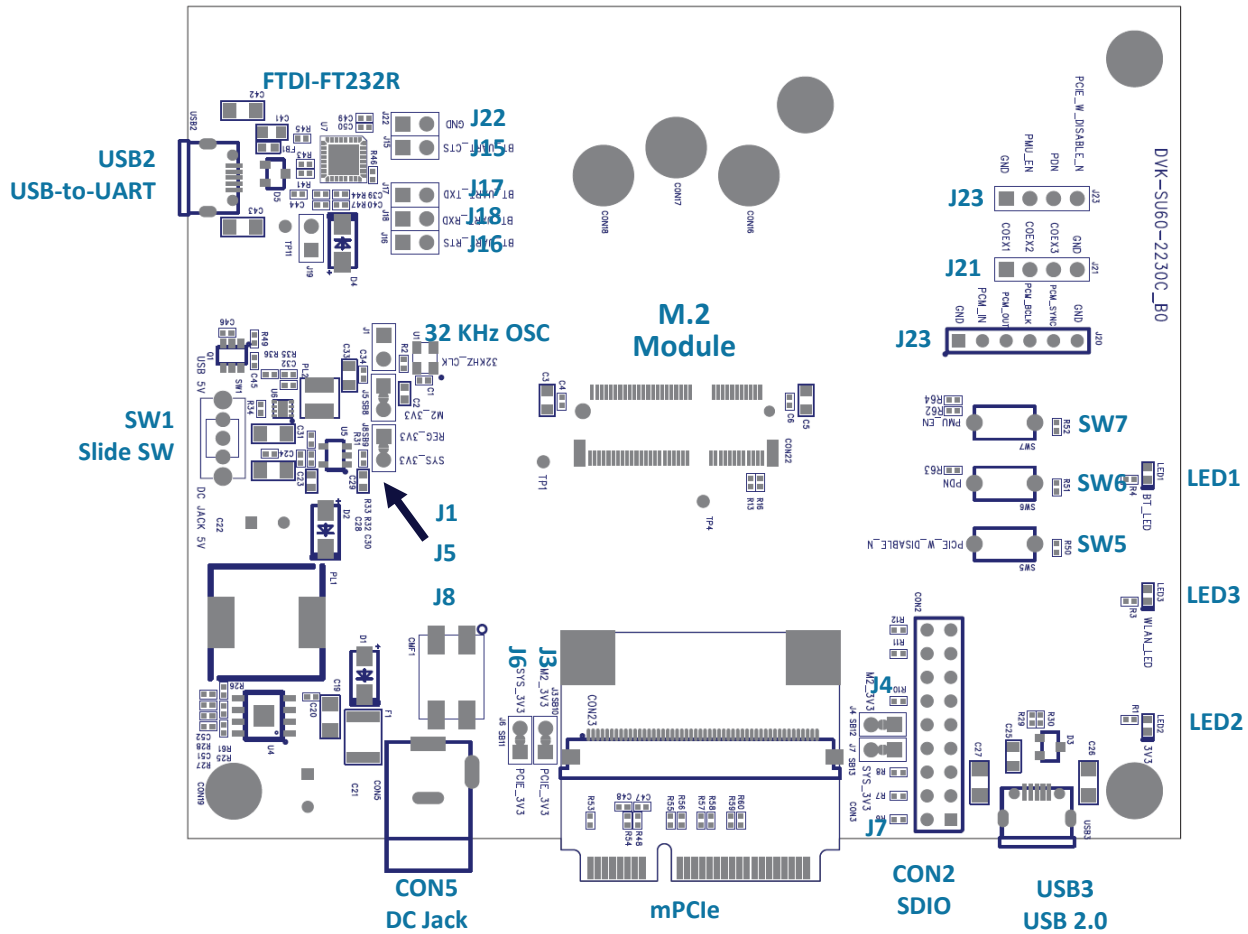


Figure 1: Development board

3 FUNCTIONAL BLOCKS

This section covers the major functional blocks that form the development board.

3.1 Pin Definitions

3.1.1 M.2 Key-E Socket

Table 1: M.2 Key-E socket pins

| Pin # | Name | Type | Voltage Ref. | Description | If Not Used |
|-------|------------------|---------|--------------|---|-------------|
| 1 | GND | - | - | Ground | GND |
| 2 | 3.3V | Power | - | 3.3V module power supply | - |
| 3 | USB_D+ | I/O | 3.3V | USB Differential Data-Positive | N/C |
| 4 | 3.3V | Power | - | 3.3V module power supply | - |
| 5 | USB_D- | I/O | 3.3V | USB Differential Data-Negative | N/C |
| 6 | LED1# | O, PU | 3.3V | LED indicator for WLAN with 10mA drive capability | N/C |
| 7 | GND | - | - | Ground | GND |
| 8 | PCM_CLK | I/O | 1.8V | PCM Clock Signal (Optional) Optimal clock used for some codecs. Output if Master mode; Input if Slave mode. | N/C |
| 9 | SDIO CLK | I, PU | 1.8V | SDIO 4-bit Mode Clock Input | N/C |
| 10 | PCM_SYNC | I/O | 1.8V | PCM Sync Pulse Signal Output if Master mode; Input if Slave mode. | N/C |
| 11 | SDIO CMD | I/O | 1.8V | SDIO 4-bit Mode Command/Response | N/C |
| 12 | PCM_IN | I | 1.8V | PCM Data | N/C |
| 13 | SDIO DATA0 | I/O, PU | 1.8V | SDIO 4-bit Mode DATA line Bit[0] | N/C |
| 14 | PCM_OUT | O | 1.8V | PCM Data | N/C |
| 15 | SDIO DATA1 | I/O, PU | 1.8V | SDIO 4-bit Mode DATA line Bit[1] | N/C |
| 16 | LED2# | O, PU | 3.3V | LED indicator for BT with 10mA drive capability. | N/C |
| 17 | SDIO DATA2 | I/O, PU | 1.8V | SDIO 4-bit Mode DATA line Bit[2] | N/C |
| 18 | GND | - | - | Ground | GND |
| 19 | SDIO DATA3 | I/O, PU | 1.8V | SDIO 4-bit Mode DATA line Bit[3] | N/C |
| 20 | UART WAKE# | N/C | N/C | N/C | N/C |
| 21 | SDIO WAKE# | N/C | N/C | N/C | N/C |
| 22 | UART TXD | O | 1.8V | UART Serial Data Output | N/C |
| 23 | SDIO RESET# | N/C | N/C | N/C | N/C |
| 32 | UART RXD | I | 1.8V | UART Serial Data Input | N/C |
| 33 | GND | - | - | Ground | GND |
| 34 | UART RTS | O, WPU | 1.8V | UART Request-to-Send (Active low) | N/C |
| 35 | PERp0 | I | 1.8V | PCIe Receive Data-Positive | N/C |
| 36 | UART CTS | I, PU | 1.8V | UART Clear-to-Send (Active low) | N/C |
| 37 | PERn0 | I | 1.8V | PCIe Receive Data-Negative | N/C |
| 38 | VENDOR DEFINED38 | N/C | N/C | N/C | N/C |

| Pin # | Name | Type | Voltage Ref. | Description | If Not Used |
|-------|------------------------------|-------|--------------|---|-------------|
| 39 | GND | - | - | Ground | GND |
| 40 | VENDOR DEFINED40 | N/C | N/C | N/C | N/C |
| 41 | PETp0 | O | 1.8V | PCIe Transmit Data-Positive | N/C |
| 42 | VENDOR DEFINED42 | N/C | N/C | N/C | N/C |
| 43 | PETn0 | O | 1.8V | PCIe Transmit Data-Negative | N/C |
| 44 | COEX3 | I/O | 1.8V | General purpose I/O pin. | N/C |
| 45 | GND | - | - | Ground | GND |
| 46 | COEX2 | O, PD | 1.8V | Serial data to external LTE device/ | N/C |
| 47 | REFCLKp0 | I | 1.8V | PCIe Differential Clock Input-Positive | N/C |
| 48 | COEX1 | I, PD | 1.8V | Serial data from external LTE device/ | N/C |
| 49 | REFCLKn0 | I | 1.8V | PCIe Differential Clock Input-Negative | N/C |
| 50 | SUSCLK(32KHz) | I, PU | 3.3V | Sleep Clock Input An external sleep clock of 32.768KHz with minimum +/-250ppm is required for power saving mode | - |
| 51 | GND | - | - | Ground | GND |
| 52 | PERST0# | I, PD | 3.3V | PCIe host indication to reset the device (input) (active low) | N/C |
| 53 | CLKREQ0# | I/O | 3.3V | PCIe clock request (input/output) (active low) | GND |
| 54 | W_DISABLE2# | I | 3.3V | Enable input for all Regulators inside the sU60-SIPT. Note: DO NOT float this pin. Pull-up to 3.3V with 100K for normal operation. | 100K, PU |
| 55 | PEWAKE0# | I/O | 3.3V | PCIe wake signal (input/output) (active low) | N/C |
| 56 | W_DISABLE1# (O)(0/3.3V) | I, PU | 3.3V | PCIe host indication to disable the WLAN function of the device (input) (active low) | N/C |
| 57 | GND | - | - | Ground | GND |
| 58 | I2C DATA (I/O) (0/3.3V) | N/C | N/C | N/C | N/C |
| 59 | RESERVED/PETp1 | N/C | N/C | N/C | N/C |
| 60 | I2C CLK (O)(0/3.3V) | N/C | N/C | N/C | N/C |
| 61 | RESERVED/PETn1 | N/C | N/C | N/C | N/C |
| 62 | ALERT# (I)(0/3.3V) | N/C | N/C | N/C | N/C |
| 63 | GND | - | - | Ground | GND |
| 64 | RESERVED | N/C | N/C | N/C | N/C |
| 65 | RESERVED/PERp1 | N/C | N/C | N/C | N/C |
| 66 | UIM_SWP/PERST1# | N/C | N/C | N/C | N/C |
| 67 | RESERVED/PERn1 | N/C | N/C | N/C | N/C |
| 68 | UIM_POWER_SNK/CLKREQ1# | N/C | N/C | N/C | N/C |
| 69 | GND | - | - | Ground | GND |
| 70 | UIM_POWER_SRC/GPIO1/PEWAKE1# | N/C | N/C | N/C | N/C |

| Pin # | Name | Type | Voltage Ref. | Description | If Not Used |
|-------|-------------------|-------|--------------|--------------------------|-------------|
| 71 | RESERVED/REFCLKp1 | N/C | N/C | N/C | N/C |
| 72 | 3.3V | Power | - | 3.3V module power supply | - |
| 73 | RESERVED/REFCLKn1 | N/C | N/C | N/C | N/C |
| 74 | 3.3V | Power | - | 3.3V module power supply | - |
| 75 | GND | - | - | Ground | GND |
| 76 | GND | - | - | Ground | GND |
| 77 | GND | - | - | Ground | GND |

3.1.2 SDIO-Pin Header

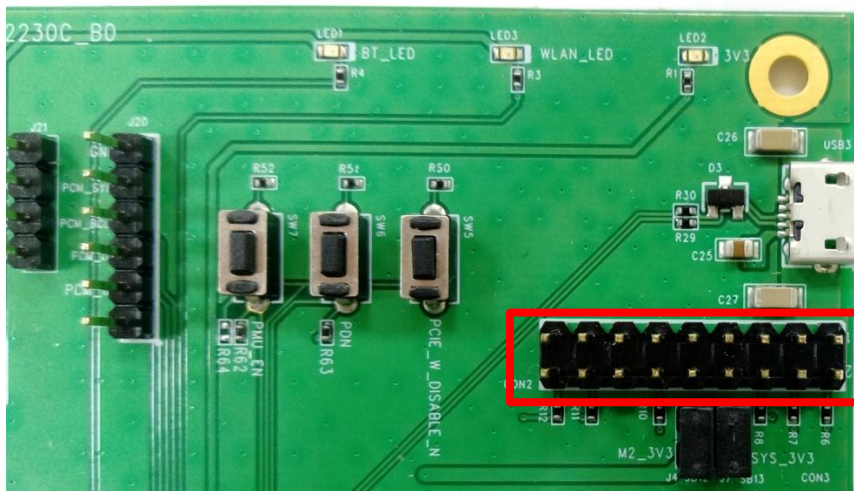


Figure 2: DVK-SU60-2230C SDIO Pin Header

Table 2: SDIO pin header

| Pin # | Name | Type | Voltage Ref. | Description | If Not Used |
|-------|------------|---------|--------------|----------------------------------|-------------|
| 1 | GND | - | - | Ground | GND |
| 2 | SDIO DATA2 | I/O, PU | 1.8V | SDIO 4-bit Mode DATA line Bit[2] | N/C |
| 3 | GND | - | - | Ground | GND |
| 4 | SDIO DATA3 | I/O, PU | 1.8V | SDIO 4-bit Mode DATA line Bit[3] | N/C |
| 5 | GND | - | - | Ground | GND |
| 6 | SDIO CMD | I/O | 1.8V | SDIO 4-bit Mode Command/Response | N/C |
| 7 | GND | - | - | Ground | GND |
| 8 | GND | - | - | Ground | GND |
| 9 | SDIO_3V3 | Power | - | 3.3V module power supply | - |
| 10 | SDIO_3V3 | Power | - | 3.3V module power supply | - |
| 11 | GND | - | - | Ground | GND |
| 12 | SDIO CLK | I, PU | 1.8V | SDIO 4-bit Mode Clock Input | N/C |
| 13 | GND | - | - | Ground | GND |
| 14 | GND | - | - | Ground | GND |

| Pin # | Name | Type | Voltage Ref. | Description | If Not Used |
|-------|------------|---------|--------------|----------------------------------|-------------|
| 15 | GND | - | - | Ground | GND |
| 16 | SDIO DATA0 | I/O, PU | 1.8V | SDIO 4-bit Mode DATA line Bit[0] | N/C |
| 17 | GND | - | - | Ground | GND |
| 18 | SDIO DATA1 | I/O, PU | 1.8V | SDIO 4-bit Mode DATA line Bit[1] | N/C |

3.1.3 PCIe Golden Finger

Table 3: PCIe golden finger pins

| Pin # | Name | Type | Voltage Ref. | Description | If Not Used |
|-------|-------------|-------|--------------|--|-------------|
| 1 | PEWAKE0# | I/O | 3.3V | PCIe wake signal (input/output) (active low) | N/C |
| 2 | PCIE_3V3 | Power | - | 3.3V module power supply | - |
| 3 | - | - | - | - | - |
| 4 | GND | - | - | Ground | GND |
| 5 | - | - | - | - | - |
| 6 | - | - | - | - | - |
| 7 | CLKREQ0# | I/O | 3.3V | PCIe clock request (input/output) (active low) | GND |
| 8 | - | - | - | - | - |
| 9 | GND | - | - | Ground | GND |
| 10 | - | - | - | - | - |
| 11 | REFCLKn0 | I | 1.8V | PCIe Differential Clock input-Negative | N/C |
| 12 | - | - | - | - | - |
| 13 | REFCLKp0 | I | 1.8V | PCIe Differential Clock input-Positive | N/C |
| 14 | - | - | - | - | - |
| 15 | GND | - | - | Ground | GND |
| 16 | - | - | - | - | - |
| 17 | - | - | - | - | - |
| 18 | GND | - | - | Ground | GND |
| 19 | - | - | - | - | - |
| 20 | W_DISABLE1# | I, PU | 3.3V | PCIe host indication to disable the WLAN function of the device (input) (active low) | N/C |
| 21 | GND | - | - | Ground | GND |
| 22 | PERST0# | I, PD | 3.3V | PCIe host indication to reset the device (input) (active low) | N/C |
| 23 | PETn0 | O | 1.8V | PCIe Transmit Data-Negative | N/C |
| 24 | PCIE_3V3 | Power | - | 3.3V module power supply | - |
| 25 | PETp0 | O | 1.8V | PCIe Transmit Data-Positive | N/C |
| 26 | GND | - | - | Ground | GND |
| 27 | GND | - | - | Ground | GND |
| 28 | - | - | - | - | - |
| 29 | GND | - | - | Ground | GND |

| Pin # | Name | Type | Voltage Ref. | Description | If Not Used |
|-------|----------|-------|--------------|---|-------------|
| 30 | - | - | - | - | - |
| 31 | PERn0 | I | 1.8V | PCIe Receive Data-Negative | N/C |
| 32 | - | - | - | - | - |
| 33 | PERp0 | I | 1.8V | PCIe Receive Data-Positive | N/C |
| 34 | GND | - | - | Ground | GND |
| 35 | GND | - | - | Ground | GND |
| 36 | USB_D- | I/O | 3.3V | USB Differential Data-Negative | N/C |
| 37 | GND | - | - | Ground | GND |
| 38 | USB_D+ | I/O | 3.3V | USB Differential Data-Positive | N/C |
| 39 | PCIE_3V3 | Power | - | 3.3V module power supply | - |
| 40 | GND | - | - | Ground | GND |
| 41 | PCIE_3V3 | Power | - | 3.3V module power supply | - |
| 42 | - | - | - | - | - |
| 43 | GND | - | - | Ground | GND |
| 44 | LED1# | O, PU | 3.3V | LED indicator for WLAN with 10mA drive capability | N/C |
| 45 | - | - | - | - | - |
| 46 | LED2# | O, PU | 3.3V | LED indicator for BT with 10mA drive capability. | N/C |
| 47 | - | - | - | - | - |
| 48 | - | - | - | - | - |
| 49 | - | - | - | - | - |
| 50 | GND | - | - | Ground | GND |
| 51 | - | - | - | - | - |
| 52 | PCIE_3V3 | Power | - | 3.3V module power supply | - |

3.2 Power Supply

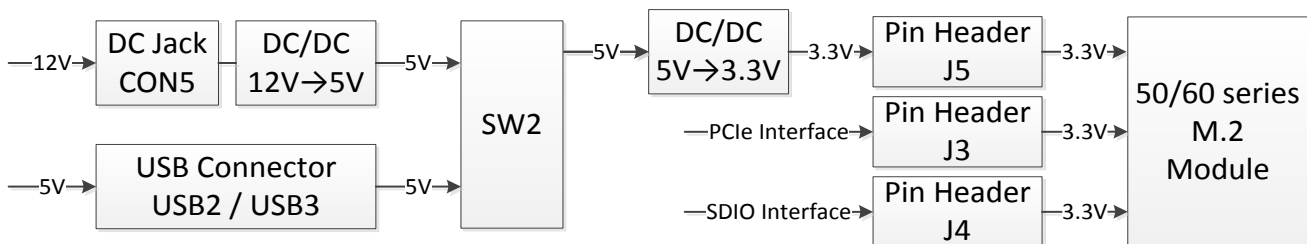


Figure 3: DVK-SU60-2230C power supply

The development board can be powered from a DC 12-volt supply (into DC jack connector CON5), USB (type micro-B connector, USB2/USB3) or the host interface (PCIe or SDIO interface). The power source fed into DC jack is regulated down to 5 volts with an on-board regulator and wire to SW2.

The 5 volts from the USB or the DC jack is regulated down to 3.3 volts with an on-board regulator on the development board. Switch SW2 selects between the regulated 5 volt and USB. The voltage from host interface (PCIe or SDIO interface) is not regulated but is fed directly to M.2 module supply pin.

Default position of SW2 is to select regulated 5 volts.

The development board has a 1.8-volt regulator for the VCCIO of FTDI-Chip.

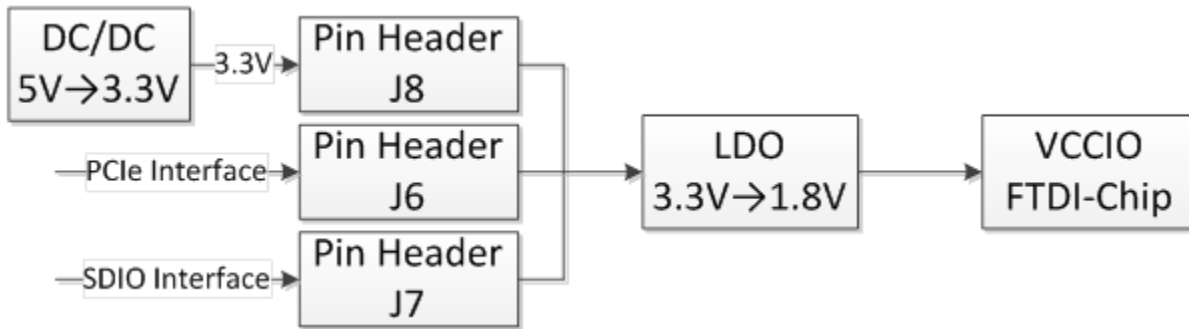


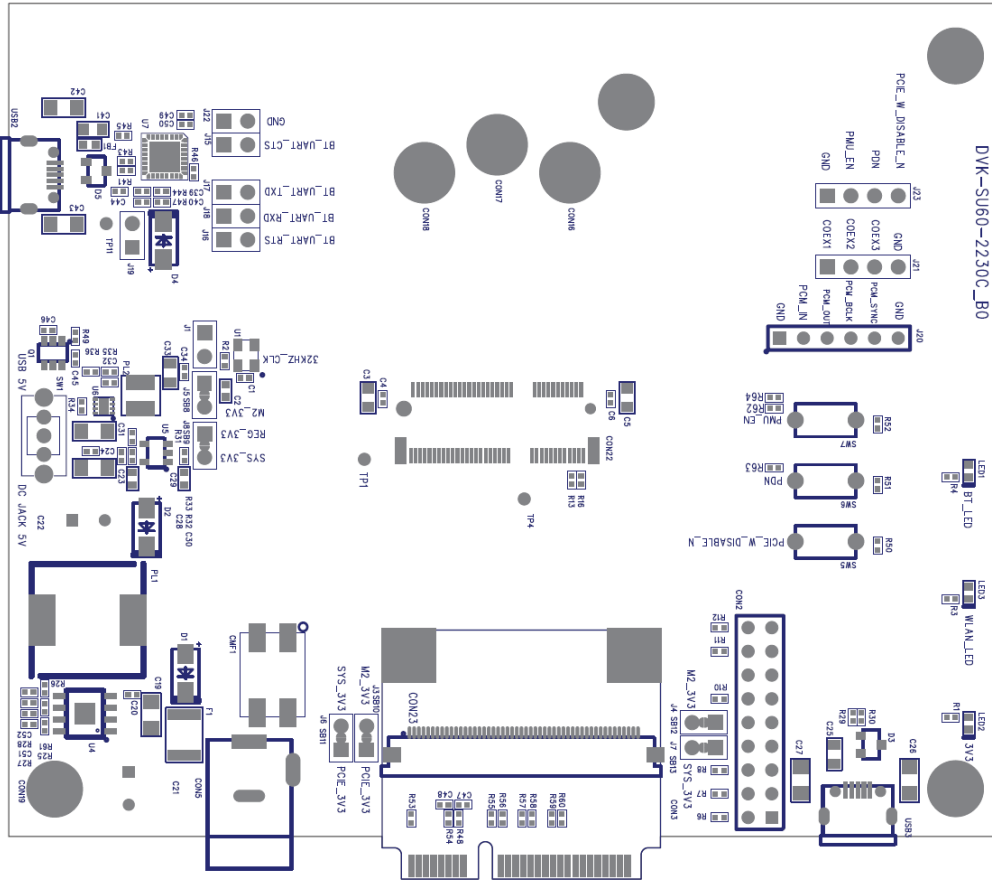
Figure 4: DVK-SU60-2230C power supply for VCCIO of FTDI chip

On the development board, the power domain:

- M2_3V3 supplies the M.2 module only.
- The header connectors (J3, J4, J5) can be used to measure the current of power domain M2_3V3.
- REG_1V8 supplies the FTDI chip IO only.

3.3 Tact Switch

3.3.1 The development board have three tact switches (SW5, SW6, SW7) for optional. To view its location, refer to Figure 1.



PCIE_W_DISABLE_N (SW5)

PCIe host indication to disable the WLAN function of the device (Input) (Active Low)



Figure 5: DVK-SU60-2230C 1.8V power supply

0 – Disable the WLAN

1 – Normal mode

- PCIE_W_DISABLE_N can accept an input of 3.3 volts.
- PCIE_W_DISABLE_N may be driven by the host
- PCIE_W_DISABLE_N must be high for normal operation

An internal pull-up resistor on this pin.

3.3.2 PDn (SW6)

Full Power-Down (Input) (Active Low)

0 – Full power-down mode

1 – Normal mode

- PDn can accept an input of 1.8 volts
- PDn may be driven by the host

- PDn must be high for normal operation

An internal pull-up resistor on this pin.

3.3.3 PMU_EN (SW7)

Enable input for internal PMU (Input) (Active Low).

0 – Disable the input for internal PMU.

1 – Normal mode

- PMU_EN can accept an input of 3.3 volts
- PMU_EN may be driven by the host
- PMU_EN must be high for normal operation

An internal pull-up resistor on this pin.

Note: PCIE_W_DISABLE_N, PDn and PMU_EN were also wired to J23 for optional.

To view its location, refer to [Figure 1](#).

3.4 4-wire UART Serial Interface

The development board provides access to the M.2 module 4-wire UART interface (TX, RX, CTS, RTS) either through USB (via U7 FTDI USB-UART convertor chip) or through a breakout header connector J15, J16, J17 and J18. Refer to [Figure 6](#).

Note: M.2 module provides 4-wire UART interface on the HW.

V_{IH} is from 1.26V to 2.2V; V_{IL} is from -0.4V to 0.54V.

3.4.1 UART Mapping

UART connection on the 50 and 60 series modules and FTDI IC are shown in table below. Refer to [Figure 6](#) to see how the 50 and 60 series module UART is mapped to the breakout header connector (J15, J16, J17 and J18).

Table 4: UART mapping

| M.2 Default Function | FTDI IC UART |
|----------------------|--------------|
| BT_UART_RXD (output) | RXD |
| BT_UART_TXD (input) | TXD |
| BT_UART_CTS (output) | CTS |
| BT_UART_RTS (input) | RTS |

3.4.2 UART Interface Driven by USB

- **USB Connector** – The development kit provides a USB Type micro-B connector (USB2) which allows connection to any USB host device. The connector optionally supplies power to the development kit and the USB signals are connected to a USB to serial convertor device (FT232R).
- **USB-UART** – The development kit is fitted with a (U7) FTDI FT232R USB to UART converter which provides USB-to-Virtual COM port on any Windows PC (XP or later). Upon connection, Windows auto-installs the

required drivers. For more details and driver downloads, visit <http://www.ftdichip.com/Products/FT232R.htm>.

- **UART interface driven by USB FTDI chip** – In normal operation, the M.2 UART interface is driven by the FTDI FT232R USB to UART converter.

3.4.3 UART Interface Driven by External Source

- **UART interface driven by external UART source** – The M.2 module UART interface (TX, RX, CTS, RTS) is presented at a 2.54 mm (0.1 in.) pitch headers (J15, J16, J17 and J18). To allow the M.2 UART interface to be driven from the breakout header connector (J15, J16, J17 and J18):
 - Development board must be powered from DC jack (CON5) and switch SW1 is in position *DC JACK 5V*.

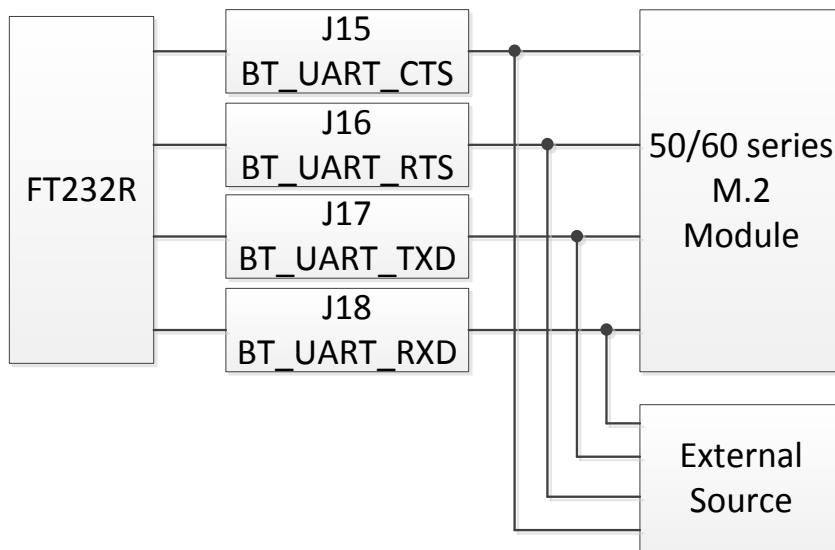


Figure 6: USB to UART Interface and Header to UART interface

3.5 32.768 KHz Oscillator

The development kit is fitted with a (U1) 32.768 KHz oscillator which provides sleep clock to M.2 module. Fit a jumper on J1 to disable the sleep clock, if needed.



Figure 7: Pin header J1

3.6 PCM

The development kit provides the PCM signal on J20.

The pin descriptions of J20 for PCM signal are shown in below table.

Table 5: PCM pins

| J20 | Description |
|-------|-------------|
| Pin 1 | GND |
| Pin 2 | PCM_IN |
| Pin 3 | PCM_OUT |
| Pin 4 | PCM_BCLK |
| Pin 5 | PCM_SYNC |
| Pin 6 | GNDGND |

Note: V_{IH} is from 1.26V to 2.2V; V_{IL} is from -0.4V to 0.54V.

3.7 LTE Coexistence

The development kit provides the LTE coexistence signal on J21.

The pin descriptions of J21 for LTE coexistence signal are shown in below table.

Table 6: LTE coexistence pins

| J21 | Description |
|-------|-------------|
| Pin 1 | COEX1 |
| Pin 2 | COEX2 |
| Pin 3 | COEX3 |
| Pin 4 | GND |

Note: V_{IH} is from 1.26V to 2.2V; V_{IL} is from -0.4V to 0.54V.

3.8 LED Indicator

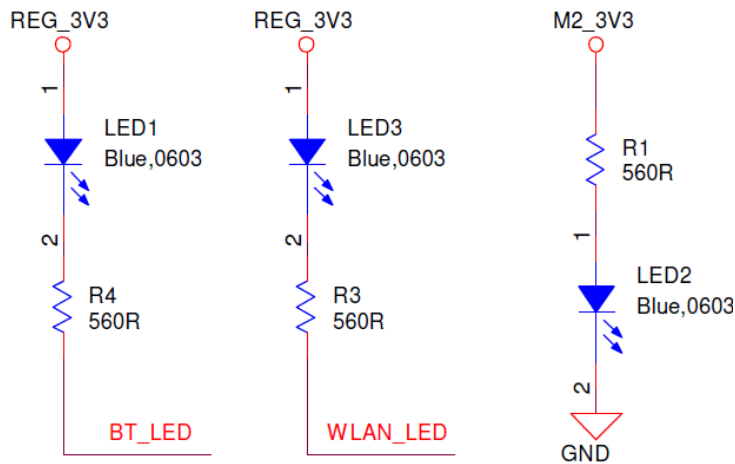


Figure 8: LED indicator

Table 7: LED descriptions

| LEDs | Description |
|------|--------------------------|
| LED1 | BT status (Active Low) |
| LED2 | 3.3V module power |
| LED3 | WLAN status (Active Low) |

4 ADDITIONAL DOCUMENTATION

Laird offers a variety of documentation and ancillary information to support our customers through the initial evaluation process and ultimately into mass production. Additional documentation includes:

- DVK-SU60-2230C – User Manual
- DVK-SU60-2230C - Schematics
- 50 and 60 series M.2 Module – User Manual – Hardware Datasheet and Integration Guide

For any additional questions or queries, or to receive local technical support for this Development Kit or for the 50 and 60 series modules, please contact wirelessinfo@lairdtech.com

5 APPENDIX

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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