Power Loss Protection with 6A eFuse

FEATURES

- **Optimized for Low Voltage Applications**
- **2.6-to-7V Operating Input Range**
- **8V Max Input Blocking Voltage**
- **Adjustable In-rush Current Control**
- **Configurable Input Power Failure Level**
- **Programmable up to 6A Input Current Limit**
- **Programmable 5V to 28V Boost Storage Voltage**
- **28V@4A Synchronous Buck Supports 100% Duty Cycle**
- **Programmable up to 2.25MHz Buck Operating Frequency for Small Inductor Size**
- **Power Loss, Vout Power Good, and Storage Cap Power Good Indicators**
- **Compatible with Different Types of Storage Caps: Super Caps, Electrolytic, Tantalum, POSCAP etc.**
- **Autonomous Health Monitoring for Detection of Earlier Storage Capacitor Failures**
- **Configurable Interrupts to Inform Host for any Faults/Status Change**
- **eFuse, Boost, and Buck UV/OV/OC Protection**
- **Thermal Alert and Protection**
- **Thermal Enhanced FCQFN 4x4-32 package**

APPLICATIONS

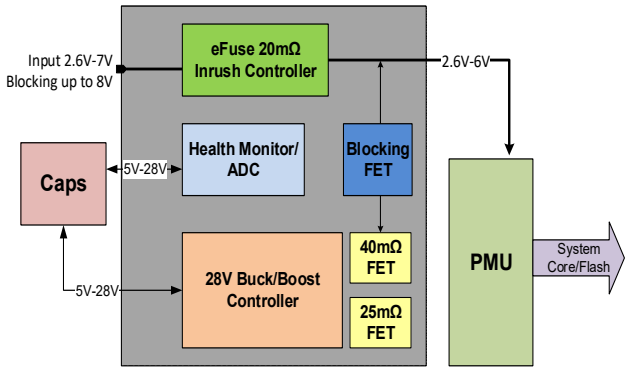
- Solid State Drives
- Power Backup Systems
- Industrial Applications
- eFuse
- Hot Plug Devices

GENERAL DESCRIPTION

The ACT4921 device is a highly integrated power loss protection IC. It provides backup storage power in the event of an input power failure. A built-in boost converter provides high voltage energy storage to minimize storage capacitor size requirements. The built-in buck converter regulates the storage voltage to a fixed output voltage. It contains internal, back-to-back eFuse FETs to provide bi-directional input to output isolation. The IC also provides hot swap and inrush current control.

The ACT4921 is very flexible and can easily be configured with I^{2}C and external components. It features programmable storage capacitor voltage to optimize the storage capacitor sizing and system run time. The internal health monitoring provide an extra layer of protection and improve system reliability and early capacitor failure notification. It automatically checks the storage capacitor health and notifies the user when the energy in the storage caps is not sufficient for backup power. The built-in synchronous buck converter maximizes energy transfer from the storage caps to the system.

ACT4921 provides an I^{2}C bus interface to allow MCU control and monitoring. There are supervisor monitors for the input voltage, output voltage, and storage voltage. It is available with the thermal enhanced QFN 4x4 32 pin package.



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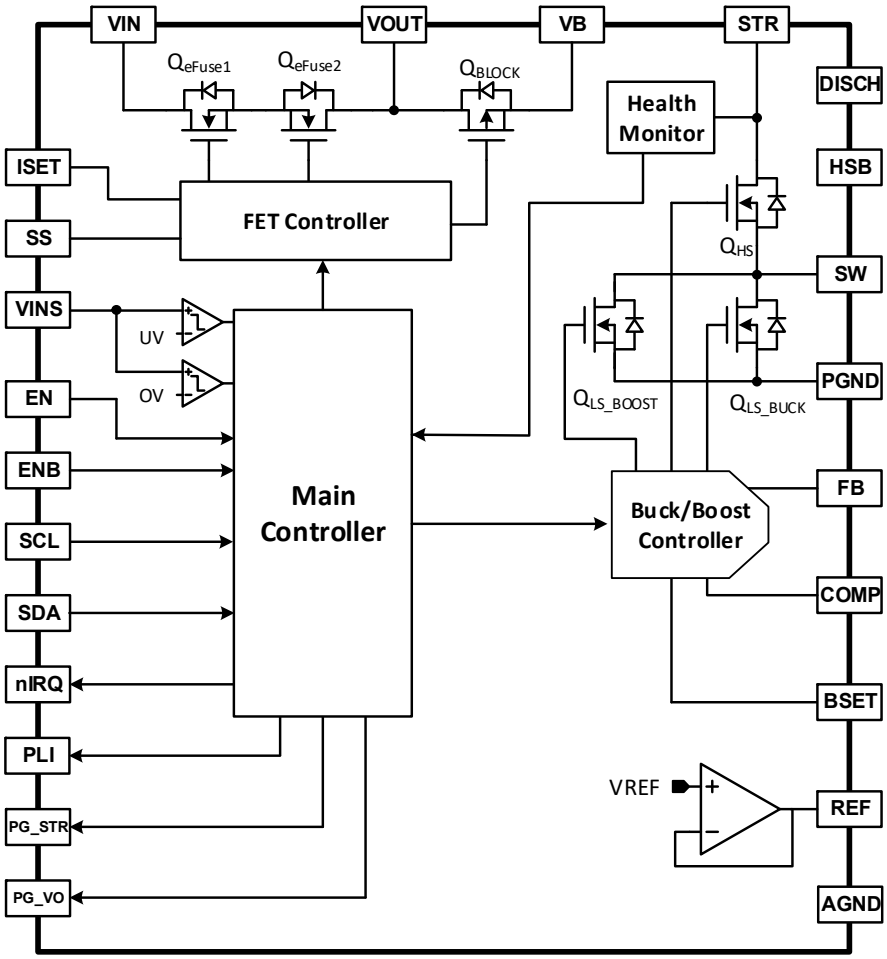
FUNCTIONAL BLOCK DIAGRAM



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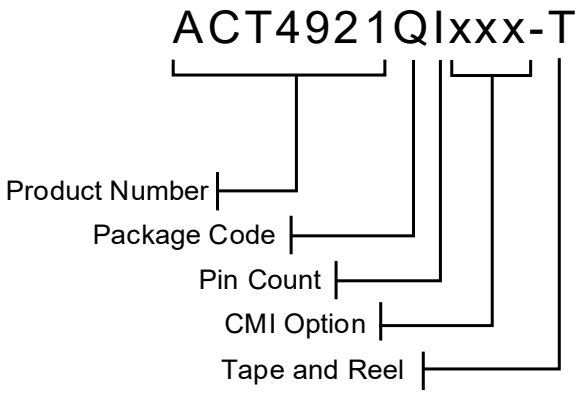
ORDERING INFORMATION

PART NUMBER	Input Voltage	Storage Voltage	Fsw	BST_CLIM	Buck Current Limit	PACKAGE
ACT4921QI301-T	3.3V	28V	1.125MHz	950mA	6A	FCQFN4x4-32



Note 1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.

Note 2: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

Note 3: Package Code designator “Q” represents QFN

Note 4: Pin Count designator “I” represents 32 pins

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PIN CONFIGURATION

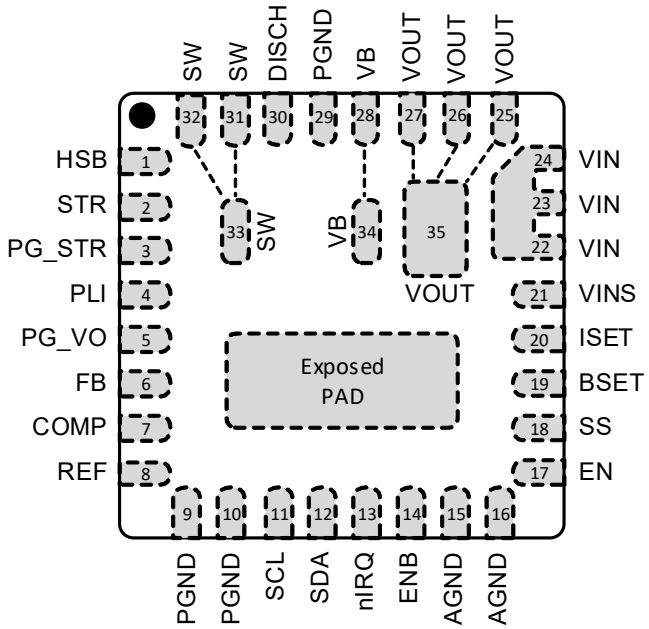

Figure 1: Pin Configuration – Top View – QFN4x4-32

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PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	HSB	High Side Bias, Boot-strap pin. This provides power to the internal high-side MOSFET gate driver circuitry. Connect a 47nF capacitor from HSB pin to SW pin
2	STR	Storage Capacitor Input. Connect the storage capacitors to STR. STR requires a minimum capacitor of 100µF to PGND.
3	PG_STR	Power Good Indicator Open-Drain Output for storage capacitor. Storage capacitor voltage is good when high, and pulls low when the storage voltage falls below 95% of the nominal voltage setting or when Buck and Boost circuits are disabled. This pin is referenced to AGND
4	PLI	Power Loss Indicator Open-Drain Output for VIN. PLI goes high when the eFuse is turned on and goes low when the IC enters supplement mode. PLI is referenced to AGND.
5	PG_VO	Power Good indicator Open-Drain for Vout. PG_VO goes high when the eFuse is fully turned on, and pulls low when the FB voltage falls below 95% of V_{FB_REF} in supplement mode. PG_VO is referenced to AGND
6	FB	Output Voltage Feedback. Kelvin connect FB to the output capacitor.
7	COMP	Compensation input pin for the buck converter.
8	REF	Internal Bias Voltage Output. Connect a 1µF capacitor between REF and AGND.
9,10,29	PGND	Power Ground. Connect to large ground plane on PCB
11	SCL	I^2C Clock Input. Needs an external pull up resistor.
12	SDA	I^2C Data Input and Output. Needs an external pull up resistor.
13	nIRQ	Interrupt Open-Drain Output. nIRQ goes low to indicate a fault condition. nIRQ is referenced to AGND.
14	ENB	Boost circuit & blocking FET enable signal. Pulled high internally. When it is pulled to AGND, Boost and Buck circuit is disabled, and blocking FET is OFF.
15,16	AGND	Analog Ground. Kelvin connect AGND to the PGND plane.
17	EN	Enable Input. This is a digital enable signal for the IC. Pulled high internally. When high, the eFuse turn on. When it is pulled to AGND, eFuse turns off, the IC goes into supplement mode, and stays in HIZ mode after supplement mode ends.
18	SS	Soft Start Input. Place a capacitor from SS to VSS to control the eFuse startup voltage slew rate.
19	BSET	Sets the storage capacitor's boosted output voltage. Place a resistor from BSET to AGND to set the desired voltage.
20	ISET	Input Current Limit pin. Connect a resistor from ISET to AGND to set the current limit. ISET can also be monitored to measure the eFuse current.
21	VINS	Input Voltage Sense for Under Voltage and Over Voltage faults. A dual comparator on VINS measures the input voltage to determine if it is under, voltage, over voltage, or within normal operating limits. Connect a resistive voltage divider to VINS to set the UV and OV limits. The UV threshold is 0.64V. The OV threshold is set by the IC's specific CMI. VINS is referenced to AGND
22,23,24	VIN	Power Supply Input. Input to the eFuse. Connect a 0.1µF capacitor between VIN and PGND as close to the IC as possible.
25,26,27,35	VOUT	Output for by-pass mode, in-rush, and eFuse functionality. Connect VOUT to the system load.
28,34	VB	Buck circuit output and Boost circuit input pin. It is isolated from VOUT with the internal blocking FET. Place the inductor between VB and SW.

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30	DISCH	Storage Cap Discharge pin. Connect a resistor between DISCHG and STR to quickly discharge the storage caps whenever device enters the POR/UV state or when user forces STR to discharge by setting the DISCHG_STR[ ] bit.
31,32,33	SW	Switching Pin. This is the boost converter switch node and the buck converter switch node. Connect the inductor to SW.
Exposed Pad	PGND	Power Ground. Connect to large ground plane on PCB with thermal vias.

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE	UNIT
FB, SS, ISET, REF, SDA, SCL, EN, BSET, nIRQ, VINS, PLI, PG_STR, PG_VO, ENB to AGND.	-0.3 to 6	V
VIN to AGND	-0.3 to 8	V
VOUT to PGND	-0.3 to 6	V
HSB to SW	-0.3 to 6	V
SW to PGND	-0.3 to STR+1	V
STR, DISCHG to PGND	-0.3 to 30	V
AGND to PGND	-0.3 to + 0.3	V
DISCHG	500	mA
ESD Rating (human body model), all pins	2	kV
Junction to Ambient Thermal Resistance, dependent on board layout (note 1)	27	°C /W
Operating Ambient Temperature Range (T_A)	-40 to 105	°C
Operating Junction Temperature (TJ), (note 2)	-40 to 125	°C
Storage Temperature	-40 to 150	°C
Lead Temperature (Soldering 10s)	300	°C

Note1: Measured on Active-Semi Evaluation Kit

Note2: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

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SYSTEM CHARACTERISTICS

(VIN = 5V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply					
Input Supply Voltage Range	VIN	2.6		7	V
Input Supply Over Voltage Lock Out (OVLO)			6		V
Input Under Voltage Lock Out (UVLO)	VIN Rising (Boost/eFuse Enabled)		2.55	2.6	V
Input UVLO Hysteresis	VIN Falling		50		mV
Input Operation Current	eFuse Enabled and Soft start completed Buck/Storage Regulator Disabled Storage Health Check Disabled			3	mA
	eFuse Enabled and Soft start completed Buck/Storage Regulator Disabled Storage Health Check Disabled			5.5	mA
Input Current (Shutdown)	V_{EN} = 0V		20		µA
Input Under Voltage Lock Out (UVLO)	VIN Rising (Boost/eFuse Enabled)		2.55	2.6	V
Input Current (Shutdown)	V_{EN}=0V		20		µA
Thermal					
Thermal Warning	Sets nIRQ		120		°C
Thermal Shutdown – Disables buck and boost			145		°C
Thermal Shutdown – Disables eFuse			155		°C
Thermal Comparators Hysteresis			10		°C
SET Thresholds					
BSET Reference	Normal operation range, otherwise uses default Boost output regulation setting	0.32		1.2	V
BSET Current Source	BSET = 1.0V (25°C)	19.6	20	20.4	µA
BSET Current Source Temperature Coefficient	BSET = 1.0V (25°C – 125°C)		0.0145		%/°C
STR Thresholds					
Input Under Voltage Lock Out (STR_UVLO)	STR Falling	2.7	2.78		V
Input Under Voltage Lock Out (STR_UVLO)	STR Rising		3.08		V
Open Drain Outputs					
Open Drain Resistance (nIRQ, PLI, PG_VO, PG_STR, SDA)	Sinking Current 500µA			100	Ω
VINS Thresholds					
Under Voltage Reference (VINS_UV_REF)	UV REF after POR release		0.64		V

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Programmable Overvoltage Reference Range (INS_OV_REF)	OV REF after POR release	0.82		1.32	V
Validation Detection	VINS UV Falling or OV Falling (Delay disabled) <Analog delay at pin>		10		µs
Validation Detection	VINS UV Falling or OV Falling (Delay disabled) <Digital delay>		125		ms
Validation Detection	VINS UV Rising or OV Rising		40		ns
Hysteresis for Reference			20		mV

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INTERNAL BUCK REGULATOR

(VIN = 5V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Input Voltage Range		3		28	V
Typical Output Voltage			3.3		V
Programmable Output Voltage Range	Using external resistor divider	1.8		6	V
Standby Supply Current	V_{OUT} = 103%, Regulator Enabled, No Load, not switching	300	450	600	µA
Feedback Voltage			0.8		V
Output Voltage Accuracy	V_{OUT} = 3.3V, I_{OUT} = 2A (continuous PWM mode)	-1%	V_{NOM}	1%	V
Output Voltage Accuracy	V_{OUT} = 3.3V, I_{OUT} = 1mA (PFM mode) Average Ripple Voltage	-1%	V_{NOM}	1%	V
Line Regulation	V_{OUT} = 3.3V V_{IN_B1} = 5.5V to 12V, PWM Regulation		0.02		%/V
Load Regulation	V_{OUT} = 3.3V PWM Regulation		0.04		%/A
Undervoltage Threshold	V_{OUT} Falling BUCK_UV_TH = 00 BUCK_UV_TH = 01 BUCK_UV_TH = 10 BUCK_UV_TH = 11		 60 70 80 90		$\%V_{NOM}$
Power Good Threshold (PG_VO)	V_{OUT} Falling		95		$\%V_{NOM}$
Power Good Hysteresis (PG_VO)	V_{OUT} Rising		2		$\%V_{NOM}$
Overvoltage Fault Threshold	V_{OUT} Rising	107	110	112.5	$\%V_{NOM}$
Overvoltage Fault Hysteresis	V_{OUT} Falling		3		$\%V_{NOM}$
Programmable Switching Frequency Range	V_{OUT} > 20% V_{NOM}		562		kHz
			1125		
			1500		
			2250		
Current Limit, Cycle-by-Cycle Settings	BKILIM_OPT = 0 BKILIM_OPT = 1		3 6		A
Current Limit, Cycle-by-Cycle Tolerance	At default BKILIM_OPT	-10		+10	%
	At other BKILIM_OPT set point	-15		+15	%
Current Limit, Shutdown	Above BKILIM_OPT threhsold		40		%
High Side On-Resistance	I_{SW} = -3A, V_{STR} = 5V		46		mΩ
Low Side On-Resistance	I_{SW} = 3A, V_{STR} = 5V		32		mΩ
SW Leakage Current	V_{STR} = 5V, V_{SW} = 0 or 3.3V			1	µA

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INTERNAL EFUSE

(VIN = 5V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Normal Mode					
Operating Voltage Range		2.6		7	V
eFuse On-Resistance	I_{SW} = -2A, VIN= 3.3V or 5V, T_J = 25°C		20		mΩ
	I_{SW} = -2A, VIN= 3.3V or 5V, T_J = 100°C		25		mΩ
Blocking FET On-Resistance	I_{OUT} = 2A, VIN= 3.3V or 5V, T_J = 25°C		30		mΩ
	I_{OUT} = 2A, VIN= 3.3V or 5V, T_J = 100°C		38		mΩ
Programmable eFuse Current Limit Range	VIN = 5V, Configured using ISET pin, Triggers nIRQ Pin	1		6	A
eFuse Current Limit Accuracy		-10		+10	%
Blocking FET Current Limit	VOUT-VB > 560mV or at initial startup		300		mA
	VOUT-VB < 560mV except at initial startup		1800		
ISET Monitor Current Ratio	ISET current divided by eFuse current		1/20,000		
eFuse Overcurrent Detection Deglitch			10		µs
eFuse Overcurrent Current Shutdown	Shuts down after deglitch time and stays off for Off Time	6			A
Current Limit Restart Time			100		ms
eFuse Soft start	C_{SS} = 10nF	5.94	6.6	7.26	mV/us
EN Input Low	V_{IO} = 1.8V			0.58	V
EN Input High	V_{IO} = 1.8V	1.22			V

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STORAGE BOOST REGULATOR

(VIN = 5V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Storage Boost Converter					
Operating Input Voltage Range		2.7		36	V
Programmable Output Voltage Range		5.0		28	V
Peak switching Current	BST _CLIM = 00 BST _CLIM = 01 BST _CLIM = 10 BST _CLIM = 11		250 500 950 1500		mA
Standby Supply Current	V_{STR} = 103%, Regulator Enabled, not switching		25	35	μA
Output Voltage Accuracy	V_{STR} = 28V, I_{OUT} = 15mA (continuous PWM mode)	-3%	V_{NOM}	3%	V
Power Good Threshold	V_{STR} Rising		99.5		$\%V_{NOM}$
Power Good Hysteresis	V_{STR} Falling		2		$\%V_{NOM}$
Undervoltage Fault Threshold	V_{STR} Falling STR_UV_TH = 00 STR_UV_TH = 01 STR_UV_TH = 10 STR_UV_TH = 11		 85 87.5 90 92.5		$\%V_{NOM}$
Undervoltage Fault Hysteresis	V_{STR} Rising	2			$\%V_{NOM}$
Overvoltage Fault Threshold	V_{STR} Rising		110		$\%V_{NOM}$
Overvoltage Fault Hysteresis	V_{STR} Falling		3		$\%V_{NOM}$
Start Period	C_{STR} = 1mF, V_{STR} = 28V			200	ms
Minimum On-Time			50		ns
Maximum Off-Time			9.7		μs
Low Side FET On-Resistance	I_{SW} = 325mA		300		mΩ
DISCHG Leakage Current				1	μA
ENB Input Low	V_{IO} = 1.8V			0.58	V
ENB Input High	V_{IO} = 1.8V	1.22			V

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HEALTH MONITOR

(VIN = 5V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Health Monitor					
STR Operating Voltage Range		4.2		28	V
Sink Current Source		9	10	11	mA
Programmable Health Monitor Current Sink Timer Range		2		1280	ms
Programmable Storage Voltage Threshold Range	Configurable 0.2% steps	95		98	%

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I²C INTERFACE ELECTRICAL CHARACTERISTICS

(VIN = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	V_{IO} = 1.8V			0.58	V
SCL, SDA Input High	V_{IO} = 1.8V	1.22			V
SDA Leakage Current	SDA=5V			1	μA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Frequency, f_{SCL}				1000	kHz
SCL Low Period, t_{LOW}		0.5			μs
SCL High Period, t_{HIGH}		0.26			μs
SDA Data Setup Time, t_{SU}		50			ns
SDA Data Hold Time, t_{HD}	(Note1)	0			ns
Start Setup Time, t_{ST}	For Start Condition	260			ns
Stop Setup Time, t_{SP}	For Stop Condition	260			ns
Capacitance on SCL or SDA Pin				10	pF
SDA Rise Time SDA, T_r	Device requirement			120	ns
SDA Fall Time SDA, T_f	Device requirement			120	ns

Note1: Comply with I²C timings for 1MHz operation - “Fast Mode Plus”.
Note2: No internal timeout for I²C operations, however, I²C communication state machine will be reset when entering UV/POR State.
Note3: This is an I²C system specification only. Rise and fall time of SCL & SDA not controlled by the device.
Note4: Device Address is factory configurable to 7’h1A, 7’h3A, 7’h5A.

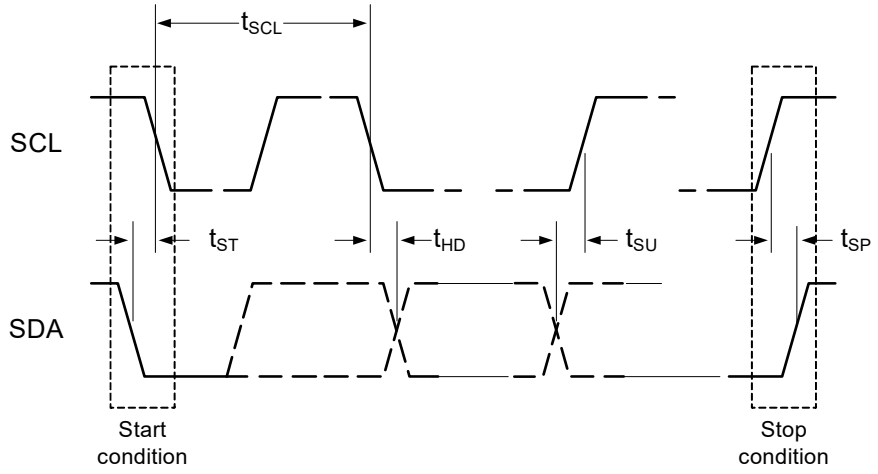

Figure 2: I²C Data Transfer

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FUNCTIONAL DESCRIPTION

General

ACT4921 provides protection, control, and supplemental storage for power failure prevention systems. This functionality goes by many names: Power Loss Protection (PLP), Power Loss Imminent (PLI) and Power Failure Protection (PFP). It provides a system with additional run time after a power failure to all the system to save critical data before shutting down. Typical applications include solid state disk drives (SSD) and servers. In normal operation when input power is good, the IC connects the input to the output through the eFuse. This powers the system load from the system input power. If an input voltage fault occurs, the IC disconnects the input from the output and enters supplement mode, where output power comes from the high voltage storage capacitor power. The internal buck converter efficiently converts the storage voltage down to the regulated output voltage. All startup, storage capacitor charging, and switching between normal and supplement mode operation is autonomous and does not require user intervention.

During start up, the ACT4921 limits the output voltage dV/dt to minimize system level inrush currents. After softstart is complete, the IC charges the storage capacitors with the internal boost converter. The IC automatically recharges the storage capacitors as needed. The IC contains extensive protection circuitry to protect against input voltage overvoltage and undervoltage, output voltage overload and short circuit, degraded storage capacitors, and thermal overload.

The IC communicates with the host processor via I²C and GPIOs. The nIRQ pin indicates general faults which can be read by the host processor via I²C. A dedicated power failure pin, PLI, automatically and immediately goes low to indicate a power loss condition. This gives the system advanced warning to complete all active tasks and shutdown. See the Pin Function section for additional PLI pin functionality.

The ACT4921 is highly flexible and contains many I²C configurable functions. The IC's default functionality is defined by its default CMI (Code Matrix Index), but much of this functionality can be changed via I²C. I²C functionality includes storage voltage setting, OV and UV fault thresholds, switching frequencies, PLI pin functionality, health check settings, and current limits. The CMI Options section shows the default settings for each available CMI option. Contact sales@active-semi.com for additional information about other configurations.

I²C Serial Interface

To ensure compatibility with a wide range of systems, the ACT4921 uses standard I²C commands. It supports clock speeds up to 1MHz. The ACT4921 always operates as a slave device, and can be factory configured to one of three 7-bit slave addresses. The 7-bit slave address is followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation. Refer to each specific CMI for the IC's slave address

7-Bit Slave Address		8-Bit Write Address	8-Bit Read Address
0x1Ah	001 1010b	0x34h	0x35h
0x3Ah	011 1010b	0x74h	0x75h
0x5Ah	101 1010b	0xB4h	0xB5h

The I²C packet processing state machine does not have a timeout function, however, any time the I²C state machine receives a start bit command, it immediately resets the packet processing, even if it is in the middle of a valid packet. The I²C functionality is operational in all states except RESET.

I²C commands are communicated using the SCL and SDA pins. SCL is the I²C serial clock input. SDA is the data input and output. SDA is open drain and must have a pull-up resistor. Signals on these pins must meet timing requirements in the Electrical Characteristics Table. For more information regarding the I²C 2-wire serial interface, refer to the NXP website: http://www.nxp.com.

I²C Registers

The ACT4921 contains an array of internal registers that contain the IC's basic instructions for setting up the IC configuration, output voltages, sequencing, fault thresholds, fault masks, etc. These registers are what give the IC its operating flexibility. The two types of registers are described below.

Basic Volatile – These are R/W (Read and Write) and RO (Read only). After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like masking certain faults. The RO registers communicate IC status such as fault conditions. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed by the factory or the end user.

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Basic Non-Volatile – These are R/W and RO. After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like output voltage settings, startup delay time, and current limit thresholds. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult sales@active-semi.com for custom options and minimum order quantities.

When modifying only certain bits within a register, take care to not inadvertently change other bits. Inadvertently changing register contents can lead to unexpected device behavior.

State Machine

ACT4921 contains an internal state machine with seven internal states: UV/POR, SOFT-START, NORMAL, HEALTH CHECK, SUPPLEMENT, SUPPLEMENT-DISABLE, and SHUTDOWN.

UV/POR State

The IC enters the UV/POR state on power up. It also enters UV/POR from SUPPLEMENT state in the following conditions:

1. When the input voltage drops below the VINS_UV threshold.
2. When the storage capacitor voltage drops below 3.0V.
3. When the buck converter output voltage goes OV or UV.

The user may force the IC into UV/POR by writing a 1 into the FORCE_PWROFF bit, register 0x06h, bit 0. When entering UV/POR from power up, all registers reset to their default state. The registers retain their existing values when the IC enters from SUPPLEMENT state or from SHUTDOWN EFUSE. The IC transitions from the UV/POR state to the SOFT-START state when EN pin is high, the input voltage is above UVLO, the VINS pin is above 0.64V, and the startup delay softstart timer has timed out. The delay timer is set by I²C register EN_STARTDLY[3:1] in register 0x0Bh. Table 1 shows the allowable delay times. 1ms is typically an acceptable delay time, but longer times can be programmed if the input voltage source rises extremely slowly.

Table 1: Softstart Delay

EN_STARTDLY[3:1]	Startup Delay Time
000	Not valid
001	1ms
010	5ms
011	10ms
100	20ms
101	40ms
110	80ms
111	125ms

SOFTSTART State

In the SOFTSTART state, the IC slowly turns on the eFuse to minimize inrush currents. The SS pin directly controls the maximum output voltage dV/dt. The IC stays in the SOFTSTART state until VIN-VOUT < 200mV and a 1ms timer times out. PG_VO goes high when the IC exits the SOFTSTART state.

NORMAL State

The NORMAL state is the normal operating state. The eFuse is fully on, VOUT = VIN, and the IC provides full operating current. When the IC transitions from the SOFTSTART state to the NORMAL state, the PG_VO pin immediately goes high and the IC starts charging the storage capacitors if ENB is pulled high.

HEALTH CHECK State

The HEALTH CHECK state can be considered a sub-state of the NORMAL state. The IC operates identical to the NORMAL state with the addition of activating the circuitry that check the storage capacitor health. The IC automatically enters HEALTH STATE every four minutes. The user may also manually enter this state by writing a 1 into the FORCE_HLTHCHK bit which is bit 1 in register 0x06h. This bit automatically resets to 0 after the health check routine completes. The IC automatically exits HEALTH CHECK and enters SUPPLEMENT state in a fault condition.

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SUPPLEMENT State

The IC enters SUPPLEMENT state when it detects a fault condition. It opens the eFuse to bi-directionally disconnect the input from the output. It automatically turn on the buck converter to power the output from the storage capacitors. The following five conditions move the IC into SUPPLEMENT state.

1. VINS voltage below UV threshold
2. VINS voltage above the OV threshold
3. Input voltage above the OV threshold
4. eFuse current above the OC threshold
5. VIN – VOUT > 300mV

SUPPLEMENT-DISABLE State

In the SUPPLEMENT-DISABLE state, VOUT is good and can power the system, but the IC cannot transition to the SUPPLEMENT state. While in this state, the open drain output PG_STR status at LOW.

In typical startup sequence, when the ACT4921 exits the SOFTSTART state, it transitions though the NORMAL state directly to SUPPLEMENT-DISABLE state. While IC is in SUPPLEMENT-DISABLE state, the blocking FET gets turned on by the ENB pin or the EN_BFET bit in register 0x06h. The blocking FET sources 300mA constant current to charge the storage caps to VIN. Then the boost converter turns on to charge the storage caps to their final voltage. When the storage capacitor is fully charged, the ACT4921 exits SUPPLEMENT-DISABLE state and moves to NORMAL state. The transition of PG_STR pin from low to high indicates that the IC transitioned to the NORMAL state.

The ACT4921 checks the following conditions to make sure the operating conditions and external components are within speck and working properly so the IC is capable of entering SUPPLEMENT state to provide backup power. If the IC Is operating in the NORMAL state and one of the following becomes invalid, the IC notifies the system by pulling nIRQ low and then enters the SUPPLEMENT-DISABLE state.

1. VOUT-VB < 200mV
2. Die temperature <145°C
3. LDO (REF) is valid
4. Bootstrap capacitor at HSB pin properly connected
5. The buck compensation is present and not shorted.

SHUTDOWN State

SHUTDOWN disables all IC functionality to protect against extreme over temperature conditions above 155°C. This includes shutting off the eFuse. I^2C functionality not available in this state. The IC transitions to SOFT-START when the junction temperature drops and there is no overcurrent fault.

The following figures and tables help describe the ACT4921 states and functionality in different situations. Figure 3 shows the ACT4921 State Diagram. Table 1 shows which functions are enabled in each state. Table 2 shows how different operating conditions and faults affect different IC functionality. Note that the current operating state can be determined by reading the I^2C register bits CURRENT_STATE in register 0x00h.

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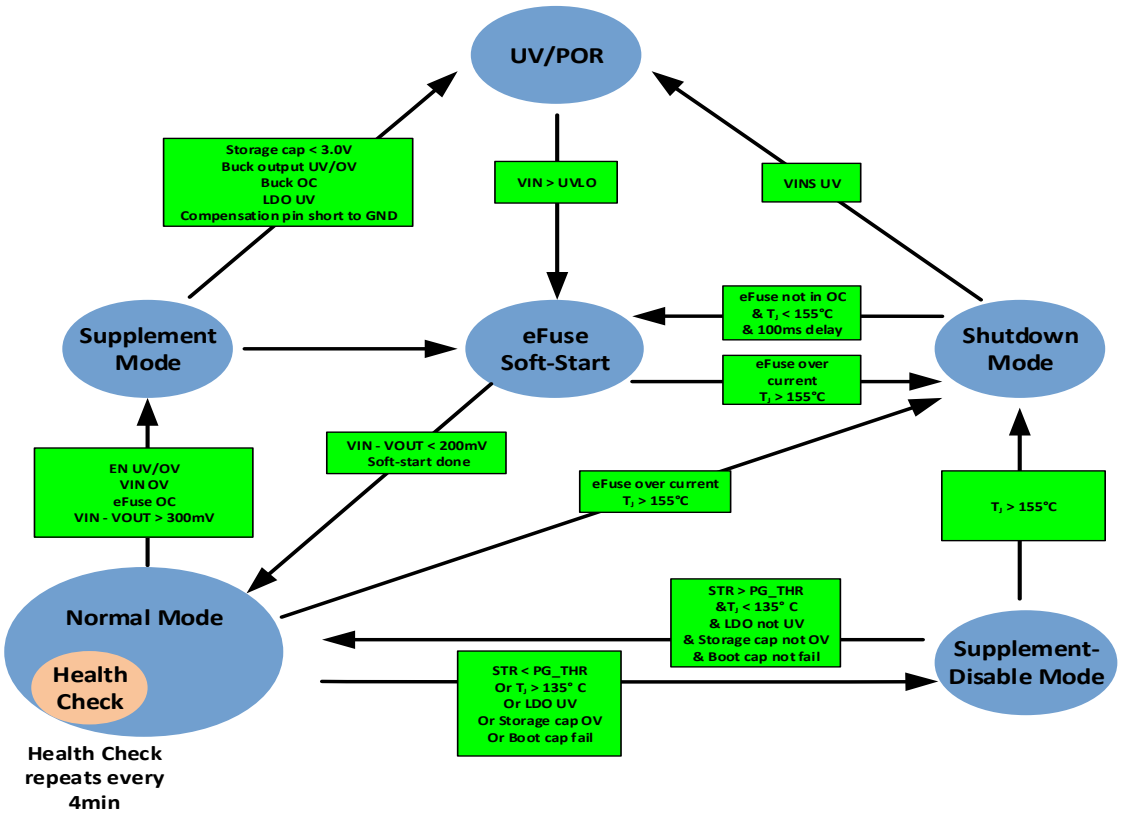

Figure 3: State Machine Diagram

Table 2: Enabled Functions in Different States

States	eFuse	Boost	Buck	BFET	V_{REF}
UV/POR	Disabled	Disabled	Disabled	Disabled	Disabled
SOFT-START	Enabled	Disabled	Disabled	Disabled	Enabled
NORMAL	Enabled	Enabled	Disabled	Enabled	Enabled
HEALT CHECK	Enabled	Enabled	Disabled	Enabled	Enabled
SUPPLEMENT	Disabled	Disabled	Enabled	Enabled	Enabled
SUPPLEMENT-DISABLE	Enabled	Disabled	Disabled	Enabled	Enabled
SHUTDOWN	Disabled	Disabled	Disabled	Disabled	Disabled

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Table 3: IC Functionality vs Operating Conditions.

Operation Conditions	eFuse	Blocking FET	Boost	Buck		PLI	PG_VO	PG_STR	nIRQ	IC Action
Normal Operation	On	On	Enabled	Off		High	High	High	High	Boost Charges STR Cap as needed
Input OC Vin - Vout < 560mV	On	On	Enabled	Off		High	High	High	Low	eFuse in LDO Mode
Input OC Vin - Vout > 560mV	On → Off	Off	Off	On		Low	Low	High → Low	Low	Enter Supplement Mode
VBUS Short	On → Off	On	Off	On		Low	Low	High → Low	Low	Enter Supplement Mode
Input Over Voltage	On → Off	On	Off	On		Low	High	High → Low	Low	Enter Supplement Mode
Input Under Voltage	On → Off	On	Off	On		Low	High	High → Low	Low	Enter Supplement Mode
EN Pin Low (@ Start up)	Off	Off	Off	Off		Low	Low	Low	Low	IC is disabled
EN Pin Low (@ Normal Operation)	On → Off	Off	Off	On		Low	Low	High → Low	Low	Enter supplement mode first, then IC is disabled
ENB Pin Low	On	Off	Off	Off		No Effect	No Effect	Depends on Vstr	Low	Disables Boost & Buck, turns off Blocking FET
Health Checking	On	On	Off	Off		High	High	High	High	If failed, PS_STR and nIRQ go low
120°C < Tj < 145 °C	On	On	Enabled	Off		High	High	High	Low	Sends out thermal alert
145 °C < Tj < 155 °C	On	On	Off	Off		High	High	Depends on Vstr	Low	PG_STG depends on Vstr
Tj > 155 °C	Off	Off	Off	Off		Low	Low	Low	Low	IC is disabled

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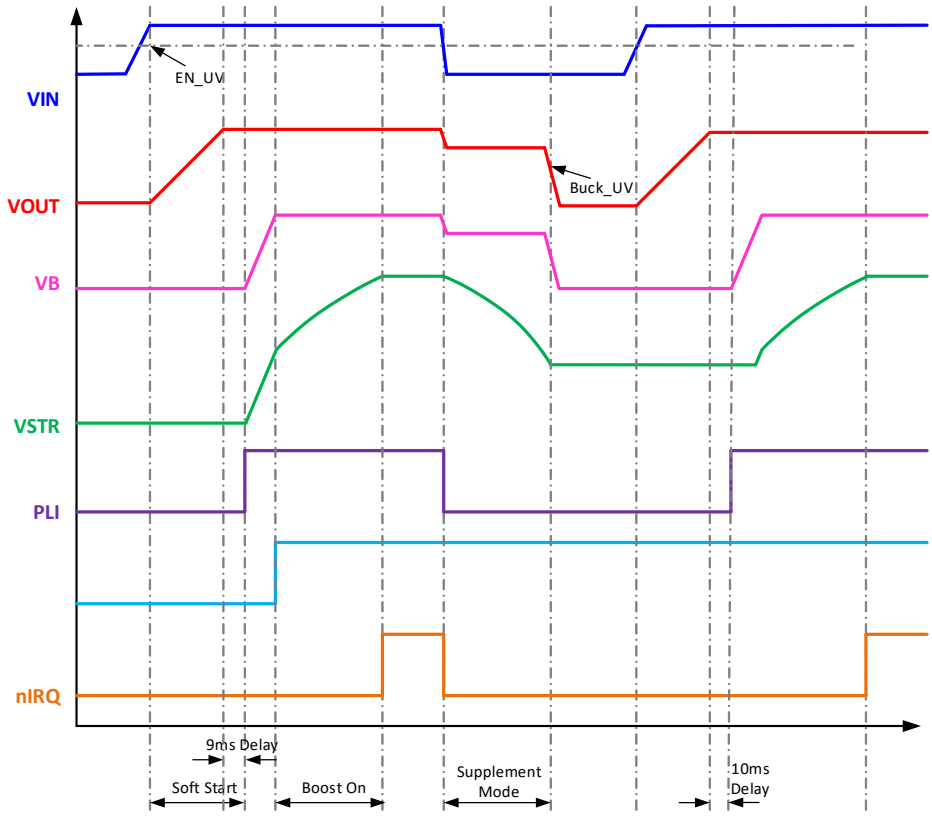

Figure 4: Operation State

Pin Functions

VIN

VIN is the input the eFuse. Connect a 0.1uF ceramic capacitor between VIN and PGND. VIN is directly connected to VOUT in normal operation. The eFuse disconnects VIN from VOUT when the IC enters supplement mode.

EN

The EN pin provides a digital input to turn the IC on or off. When EN is low when input power is applied, the IC remains disabled. Pulling EN high moves the IC into the SOFTSTART state. When EN is pulled low while input power is valid, the IC immediately enters SUPPLEMENT mode. After the storage capacitor is depleted, the IC is disabled.

VINS

The VINS pin provides both overvoltage and undervoltage protection thresholds. The VINS pin contains two precision comparators with hysteresis. It can be directly driven from a digital input to turn the eFuse on and off. The EN pin is typically used with a resistor divider from VIN to AGND to program an eFuse startup voltage higher than the IC's UVLO value. The eFuse turns on when the input EN is high and the VINS voltage goes above the VINS_UV_REF threshold. Once the eFuse is on, it turns off and enters supplement mode if the VINS pin goes above the VINS_OV_REF threshold or below the VINS_UV_REF threshold.

The VINS pin should not be left floating. It can be driven from standard logic signals greater than VINS_UV_REF. It can also be driven with open-drain logic to provide. When driving it with an open-drain, ensure that the pullup voltage is not higher than the VINS_OV_REF setting.

VINS_UV_REF is fixed at 0.64V. However, the VINS_OV_REF can be programmed by I^2C bits VINS_OV_REF [2:0]. The default VINS_OV_REF voltage is set by the IC's CMI.

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Table 4: Over Voltage Reference Settings

VINS_OV_REF[2:0]	OV Threshold (V)
000	Disabled
001	0.82
010	0.92
011	1.00
100	1.08
101	1.16
110	1.24
111	1.32

ENB

The ENB pin enables the blocking FET, the buck converter, and the boost converter. They are disabled when ENB is low and enabled when ENB is high. ENB provides two main system level functions. The first is to isolate the storage capacitors as startup to allow faster system startup. ENB is typically held low by the system processor at startup. After the system starts up, the processor pulls ENB high to allow the boost converter to charge the storage caps. The second function is to provide fault isolation. In the event of a storage capacitor failure, ENB can be pulled low to isolate the capacitors from the system. This allows the system to continue operating until it can be safely shutdown.

STR

STR is the output to the storage capacitor bank. In normal operation the internal boost converter charges the storage capacitors through the STR pin. When the IC enters supplement mode, the internal buck converter uses the STR pin as its input to power the system. The STR pin is typically connected to hundreds of microfarads of storage capacitance. It always requires a 22uF or greater ceramic capacitor. See the Buck Converter section for more information.

nIRQ—Interrupt

ACT4921 has an interrupt pin to inform the host of any fault conditions. In general, any IC function with a status bit asserts nIRQ pin low if the status changes. The status changes can be masked by setting their corresponding register bits. If nIRQ is asserted low, the fault must be read before the IC deasserts nIRQ. If the fault remains after reading the status bits, nIRQ remains asserted.

The status changes shown below assert the nIRQ pin:

- Input overvoltage, undervoltage
- Thermal warning, thermal shutdown
- eFuse VIN to VOUT over limits
- eFuse current warning and limit
- VB pin is not valid (VB or STR short)
- Storage capacitor overvoltage, undervoltage
- Supplemental mode active
- Buck operation faults
- Buck undervoltage shutdown
- REF LDO undervoltage

nIRQ is an open-drain output and should be pulled up to an appropriate supply voltage with a 10kΩ or greater pull-up resistor.

SCL, SDA

SCL and SDA are the I^2C clock and data pins to the IC They have standard I^2C functionality. They are open-drain outputs and each require a pull-up resistor. The pull-up resistor is typically tied to the system's uP IO pins. The pullup voltage can range from 1.8V to 5.0V.

REF

The REF pin is an internal bias voltage output pin. Connect a 1µF capacitor between REF and AGND. Do not apply an external load to the REF pin.

BSET

BSET sets the boost converter output voltage. The output voltage is a function of both a resistor connected between BSET and AGND as well as internal I^2C register settings. See the Storage Boost Converter section for more information.

ISET

ISET sets the eFuse current limit with a resistor connected to AGND. See the eFuse section for more information.

SS

The SS pin uses a capacitor to AGND to control the eFuse softstart timing. See the eFuse section for more information.

PGND

The PGND pin is the buck and boost converters' power ground. The internal FETs connect directly to the PGND pins. The power supply input and output capacitors should connect to the PGND pins.

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AGND

The AGND pin is the IC's analog ground pin. It is a "quiet" ground pin that is separate and isolated from the high power, high current carrying PGND ground plane. Connect the non-power components to AGND. AGND must be kelvin connected to the PGND pin in a single location.

COMP

COMP is the output of a transconductance amplifier that is used to compensate the internal buck converter. The compensation components, which are typically a standard type-2 compensation should be grounded to the AGND pin. See the Application section for more information on compensating the internal buck converter.

PLI

PLI (Power Loss Indicator) goes high after softstart and stays high in normal operation. PLI immediately goes low when the IC enters supplement mode. This setting is used to let the system uP know that power loss is imminent.

The PLI pin is an open-drain output and is 5V compliant.

FB

The FB pin is used to regulate the buck converter output voltage when the IC is in supplement mode.

HSB

HSB provides power to the internal high-side MOSFET gate driver circuitry. Connect a 47nF capacitor from HSB pin to SW pin.

SW

SW is the switch node for the internal buck and boost converters. Connect the inductor to the SW pin.

VOUT

VOUT is the output of the eFuse and connects to the system load. The eFuse connects VOUT to VIN in normal operation, and it disconnects it in supplement mode.

VB

VB is the output pin from the blocking FET. Depending on the operating mode, power either flows into or out of VB. In normal operation, power flows from VIN, through the eFuse and blocking FETs and out of VB to provide input power to the boost converter. ENB must be pulled high to enable this functionality.

During supplement mode, the buck converter output power flows into VB, through the blocking FET, and out of VOUT to the system.

DISCHG

DISCHG is the discharge pin for the storage capacitors. When the IC enters the UV/POR state, DISCHG is internally connected to PGND through an internal FET. Connect a resistor between DISCHG and STR to quickly discharge the storage capacitance. The user can manually turn on the DISCHG FET by setting the DISCHG_STR bit to 1.

The discharge function is typically only used during product development and evaluation. It allows the user to quickly discharge large storage capacitor values between testing to ensure the next power cycle starts with discharged capacitors. If the function is not used in production, the discharge resistor can be removed from the board and the DISCHG pin can be connected to PGND or left open. The discharge resistor should be chosen to keep the discharge current less than 100mA.

PG_STR

PG_STR is a power good indicator for the storage capacitors. It goes high when the storage capacitor voltage goes into regulation. It goes low when the voltage drops below 95% of the setpoint. It also goes low when either the buck or boost converter is disabled. It is open drain and is 5V compliant.

PG_VO

PG_VO is a power good indicator for VOUT. It goes high when the eFuse is fully turned on. In supplement mode, it starts high and then goes low when the FB pin drops below 95% of V_{FB_REF} (0.8V). It is open drain and is 5V compliant.

General Description

eFuse

The ACT4921 eFuse is an "electronic" fuse that disconnects the input from the output. It has considerable advantages over mechanical fuses because it has adjustable current thresholds and it resets after the fault condition is gone. The eFuse consists of two back-to-back MOSFETS to provide bi-directional protection. This provides protection against both input and output short circuit conditions by preventing current flow in both directions. Hot swap functionality is provided by the eFuse softstart function and current limiting circuitry. This prevents large inrush

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currents from pulling down the input voltage. The eFuse also provides protection against high input voltage transients up to 7V by opening when the input voltage goes above the programmed threshold.

The eFuse turns off in the following conditions.

1. VINS voltage below UV threshold
2. VINS voltage above the OV threshold
3. Input voltage above the OV threshold
4. eFuse current above the OC threshold
5. VIN – VOUT > 300mV

Blocking FET

The blocking FET is an internal MOSFET that provides isolation between the system output voltage (VOUT) and the storage capacitors. It provides system level fault tolerance that allows the system to continue operating normally in the event of a storage capacitor failure. During the blocking FET softstart, it provides 300mA constant current. The blocking FET stays in softstart until the voltage across it (VOUT-VB) approaches 0V. After softstart is complete, the blocking FET turns on fully, and has a 1.8A current limit setting. The blocking FET enters softstart again when VOUT-VB < 560mV.

During startup, the 300mA constant current source linearly charges up the storage capacitors. If the storage capacitors are not charged up to VIN within 1s, the blocking FET turns off for 1s and then retries. With extremely large storage capacitors such as supercapacitors, the blocking FET will turn on and off at a 2s period. This is expected functionality and minimizes the power dissipation in the IC.

In normal operation, when the blocking FET is fully turned on, it applies power to the boost converter, allowing the storage capacitors to charge up to their final value. When the IC enters supplement mode, the buck output power flows into the VB pin, through the blocking FET, and out of VOUT to the system.

The blocking FET limits a storage capacitor overload condition to 1.8A. This causes the voltage at VB to drop, generates a VB undervoltage fault, and the IC pulls nIRQ low. If VB voltage drops below VOUT-560mV, the current limit drops from 1.8A to 300mA. During this condition, the eFuse stays on and system continues to operate normally.

If the overload condition remains for longer than 1s, the blocking FET enters a hiccup mode where it turns on and off for a 2s period. Hiccup mode applies to both normal startup with very large storage capacitors and to short circuit conditions. Note that the IC enters the SUPPLEMENT-DISABLE state during both startup and short circuit conditions.

The blocking FET can be manually turned on and off by the ENB pin or the EN_BFET bit in register 0x06h. When register EN_ENB_REG = 0, the ENB pin controls the blocking FET. Pulling ENB low turns it off and pulling ENB high turns it on. When register EN_ENB_REG = 1, the EN_BFET bit pin controls the blocking FET. Setting EN_BFET = 0 turns it off and setting EN_BFET high turns it on.

Note that disabling the blocking FET also disables the boost converter. This allows systems to startup faster by keeping the boost disabled until the system is up and running.

Current Limit Setting

A resistor connected between the ISET pin and VSS programs the ACT4921 eFuse maximum DC current limits. The input current limit is linearly proportional to the resistor value on the ISET pin. The following equation calculates the correct resistor value to get the desired current limit threshold.

$$R_{ILIM} = \frac{20000}{I_{ILIM}} \qquad \text{Equation 1}$$

Where R_{ILIM} is the current limit resistor in ohms and I_{ILIM} is the desired current limit threshold in Amperes. Figure 5 shows the current limit setting vs R_{ILIM} value. Note that the maximum allowable eFuse current limit setting is 6A, which corresponds to a 3.32kohm resistor.

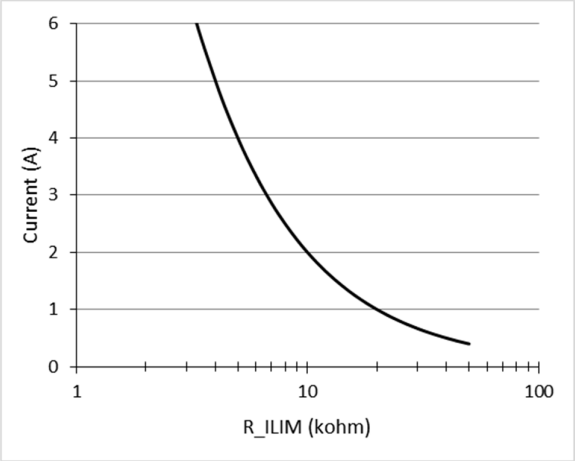

Figure 5: Current Limit Threshold vs R_{ILIM}

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Note that the eFuse current can be measured using the ILIM pin. If eFuse current is measured via the ILIM pin, the measurement circuit must have a high impedance input to minimize errors. The current flowing out of ILIM is 1/20000 of the current through the eFuse. The following equation calculates the eFuse current when measured via the ILIM pin.

$$I_{eFuse}=\frac{V_{ILIM}*20000}{R_{\mathrm{ILIM}}} \quad \text{Equation 2}$$

Where R_{ILIM} is the current limit resistor in ohms and V_{ILIM} is the voltage measured on the ILIM pin in volts.

When the eFuse reaches the current limit threshold, it clamps the output current. If the load tries to draw additional current, the eFuse opens.

Soft-Start

The SS pin controls the eFuse start-up. The SS pin drives a constant 5μA internal current source into the external soft-start capacitor to provide a linear ramping voltage at the SS pin. The output voltage linearly ramps with the SS pin voltage, resulting in a well-controlled linear softstart ramp on VOUT, regardless of the load conditions. The following equation calculates the required soft-start capacitance.

$$C_{SS}(nF) = \frac{65\times T_{SS}(mS)}{V_{OUT}(V)} \quad \text{Equation 3}$$

Where the T_{SS} is the soft-start time in ms and V_{OUT} is the output voltage.

The softstart current must be less than 90% of the programmed eFuse current limit. If the softstart current is greater than 90% of the eFuse current limit, the IC enters the SHUTDOWN state, turns off the eFuse, and then retries to softstart again. The following equation calculates the minimum allowable softstart time.

$$T_{SS\_min}(ms) = \frac{C_{OUT}(mF)* V_{OUT}}{0.9*I_{ILIM}(A)} \quad \text{Equation 4}$$

Where C_{OUT} is the sum of the output capacitance and storage capacitance in mF, V_{OUT} is the output voltage in volts, and I_{ILIM} is the eFuse current limit in Amperes programmed by the ILIM resistor.

Buck Converter

General Description

The ACT4921 contains current-mode, synchronous PWM step-down converter that achieves peak efficiencies of 95%. The buck converter minimizes noise in sensitive applications and allows the use of small external components. It is highly flexible with external component selection and can be reconfigured via I²C registers. External components set the output voltage and compensation while I²C registers set the switching frequency and current limit. The buck converter operates in fixed frequency PWM mode. Its switching frequency is programmable between 562kHz to 2250 kHz via the I²C register BK_FREQ[1:0] which allows the system to be optimized for different applications. It has two peak current limit options of 6A and 10A allowing for further system optimization. Overcurrent is set by a non-I²C bit BKILIM_OPT in register 0x0Eh. Refer to the CMI section at the back of the datasheet for each IC's specific setting. The buck output voltage is externally programmable between 1.8V and 6V.

The buck converter generates a regulated output voltage at the VB pin from the storage capacitors when the IC enters supplement mode. This provides the backup power when the system experiences fault conditions. Note that the buck output voltage goes into the VB pin, through the blocking FET and out of the VOUT pin to the system. After the IC exits the SOFTSTART state, the buck converter is enabled but remains turned off. It automatically turns on when the IC enters supplement mode, and remains on until the storage capacitors discharge to 3.0V. Note that ENB must be pulled high to enable the buck converter. Most systems wait until the system is up and running before enabling the buck and boost with the ENB pin.

Frequency Setting

Higher switching frequencies result in smaller solution sizes at the cost of slightly lower efficiency. Lower switching frequencies result in larger solution sizes with higher efficiency. The following table gives the maximum allowable switching frequency as a function of storage voltage.

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Table 5: Maximum Allowable Buck Switching Frequency

Storage Voltage	Maximum Buck Switching Frequency
< 18V	2.25MHz
18V to 25V	1.5MHz
> 25V to 28V	1.125MHz

Output Voltage Setting

The buck converter output voltage is programmed by an external resistor divider connected between the VB pin and AGND, with the center tap connected to the FB pin. The buck output voltage can be set above, below, or equal to the input voltage supplement threshold. When the input voltage goes outside the normal operating voltage set by the VINS pin, the IC enters supplement mode and regulates the output voltage to the programmed buck voltage. Although the buck converter immediately starts up when the IC enters supplement mode, the output voltage still has a small, but finite drop in output voltage between the time the eFuse turns off and the buck converter is fully on. This voltage drop should be considered when setting the output voltage. The following equation calculates the correct resistor values to set the desired output voltage.

$$R1 = \mathrm{R2} * \left(\frac{V_{\mathrm{BUCK}}}{V_{\mathrm{FB}}} - 1\right) \qquad \text{Equation 5}$$

Where R1 is the top feedback resistor, R2 is the bottom feedback resistor, V_{BUCK} is the desired output voltage, and V_{FB} is the fixed 0.8V reference voltage on the FB pin. Choose R2 in the range of 10kohm. Smaller resistor values are acceptable, but larger values will affect voltage accuracy due to bias currents into the FB pin.

Protection

The buck converter has several protection mechanisms to insure safe operation. It stops operation when input voltage from storage cap drops below STR_UVLO (3.0V) or when the output voltage drops below the power good threshold which is fixed at 93% of the output setpoint. Note that the output undervoltage protection is masked by default, but can be unmasked by the I²C register bit Mask_BK_UV REG0x11 [0].

The buck converter provides overcurrent and short circuit protection. Overcurrent protection is achieved with cycle-by-cycle current limiting. The peak current threshold is set to either 6A or 10A by BKILIM_OPT. If the peak current reaches the programmed threshold, the IC turns off the power FET. This condition typically results in shutdown due to an output voltage UV condition due to the shortened switching cycle.

A short circuit condition that results in the peak switch current being 122.5% of BKILIM_OPT immediately shuts down the supply and asserts nIRQ low. A buck overcurrent, undervoltage, or overvoltage condition moves the IC into the UV/POR state.

Compensation

The Buck regulator utilizes type 2 external compensation placed on the COMP pin. Contact the factory for compensation details.

Input Capacitor Selection

The STR pin is the input voltage to the buck converter. It requires a dedicated high quality, low-ESR, ceramic input capacitor that is optimally placed to minimize the power routing. For optimal PCB layout considerations, 1206 or 1210 sized input capacitors are recommended. A 22uF capacitor is typically suitable, but the actual value is application dependent. The input capacitor can be increased without limit. Choose the input capacitor value to keep the input voltage ripple less than 50mV

$$C_{IN} = Iout * \frac{\frac{V_{BUCK}}{V_{STR}} * \left(1 - \frac{V_{BUCK}}{V_{STR}}\right)}{F_{SW} * V_{ripple}} \qquad \text{Equation 6}$$

Where Iout is the maximum eFuse load current in Amperes, V_{STR} is the maximum storage voltage, V_{BUCK} is the buck output voltage, F_{SW} is the switching frequency, and V_{ripple} is the maximum allowable ripple voltage on the input of the buck converter. Note that the storage capacitor values should not be considered when calculating the input voltage ripple because they are not typically designed for high frequency functionality.

Be sure to consider the input capacitor's DC bias effects. A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The input capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics is not recommended. Input capacitor placement is critical for proper operation. The buck's input capacitor must be placed as close to the IC as possible. The traces from STR to the capacitor and from the capacitor to PGND should as short and wide as possible.

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Inductor Selection

The Buck regulator utilizes current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. The ACT4921 is optimized for operation with 1uH to 3.3uH inductors. Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current by at least 30%. Due to the requirement for the buck converter to start up as quickly as possible, the inductor should be designed to give a maximum ripple current, ΔI_L, of 50% to 60% of the maximum output current. The following equation calculates the recommended inductor value.

$$L = \frac{\left(1-\frac{V_{BUCK}}{V_{STR}}\right) * V_{BUCK}}{F_{SW} * \Delta I_L} \qquad \text{Equation 7}$$

Where L is the inductor value in μH, V_{BUCK} is the output voltage, V_{STR} is the maximum storage voltage, F_{SW} is the switching frequency in Hz, and ΔI_L is the desired ripple current in Amperes.

Output Capacitor Selection

The buck converter is designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR. The buck converter is designed to operate with 44μF output capacitor over most of its operating ranges, although more capacitance may be desired depending on the duty cycle and load step requirements. Choose a ripple voltage that is approximately 1% of the output voltage setpoint. Note that the output capacitance must be placed at the output of the buck converter. Additional downstream capacitance will be placed at the loads, but this capacitance should not be considered when calculating the buck output capacitance. However, the downstream capacitance should be considered when compensating the power supply. The following equation calculates the output voltage ripple as a function of output capacitance. Note that the worst case ripple voltage occurs at the beginning of supplement mode when the storage capacitors are fully charged.

$$C_{OUT} = \frac{\Delta I_L}{8 * F_{SW} * V_{ripple}} \qquad \text{Equation 8}$$

Where V_{ripple} is the desired output ripple voltage, F_{SW} is the switching frequency in Hz, and ΔI_L is the maximum ripple current in Amperes.

As with the input capacitor selection, use X5R or X7R dielectrics and be sure to consider the capacitor's DC bias effects.

Storage Boost Converter

General Description

The ACT4921 contains an integrated peak current-mode, synchronous boost converter. It minimizes system level costs by using the same components as the buck converter. The peak current is adjustable between 250mA and 950mA, allowing for system optimization. The output voltage is adjustable between 5V and 28V via I²C registers and an external resistor. The peak current-mode control topology eliminates the need for compensation. The boost automatically charges up the storage capacitors from the input voltage so they are ready to provide backup power in the event of a system fault.

Startup

The boost converter automatically starts when the IC exits the SOFTSTART state and the ENB pin is pulled high. Note that the IC exits the SOFTSTART state 10ms after the output voltage is within 200mV of the input voltage. Most systems wait until the system is up and running before enabling the buck and boost with the ENB pin.

When the storage voltage reaches regulation, the boost enters standby mode and monitors the storage voltage. It automatically turns back on and "tops off" the storage capacitors when the storage voltage drops below 95% of the programmed voltage. The boost converter automatically turns off if it is "topping off" the storage capacitors when the IC enters supplement mode.

The average input current when the boost charges the storage capacitors is approximately ½ of the peak switching current. The peak switch current is programed by register BST_CLIM[1:0].

Table 6: Boost Peak Current Settings

BST_CLIM[1:0]	(mA)
00	250
01	500
10	950
11	1500

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Operating Mode

The boost converter operates in peak current mode, non-fixed frequency mode. The power FET stays on until its current reaches programmed peak current. It then turns off until the inductor current drops to 0A, at which time it turns on again.

Storage Capacitor Voltage Setting

The buck converter output voltage is set by either the I²C register BSTVSET[4:0], or a combination the register and a resistor placed between the BSET pin to VSS.

When using only the BSTVSET[4:0] leave the BSET pin floating. Table 6 shows the programmed storage voltage. The default value is determined by the IC's specific CMI option. Note that the IC accepts BSTVSET values between 11000 and 11111 and each of these values sets the boost voltage to 28V.

Table 7: Storage Capacitor Voltage Settings with BSET Pin Open

BSTVSET[3:0]	BSTVSET[4]	
	0	1
0000	5V	21V
0001	5.6V	22V
0010	7V	23V
0011	8V	24V
0100	9V	25V
0101	10V	26V
0110	11V	27V
0111	12V	28V
1000	13V	28V
1001	14V	28V
1010	15V	28V
1011	16V	28V
1100	17V	28V
1101	18V	28V
1110	19V	28V
1111	20V	28V

Using both the BSTVSET[4:0] register and an external resistor provides additional output voltage resolution. In this configuration, the following equation calculates the output voltage.

$$V_{STR} = V_{BSTVSET} * \frac{R_{BSET}}{60k\Omega} \qquad \text{Equation 8}$$

Where $V_{BSTVSET}$ is the voltage set by the BSTVSET register in Table 6 and R_{BSET} is the resistor on the BSET pin in ohms.

As an example, to set the storage voltage to 12.8V when the default BSTVSET[4:0] = 10111, first look up the storage voltage when the BSET pin is open per table 7. This sets $V_{BSTVSET}$ = 28V. Using equation 8, setting R_{BSET} = 27.4kΩ sets V_{STR} = 12.8V. Note that R_{BSET} should be set between 20kΩ and 60kΩ. Setting R_{BSET} below 20kΩ gives the same result as using a 20kΩ resistor. Setting R_{BSET} above 60kΩ gives the same result as using a 60kΩ resistor. Using R_{BSET} outside the range is acceptable and does not damage the IC.

Input Capacitor Selection

There are no special considerations for the boost converter input capacitor. The IC topology uses the buck converter output capacitor for the boost input capacitor. Proper selection of the buck converter output capacitor automatically results in an acceptable boost converter input capacitor.

Output Inductor Selection

There are no special considerations for the boost converter inductor. The IC topology uses the buck converter inductor for the boost converter inductor. Proper selection of the buck converter output capacitor automatically results in an acceptable boost converter input capacitor.

Output Capacitor Selection

The IC topology uses the buck converter input capacitor for the boost converter output capacitor. Note that the storage capacitors are also included in the boost converter output capacitors. Proper selection of the buck converter input capacitor typically results in an acceptable boost converter output capacitor. The boost output capacitor has two criteria. The first is that it must consist of at least 10µF of high quality X5R or X7R ceramic capacitance placed directly between the STR pin and PGND. The second criteria is that the sum of the ceramic capacitor and storage capacitors must be greater than 100µF. There is no requirement for the additional capacitance dielectric material. This provides flexibility for the storage capacitors, which allows the use of super capacitors, electrolytic, polymer, Tantalum, ceramic, or any capacitors in the design.

Output Voltage UVLO Setting

The storage capacitor power good signal indicates that the STR voltage is above the UVLO threshold. The UVLO threshold is shared with the storage capacitor

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health check, and is set by the I²C register HMON_THR [3:0]. The default value is determined by the IC's specific CMI option.

Table 8: Storage Capacitor PG Threshold

HMON_THR[2:0]	HMON_THR[3]	
	0	1
000	95.0%	96.6%
001	95.2%	96.8%
010	95.4%	97.0%
011	95.6%	97.2%
100	95.8%	97.4%
101	96.0%	97.6%
110	96.2%	97.8%
111	96.4%	98.0%

Storage Capacitor Health Monitor

General Description

The ACT4921 has an internal health monitor for the storage capacitors. It applies a constant current sink to the capacitors and monitors the voltage drop. If the voltage drops below a predetermined threshold, the IC asserts nIRQ to indicate that the storage capacitance has dropped below the allowable threshold. Health monitoring is completely autonomous, but can also be manually initiated by the system uP. Health monitoring can also be configured so that it is only a manual operation so it can be triggered on demand to avoid any critical system operations. The health monitor parameters are adjustable via I²C registers to allow flexibility for different capacitor values.

Health Monitor Algorithm

The health check algorithm sinks 10mA into the STR pin for a time determined by I²C register HMON_TSET. It then sinks 50mA for 200us. It monitors the voltage on the STR pin, and if the voltage drops more than the percentage set by I²C register HMON_THR, it asserts nIRQ low and sets the fault bit. The IC's specific CMI option sets the default HMON_TSET and HMON_THR settings. After the HMON_TSET time, the boost turns back on to recharge the storage capacitor.

The health check function can be enabled and disabled by the DIS_HEALTH_CHK bit 0x0Bh [4]. It also can be forced to perform a one-shot health check by the FORCE_HLTHCHK bit 0x06h [1]. Forcing a single health check is valid even when the DIS_HEALTH_CHK bit = 1. If set in continuous mode, the IC performs a health check every 4 minutes. This timing can be configured for every 8 minutes or 16 minutes by bits SCALE_HCHK _2X and SCALE_HCHK _4X in register 0x10h [1:0].

The ACT4921 allows for very flexible health checking routines by allowing the system to manually enable the 10mA discharge current by setting the EN_STR10mASINK bit 0x06h [2] = 1. In this situation, the system manually turns the discharge current on and off. The storage capacitor voltage threshold is still determined by the HMON_THR register. This function is useful for checking extremely large capacitor values which need very long discharge times.

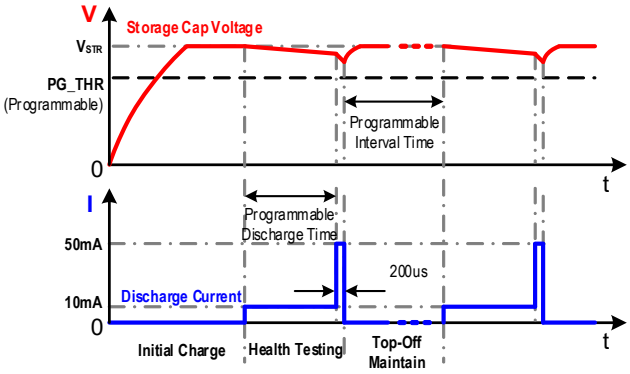

Figure 6: Storage Voltage at Different Stages

The register HMON_TSET [3:0] sets the health check discharge time as shown in Table 9.

Table 9: Health Check Discharge Time

HMON_TSET[2:0]	HMON_TSET[3] (ms)	
	0	1
000	2	384
001	4	512
010	8	640
011	16	768
100	32	896
101	64	1024
110	128	1152
111	256	1280

PC board layout guidance

Proper parts placement and PCB layout are critical to the operation of switching power supplies. Follow the

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following layout guidelines when designing the ACT4921 PCB. Refer to the Active-Semi ACT4921 Evaluation Kit for layout guidance.

Place the buck input capacitors as close as possible to the IC. Connect the input capacitors directly between STR and PGND pins on the top layer. Routing these traces on the top layer eliminates the need for vias.

1. Minimize the switch node trace length between the SW pin and the inductor. Optimal switch node routing is to run the trace between the input capacitor's pads. Using 1206 or larger sized input capacitors is recommended. Avoid routing sensitive analog signals near these high frequency, high dV/dt traces.
2. The Buck output capacitors should be placed by the VOUT pin and connected directly to the VOUT pin and ground plane with short and wide traces. Note that the buck output capacitors do not connect to the VB pin or inductor. The output capacitor ground should make a short connection to the input capacitor ground. If required, use multiple vias.
3. The FB pin should be Kelvin connected to the output capacitor through the shortest possible route, while keeping sufficient distance from switching node to prevent noise injection. The IC regulates the output voltage to this Kelvin connection.
4. Connect the PGND and AGND ground pins must be electrically connected together. The AGND ground plane should be isolated from the rest of the PCB power ground.
5. Remember that all open drain outputs need pull-up resistors.
6. Connect the exposed pad directly to the top layer ground plane. Connect the top layer ground plane to both internal ground planes and the PCB backside ground plane with thermal vias. Provide ground plane routing on multiple layers to allow the IC's heat to flow into the PCB and then spread radially from the IC. Avoid cutting the ground planes or adding vias that restrict the radial flow of heat.
7. The following components should be connected to the AGND plane.

   SS cap

   BSET resistor

   ISET resistor

   COMP resistor and capacitors

   FB resistor

   VINS resistor
8. The ACT4921 footprint should connect pins 31, 32, and 33 on the top layer. It should connect pins 28 and 29 on the top layer. It should connect pins 25, 26, 27, and 35 on the top layer. It should connect pins 9 and 10 to the exposed pad on the top layer. Refer to the evaluation kit layout for

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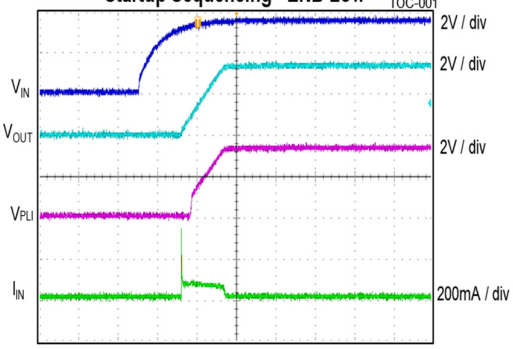
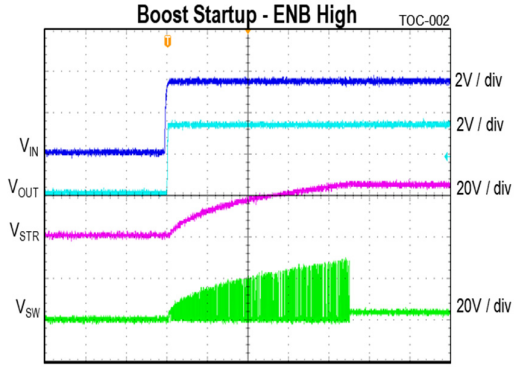
Typical Operating Characteristics

CMI 301
Startup Sequencing - ENB Low
TOC-001



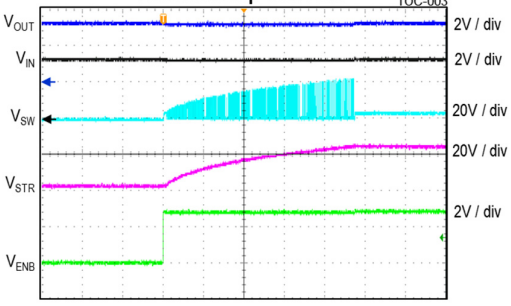
4ms / div

CMI 301
Boost Startup - ENB High
TOC-002



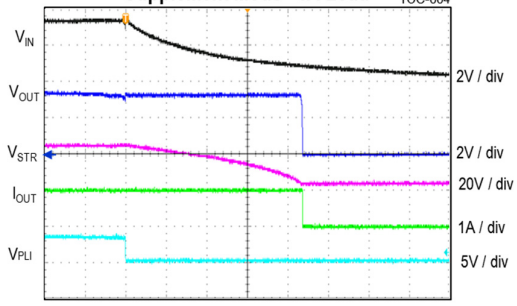
100ms / div

CMI 301
Boost Startup with ENB
TOC-003



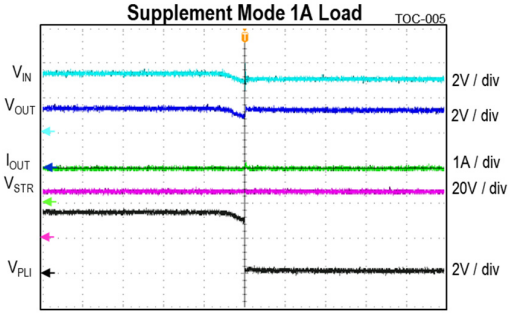
40ms / div

CMI 301
Supplement Mode - 1A Load
TOC-004



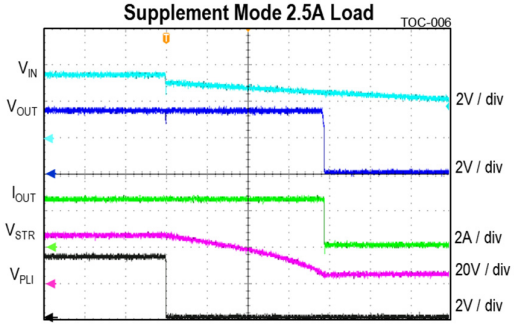
20ms / div

CMI 301
Supplement Mode 1A Load
TOC-005



200us / div

CMI 301
Supplement Mode 2.5A Load
TOC-006



10ms / div

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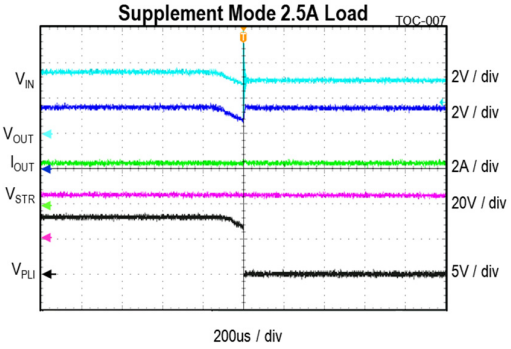
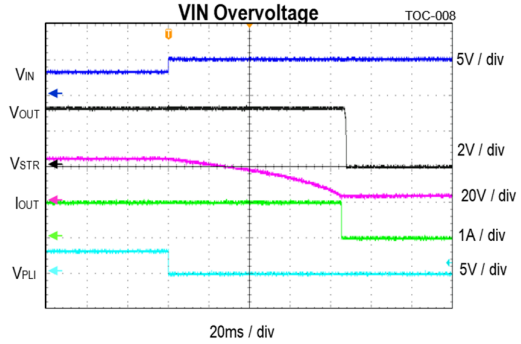
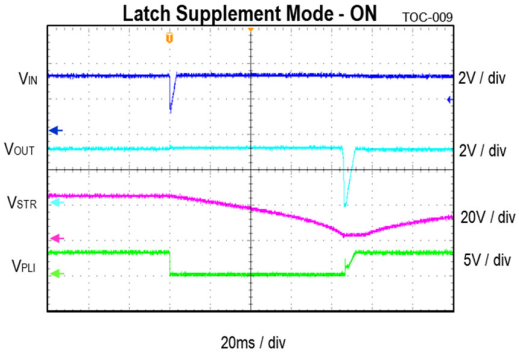
CMI 301
Supplement Mode 2.5A Load
TOC-007



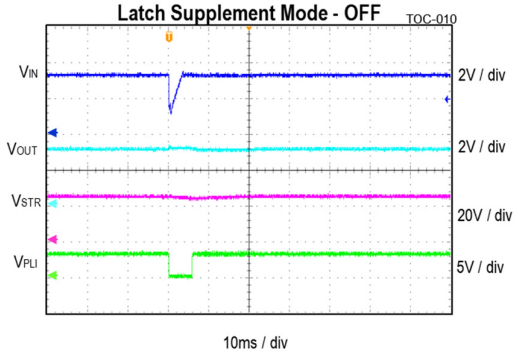
CMI 301
Supplement Mode
VIN Overvoltage
TOC-008

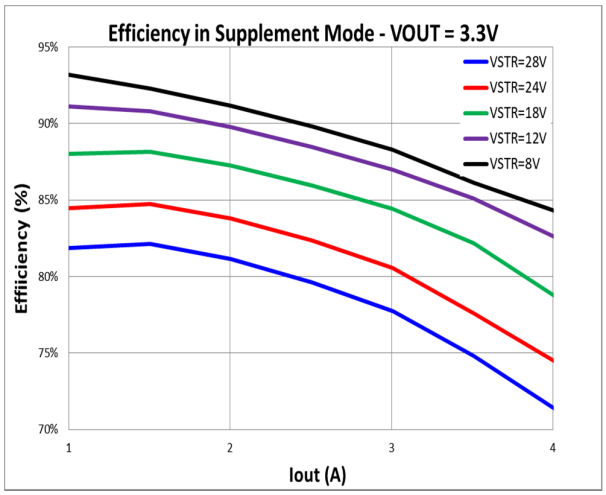


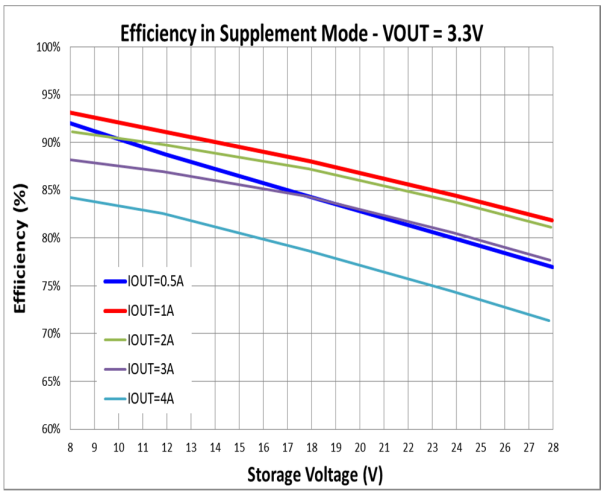
CMI 301
Latch Supplement Mode - ON
TOC-009



CMI 301
Latch Supplement Mode - OFF
TOC-010







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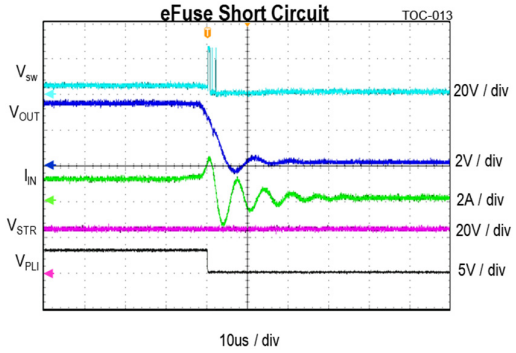
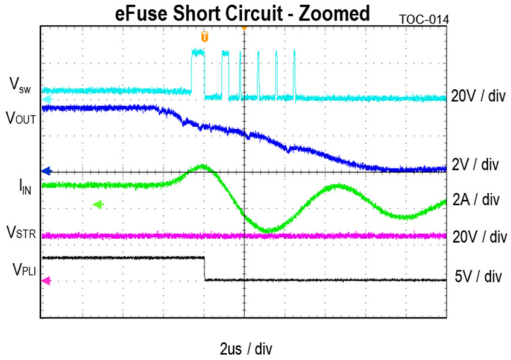
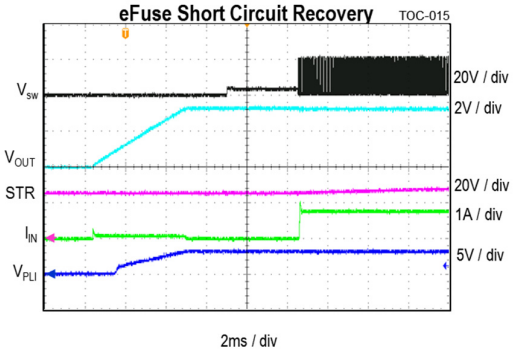
CMI 301
eFuse Short Circuit
TOC-013



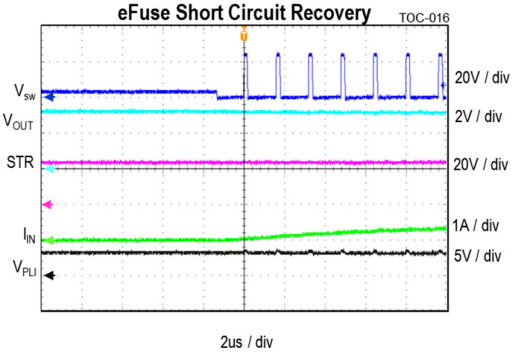
CMI 301
eFuse Short Circuit - Zoomed
TOC-014



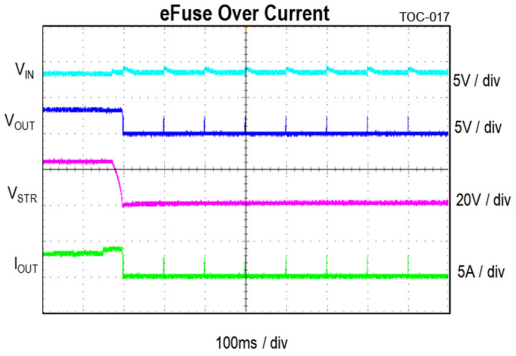
CMI 301
eFuse Short Circuit Recovery
TOC-015



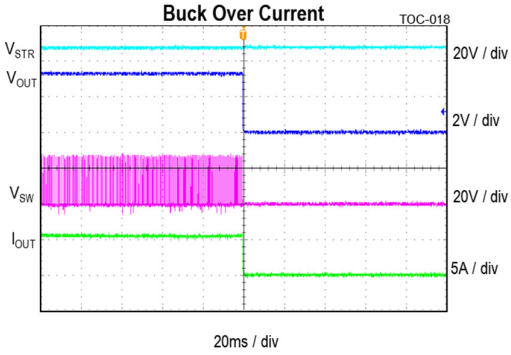
CMI 301
eFuse Short Circuit Recovery
TOC-016



CMI 301
eFuse Over Current
TOC-017



CMI 301
Buck Over Current
TOC-018



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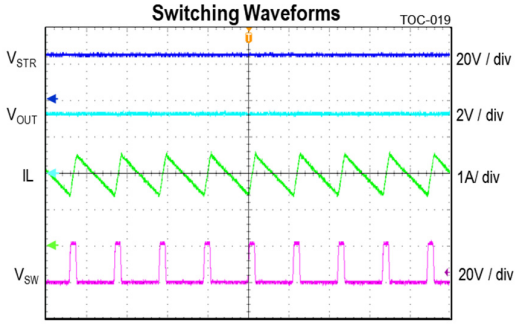
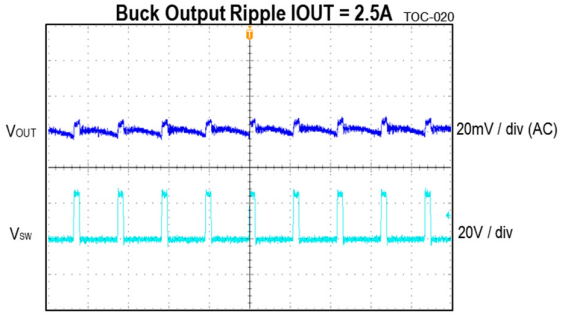
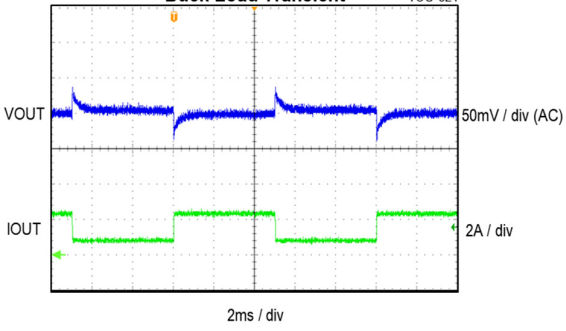
CMI 301
Switching Waveforms
TOC-019



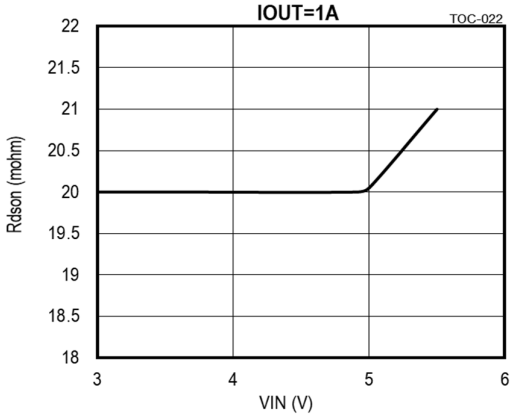
CMI 301
Buck Output Ripple IOUT = 2.5A
TOC-020



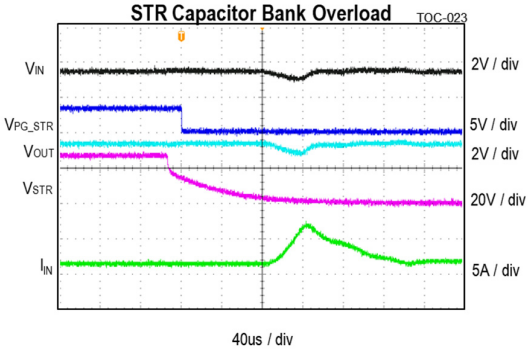
CMI 301
Buck Load Transient
TOC-021



eFuse Rdson vs VIN
IOUT=1A
TOC-022



CMI 301
STR Capacitor Bank Overload
TOC-023



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CMI OPTIONS

This section provides the basic default configuration settings for each available ACT4921 CMI option.

CMI 301: ACT4921QI301

CMI 301 is designed for standard 3.3V input applications. CMI 301 default settings are appropriate for most typical applications. It operates with a buck switching frequency of 1.125MHz to provide an optimal tradeoff between overall size and efficiency. Table 10 shows the default register settings.

Table 10: CMI 301 Default Register Settings

Function	Value	Register	Register Settings
Storage Voltage	28V	0x0Dh	BST_VSET[4:0] = 10111
Boost Current Limit	950mA	0x0Dh	BST_CLIM[1:0] = 10
Buck Switching Frequency	1125kHz	0x10h	BK_FREQ[1:0] = 01
Buck Peak Current Limit	6A	0x0Fh	BKILIM_OPT = 1
Buck Undervoltage Threshold	80%	0x0Fh	BKUV[1:0] = 10
Input Voltage Overvoltage Reference	0.82V	0x0Eh	VINS_OV_REF[2:0] = 001
Health Monitor Time	32ms	0x0Bh	HMON_TSET[3:0] = 0100
Health Monitor Threshold	95%	0x0Ch	HMON_THR[3:0] = 0000
Startup Delay	1ms	0x0Ch	EN_STARTDLY[2:0] = 001
Latch Supplement Mode	Yes	0x0Ch	EN_LATCH_SPLMNT = 1
Blocking FET Control	Pin Enabled	0x0Bh	EN_ENB_REG = 0
7-bit I^2C Address	0x5Ah	n/a	n/a
CMI Identification	0x00h	0x2Ah	CMI_ID[7:0] = 0x00h

I2C Address

The CMI 301 7-bit I2C address is 0x5Ah. This results in 0xB4h for a write address and 0xB5h for a read address.

CMI Identification

The CMI 301 CMI identification (register 0x2Ah) = 0x00h. This register can be used to distinguish between different CMI versions.

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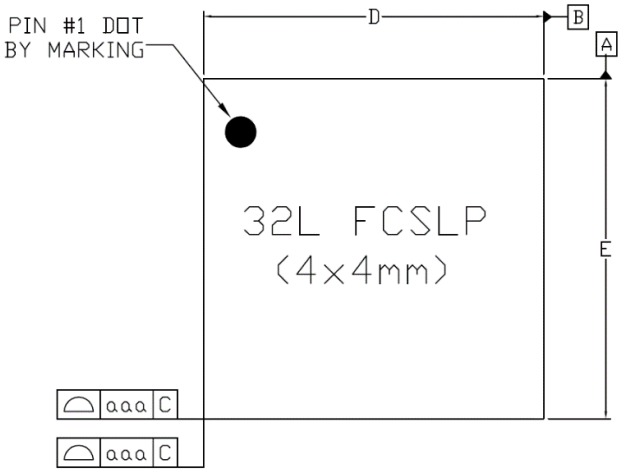
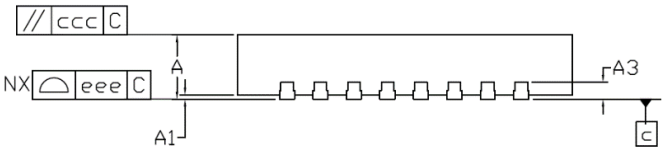
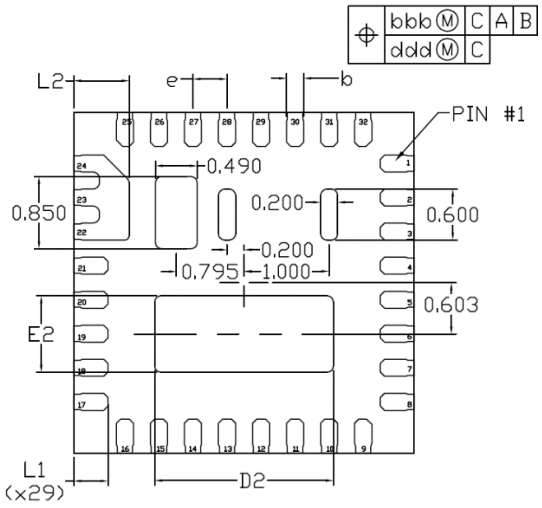
PACKAGE OUTLINE AND DIMENSIONS QFN4X4-32



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	---	---	0.050
A3	0.203 Ref.		
D	3.950	4.000	4.050
E	3.950	4.000	4.050
D2	2.050	2.100	2.150
E2	0.850	0.900	0.950
	--		
b	0.150	0.200	0.250
e	0.400 BSC		
L1	0.350	0.400	0.450
L2	0.600	0.650	0.700
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

All dimensions are in millimeters

Dimensioning and tolerancing per JEDED MO-232

See Active Semi Application note AN-104, QFN PCB Layout Guidelines for more information on generating the ACT4921 land pattern.

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