



# PCA9552

16-bit I<sup>2</sup>C-bus LED driver with programmable blink rates

Rev. 05 — 9 March 2006

Product data sheet

## 1. General description

The PCA9552 LED blinker blinks LEDs in I<sup>2</sup>C-bus and SMBus applications where it is necessary to limit bus traffic or free up the I<sup>2</sup>C-bus master's (MCU, MPU, DSP, chip set, etc.) timer. The uniqueness of this device is the internal oscillator with two programmable blink rates. To blink LEDs using normal I/O expanders like the PCF8574 or PCA9554, the bus master must send repeated commands to turn the LED on and off. This greatly increases the amount of traffic on the I<sup>2</sup>C-bus and uses up one of the master's timers. The PCA9552 LED blinker instead requires only the initial setup command to program BLINK RATE 1 and BLINK RATE 2 (that is, the frequency and duty cycle) for each individual output. From then on, only one command from the bus master is required to turn each individual open-drain output on, off, or to cycle at BLINK RATE 1 or BLINK RATE 2. Maximum output sink current is 25 mA per bit and 200 mA per package.

Any bits not used for controlling the LEDs can be used for General Purpose Parallel Input/Output (GPIO) expansion.

The active LOW hardware reset pin ( $\overline{\text{RESET}}$ ) and Power-On Reset (POR) initializes the registers to their default state, all zeroes, causing the bits to be set HIGH (LED off).

Three hardware address pins on the PCA9552 allow eight devices to operate on the same bus.

## 2. Features

- 16 LED drivers (on, off, flashing at a programmable rate)
- 2 selectable, fully programmable blink rates (frequency and duty cycle) between 0.172 Hz and 44 Hz (5.82 seconds and 0.023 seconds)
- Input/outputs not used as LED drivers can be used as regular GPIOs
- Internal oscillator requires no external components
- I<sup>2</sup>C-bus interface logic compatible with SMBus
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- Active LOW reset input
- 16 open-drain outputs directly drive LEDs to 25 mA
- Edge rate control on outputs
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 0 Hz to 400 kHz clock frequency

**PHILIPS**

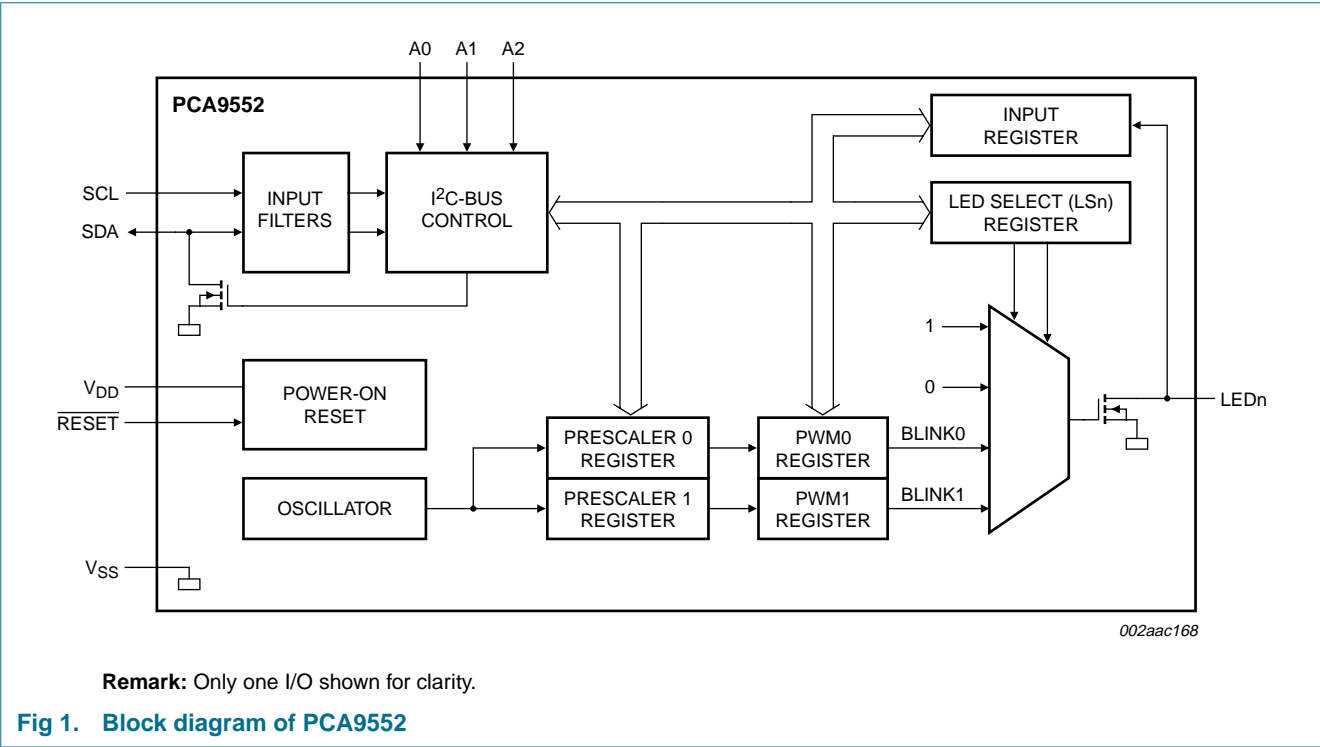
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO24, TSSOP24, HVQFN24

3. Ordering information

Table 1: Ordering information  
*T<sub>amb</sub> = -40 °C to +85 °C*

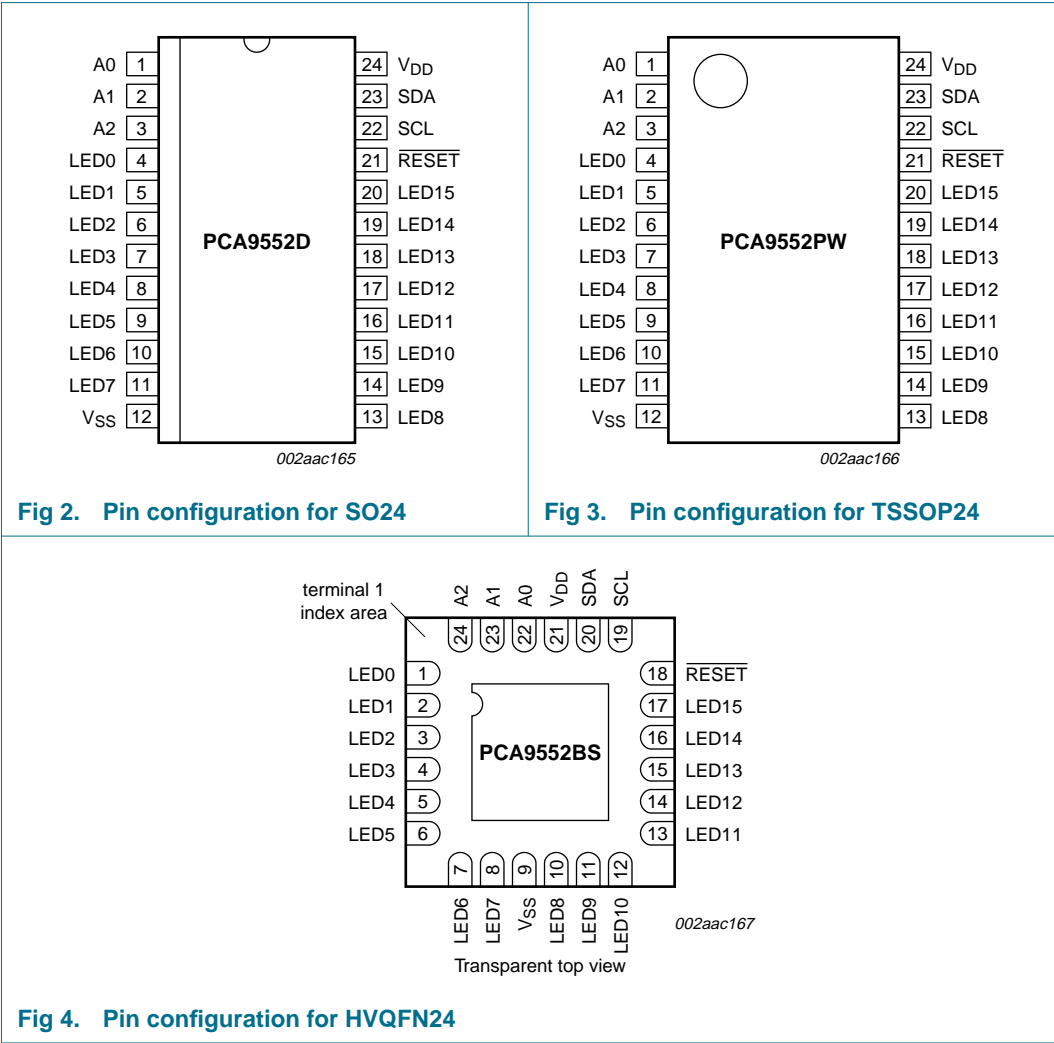
Type number	Topside mark	Package		
		Name	Description	Version
PCA9552D	PCA9552D	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
PCA9552PW	PCA9552	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
PCA9552BS	9552	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-1

4. Block diagram



5. Pinning information

5.1 Pinning



## 5.2 Pin description

Table 2: Pin description

Symbol	Pin		Description
	SO24, TSSOP24	HVQFN24	
A0	1	22	address input 0
A1	2	23	address input 1
A2	3	24	address input 2
LED0	4	1	LED driver 0
LED1	5	2	LED driver 1
LED2	6	3	LED driver 2
LED3	7	4	LED driver 3
LED4	8	5	LED driver 4
LED5	9	6	LED driver 5
LED6	10	7	LED driver 6
LED7	11	8	LED driver 7
V <sub>SS</sub>	12	9 <sup>[1]</sup>	ground supply
LED8	13	10	LED driver 8
LED9	14	11	LED driver 9
LED10	15	12	LED driver 10
LED11	16	13	LED driver 11
LED12	17	14	LED driver 12
LED13	18	15	LED driver 13
LED14	19	16	LED driver 14
LED15	20	17	LED driver 15
RESET	21	18	active LOW reset input
SCL	22	19	serial clock line
SDA	23	20	serial data line
V <sub>DD</sub>	24	21	supply voltage

[1] HVQFN package die supply ground is connected to both V<sub>SS</sub> pin and exposed center pad. V<sub>SS</sub> pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

## 6. Functional description

Refer to [Figure 1 “Block diagram of PCA9552”](#).

### 6.1 Device address

Following a START condition, the bus master must output the address of the slave it is accessing. The address of the PCA9552 is shown in [Figure 5](#). To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

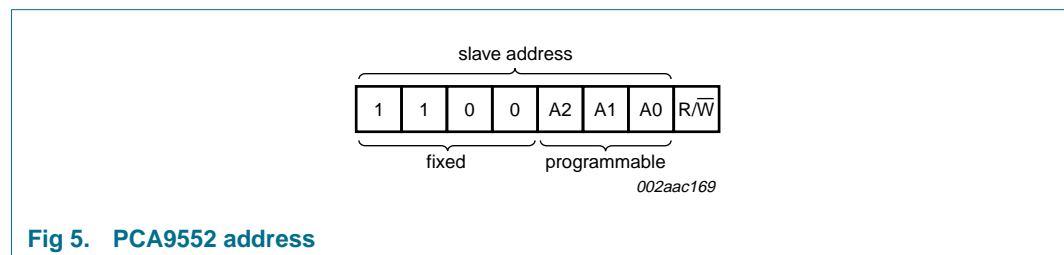


Fig 5. PCA9552 address

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

### 6.2 Control Register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9552, which will be stored in the Control Register. This register can be read and written via the I<sup>2</sup>C-bus.

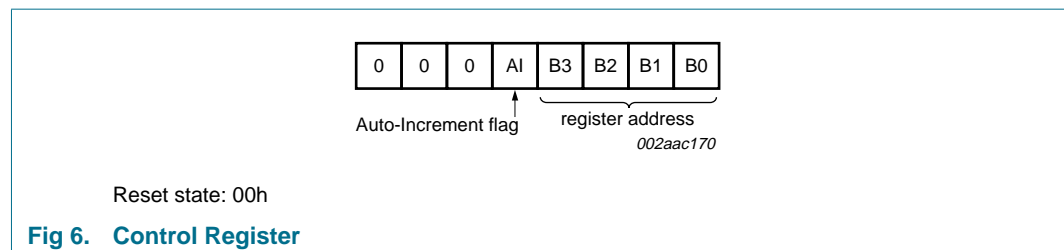


Fig 6. Control Register

The lowest 3 bits are used as a pointer to determine which register will be accessed.

If the Auto-Increment flag (AI) is set, the four low order bits of the Control Register are automatically incremented after a read or write. This allows the user to program the registers sequentially. The contents of these bits will rollover to '0000' after the last register is accessed.

When the Auto-Increment flag is set (AI = 1) and a read sequence is initiated, the sequence must start by reading a register different from '0' (B3 B2 B1 B0 ≠ 0000).

Only the 4 least significant bits are affected by the AI flag. Unused bits must be programmed with zeroes.

## 6.2.1 Control Register definition

Table 3: Register summary

B3	B2	B1	B0	Symbol	Access	Description
0	0	0	0	INPUT0	read only	input register 0
0	0	0	1	INPUT1	read only	input register 1
0	0	1	0	PSC0	read/write	frequency prescaler 0
0	0	1	1	PWM0	read/write	PWM register 0
0	1	0	0	PSC1	read/write	frequency prescaler 1
0	1	0	1	PWM1	read/write	PWM register 1
0	1	1	0	LS0	read/write	LED0 to LED3 selector
0	1	1	1	LS1	read/write	LED4 to LED7 selector
1	0	0	0	LS2	read/write	LED8 to LED11 selector
1	0	0	1	LS3	read/write	LED12 to LED15 selector

## 6.3 Register descriptions

### 6.3.1 INPUT0 - Input register 0

The Input register 0 reflects the state of the device pins (inputs LED0 to LED7). Writes to this register will be acknowledged but will have no effect.

Table 4: INPUT0 - input register 0 description

Bit	7	6	5	4	3	2	1	0
Symbol	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
Default	X	X	X	X	X	X	X	X

**Remark:** The default value 'X' is determined by the externally applied logic level (normally logic 1) when used for directly driving LED with pull-up to  $V_{DD}$ .

### 6.3.2 INPUT1 - Input register 1

The Input register 1 reflects the state of the device pins (inputs LED8 to LED15). Writes to this register will be acknowledged but will have no effect.

Table 5: INPUT1 - input register 1 description

Bit	7	6	5	4	3	2	1	0
Symbol	LED15	LED14	LED13	LED12	LED11	LED10	LED9	LED8
Default	X	X	X	X	X	X	X	X

**Remark:** The default value 'X' is determined by the externally applied logic level (normally logic 1) when used for directly driving LED with pull-up to  $V_{DD}$ .

### 6.3.3 PCS0 - Frequency Prescaler 0

PCS0 is used to program the period of the PWM output.

The period of BLINK0 = (PSC0 + 1) / 44.

**Table 6: PCS0 - Frequency Prescaler 0 register description**

Bit	7	6	5	4	3	2	1	0
Symbol	PSC0[7]	PSC0[6]	PSC0[5]	PSC0[4]	PSC0[3]	PSC0[2]	PSC0[1]	PSC0[0]
Default	1	1	1	1	1	1	1	1

### 6.3.4 PWM0 - Pulse Width Modulation 0

The PWM0 register determines the duty cycle of BLINK0. The outputs are LOW (LED off) when the count is less than the value in PWM0 and HIGH when it is greater. If PWM0 is programmed with 00h, then the PWM0 output is always LOW.

The duty cycle of BLINK0 = (256 – PWM0) / 256.

**Table 7: PWM0 - Pulse Width Modulation 0 register description**

Bit	7	6	5	4	3	2	1	0
Symbol	PWM0 [7]	PWM0 [6]	PWM0 [5]	PWM0 [4]	PWM0 [3]	PWM0 [2]	PWM0 [1]	PWM0 [0]
Default	1	0	0	0	0	0	0	0

### 6.3.5 PCS1 - Frequency Prescaler 1

PCS1 is used to program the period of the PWM output.

The period of BLINK1 = (PSC1 + 1) / 44.

**Table 8: PCS1 - Frequency Prescaler 1 register description**

Bit	7	6	5	4	3	2	1	0
Symbol	PSC1[7]	PSC1[6]	PSC1[5]	PSC1[4]	PSC1[3]	PSC1[2]	PSC1[1]	PSC1[0]
Default	1	1	1	1	1	1	1	1

### 6.3.6 PWM1 - Pulse Width Modulation 1

The PWM1 register determines the duty cycle of BLINK1. The outputs are LOW (LED off) when the count is less than the value in PWM1 and HIGH when it is greater. If PWM1 is programmed with 00h, then the PWM1 output is always LOW.

The duty cycle of BLINK1 = (256 – PWM1) / 256.

**Table 9: PWM1 - Pulse Width Modulation 1 register description**

Bit	7	6	5	4	3	2	1	0
Symbol	PWM1 [7]	PWM1 [6]	PWM1 [5]	PWM1 [4]	PWM1 [3]	PWM1 [2]	PWM1 [1]	PWM1 [0]
Default	1	0	0	0	0	0	0	0

### 6.3.7 LS0 to LS3 - LED selector registers

The LSn LED select registers determine the source of the LED data.

00 = output is set LOW (LED on)

01 = output is set high-impedance (LED off; default)

10 = output blinks at PWM0 rate

11 = output blinks at PWM1 rate

**Table 10: LS0 to LS3 - LED selector registers bit description**

Legend: \* default value

Register	Bit	Value	Description
<b>LS0 - LED0 to LED3 selector</b>			
LS0	7:6	01*	LED3 selected
	5:4	01*	LED2 selected
	3:2	01*	LED1 selected
	1:0	01*	LED0 selected
<b>LS1 - LED4 to LED7 selector</b>			
LS1	7:6	01*	LED7 selected
	5:4	01*	LED6 selected
	3:2	01*	LED5 selected
	1:0	01*	LED4 selected
<b>LS2 - LED8 to LED11 selector</b>			
LS2	7:6	01*	LED11 selected
	5:4	01*	LED10 selected
	3:2	01*	LED9 selected
	1:0	01*	LED8 selected
<b>LS3 - LED12 to LED15 selector</b>			
LS3	7:6	01*	LED15 selected
	5:4	01*	LED14 selected
	3:2	01*	LED13 selected
	1:0	01*	LED12 selected



## 6.4 Pins used as GPIOs

LED pins not used to control LEDs can be used as general purpose I/Os (GPIOs).

For use as input, set LEDn to high-impedance (01) and then read the pin state via the input register.

For use as output, connect external pull-up resistor to the pin and size it according to the DC recommended operating characteristics. LED output pin is HIGH when the output is programmed as high-impedance, and LOW when the output is programmed LOW through the 'LED selector' register. The output can be pulse-width controlled when PWM0 or PWM1 are used.

## 6.5 Power-on reset

When power is applied to  $V_{DD}$ , an internal Power-On Reset (POR) holds the PCA9552 in a reset condition until  $V_{DD}$  has reached  $V_{POR}$ . At that point, the reset condition is released and the PCA9552 registers are initialized to their default states. Thereafter,  $V_{DD}$  must be lowered below 0.2 V to reset the device.

## 6.6 External RESET

A reset can be accomplished by holding the  $\overline{\text{RESET}}$  pin LOW for a minimum of  $t_{w(\text{rst})}$ . The PCA9552 registers and I<sup>2</sup>C-bus state machine will be held in their default states until the  $\overline{\text{RESET}}$  input is once again HIGH.

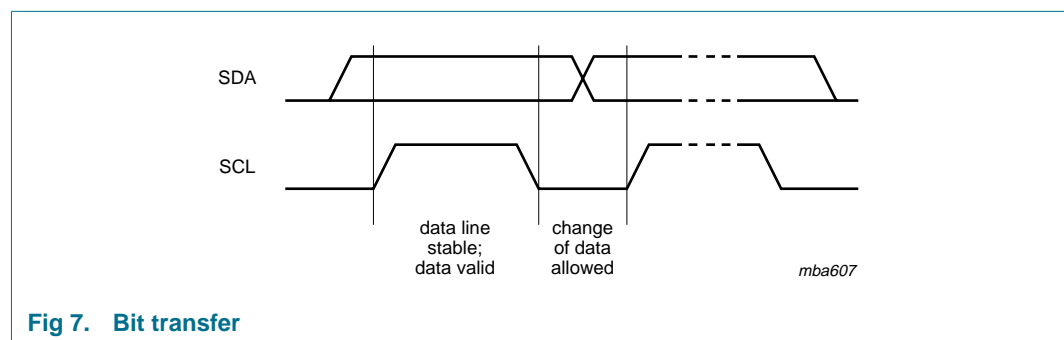
This input requires a pull-up resistor to  $V_{DD}$  if no active connection is used.

## 7. Characteristics of the I<sup>2</sup>C-bus

The I<sup>2</sup>C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

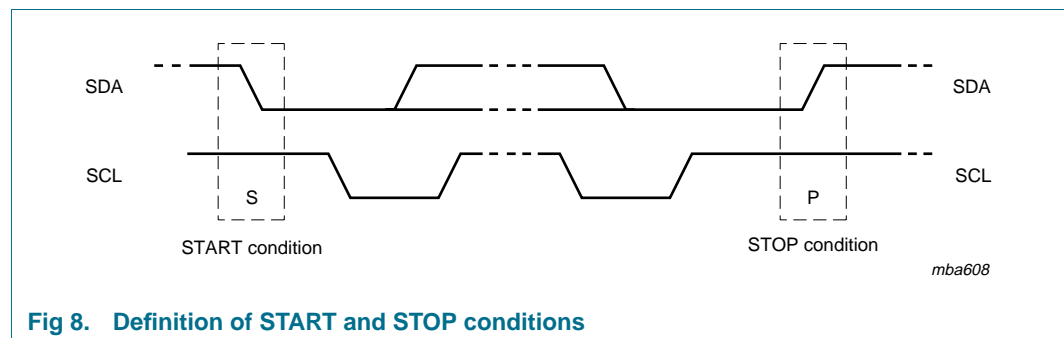
### 7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see [Figure 7](#)).



#### 7.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see [Figure 8](#).)



### 7.2 System configuration

A device generating a message is a 'transmitter'; a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see [Figure 9](#)).

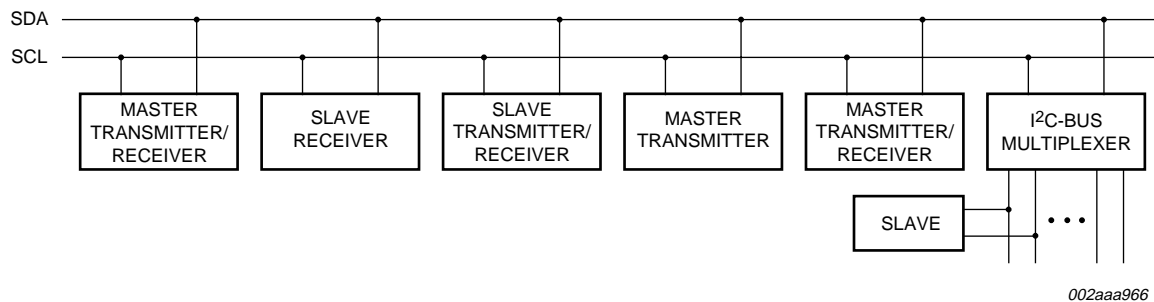


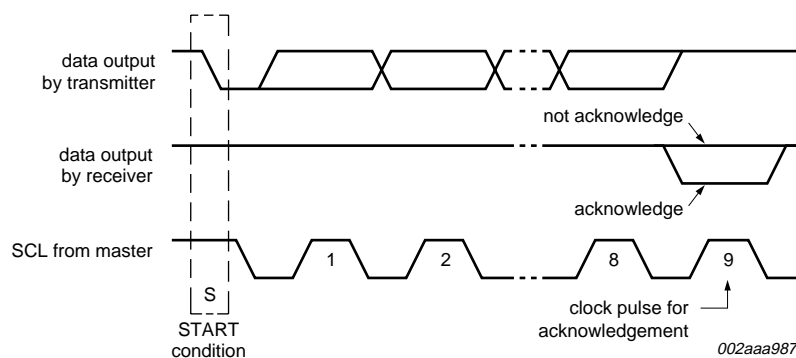
Fig 9. System configuration

### 7.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Fig 10. Acknowledgement on the I<sup>2</sup>C-bus

## 7.4 Bus transactions

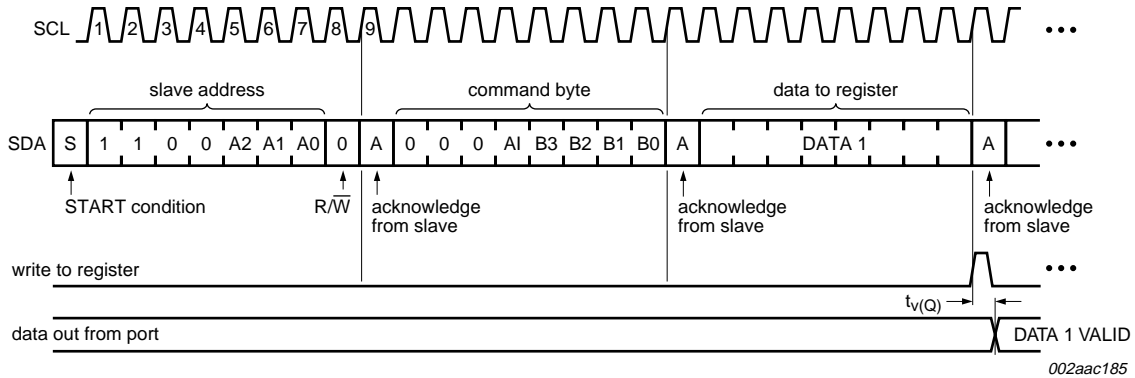


Fig 11. Write to register

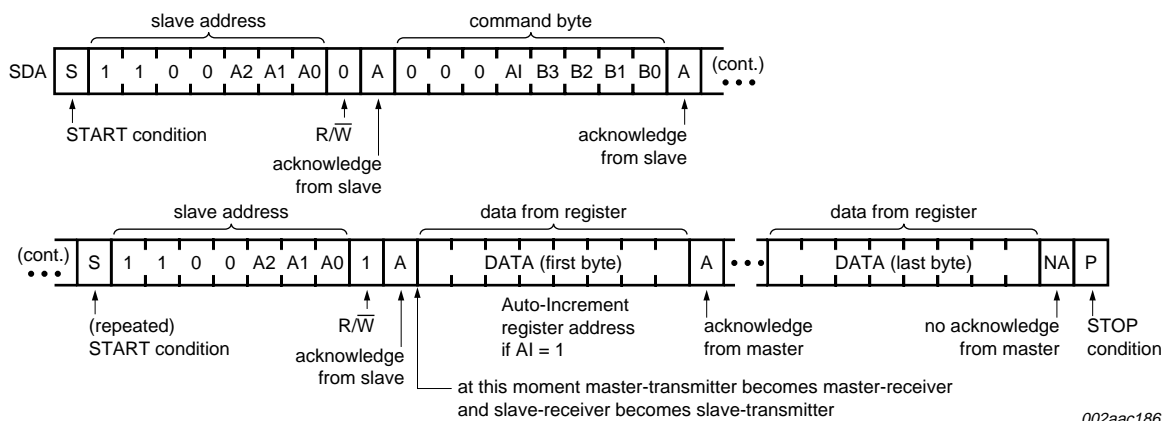
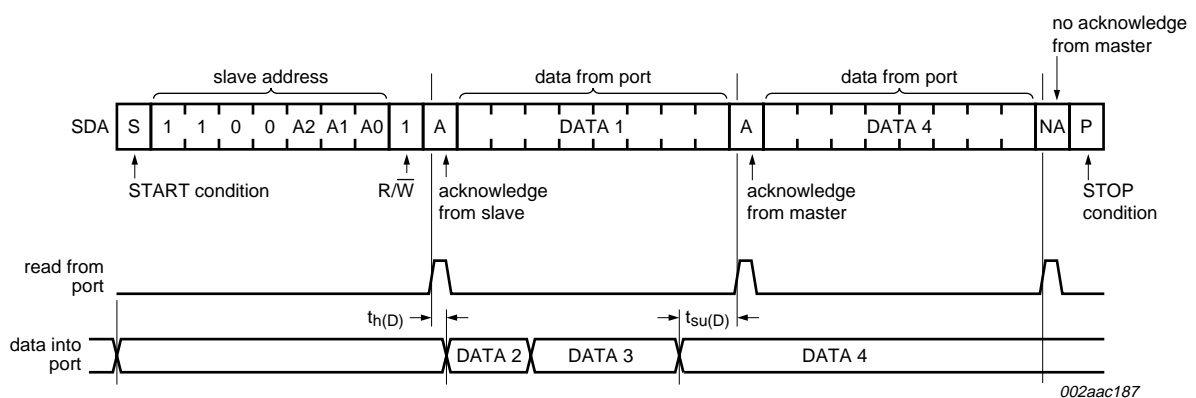


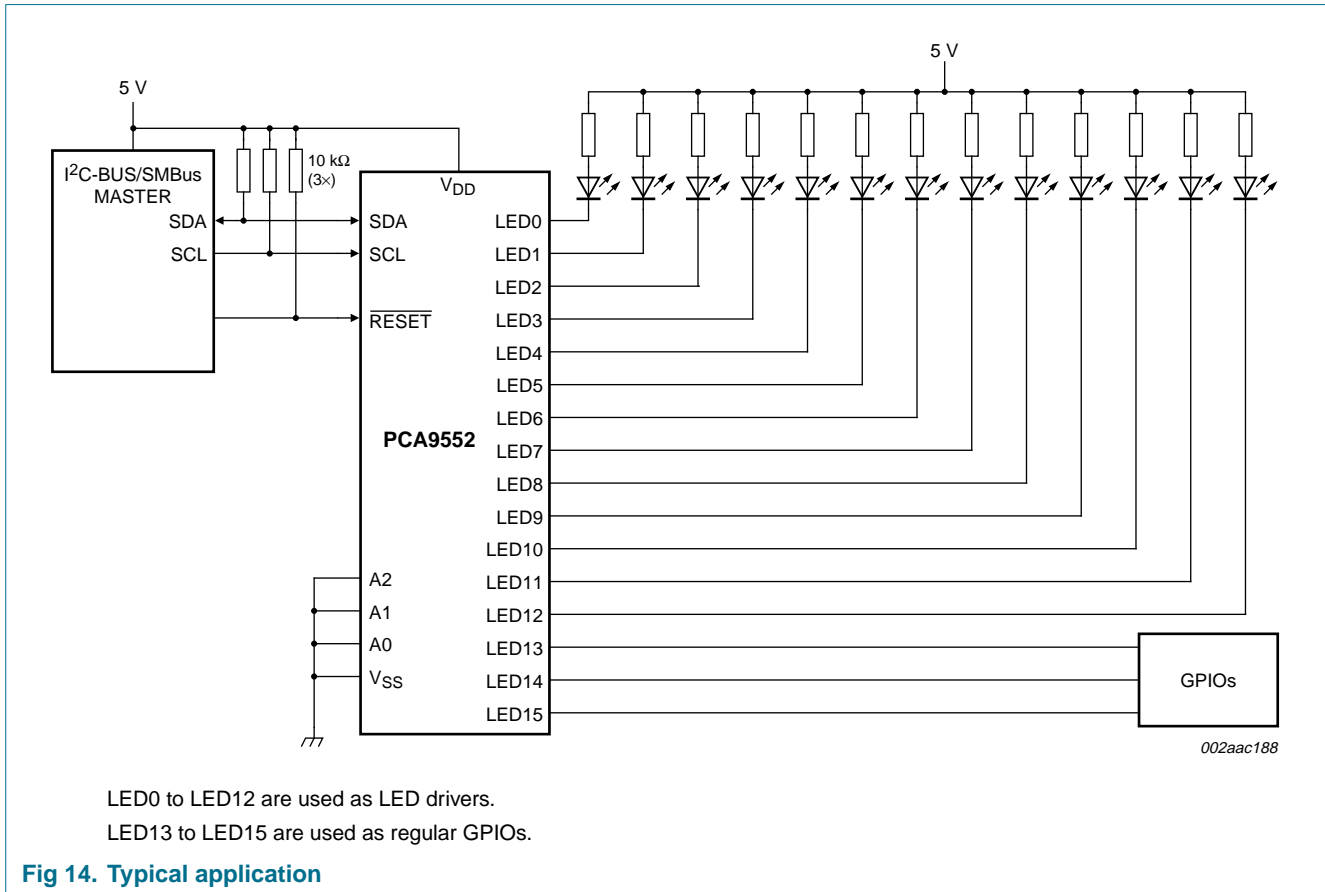
Fig 12. Read from register



**Remark:** This figure assumes the command byte has previously been programmed with 00h.

Fig 13. Read Input Port register

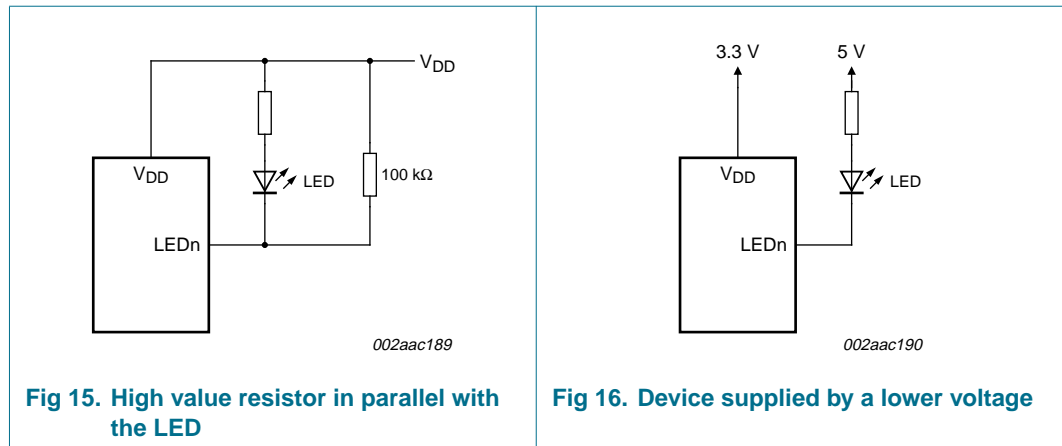
## 8. Application design-in information



### 8.1 Minimizing $I_{DD}$ when the I/O is used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to  $V_{DD}$  through a resistor as shown in [Figure 15](#). Since the LED acts as a diode, when the LED is off the I/O  $V_I$  is about 1.2 V less than  $V_{DD}$ . The supply current,  $I_{DD}$ , increases as  $V_I$  becomes lower than  $V_{DD}$  and is specified as  $\Delta I_{stb}$  in [Table 13 "Static characteristics"](#).

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to  $V_{DD}$  when the LED is off. [Figure 15](#) shows a high value resistor in parallel with the LED. [Figure 16](#) shows  $V_{DD}$  less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the input/output  $V_I$  at or above  $V_{DD}$  and prevents additional supply current consumption when the LED is off.



## 8.2 Programming example

The following example will show how to set LED0 to LED3 on. It will then set LED4 and LED5 to blink at 1 Hz at a 50 % duty cycle. LED6 and LED7 will be set to blink at 4 Hz and at a 25 % duty cycle. LED8 to LED15 will be set to off.

**Table 11: Programming PCA9552**

Program sequence	I <sup>2</sup> C-bus
START	S
PCA9552 address with A0 to A2 = LOW	C0h
PSC0 subaddress + Auto-Increment	12h
Set prescaler PSC0 to achieve a period of 1 second:	2Bh
$\text{Blink period} = 1 = \frac{\text{PSC0} + 1}{44}$	
PSC0 = 43	
Set PWM0 duty cycle to 50 %:	80h
$\frac{256 - \text{PWM0}}{256} = 0.5$	
PWM0 = 128	
Set prescaler PCS1 to achieve a period of 0.25 seconds:	0Ah
$\text{Blink period} = 0.25 = \frac{\text{PSC1} + 1}{44}$	
PSC1 = 10	
Set PWM1 output duty cycle to 25 %:	C0h
$\frac{256 - \text{PWM1}}{256} = 0.25$	
PWM1 = 192	
Set LED0 to LED3 on	00h
Set LED4 and LED5 to PWM0, and LED6 or LED7 to PWM1	FAh
Set LED8 to LED11 off	55h
Set LED12 to LED15 off	55h
STOP	P

## 9. Limiting values

**Table 12: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		−0.5	+6.0	V
V <sub>I/O</sub>	voltage on an input/output pin	LEDn used as an I/O	V <sub>SS</sub> − 0.5	5.5	V
I <sub>O(LEDn)</sub>	output current on pin LEDn	LEDn used as an I/O	-	±25	mA
I <sub>SS</sub>	ground supply current		-	200	mA
P <sub>tot</sub>	total power dissipation		-	400	mW
T <sub>stg</sub>	storage temperature		−65	+150	°C
T <sub>amb</sub>	ambient temperature	operating	−40	+85	°C

## 10. Static characteristics

**Table 13: Static characteristics**

V<sub>DD</sub> = 2.3 V to 5.5 V; V<sub>SS</sub> = 0 V; T<sub>amb</sub> = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
<b>Supply</b>						
V <sub>DD</sub>	supply voltage		2.3	-	5.5	V
I <sub>DD</sub>	supply current	Operating mode; V <sub>DD</sub> = 5.5 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; f <sub>SCL</sub> = 100 kHz	-	350	550	μA
I <sub>stb</sub>	standby current	Standby mode; V <sub>DD</sub> = 5.5 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; f <sub>SCL</sub> = 0 kHz	-	2.1	5.0	μA
ΔI <sub>stb</sub>	additional standby current	Standby mode; V <sub>DD</sub> = 5.5 V; every LED I/O at V <sub>I</sub> = 4.3 V; f <sub>SCL</sub> = 0 kHz	-	-	2	mA
V <sub>POR</sub>	power-on reset voltage <sup>[2]</sup>	V <sub>DD</sub> = 3.3 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-	1.7	2.2	V
<b>Input SCL; input/output SDA</b>						
V <sub>IL</sub>	LOW-level input voltage		−0.5	-	0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	-	5.5	V
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V	3	6.5	-	mA
I <sub>L</sub>	leakage current	V <sub>I</sub> = V <sub>DD</sub> = V <sub>SS</sub>	−1	-	+1	μA
C <sub>i</sub>	input capacitance	V <sub>I</sub> = V <sub>SS</sub>	-	4.4	5	pF
<b>I/Os</b>						
V <sub>IL</sub>	LOW-level input voltage		−0.5	-	0.8	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	5.5	V
I <sub>OL</sub>	LOW-level output current	V <sub>OL</sub> = 0.4 V; V <sub>DD</sub> = 2.3 V	<sup>[3]</sup> 9	-	-	mA
		V <sub>OL</sub> = 0.4 V; V <sub>DD</sub> = 3.0 V	<sup>[3]</sup> 12	-	-	mA
		V <sub>OL</sub> = 0.4 V; V <sub>DD</sub> = 5.0 V	<sup>[3]</sup> 15	-	-	mA
		V <sub>OL</sub> = 0.7 V; V <sub>DD</sub> = 2.3 V	<sup>[3]</sup> 15	-	-	mA
		V <sub>OL</sub> = 0.7 V; V <sub>DD</sub> = 3.0 V	<sup>[3]</sup> 20	-	-	mA
		V <sub>OL</sub> = 0.7 V; V <sub>DD</sub> = 5.0 V	<sup>[3]</sup> 25	-	-	mA
I <sub>LI</sub>	input leakage current	V <sub>DD</sub> = 3.6 V; V <sub>I</sub> = 0 V or V <sub>DD</sub>	−1	-	+1	μA
C <sub>io</sub>	input/output capacitance		-	2.6	5	pF

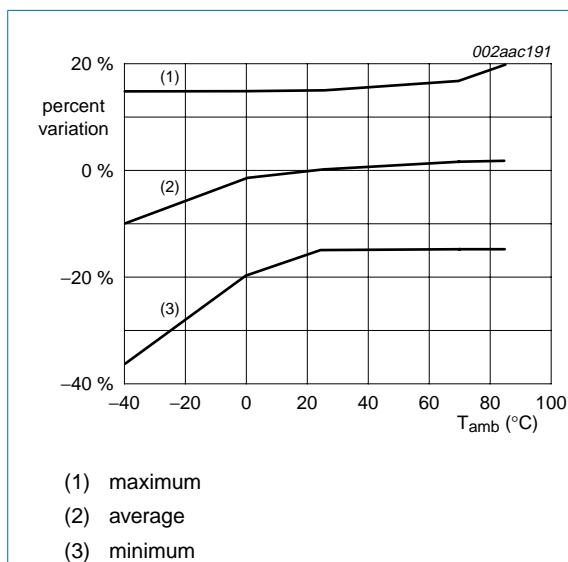
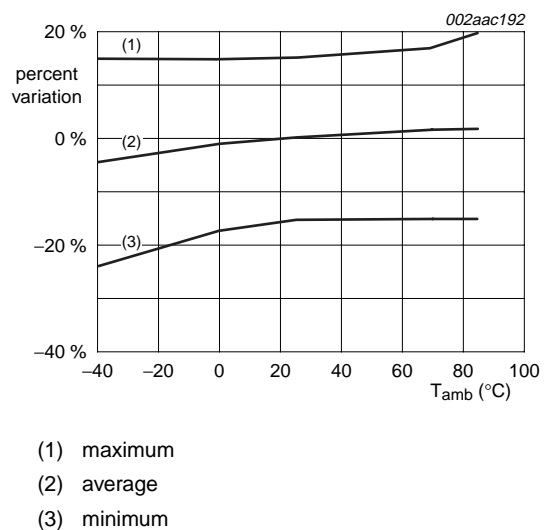
**Table 13: Static characteristics ...continued** $V_{DD} = 2.3 \text{ V to } 5.5 \text{ V}$ ;  $V_{SS} = 0 \text{ V}$ ;  $T_{amb} = -40^\circ\text{C to } +85^\circ\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
<b>Select inputs A0, A1, A2; RESET</b>						
$V_{IL}$	LOW-level input voltage		-0.5	-	0.8	V
$V_{IH}$	HIGH-level input voltage		2.0	-	5.5	V
$I_{LI}$	input leakage current		-1	-	+1	$\mu\text{A}$
$C_i$	input capacitance	$V_I = V_{SS}$	-	2.3	5	pF

[1] All typical values at 3.3 V and 25 °C.

[2]  $V_{DD}$  must be lowered to 0.2 V in order to reset part.

[3] Each I/O must be externally limited to a maximum of 25 mA and each octal ([LED0 to LED7] and [LED8 to LED15]) must be limited to a maximum current of 100 mA for a device total of 200 mA.

**Fig 17. Typical frequency variation over process at  $V_{DD} = 2.3 \text{ V to } 3.0 \text{ V}$** **Fig 18. Typical frequency variation over process at  $V_{DD} = 3.0 \text{ V to } 5.5 \text{ V}$**



## 11. Dynamic characteristics

Table 14: Dynamic characteristics

Symbol	Parameter	Conditions	Standard mode I <sup>2</sup> C-bus		Fast mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
f <sub>SCL</sub>	SCL clock frequency		0	100	0	400	kHz
t <sub>BUF</sub>	bus free time between a STOP and START condition		4.7	-	1.3	-	μs
t <sub>HD;STA</sub>	hold time (repeated) START condition		4.0	-	0.6	-	μs
t <sub>SU;STA</sub>	set-up time for a repeated START condition		4.7	-	0.6	-	μs
t <sub>SU;STO</sub>	set-up time for STOP condition		4.0	-	0.6	-	μs
t <sub>HD;DAT</sub>	data hold time		0	-	0	-	ns
t <sub>VD;ACK</sub>	data valid acknowledge time		[1]	-	600	-	ns
t <sub>VD;DAT</sub>	data valid time	LOW-level	[2]	-	600	-	ns
		HIGH-level	[2]	-	1500	-	ns
t <sub>SU;DAT</sub>	data set-up time		250	-	100	-	ns
t <sub>LOW</sub>	LOW period of the SCL clock		4.7	-	1.3	-	μs
t <sub>HIGH</sub>	HIGH period of the SCL clock		4.0	-	0.6	-	μs
t <sub>f</sub>	fall time of both SDA and SCL signals		-	300	20 + 0.1C <sub>b</sub> [3]	300	ns
t <sub>r</sub>	rise time of both SDA and SCL signals		-	1000	20 + 0.1C <sub>b</sub> [3]	300	ns
t <sub>SP</sub>	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
<b>Port timing</b>							
t <sub>V(Q)</sub>	data output valid time		-	250	-	250	ns
t <sub>SU(D)</sub>	data input setup time		100	-	100	-	ns
t <sub>H(D)</sub>	data input hold time		1	-	1	-	μs
<b>Reset</b>							
t <sub>w(rst)</sub>	reset pulse width		10	-	10	-	ns
t <sub>rec(rst)</sub>	reset recovery time		0	-	0	-	ns
t <sub>rst</sub>	reset time	[4] [5]	400	-	400	-	ns

[1] t<sub>VD;ACK</sub> = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] t<sub>VD;DAT</sub> = minimum time for SDA data out to be valid following SCL LOW.

[3] C<sub>b</sub> = total capacitance of one bus line in pF.

[4] Resetting the device while actively communicating on the bus may cause glitches or errant STOP conditions.

[5] Upon reset, the full delay will be the sum of t<sub>rst</sub> and the RC time constant of the SDA bus.

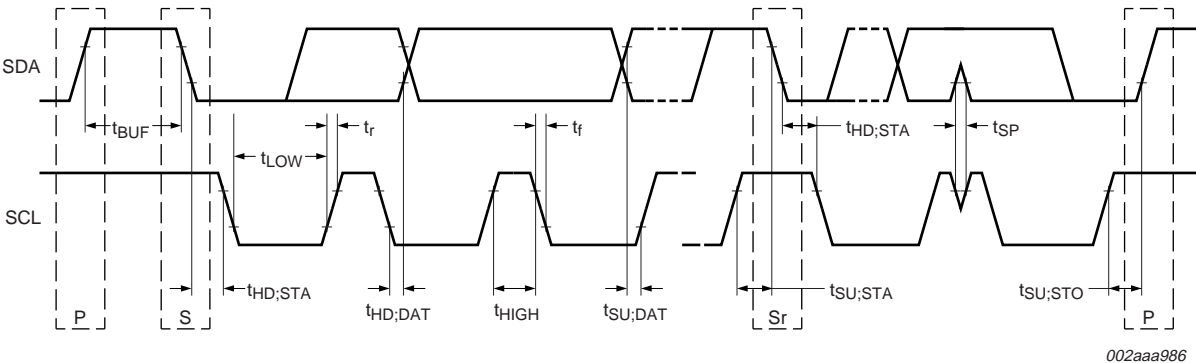
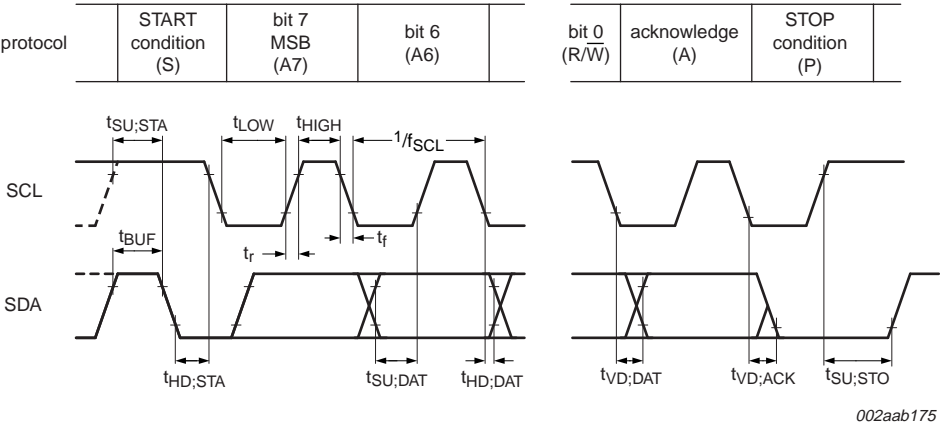


Fig 19. Definition of timing on the I<sup>2</sup>C-bus



Rise and fall times refer to  $V_{IL}$  and  $V_{IH}$ .

Fig 20. I<sup>2</sup>C-bus timing diagram

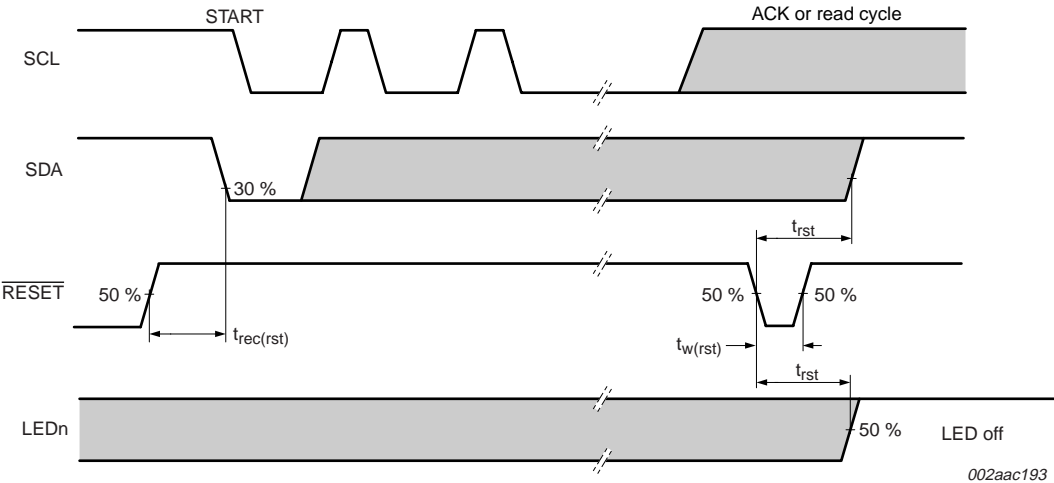
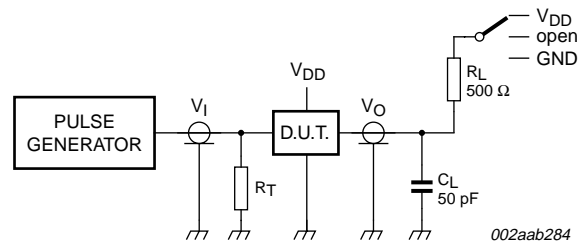


Fig 21. Reset timing

## 12. Test information



$R_L$  = load resistor for LEDn.  $R_L$  for SDA and SCL > 1 kΩ (3 mA or less current)

$C_L$  = load capacitance includes jig and probe capacitance

$R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generators.

**Fig 22. Test circuitry for switching times**

13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

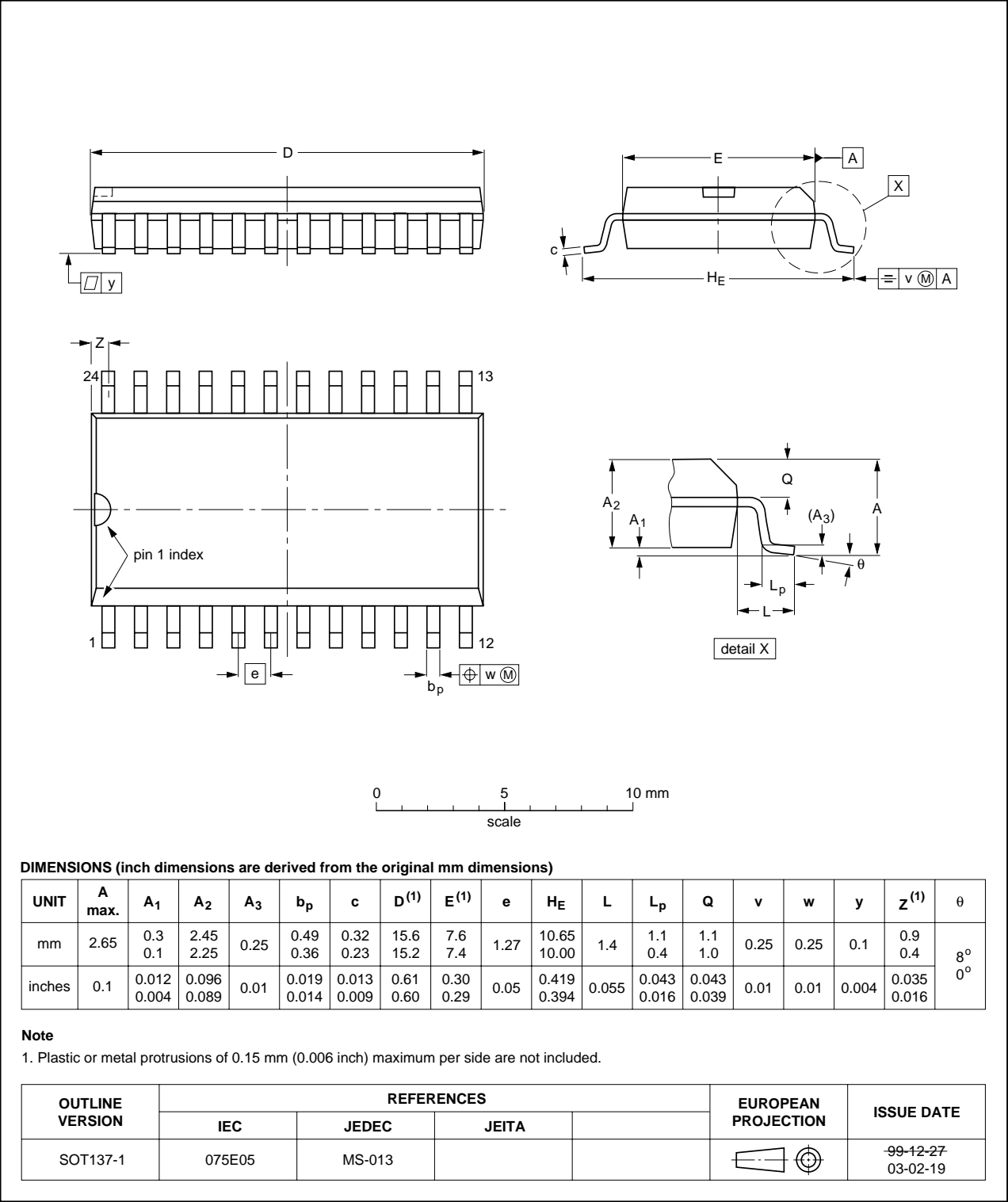


Fig 23. Package outline SOT137-1 (SO24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

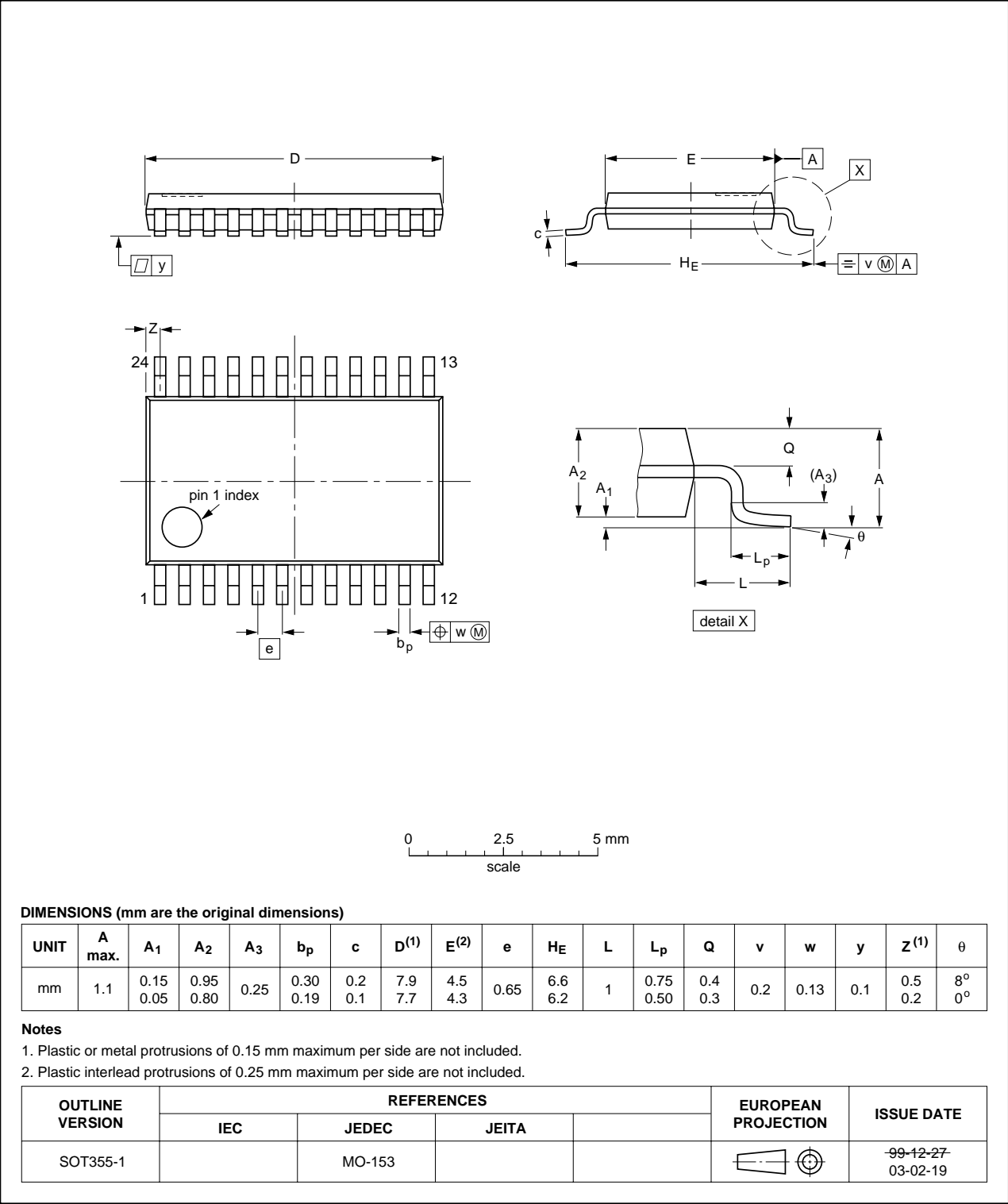


Fig 24. Package outline SOT355-1 (TSSOP24)

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads;  
24 terminals; body 4 x 4 x 0.85 mm

SOT616-1

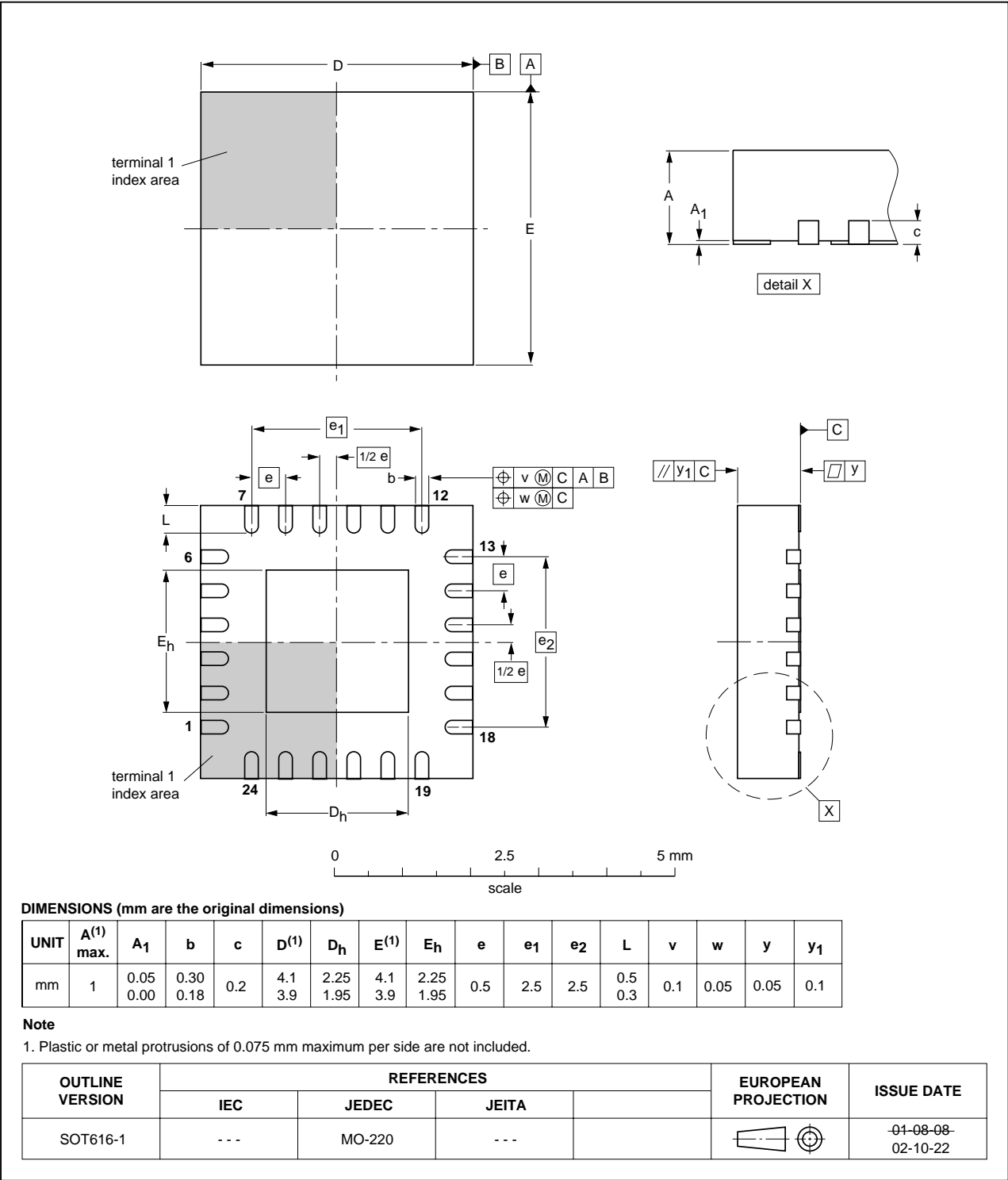


Fig 25. Package outline SOT616-1 (HVQFN24)

## 14. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

## 15. Soldering

### 15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

### 15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness  $\geq 2.5$  mm
  - for packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

### 15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

## 15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

## 15.5 Package related soldering information

**Table 15: Suitability of surface mount IC packages for wave and reflow soldering methods**

Package <sup>[1]</sup>	Soldering method	
	Wave	Reflow <sup>[2]</sup>
BGA, HTSSON..T <sup>[3]</sup> , LBGA, LFBGA, SQFP, SSOP..T <sup>[3]</sup> , TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable <sup>[4]</sup>	suitable
PLCC <sup>[5]</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>[5]</sup> <sup>[6]</sup>	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended <sup>[7]</sup>	suitable
CWQCCN..L <sup>[8]</sup> , PMFP <sup>[9]</sup> , WQCCN..L <sup>[8]</sup>	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.



- [2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.
- [3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding  $217\text{ }^{\circ}\text{C} \pm 10\text{ }^{\circ}\text{C}$  measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a  $45^{\circ}$  angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.

## 16. Abbreviations

Table 16: Abbreviations

Acronym	Description
CDM	Charged Device Model
DSP	Digital Signal Processor
ESD	ElectroStatic Discharge
HBM	Human Body Model
GPIO	General Purpose Input/Output
IC	Integrated Circuit
I <sup>2</sup> C-bus	Inter IC bus
LED	Light Emitting Diode
MCU	Microcontroller
MM	Machine Model
MPU	Microprocessor
POR	Power-On Reset
PWM	Pulse Width Modulation
SMBus	System Management Bus

## 17. Revision history

Table 17: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PCA9552_5	20060309	Product data sheet	-	-	PCA9552_4
Modifications: <ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.</li> <li><a href="#">Table 1 "Ordering information"</a>: changed Topside mark of TSSOP24 package from 'PCA9552PW' to 'PCA9552'</li> <li><a href="#">Table 2 "Pin description"</a>: added <a href="#">Table note 1</a> regarding V<sub>SS</sub> pin on HVQFN24 package</li> <li><a href="#">Section 6.6 "External RESET"</a>: changed symbol "t<sub>W</sub>" to "t<sub>W(rst)</sub>"</li> <li><a href="#">Figure 11</a>: changed symbol "t<sub>pV</sub>" to "t<sub>V(Q)</sub>"</li> <li><a href="#">Figure 13</a>: changed symbol "t<sub>ph</sub>" to "t<sub>h(D)</sub>"; changed symbol "t<sub>ps</sub>" to "t<sub>su(D)</sub>"</li> <li><a href="#">Section 8.1 "Minimizing I<sub>DD</sub> when the I/O is used to control LEDs"</a>:               <ul style="list-style-type: none"> <li>1st paragraph, 3rd sentence: changed symbol "ΔI<sub>DD</sub>" to "ΔI<sub>stb</sub>"</li> <li>2nd paragraph, 4th sentence: changed symbol "V<sub>IN</sub>" to "V<sub>I</sub>"</li> </ul> </li> <li><a href="#">Table 12 "Limiting values"</a>:               <ul style="list-style-type: none"> <li>changed parameter description of V<sub>I/O</sub> from "DC voltage on an I/O" to "voltage on an input/output pin"</li> <li>changed symbol "I<sub>I/O</sub> (DC output current on an I/O)" to 'I<sub>O(LEDn)</sub> (output current on pin LEDn)</li> </ul> </li> <li><a href="#">Table 13 "Static characteristics"</a>:               <ul style="list-style-type: none"> <li>moved second sentence of description below title to (new) <a href="#">Table note 1</a> and added its reference at column "Typ"</li> <li>changed symbol "ΔI<sub>DD</sub>" to "ΔI<sub>stb</sub>"</li> <li>under subsection "I/Os", changed symbol "I<sub>L</sub>" to "I<sub>LI</sub>"</li> </ul> </li> <li><a href="#">Table 14 "Dynamic characteristics"</a>:               <ul style="list-style-type: none"> <li>updated parameter descriptions</li> <li>under subsection "Port timing": changed symbol "t<sub>pV</sub>" to "t<sub>V(Q)</sub>"; changed symbol "t<sub>ps</sub>" to "t<sub>su(D)</sub>"; changed symbol "t<sub>ph</sub>" to "t<sub>h(D)</sub>"</li> <li>under subsection "Reset": changed symbol "t<sub>W</sub>" to "t<sub>W(rst)</sub>"; changed symbol "t<sub>REC</sub>" to "t<sub>rec(rst)</sub>"; changed symbol "t<sub>RESET</sub>" to "t<sub>rst</sub>" (also in <a href="#">Table note 5</a>)</li> </ul> </li> <li><a href="#">Figure 21 "Reset timing"</a> modified to harmonize letter symbols</li> </ul>					
PCA9552_4	20041001	Product data sheet	-	9397 750 13727	PCA9552_3
PCA9552_3	20030502	Product data	853-2374 29857 of 2003 Apr 24	9397 750 11463	PCA9552_2
PCA9552_2	20030224	Product data	853-2374 29331 of 2002 Dec 20	9397 750 11156	PCA9552_1
PCA9552_1	20020927	Product data	853-2374 28878 of 2002 Sep 09	9397 750 10329	-

## 18. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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## 23. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>	<b>16</b>	<b>Abbreviations</b> .....	<b>25</b>
<b>2</b>	<b>Features</b> .....	<b>1</b>	<b>17</b>	<b>Revision history</b> .....	<b>26</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>	<b>18</b>	<b>Data sheet status</b> .....	<b>27</b>
<b>4</b>	<b>Block diagram</b> .....	<b>2</b>	<b>19</b>	<b>Definitions</b> .....	<b>27</b>
<b>5</b>	<b>Pinning information</b> .....	<b>3</b>	<b>20</b>	<b>Disclaimers</b> .....	<b>27</b>
5.1	Pinning .....	3	<b>21</b>	<b>Trademarks</b> .....	<b>27</b>
5.2	Pin description .....	4	<b>22</b>	<b>Contact information</b> .....	<b>27</b>
<b>6</b>	<b>Functional description</b> .....	<b>5</b>			
6.1	Device address .....	5			
6.2	Control Register .....	5			
6.2.1	Control Register definition .....	6			
6.3	Register descriptions .....	6			
6.3.1	INPUT0 - Input register 0 .....	6			
6.3.2	INPUT1 - Input register 1 .....	6			
6.3.3	PCS0 - Frequency Prescaler 0 .....	7			
6.3.4	PWM0 - Pulse Width Modulation 0 .....	7			
6.3.5	PCS1 - Frequency Prescaler 1 .....	7			
6.3.6	PWM1 - Pulse Width Modulation 1 .....	7			
6.3.7	LS0 to LS3 - LED selector registers .....	8			
6.4	Pins used as GPIOs .....	9			
6.5	Power-on reset .....	9			
6.6	External RESET .....	9			
<b>7</b>	<b>Characteristics of the I<sup>2</sup>C-bus</b> .....	<b>10</b>			
7.1	Bit transfer .....	10			
7.1.1	START and STOP conditions .....	10			
7.2	System configuration .....	10			
7.3	Acknowledge .....	11			
7.4	Bus transactions .....	12			
<b>8</b>	<b>Application design-in information</b> .....	<b>13</b>			
8.1	Minimizing I <sub>DD</sub> when the I/O is used to control LEDs .....	13			
8.2	Programming example .....	14			
<b>9</b>	<b>Limiting values</b> .....	<b>15</b>			
<b>10</b>	<b>Static characteristics</b> .....	<b>15</b>			
<b>11</b>	<b>Dynamic characteristics</b> .....	<b>17</b>			
<b>12</b>	<b>Test information</b> .....	<b>19</b>			
<b>13</b>	<b>Package outline</b> .....	<b>20</b>			
<b>14</b>	<b>Handling information</b> .....	<b>23</b>			
<b>15</b>	<b>Soldering</b> .....	<b>23</b>			
15.1	Introduction to soldering surface mount packages .....	23			
15.2	Reflow soldering .....	23			
15.3	Wave soldering .....	23			
15.4	Manual soldering .....	24			
15.5	Package related soldering information .....	24			

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