

2.5A SINGLE CHANNEL CURRENT-LIMITED POWER SWITCH
Description

The AP2501 and AP2511 are single channel current-limited integrated high-side power switches optimized for Universal Serial Bus (USB) and other hot-swap applications. The family of devices complies with USB standards and is available with both polarities of Enable input.

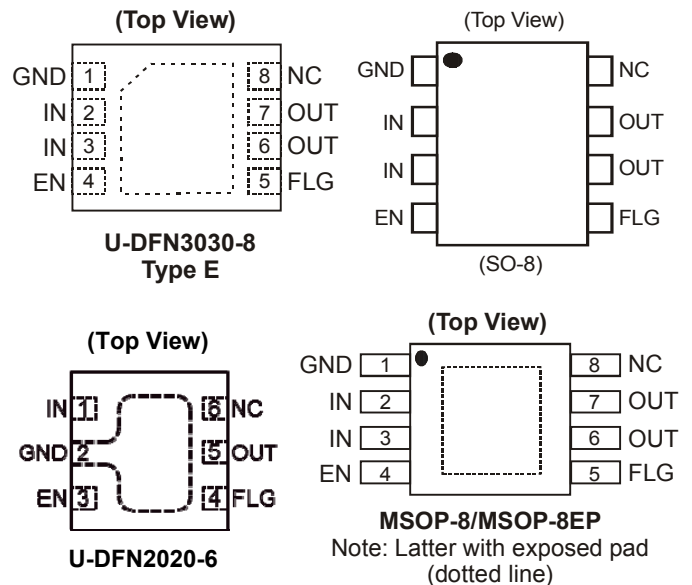
The devices have fast short-circuit response time for improved overall system robustness, and have integrated output discharge function to ensure completely controlled discharging of the output voltage capacitor. They provide a complete protection solution for applications subject to heavy capacitive loads and the prospect of short circuit, and offer reverse current blocking, over-current, over-temperature and short-circuit protection, as well as controlled rise time and under-voltage lockout functionality. A 7ms deglitch capability on the open-drain Flag output prevents false over-current reporting and does not require any external components.

All devices are available in SO-8, MSOP-8, MSOP-8EP, U-DFN3030-8 and U-DFN2020-6 packages.

Features

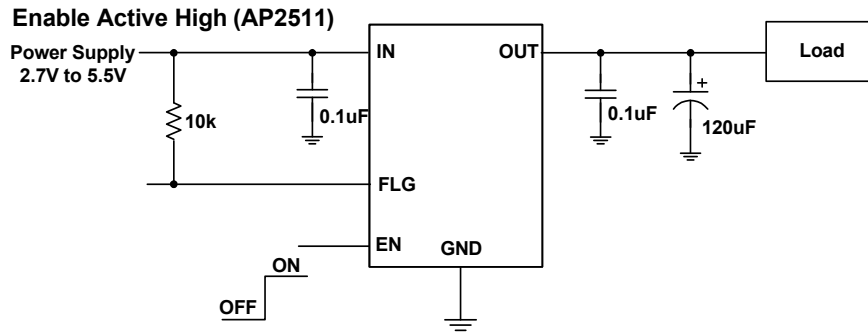
- Single channel current-limited power switch
- Output discharge function
- Fast short-circuit response time: 2 μ s
- 3.7A accurate current limiting (typ)
- Reverse current blocking
- 70m Ω on-resistance (typ)
- Input voltage range: 2.7V – 5.5V
- Built-in soft-start with 0.6ms typical rise time
- Over-current and thermal protection
- Fault report (FLG) with blanking time (7ms typ)
- ESD protection: 2kV HBM, 200V MM
- Active low (AP2501) or active high (AP2511) enable
- Ambient temperature range: -40°C to +85°C
- SO-8, MSOP-8, MSOP-8EP, U-DFN3030-8 and U-DFN2020-6: Available in "Green" Molding Compound (No Br, Sb)
 - **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
 - **Halogen and Antimony Free. "Green" Device (Note 3)**
- UL Recognized, File Number E322375
- IEC60950-1 CB Scheme Certified

- Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Assignments

Applications

- LCD TVs & Monitors
- Set-Top-Boxes, Residential Gateways
- Laptops, Desktops, Servers, e-Readers
- Printers, Docking Stations, HUBs

Typical Applications Circuit



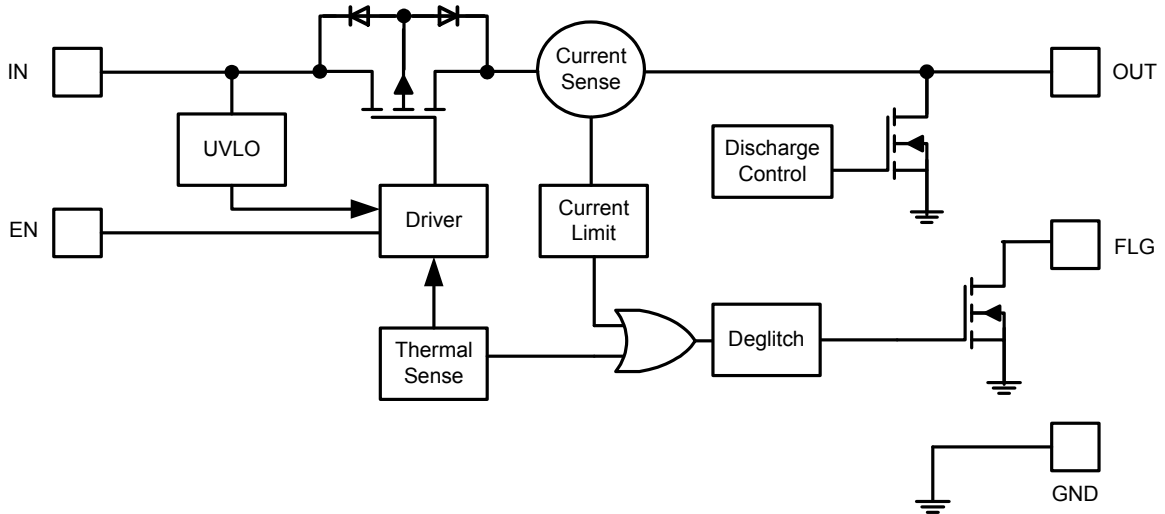
Available Options

| Part Number | Channel | Enable Pin (EN) | Recommended Maximum Continuous Load Current (A) | Typical Current Limit (A) | Package |
|-------------|---------|-----------------|---|---------------------------|-------------|
| AP2501 | 1 | Active Low | 2.5A | 3.7A | SO-8 |
| AP2511 | 1 | Active High | | | MSOP-8 |
| | | | | | MSOP-8EP |
| | | | | | U-DFN3030-8 |
| | | | | | U-DFN2020-6 |

Pin Descriptions

| Pin Name | Pin Number | | | Function |
|-------------|-----------------------|----------------|-------------|--|
| | MSOP-8EP, U-DFN3030-8 | SO-8, MSOP-8 | U-DFN2020-6 | |
| GND | 1 | 1 | 2 | Ground |
| IN | 2, 3 | 2, 3 | 1 | Voltage Input Pin. Connect a 0.1µF or larger ceramic capacitor from IN to GND as close as possible. (all IN pins must be tied together externally) |
| EN | 4 | 4 | 3 | Enable Input. Active low (AP2501) or active high (AP2511). |
| FLG | 5 | 5 | 4 | Over-temperature and over-current fault reporting with 7ms deglitch; active low open-drain output. FLG is disabled for 7ms after turn-on. |
| OUT | 6, 7 | 6, 7 | 5 | Voltage Output Pin (all OUT pins must be tied together externally) |
| NC | 8 | 8 | 6 | No internal connection; recommend tie to OUT pins. |
| Exposed Pad | Exposed Pad | Not applicable | Exposed Pad | Exposed pad. It should be externally connected to GND and thermal mass for enhanced thermal impedance. It should not be used as electrical ground conduction path. |

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

| Symbol | Parameter | Rating | Unit |
|------------------------------------|------------------------------------|--------------------------------------|------|
| ESD HBM | Human Body Model ESD Protection | 2 | kV |
| ESD MM | Machine Model ESD Protection | 200 | V |
| V _{IN} | Input Voltage (Note 4) | -0.3 to +6.5 | V |
| V _{OUT} | Output Voltage (Note 4) | -0.3 to 6.5 or V _{IN} + 0.3 | V |
| V _{EN} , V _{FLG} | Enable Voltage (Note 4) | -0.3 to 6.5 or V _{IN} + 0.3 | V |
| I _{LOAD} | Maximum Continuous Load Current | Internal Limited | A |
| T _{JMAX} | Maximum Junction Temperature | 150 | °C |
| T _{ST} | Storage Temperature Range (Note 5) | -65 to +150 | °C |

- Notes: 4. All voltages referred to GND pin. Maximums are the lower of V_{IN} + 0.3 and 6.5V
 5. UL Recognized Rating from -30°C to +70°C (Diodes qualified T_{ST} from -65°C to +150°C)

Caution: Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.

Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

| Symbol | Parameter | Min | Max | Unit |
|------------------|---|-----|-----------------|------|
| V _{IN} | Input voltage | 2.7 | 5.5 | V |
| I _{OUT} | Output Current | 0 | 2.5 | A |
| V _{IH} | High-Level Input Voltage on EN | 2.0 | V _{IN} | V |
| V _{IL} | Low-Level Input Voltage on EN | 0 | 0.8 | V |
| T _A | Operating Ambient Temperature (Note 6), | -40 | +85 | °C |

- Note: 6. T_{A(MAX)} = +70°C if V_{IN} ≤ 4.1V and I_{OUT} = 2.5A to keep device from going into thermal protection.

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, $V_{IN} = +5.0\text{V}$, $C_{IN} = 0.1\mu\text{F}$, $C_L = 1\mu\text{F}$, unless otherwise specified.)

| Symbol | Parameter | Conditions (Note 7) | Min | Typ | Max | Unit | |
|-------------------|--|---|--|------|------|---------------|--------------------|
| V_{UVLO} | Input UVLO | V_{IN} rising | 1.6 | 2.0 | 2.4 | V | |
| ΔV_{UVLO} | Input UVLO Hysteresis | V_{IN} decreasing | | 50 | | mV | |
| I_{SHDN} | Input Shutdown Current | Disabled, OUT = open | | 0.1 | 1.0 | μA | |
| I_Q | Input Quiescent Current | Enabled, OUT = open | | 60 | 100 | μA | |
| I_{LEAK} | Input Leakage Current | Disabled, OUT grounded | | 0.1 | 1.0 | μA | |
| I_{REV} | Reverse Leakage Current | Disabled, $V_{IN} = 0\text{V}$, $V_{OUT} = 5\text{V}$, I_{REV} at V_{IN} | | 0.01 | 1.00 | μA | |
| $R_{DS(ON)}$ | Switch on-resistance | $V_{IN} = 5\text{V}$, $I_{OUT} = 1\text{A}$ | $T_A = 25^\circ\text{C}$ | | 70 | 78 | m Ω |
| | | | $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ | | | 105 | |
| | | $V_{IN} = 3.3\text{V}$, $I_{OUT} = 1\text{A}$ | $T_A = 25^\circ\text{C}$ | | 90 | 108 | |
| | | | $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ | | | 135 | |
| I_{LIMIT} | Over-Load Current Limit (Note 7) | $V_{IN} = 5\text{V}$, $V_{OUT} = 4.5\text{V}$ | $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ | 2.8 | 3.7 | 4.6 | A |
| I_{TRIG} | Current limiting trigger threshold | Output Current Slew rate (<100A/s) | | 3.7 | | | A |
| I_{SHORT} | Short-Circuit Current Limit | Enabled into short circuit | | 3.7 | | | A |
| T_{SHORT} | Short-Circuit Response Time | $V_{OUT} = 0\text{V}$ to $I_{OUT} = I_{LIMIT}$ (OUT shorted to ground) | | 2 | | | μs |
| V_{IL} | EN Input Logic Low Voltage | $V_{IN} = 2.7\text{V}$ to 5.5V | | | 0.8 | | V |
| V_{IH} | EN Input Logic High Voltage | $V_{IN} = 2.7\text{V}$ to 5.5V | 2 | | | | V |
| $I_{LEAK-EN}$ | EN Input leakage | $V_{IN} = 5\text{V}$, $V_{EN} = 0\text{V}$ and 5.5V | | 0.01 | 1.00 | | μA |
| I_{LEAK-O} | Output leakage current | Disabled, $V_{OUT} = 0\text{V}$ | | 0.5 | 1 | | μA |
| $T_{D(ON)}$ | Output turn-on delay time | $C_L = 1\mu\text{F}$, $R_{LOAD} = 5\Omega$ | | 0.1 | | | ms |
| T_R | Output turn-on rise time | $C_L = 1\mu\text{F}$, $R_{LOAD} = 5\Omega$ | | 0.6 | 1.5 | | ms |
| $T_{D(OFF)}$ | Output turn-off delay time | $C_L = 1\mu\text{F}$, $R_{LOAD} = 5\Omega$ | | 0.1 | | | ms |
| T_F | Output turn-off fall time | $C_L = 1\mu\text{F}$, $R_{LOAD} = 5\Omega$ | | 0.05 | 0.10 | | ms |
| R_{FLG} | FLG output FET on-resistance | $I_{FLG} = 10\text{mA}$ | | 20 | 40 | | Ω |
| I_{FOH} | FLG Off Current | $V_{FLG} = 5\text{V}$ | | 0.01 | 1.00 | | μA |
| T_{BLANK} | FLG Blanking Time | Assertion or deassertion due to overcurrent and over-temperature condition | 4 | 7 | 15 | | ms |
| T_{DIS} | Discharge time | $C_L = 1\mu\text{F}$, $V_{IN} = 5\text{V}$, disabled to $V_{OUT} < 0.5\text{V}$ | | 0.6 | | | ms |
| R_{DIS} | Discharge resistance (Note 8) | $V_{IN} = 5\text{V}$, disabled, $I_{OUT} = 1\text{mA}$ | | 100 | | | Ω |
| T_{SHDN} | Thermal Shutdown Threshold | Enabled | | 140 | | | $^\circ\text{C}$ |
| T_{HYS} | Thermal Shutdown Hysteresis | | | 20 | | | $^\circ\text{C}$ |
| θ_{JA} | Thermal Resistance Junction-to-Ambient | SO-8 (Note 9) | | 96 | | | $^\circ\text{C/W}$ |
| | | MSOP-8 (Note 9) | | 130 | | | $^\circ\text{C/W}$ |
| | | MSOP-8EP (Note 10) | | 92 | | | $^\circ\text{C/W}$ |
| | | U-DFN3030-8 (Note 10) | | 84 | | | $^\circ\text{C/W}$ |
| | | U-DFN2020-6 (Note 11) | | 90 | | | $^\circ\text{C/W}$ |

- Notes:
- Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
 - The discharge function is active when the device is disabled (when enable is de-asserted or during power-up power-down when $V_{IN} < V_{UVLO}$). The discharge function offers a resistive discharge path for the external storage capacitor for limited time.
 - Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad layout.
 - Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.
 - Device mounted on 1"x1" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground

Typical Performance Characteristics

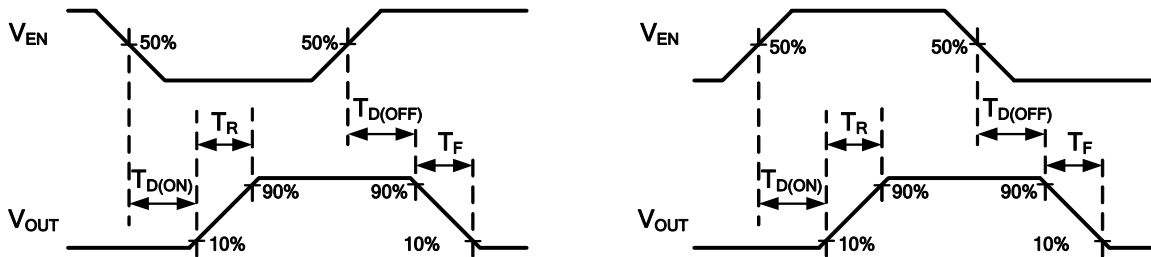
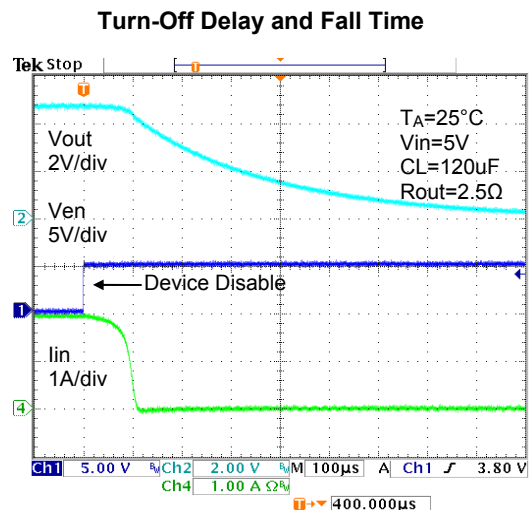
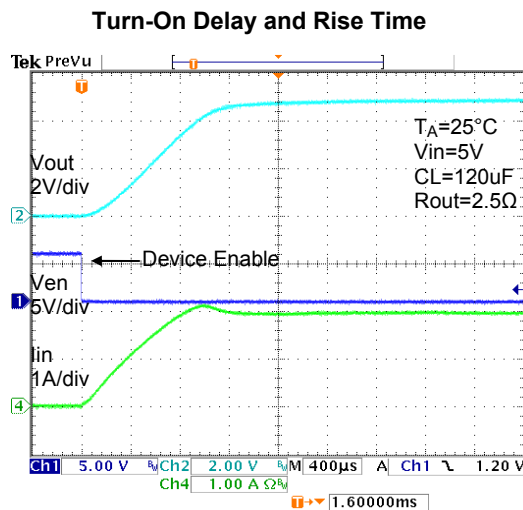
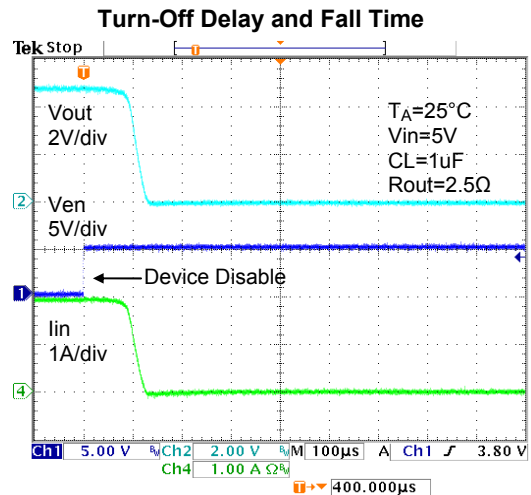
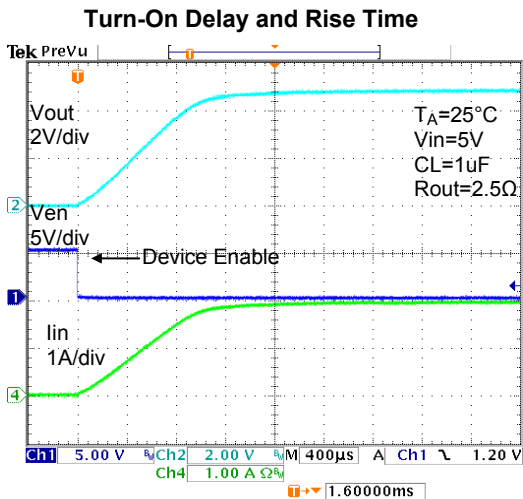


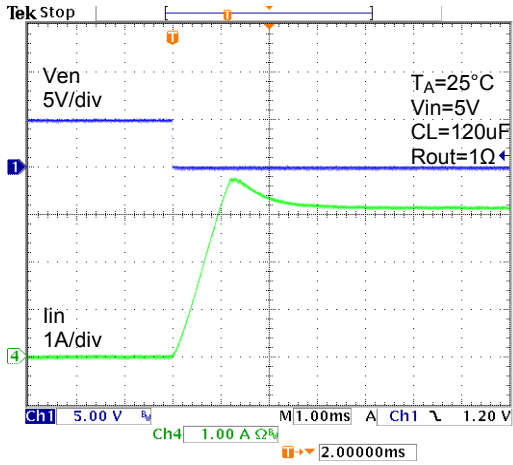
Figure 1 Voltage Waveforms: AP2501 (left), AP2511 (right)

All Enable Plots are for Enable Active Low

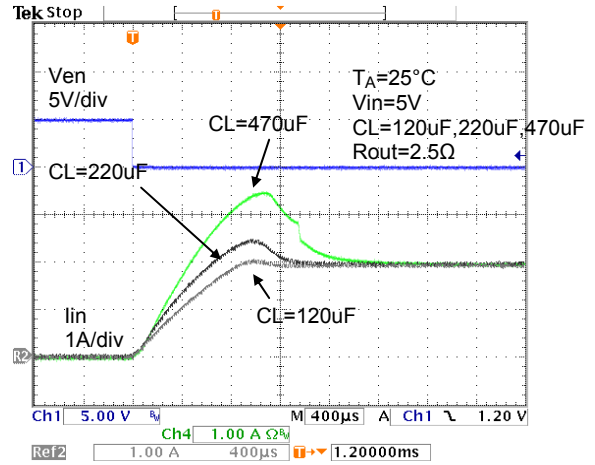


Typical Performance Characteristics (cont.)

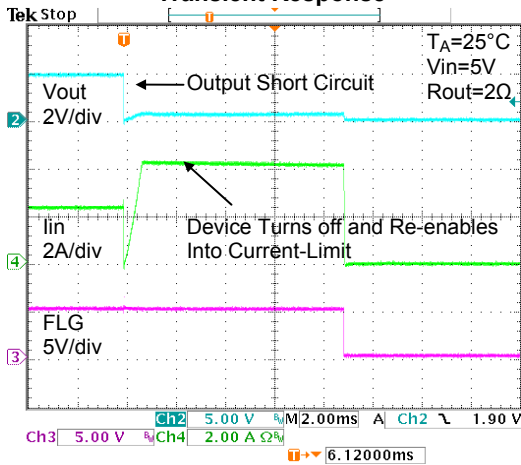
Device Enabled Into Short-Circuit



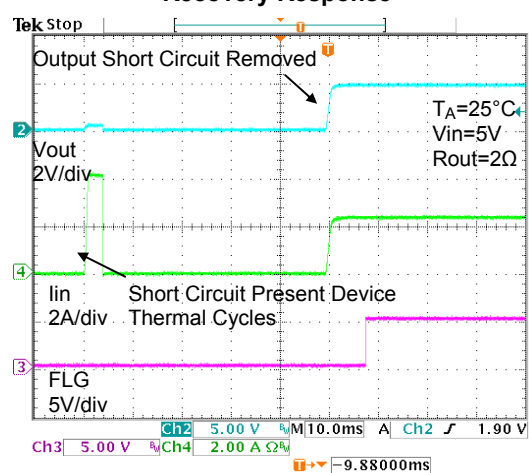
Inrush Current



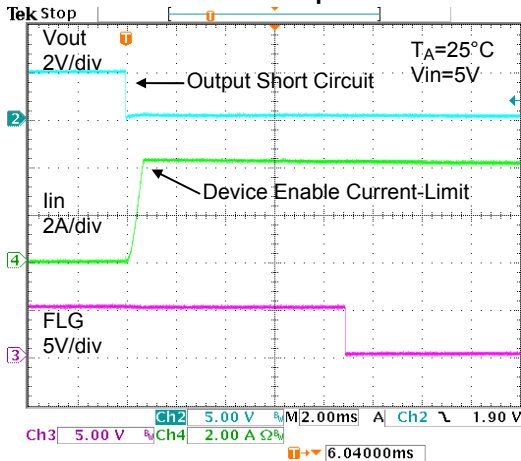
Full-Load to Short-Circuit Transient Response



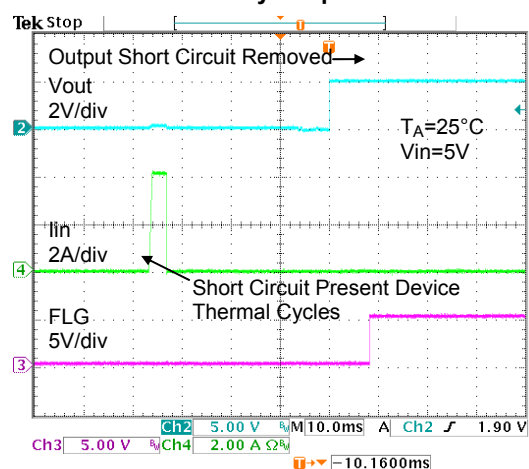
Short-Circuit to Full-Load Recovery Response



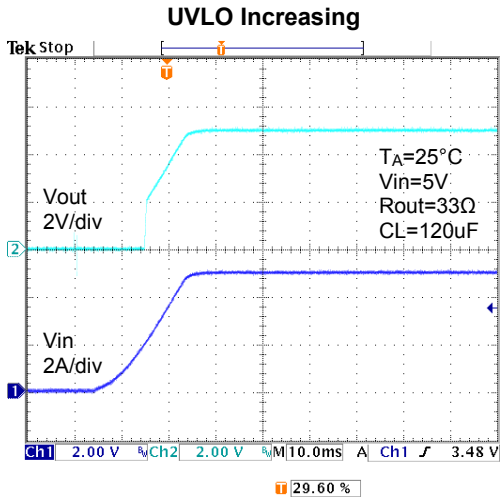
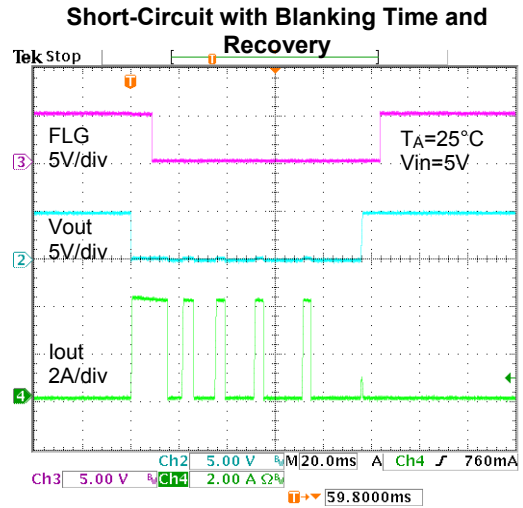
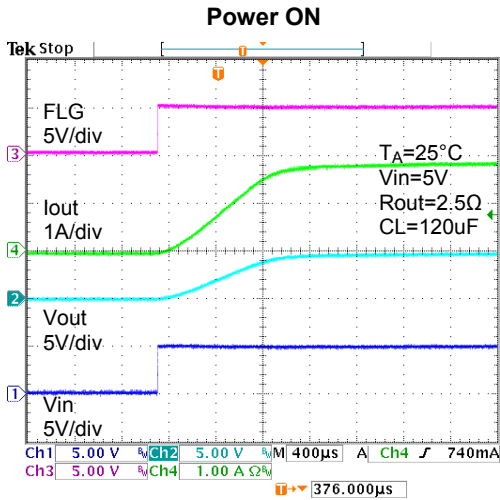
No-Load to Short-Circuit Transient Response



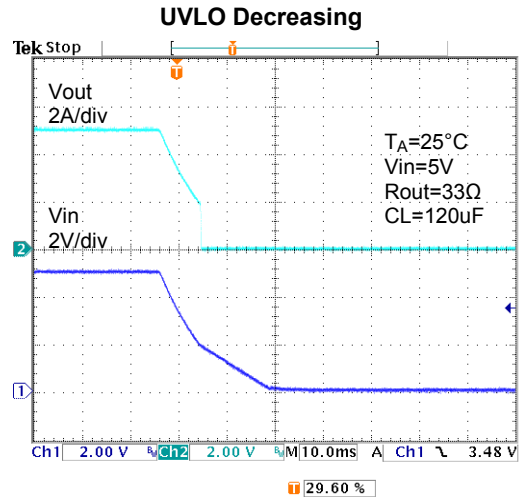
Short-Circuit to No-Load Recovery Response



Typical Performance Characteristics (cont.)

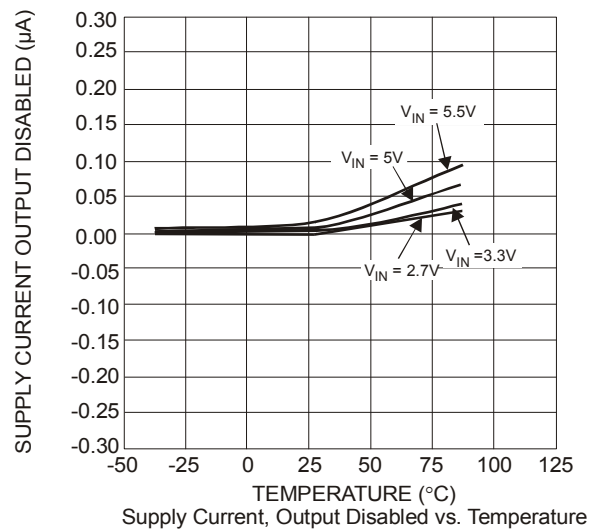
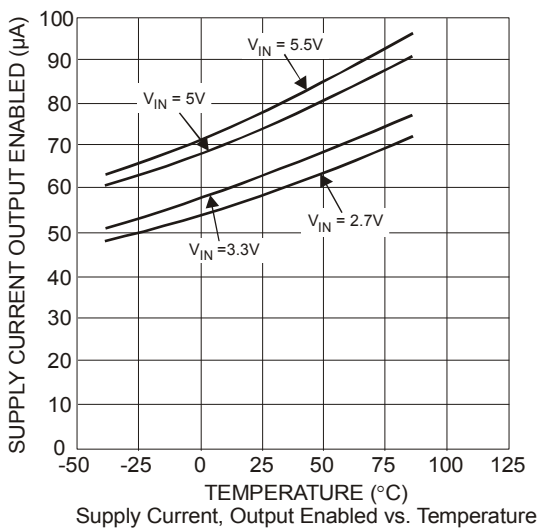
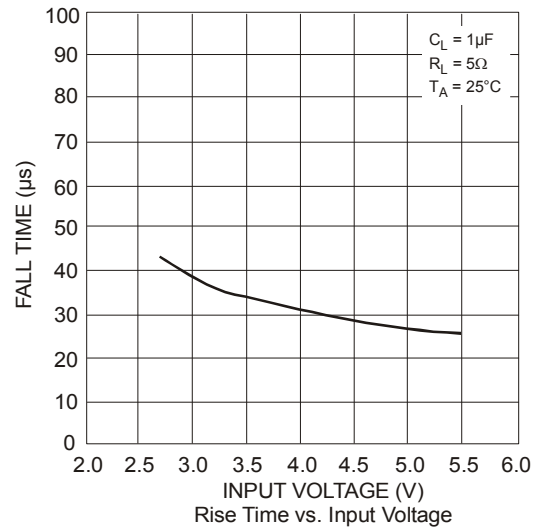
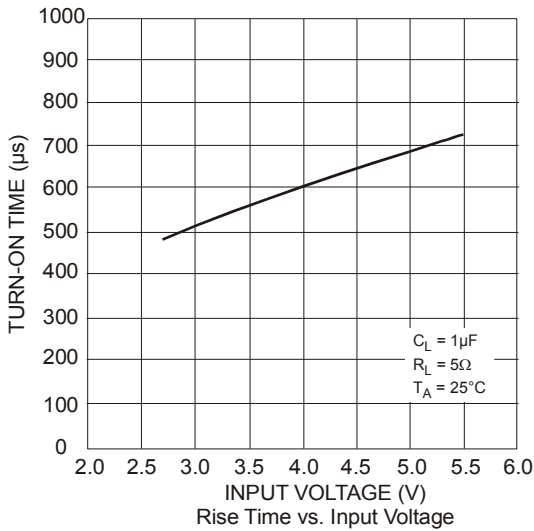
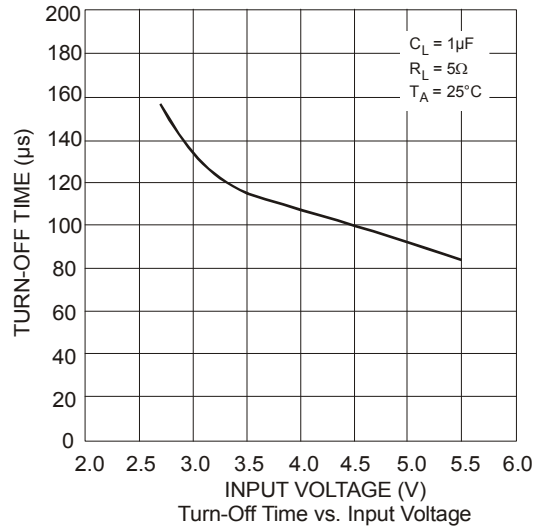
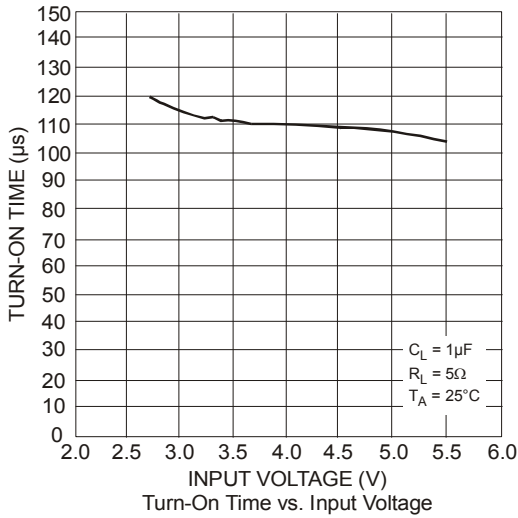


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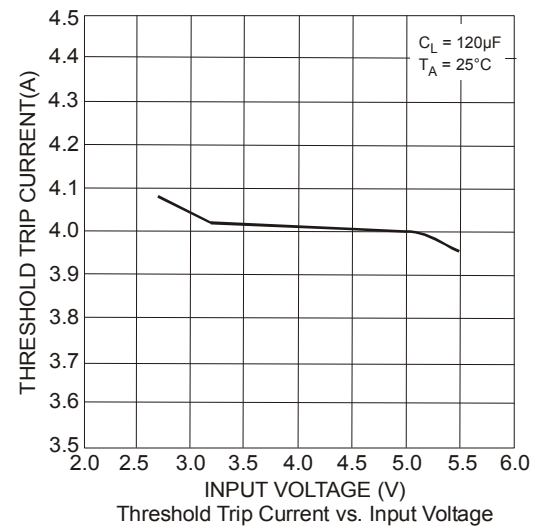
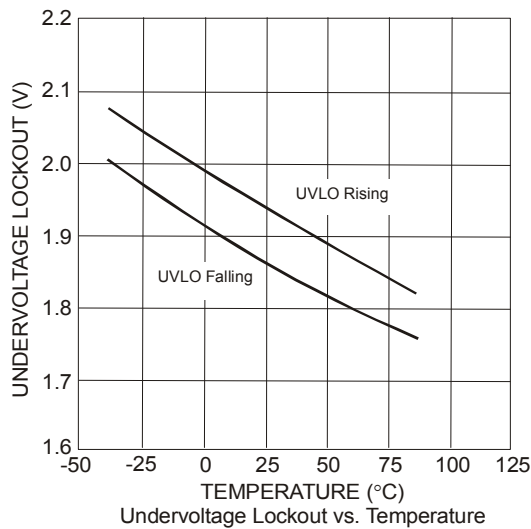
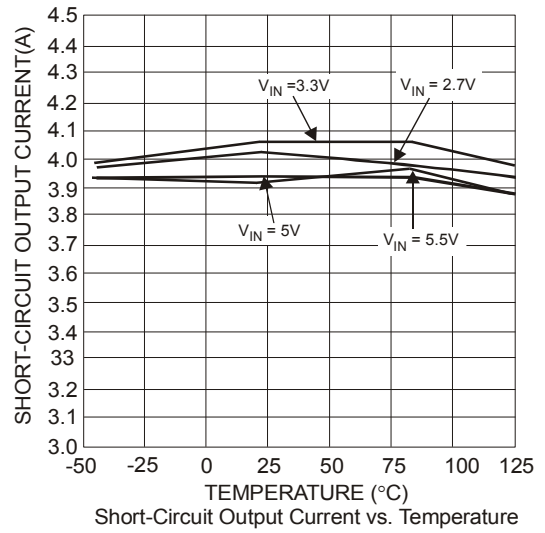
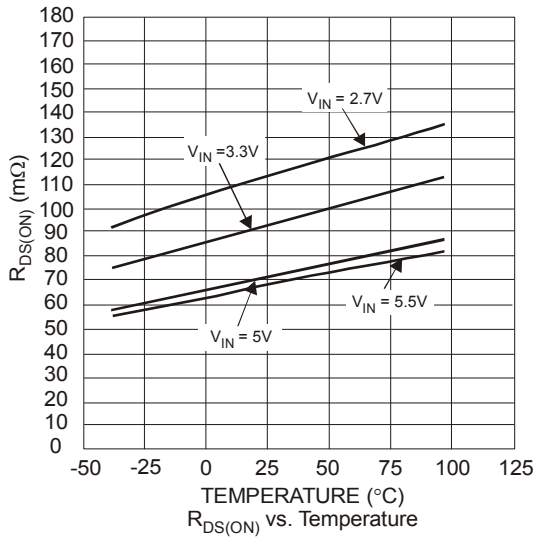


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Typical Performance Characteristics (cont.)



Typical Performance Characteristics (cont.)



Application Note

Power Supply Considerations

A 0.1µF to 2.2µF X7R or X5R ceramic bypass capacitor placed between IN and GND, close to the device, is recommended. When an external power supply is used, or an additional ferrite bead is added to the input, high inrush current may cause voltage spikes higher than the device maximum input rating during short circuit condition. In this case a 2.2µF or bigger capacitor is recommended. Placing a high-value electrolytic capacitor on the input and output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.1µF to 1.0µF ceramic capacitor improves the immunity of the device to short circuit transients.

Over-Current and Short Circuit Protection

An internal sensing FET is employed to check for over-current conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an over-current condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault stays long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted to GND before the device is enabled or before VIN has been applied. The AP2501/AP2511 senses the short circuit and immediately clamps output current to a certain safe level namely I_{LIMIT} .

In the second condition, an output short or an overload occurs while the device is enabled. At the instance the overload occurs, higher inrush current may flow for a very short period of time before the current limit function can react. The input capacitor(s) rapidly discharge through the device, activating current limit circuitry. Protection is achieved by momentarily opening the P-MOS high-side power switch and then gradually turning it on. After the current limit function has tripped (reached the over-current trip threshold), the device switches into current limiting mode and the current is clamped at I_{LIMIT} .

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold (I_{TRIG}) is reached or until the thermal limit of the device is exceeded. The AP2501/AP2511 is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its current limiting mode and is set at I_{LIMIT} .

FLG Response

When an over-current or over-temperature shutdown condition is encountered, the FLG open-drain output goes active low after a nominal 7-ms deglitch timeout. The FLG output remains low until both over-current and over-temperature conditions are removed.

Connecting a heavy capacitive load to the output of the device can cause a momentary over-current condition, which does not trigger the FLG due to the 7-ms deglitch timeout. The AP2501/AP2511 is designed to eliminate false over-current reporting without the need of external components to remove unwanted pulses.

Power Dissipation and Junction Temperature

The low on-resistance of the internal MOSFET allows the small surface-mount packages to pass large current. Using the maximum operating ambient temperature (T_A) and $R_{DS(ON)}$, the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient temperature °C

$R_{\theta JA}$ = Thermal resistance

P_D = Total power dissipation

Thermal Protection

Thermal protection prevents the IC from damage when heavy-overload or short-circuit faults are present for extended periods of time. The AP2501/AP2511 implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately 140°C due to excessive power dissipation in an over-current or short-circuit condition the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit allowing the device to cool down approximately 20°C before the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The FLG open-drain output is asserted when an over-temperature shutdown or over-current occurs with 7-ms deglitch.

Application Note (cont.)

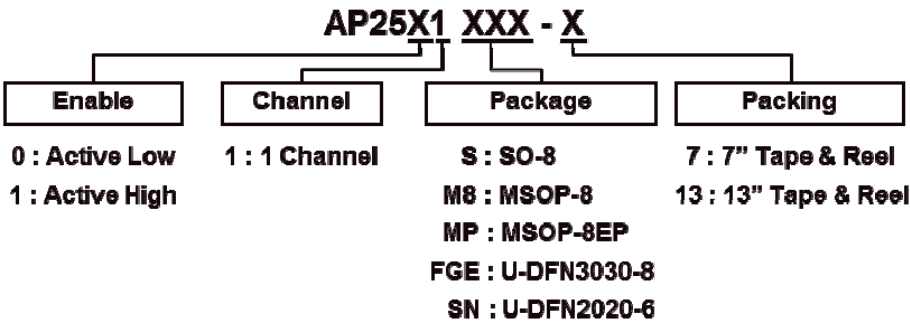
Under-voltage Lockout (UVLO)

Under-voltage lockout function (UVLO) keeps the internal power switch from being turned on until the power supply has reached at least 2V, even if the switch is enabled. Whenever the input voltage falls below approximately 2V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

Discharge Function

The discharge function of the device is active when enable is disabled or de-asserted. The discharge function with the N-MOS power switch implementation is activated and offers a resistive discharge path for the external storage capacitor. This is designed for discharging any residue of the output voltage when either no external output resistance or load resistance is present at the output.

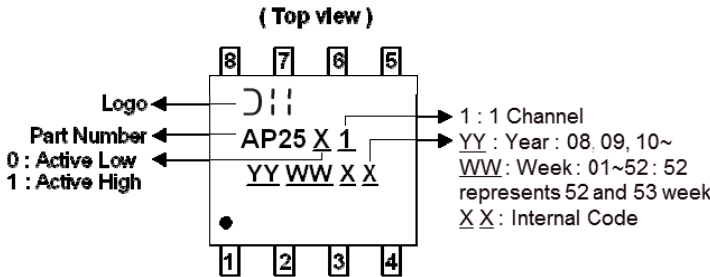
Ordering Information



| Part Number | Package Code | Packaging | 7"/13" Tape and Reel | |
|-------------|--------------|-------------|----------------------|--------------------|
| | | | Quantity | Part Number Suffix |
| AP25X1S-13 | S | SO-8 | 2500/Tape & Reel | -13 |
| AP25X1M8-13 | M8 | MSOP-8 | 2500/Tape & Reel | -13 |
| AP25X1MP-13 | MP | MSOP-8EP | 2500/Tape & Reel | -13 |
| AP25X1FGE-7 | FGE | U-DFN3030-8 | 3000/Tape & Reel | -7 |
| AP25X1SN-7 | SN | U-DFN2020-6 | 3000/Tape & Reel | -7 |

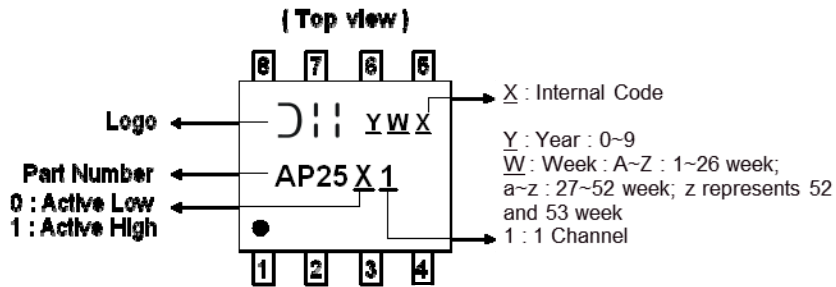
Marking Information

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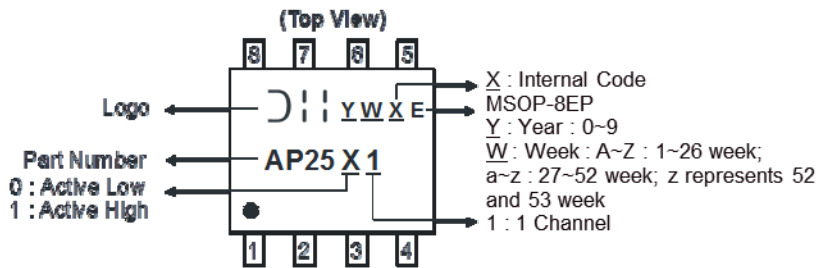


Marking Information (cont.)

(2) MSOP-8

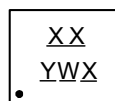


(3) MSOP-8EP



(4) U-DFN3030-8

(Top View)



XX : Identification Code

Y : Year : 0~9

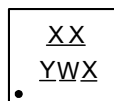
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week

X : A~Z : Internal Code

| Part Number | Package | Identification Code |
|-------------|-------------|---------------------|
| AP2501FGE-7 | U-DFN3030-8 | BP |
| AP2511FGE-7 | U-DFN3030-8 | BR |

(5) U-DFN2020-6

(Top View)



XX : Identification Code

Y : Year : 0~9

W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week

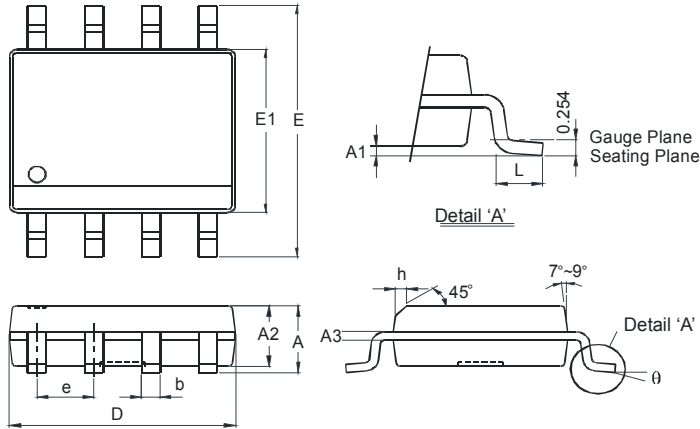
X : A~Z : Internal Code

| Part Number | Package | Identification Code |
|-------------|-------------|---------------------|
| AP2501SN-7 | U-DFN2020-6 | DP |
| AP2511SN-7 | U-DFN2020-6 | DR |

Package Outline Dimensions (All dimensions in mm.)

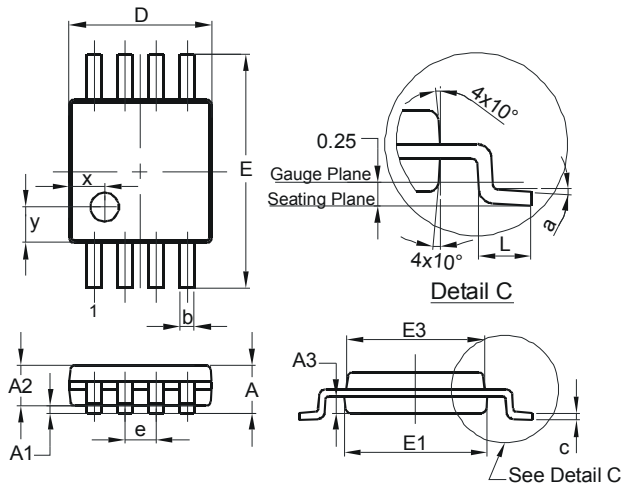
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.

1. Package type: SO-8



| SO-8 | | |
|----------------------|----------|------|
| Dim | Min | Max |
| A | - | 1.75 |
| A1 | 0.10 | 0.20 |
| A2 | 1.30 | 1.50 |
| A3 | 0.15 | 0.25 |
| b | 0.3 | 0.5 |
| D | 4.85 | 4.95 |
| E | 5.90 | 6.10 |
| E1 | 3.85 | 3.95 |
| e | 1.27 Typ | |
| h | - | 0.35 |
| L | 0.62 | 0.82 |
| θ | 0° | 8° |
| All Dimensions in mm | | |

2. Package type: MSOP-8

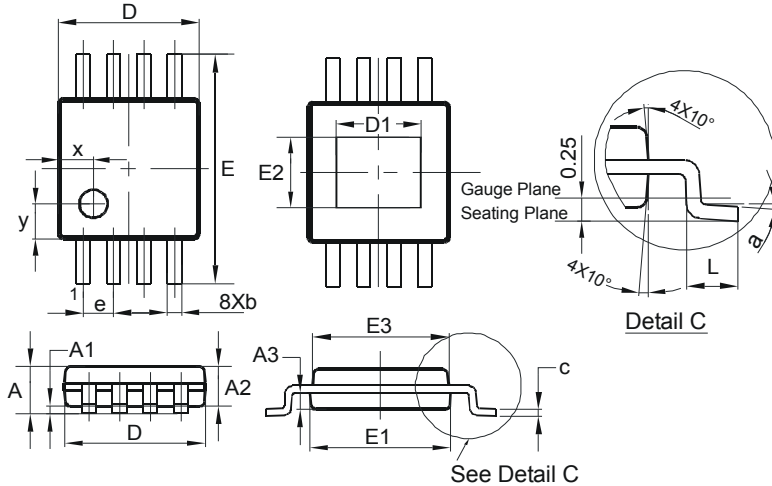


| MSOP-8 | | | |
|----------------------|------|------|-------|
| Dim | Min | Max | Typ |
| A | - | 1.10 | - |
| A1 | 0.05 | 0.15 | 0.10 |
| A2 | 0.75 | 0.95 | 0.86 |
| A3 | 0.29 | 0.49 | 0.39 |
| b | 0.22 | 0.38 | 0.30 |
| c | 0.08 | 0.23 | 0.15 |
| D | 2.90 | 3.10 | 3.00 |
| E | 4.70 | 5.10 | 4.90 |
| E1 | 2.90 | 3.10 | 3.00 |
| E3 | 2.85 | 3.05 | 2.95 |
| e | - | - | 0.65 |
| L | 0.40 | 0.80 | 0.60 |
| a | 0° | 8° | 4° |
| x | - | - | 0.750 |
| y | - | - | 0.750 |
| All Dimensions in mm | | | |

Package Outline Dimensions (cont.) (All dimensions in mm.)

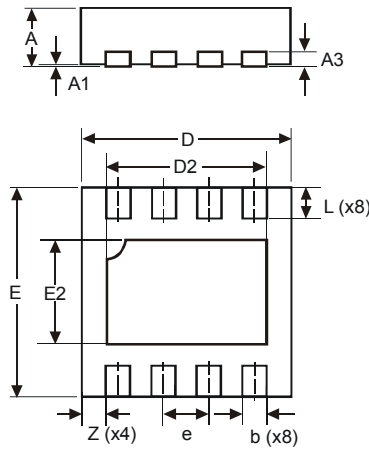
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.

3. Package type: MSOP-8EP



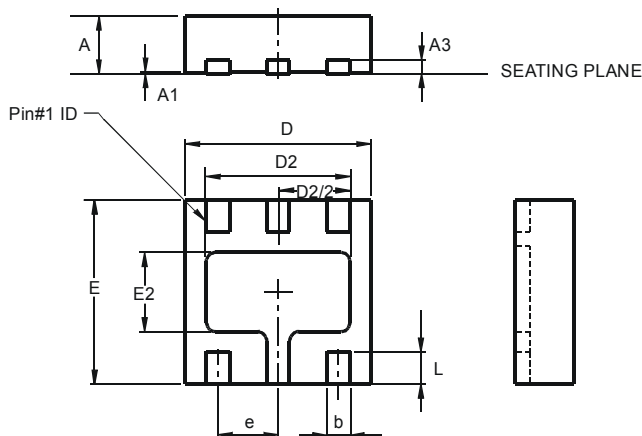
| MSOP-8EP | | | |
|----------------------|------|------|-------|
| Dim | Min | Max | Typ |
| A | - | 1.10 | - |
| A1 | 0.05 | 0.15 | 0.10 |
| A2 | 0.75 | 0.95 | 0.86 |
| A3 | 0.29 | 0.49 | 0.39 |
| b | 0.22 | 0.38 | 0.30 |
| c | 0.08 | 0.23 | 0.15 |
| D | 2.90 | 3.10 | 3.00 |
| D1 | 1.60 | 2.00 | 1.80 |
| E | 4.70 | 5.10 | 4.90 |
| E1 | 2.90 | 3.10 | 3.00 |
| E2 | 1.30 | 1.70 | 1.50 |
| E3 | 2.85 | 3.05 | 2.95 |
| e | - | - | 0.65 |
| L | 0.40 | 0.80 | 0.60 |
| a | 0° | 8° | 4° |
| x | - | - | 0.750 |
| y | - | - | 0.750 |
| All Dimensions in mm | | | |

4. Package type: U-DFN3030-8 Type E



| U-DFN3030-8 Type E | | | |
|-----------------------|------|------|------|
| Dim | Min | Max | Typ |
| A | 0.57 | 0.63 | 0.60 |
| A1 | 0 | 0.05 | 0.02 |
| A3 | - | - | 0.15 |
| b | 0.20 | 0.30 | 0.25 |
| D | 2.95 | 3.05 | 3.00 |
| D2 | 2.15 | 2.35 | 2.25 |
| E | 2.95 | 3.05 | 3.00 |
| e | - | - | 0.65 |
| E2 | 1.40 | 1.60 | 1.50 |
| L | 0.30 | 0.60 | 0.45 |
| Z | - | - | 0.40 |
| All Dimensions in mm | | | |

5. Package type: U-DFN2020-6

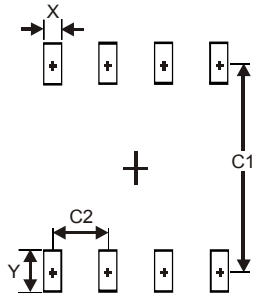


| U-DFN2020-6 | | | |
|----------------------|------|-------|------|
| Dim | Min | Max | Typ |
| A | 0.57 | 0.63 | 0.60 |
| A1 | 0 | 0.05 | 0.03 |
| A3 | - | - | 0.15 |
| b | 0.20 | 0.30 | 0.25 |
| D | 1.95 | 2.075 | 2.00 |
| D2 | 1.45 | 1.65 | 1.55 |
| e | - | - | 0.65 |
| E | 1.95 | 2.075 | 2.00 |
| E2 | 0.76 | 0.96 | 0.86 |
| L | 0.30 | 0.40 | 0.35 |
| All Dimensions in mm | | | |

Suggested Pad Layout

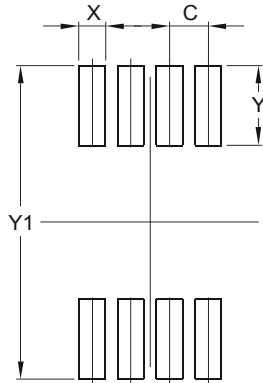
Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.

(1) Package type: SO-8



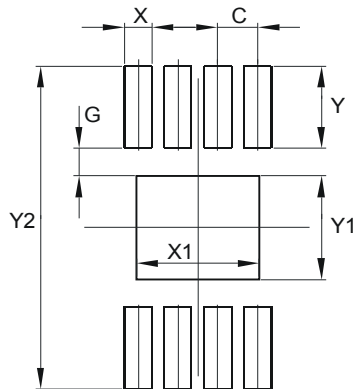
| Dimensions | Value (in mm) |
|------------|---------------|
| X | 0.60 |
| Y | 1.55 |
| C1 | 5.4 |
| C2 | 1.27 |

(2) Package type: MSOP-8



| Dimensions | Value (in mm) |
|------------|---------------|
| C | 0.650 |
| X | 0.450 |
| Y | 1.350 |
| Y1 | 5.300 |

(3) Package type: MSOP-8EP

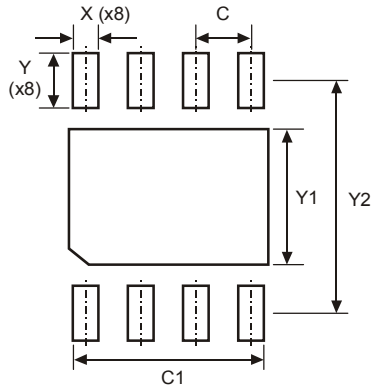


| Dimensions | Value (in mm) |
|------------|---------------|
| C | 0.650 |
| G | 0.450 |
| X | 0.450 |
| X1 | 2.000 |
| Y | 1.350 |
| Y1 | 1.700 |
| Y2 | 5.300 |

Suggested Pad Layout (cont.)

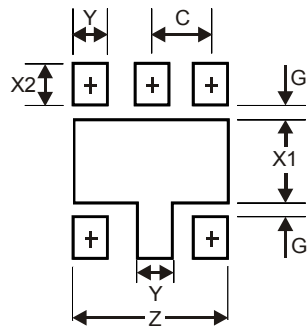
Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.

(4) Package type: U-DFN3030-8 Type E



| Dimensions | Value (in mm) |
|------------|---------------|
| C | 0.65 |
| C1 | 2.35 |
| X | 0.30 |
| Y | 0.65 |
| Y1 | 1.60 |
| Y2 | 2.75 |

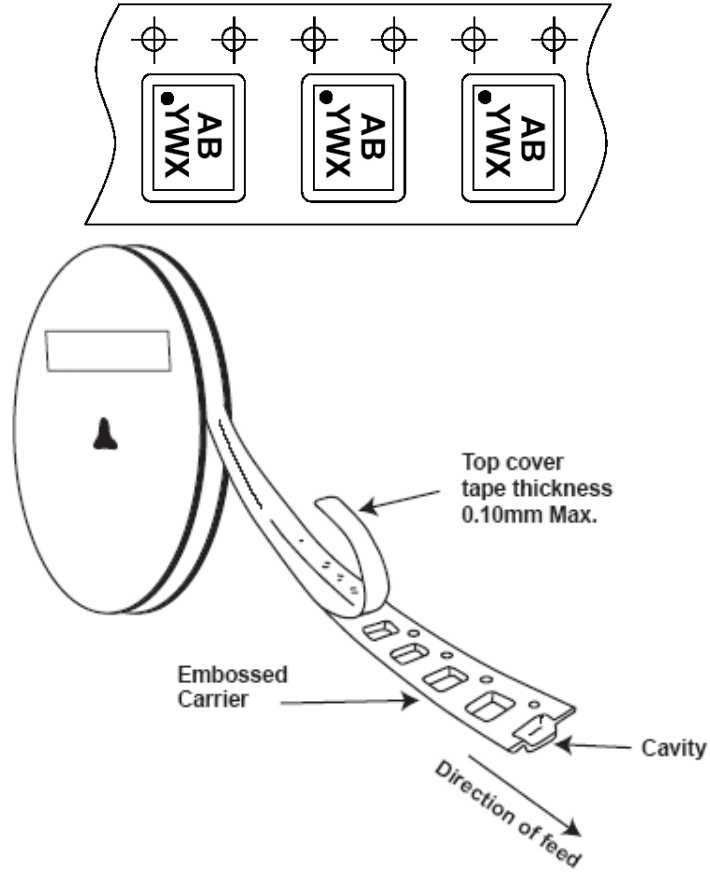
(5) Package type: U-DFN2020-6



| Dimensions | Value (in mm) |
|------------|---------------|
| Z | 1.67 |
| G | 0.15 |
| X1 | 0.90 |
| X2 | 0.45 |
| Y | 0.37 |
| C | 0.65 |

Taping Orientation (Note 12)

For U-DFN2020-6 and U-DFN3030-8 Type E



Note: 12. The taping orientation of the other package type can be found on our website at <http://www.diodes.com/datasheets/ap02007.pdf>

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