

**PI6C5912016**

**16 Output LVPECL Fanout Buffer**

**Features**

- 16 differential LVPECL outputs
- 2 selectable reference inputs support either single-ended or differential
- Up to 2GHz output frequency
- Ultra low additive phase jitter: < 0.01 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Low skew between outputs
- Low delay from input to output (Tpd typ. < 1.7ns)
- Separate Input output supply voltage for level shifting
- 2.5V / 3.3V power supply
- Industrial temperature support
- Package: TQFN-48

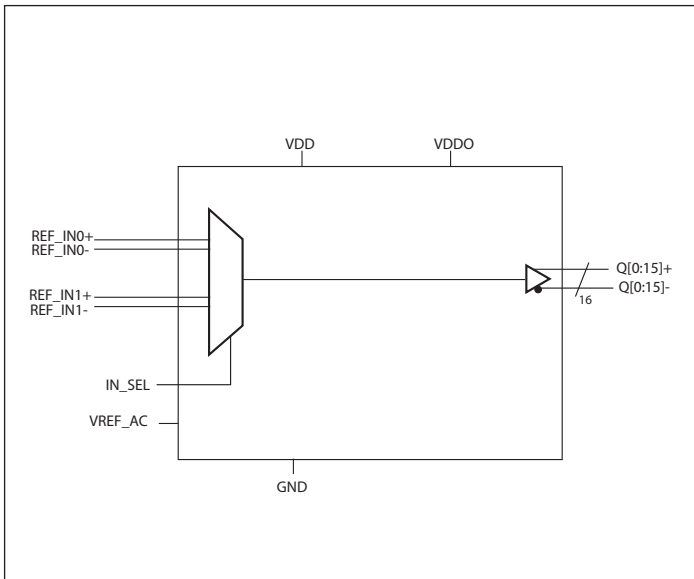
**Description**

The PI6C5912016 is a high performance LVPECL fanout buffer device which supports up to 2GHz frequency. This device is ideal for systems that need to distribute low jitter LVPECL clock signals to multiple destinations.

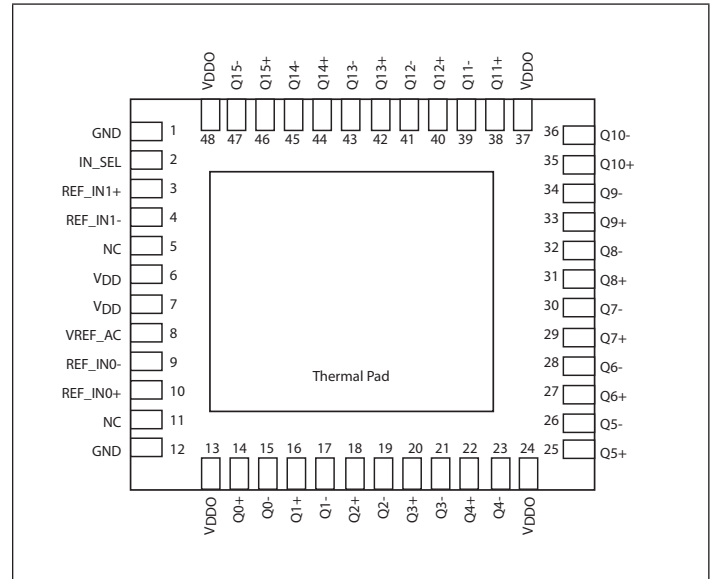
**Applications**

- Networking systems including switches and routers
- High frequency backplane based computing and telecom platforms

**Block Diagram**



**Pin Configuration**



## Pin Description

| Pin #          | Pin Name             | Type   |          | Description  |
|----------------|----------------------|--------|----------|--|
| 1, 12          | GND                  | Power  |          | Power supply ground  |
| 2              | IN_SEL               | Input  | Pulldown | Input clock select. See Table 1 for function. LVCMOS/LVTTL interface levels. |
| 3, 4           | REF_IN1+<br>REF_IN1- | Input  |          | Reference input 1. Accepts Differential or Single Ended inputs               |
| 5, 11          | NC                   | -      |          | No Connect   |
| 6, 7           | VDD                  | Power  |          | Core power supply  |
| 8              | VREF_AC              | Output |          | Bias voltage output.   |
| 9, 10          | REF_IN0+<br>REF_IN0- | Input  |          | Reference input 0. Accepts Differential or Single Ended inputs               |
| 13, 24, 37, 48 | VDDO                 | Power  |          | Output power supply  |
| 14, 15         | Q0+<br>Q0-           | Output |          | LVPECL output pair 0.  |
| 16, 17         | Q1+<br>Q1-           | Output |          | LVPECL output pair 1.  |
| 18, 19         | Q2+<br>Q2-           | Output |          | LVPECL output pair 2.  |
| 20, 21         | Q3+<br>Q3-           | Output |          | LVPECL output pair 3.  |
| 22, 23         | Q4+<br>Q4-           | Output |          | LVPECL output pair 4.  |
| 25, 26         | Q5+<br>Q5-           | Output |          | LVPECL output pair 5.  |
| 27, 28         | Q6+<br>Q6-           | Output |          | LVPECL output pair 6.  |
| 29, 30         | Q7+<br>Q7-           | Output |          | LVPECL output pair 7.  |
| 31, 32         | Q8+<br>Q8-           | Output |          | LVPECL output pair 8.  |
| 33, 34         | Q9+<br>Q9-           | Output |          | LVPECL output pair 9.  |
| 35, 36         | Q10+<br>Q10-         | Output |          | LVPECL output pair 10.   |

### Pin Description Cont.

| Pin #       | Pin Name | Type   | Description                     |
|-------------|----------|--------|---------------------------------|
| 38, 39      | Q11+     | Output | LVPECL output pair 11.          |
|             | Q11-     |        |                                 |
| 40, 41      | Q12+     | Output | LVPECL output pair 12.          |
|             | Q12-     |        |                                 |
| 42, 43      | Q13+     | Output | LVPECL output pair 13.          |
|             | Q13-     |        |                                 |
| 44, 45      | Q14+     | Output | LVPECL output pair 14.          |
|             | Q14-     |        |                                 |
| 46, 47      | Q15+     | Output | LVPECL output pair 15.          |
|             | Q15-     |        |                                 |
| Thermal pad | -        | -      | Thermal pad. Connect to ground. |

### Function Table

Table 1: Input select function

| IN_SEL | Function                                |
|--------|---|
| 0      | REF_IN0 is the selected reference input |
| 1      | REF_IN1 is the selected reference input |
| Open   | No inputs selected. Outputs Hi-Z        |

| Symbol         | Parameter               | Test Condition | Min. | Typ. | Max. | Units      |
|----------------|-------------------------|----------------|------|------|------|------------|
| $C_{IN}$       | Input Capacitance       |                |      | 2    |      | pF         |
| $R_{PULLDOWN}$ | Input Pulldown Resistor |                |      | 200  |      | k $\Omega$ |
| $R_{PULLUP}$   | Input Pullup Resistor   |                |      | 200  |      | k $\Omega$ |

**Maximum Ratings** (Above which the useful life may be impaired. For user guidelines, not tested)

|   |                       |
|---|-----------------------|
| Storage temperature.....                                    | -55 to +150°C         |
| Supply Voltage to Ground Potential ( $V_{DD}, V_{DDO}$ )... | -0.5 to +4.6V         |
| Inputs (Referenced to GND) .....                            | -0.5 to $V_{DD}+0.5V$ |
| Clock Output (Referenced to GND).....                       | -0.5 to $V_{DD}+0.5V$ |
| Latch up .....  | 200mA                 |
| ESD Protection (Input) .....                                | 2000 V min (HBM)      |
| ESD Protection (Input) .....                                | 1000 V min (CDM)      |

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Power Supply Characteristics and Operating Conditions**

| Symbol    | Parameter                     | Test Condition | Min.  | Typ. | Max.  | Units |
|-----------|-------------------------------|----------------|-------|------|-------|-------|
| $V_{DD}$  | Core Supply Voltage           |                | 3.135 | 3.3  | 3.465 | V     |
|           |                               |                | 2.375 | 2.5  | 2.625 | V     |
| $V_{DDO}$ | Output Supply Voltage         |                | 3.135 | 3.3  | 3.465 | V     |
|           |                               |                | 2.375 | 2.5  | 2.625 | V     |
| $I_{EE}$  | Supply Internal Current       |                |       | 127  | 146   | mA    |
| $I_{DD}$  | Core Power Supply Current     |                |       | 91   | 105   |       |
| $T_A$     | Ambient Operating Temperature |                | -40   |      | 85    | °C    |

**DC Electrical Specifications - Differential Inputs**

| Symbol      | Parameter                          |                  | Min.      | Typ. | Max.          | Units |
|-------------|------------------------------------|------------------|-----------|------|---------------|-------|
| $I_{IH}$    | Input High current                 | Input = $V_{DD}$ |           |      | 20            | uA    |
| $I_{IL}$    | Input Low current                  | Input = GND      | -20       |      |               | uA    |
| $V_{IH}$    | Input high voltage                 |                  |           |      | $V_{DD}+0.3$  | V     |
| $V_{IL}$    | Input low voltage                  |                  | -0.3      |      |               | V     |
| $V_{ID}$    | Input Differential Amplitude PK-PK |                  | 0.1       |      |               | V     |
| $V_{CM}$    | Common mode input voltage          |                  | GND + 0.5 |      | $V_{DD}-0.85$ | V     |
| $ISO_{MUX}$ | MUX isolation                      |                  |           | -89  |               | dBc   |

### DC Electrical Specifications - LVCMOS Inputs

| Symbol   | Parameter          | Conditions       | Min. | Typ. | Max.         | Units   |
|----------|--------------------|------------------|------|------|--------------|---------|
| $I_{IH}$ | Input High current | Input = $V_{DD}$ |      |      | 50           | $\mu A$ |
| $I_{IL}$ | Input Low current  | Input = GND      | -50  |      |              | $\mu A$ |
| $V_{IH}$ | Input high voltage | $V_{DD}=3.3V$    | 2.0  |      | $V_{DD}+0.3$ | V       |
| $V_{IL}$ | Input low voltage  | $V_{DD}=3.3V$    | -0.3 |      | 0.8          | V       |
| $V_{IH}$ | Input high voltage | $V_{DD}=2.5V$    | 1.7  |      | $V_{DD}+0.3$ | V       |
| $V_{IL}$ | Input low voltage  | $V_{DD}=2.5V$    | -0.3 |      | 0.7          | V       |

### DC Electrical Specifications- LVPECL Outputs

| Parameter | Description         | Conditions    | Min.          | Typ. | Max.           | Units |
|-----------|---------------------|---------------|---------------|------|----------------|-------|
| $V_{OH}$  | Output High voltage |               | $V_{DDO}-1.4$ |      | $V_{DDO}-0.9$  | V     |
| $V_{OL}$  | Output Low voltage  | $V_{DD}=2.5V$ | $V_{DDO}-1.9$ |      | $V_{DDO}-1.25$ | V     |
|           |                     | $V_{DD}=3.3V$ | $V_{DDO}-2.2$ |      | $V_{DDO}-1.25$ | V     |

### AC Electrical Specifications – Differential Inputs

| Parameter  | Description                             | Conditions                      | Min. | Typ. | Max. | Units |
|------------|---|---------------------------------|------|------|------|-------|
| $F_{IN}$   | Clock input frequency                   |                                 |      |      | 2000 | MHz   |
| $V_{INPP}$ | Differential Input peak to peak voltage | $1.5GHz \leq F_{IN} \leq 2 GHz$ | 0.2  |      | 1.5  | V     |
|            |   | $F_{IN} \leq 1.5 GHz$           | 0.1  |      | 1.5  | V     |
| ER         | Input Edge Rate                         |                                 | 1.5  |      |      | V/ns  |

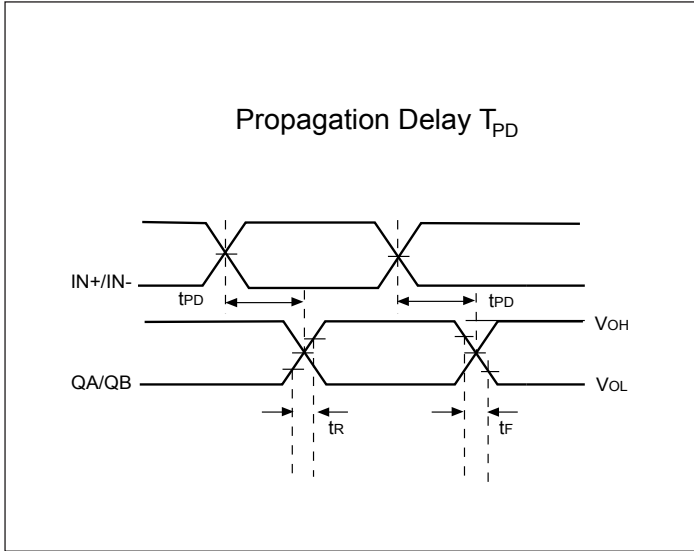
### AC Electrical Specifications – LVCMOS Inputs

| Parameter  | Description                       | Conditions         | Min. | Typ. | Max. | Units |
|------------|-----------------------------------|--------------------|------|------|------|-------|
| $F_{IN}$   | Clock input frequency             | REF_IN0+, REF_IN1+ |      |      | 200  | MHz   |
| $V_{INPP}$ | LVCMOS Input peak to peak voltage |                    | 0.8  |      | VDD  | V     |
| ER         | Input Edge Rate                   |                    | 1.5  |      |      | V/ns  |

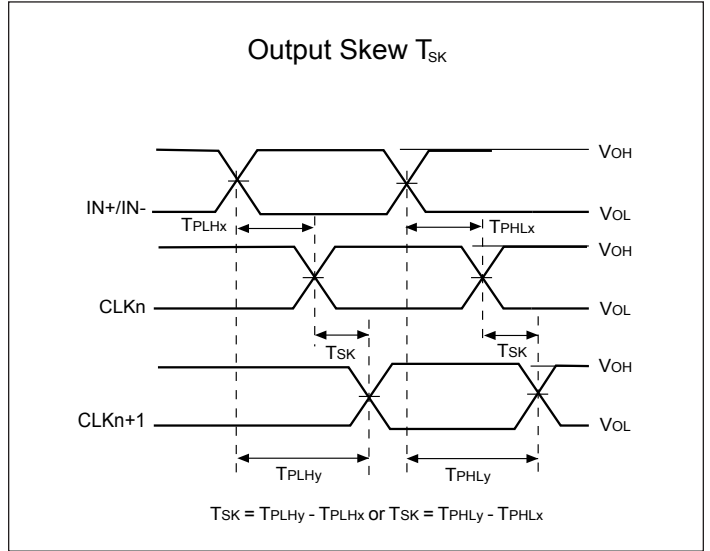
### AC Electrical Specifications – LVPECL Outputs

| Parameter             | Description                    | Conditions                | Min.                 | Typ. | Max.                 | Units |
|-----------------------|--------------------------------|---------------------------|----------------------|------|----------------------|-------|
| F <sub>OUT</sub>      | Clock output frequency         | LVPECL                    |                      |      | 2000                 | MHz   |
| T <sub>r</sub>        | Output rise time               | From 20% to 80%           |                      | 150  |                      | ps    |
| T <sub>f</sub>        | Output fall time               | From 80% to 20%           |                      | 150  |                      | ps    |
| T <sub>ODC</sub>      | Output duty cycle              |                           | 48                   |      | 52                   | %     |
| V <sub>PP</sub>       | Output swing Single-ended      | @1GHz to ≤2GHz            | 250                  |      | 850                  | mV    |
|                       |                                | @ ≤1GHz                   | 500                  |      | 950                  | mV    |
| T <sub>j</sub>        | Buffer additive jitter RMS     | 156.25MHz, 12kHz to 20MHz |                      | 0.04 | 0.08                 | ps    |
|                       |                                | 156.25MHz, 10kHz to 1MHz  |                      | 0.03 | 0.08                 | ps    |
| T <sub>SK</sub>       | Output Skew                    |                           |                      | 13   | 30                   | ps    |
| T <sub>PD</sub>       | Propagation Delay              |                           |                      | 620  | 700                  | ps    |
| T <sub>OD</sub>       | Valid to HiZ                   |                           |                      |      | 100                  | ns    |
| T <sub>OE</sub>       | HiZ to valid                   |                           |                      |      | 100                  | ns    |
| T <sub>P2P Skew</sub> | Part to Part Skew <sup>1</sup> |                           | -50                  |      | 50                   | ps    |
| V <sub>REF_AC</sub>   | Input bias voltage             | I <sub>AC</sub> = 2mA     | V <sub>DD</sub> -1.6 |      | V <sub>DD</sub> -1.1 | V     |

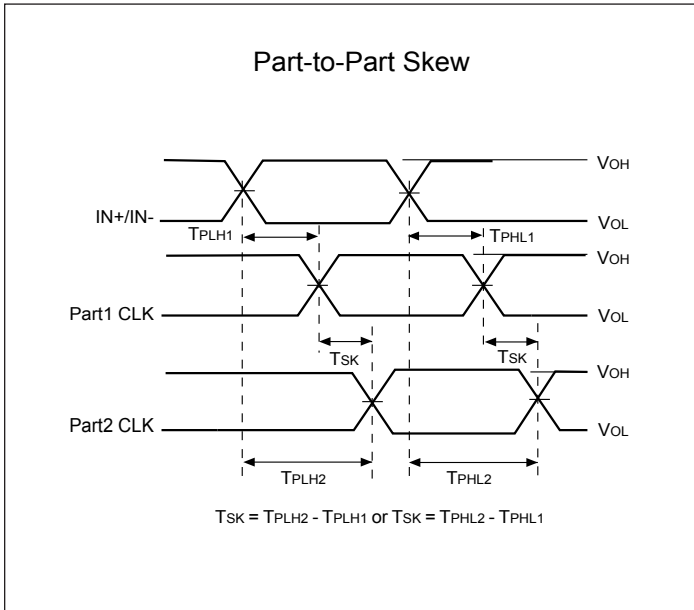
**Propagation Delay**



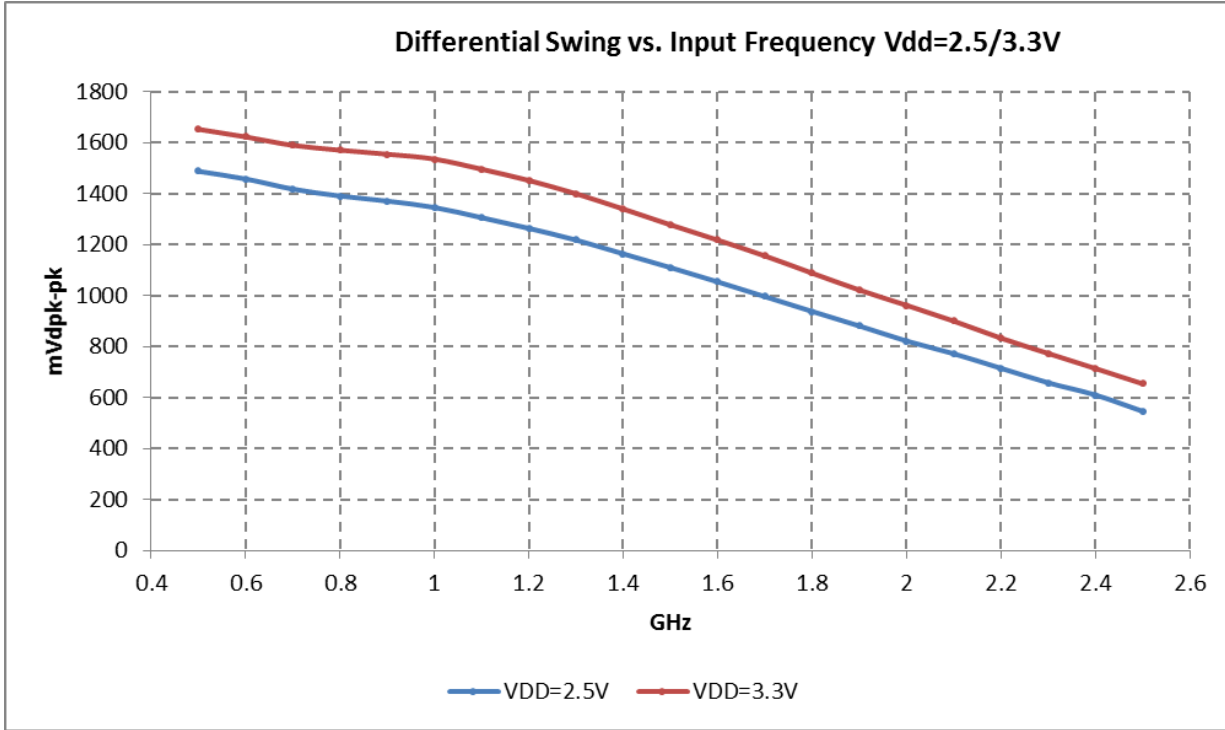
**Output Skew**



**Part to Part Skew**



**LVPECL Output Swing vs. Frequency**

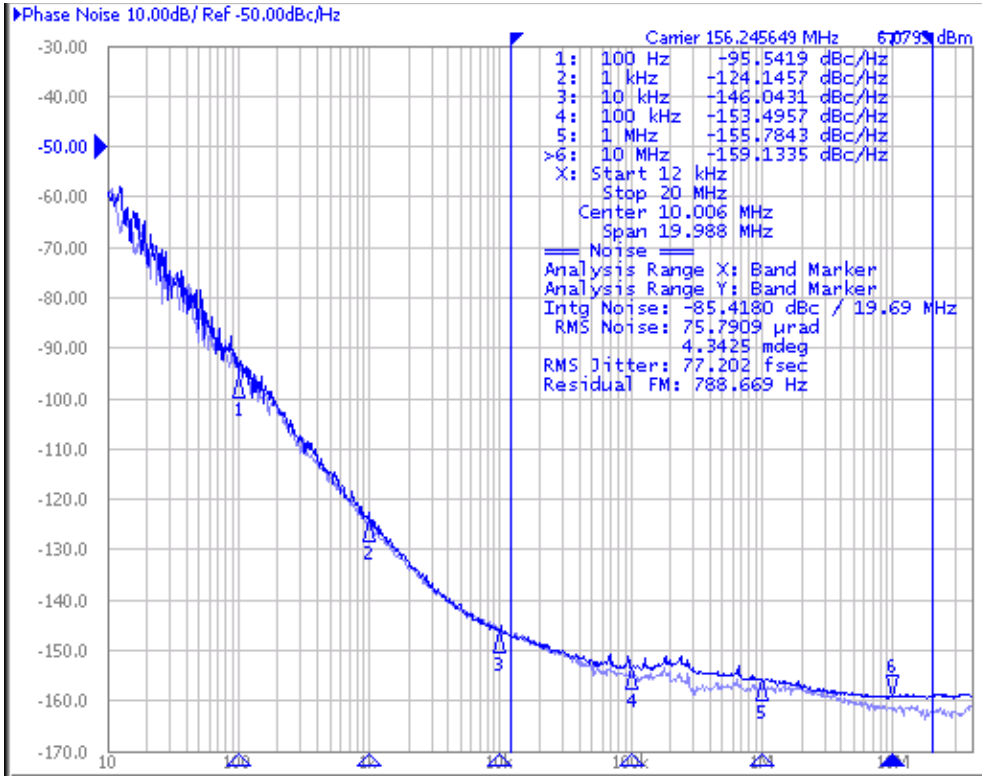




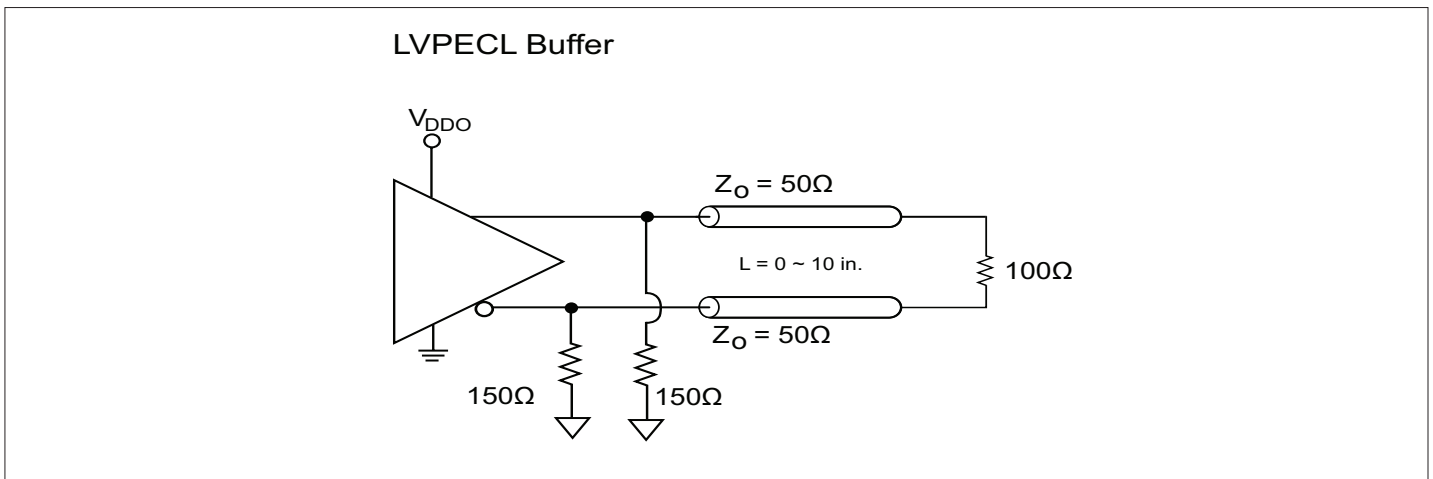
### Phase Noise and Additive Jitter

Output phase noise (Dark Blue) vs Input Phase noise (light blue)

$$\text{Additive jitter} = \sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$$

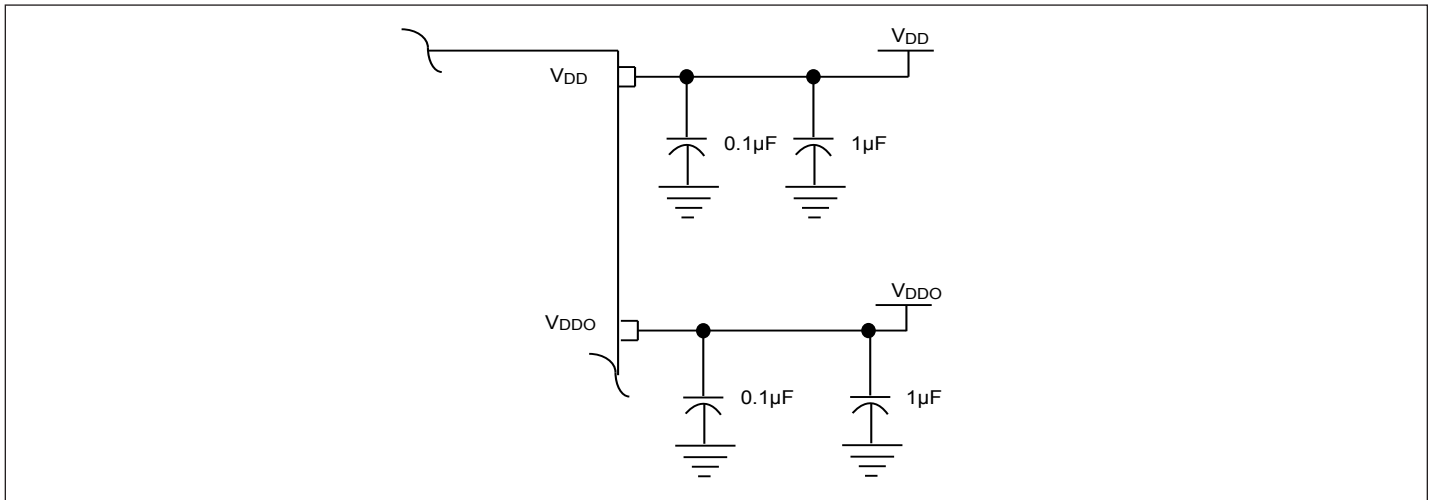


### Configuration Test Load Board Termination for LVPECL Outputs

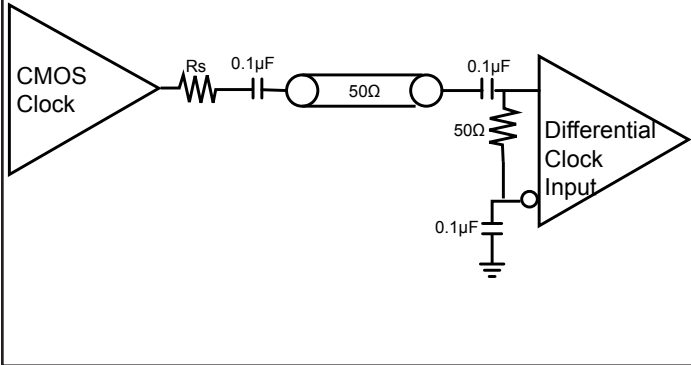


## Power Supply Filtering Techniques

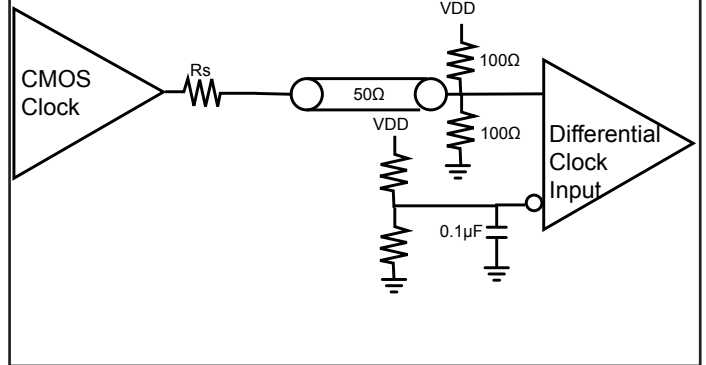
As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. All power pins should be individually connected to the power supply plane through vias, and 0.1 $\mu$ F and 1 $\mu$ F bypass capacitors should be used for each pin.



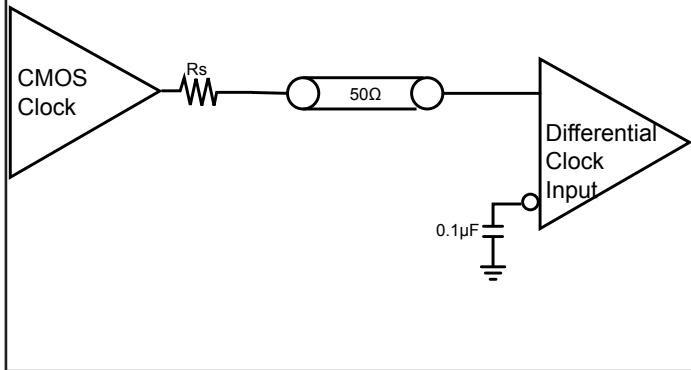
**Single Ended Input, AC couple**



**Single Ended Input, DC couple**

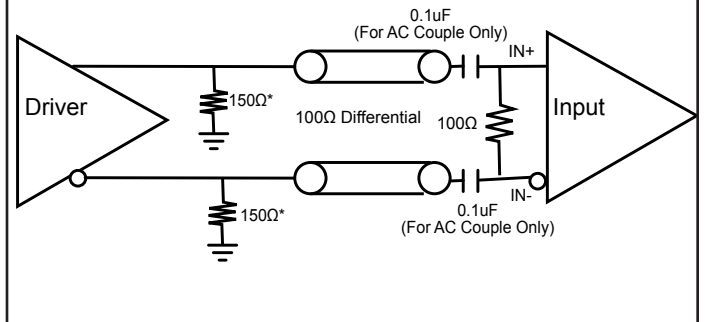


**Single Ended Input, DC couple**

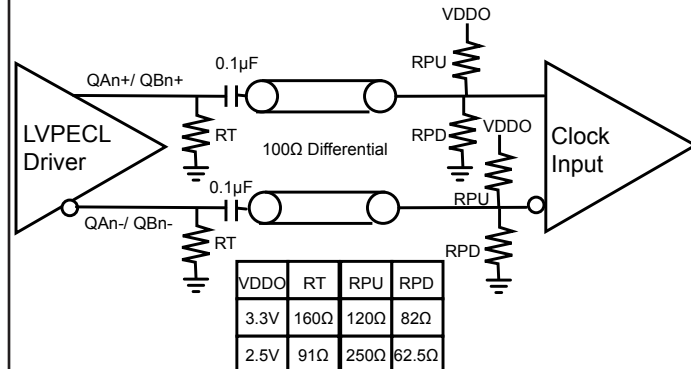


**LVPECL/ LVDS AC and DC input**

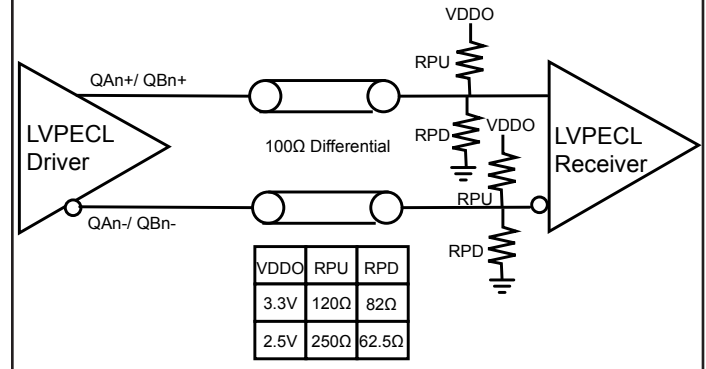
\*Remove for LVDS

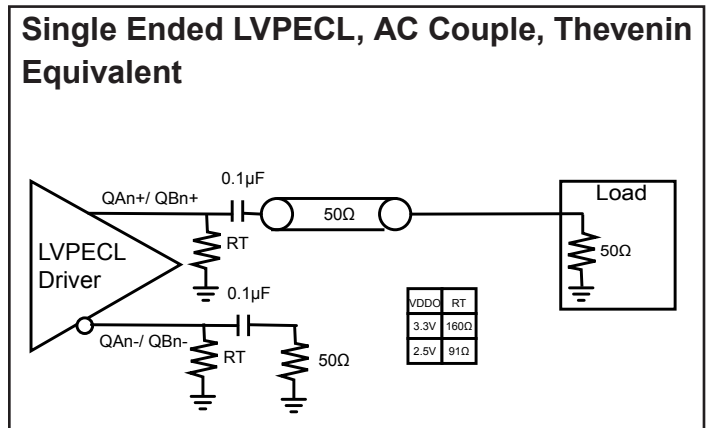
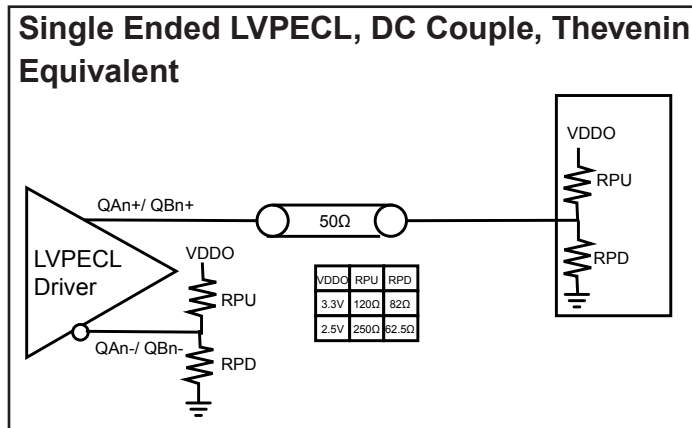
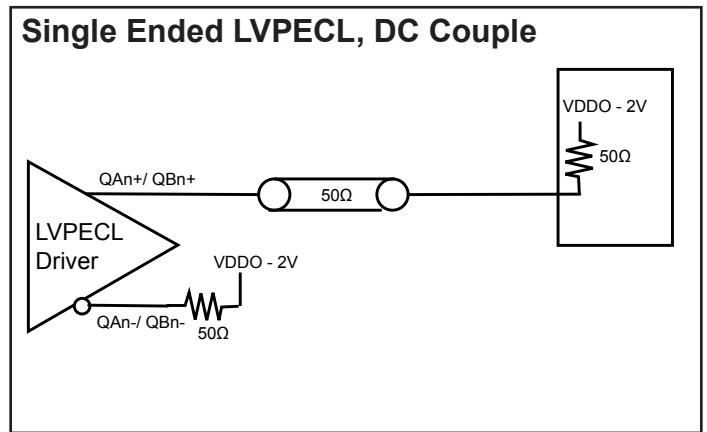
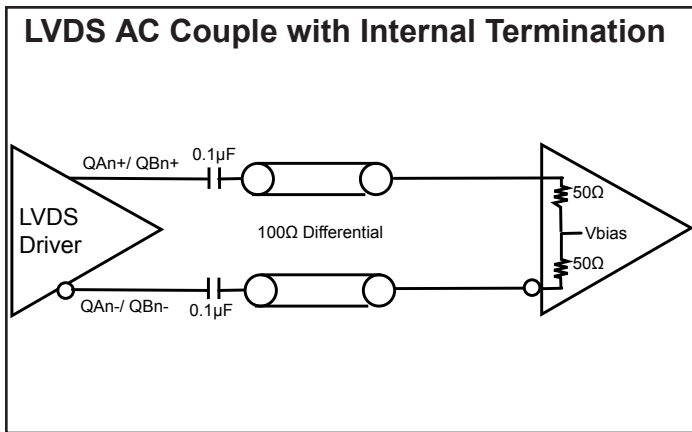
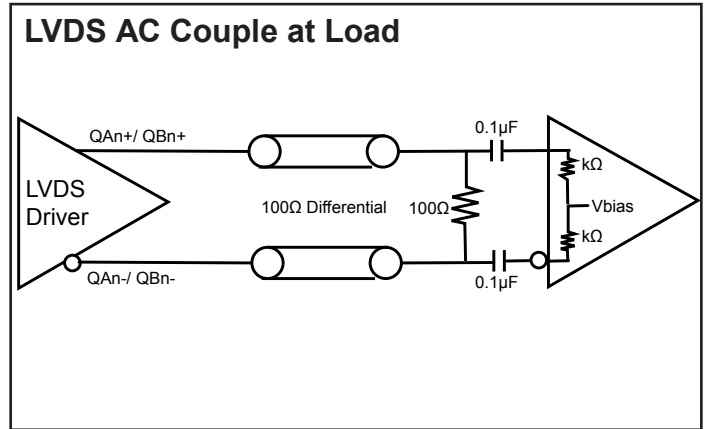
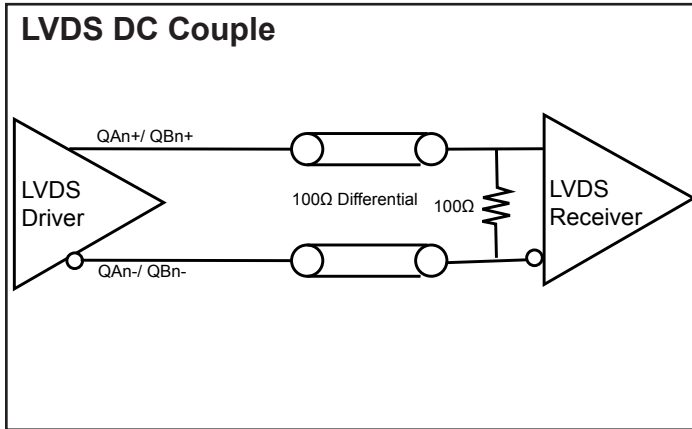


**LVPECL, AC Couple, Thevenin Equivalent**



**LVPECL, DC Couple, Thevenin Equivalent**





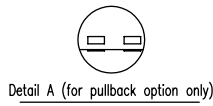
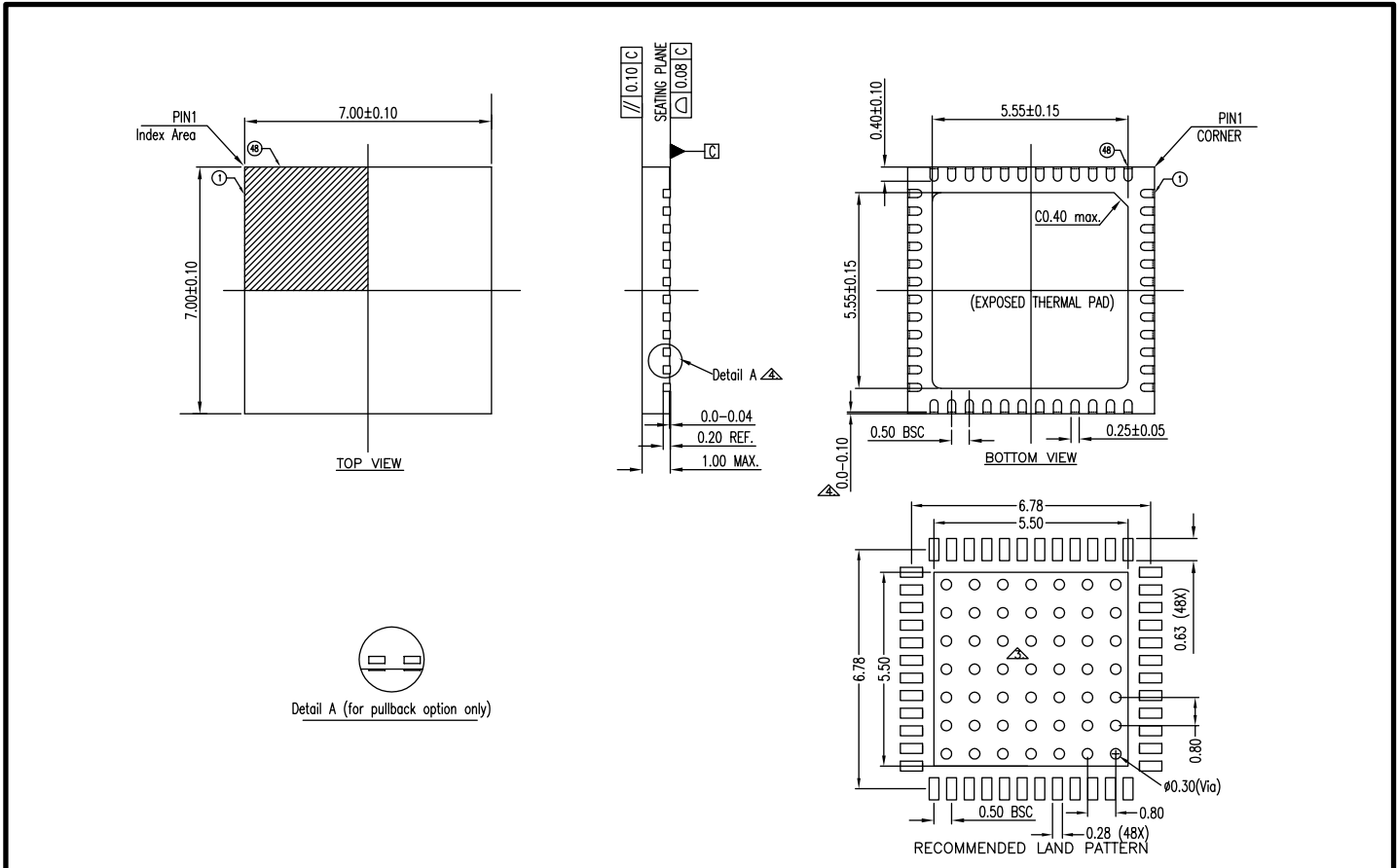
**Thermal Information**

| Symbol        | Description                            | Condition |            |
|---------------|--|-----------|------------|
| $\Theta_{JA}$ | Junction-to-ambient thermal resistance | Still air | 23.65 °C/W |
| $\Theta_{JC}$ | Junction-to-case thermal resistance    |           | 9.10 °C/W  |

**Part Marking**

Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

**Packaging Mechanical: 48-TQFN (ZD)**



- NOTE :
1. All dimensions are in mm. Angles in degree.
  2. Refer JEDEC MO-220
  3. Thermal Pad Soldering Area
  4. Depending on the method of lead termination at the edge of the package, pull back maybe present.
  5. Recommended Land Pattern is for reference only.

|  |   |                |
|--|---|----------------|
| <b>DIODES</b><br>INCORPORATED                                      | <b>PERICOM</b><br>A PRODUCT LINE OF DIODES INCORPORATED<br>ENABLING SERIAL CONNECTIVITY | DATE: 07/26/16 |
| <b>DESCRIPTION: 48-Contact, Very Thin Quad Flat No-Lead (TQFN)</b> |   |                |
| <b>PACKAGE CODE: ZD (ZD48)</b>                                     |   |                |
| <b>DOCUMENT CONTROL #: PD-2045</b>                                 |   |                |
| <b>REVISION: F</b>   |   |                |

16-0151

For latest package info.  
please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

**Ordering Information**

| Ordering Code    | Package Code | Package Type                                   | Operating Temperature |
|------------------|--------------|--|-----------------------|
| PI6C5912016ZDIEX | ZD           | 48-Contact, Very Thin Quad Flat No-Lead (TQFN) | -40°C to 85°C         |

**Notes:**

1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See <http://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. Thermal characteristics can be found on the company web site at [www.diodes.com/design/support/packaging/](http://www.diodes.com/design/support/packaging/)
3. E = Pb-free and Green
4. X suffix = Tape/Reel

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- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
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- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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