8-Bit, High Speed, Multiplying D/A Converter

Data Sheet

DAC08

FEATURES

Fast settling output current: 85 ns
Full-scale current prematched to ±1 LSB
Direct interface to TTL, CMOS, ECL, HTL, PMOS
Nonlinearity to 0.1% maximum over temperature range
High output impedance and compliance: −10 V to +18 V
Complementary current outputs
Wide range multiplying capability: 1 MHz bandwidth
Low FS current drift: ±10 ppm/°C
Wide power supply range: ±4.5 V to ±18 V
Low power consumption: 33 mW at ±5 V
Low cost

GENERAL DESCRIPTION

The DAC08 series of 8-bit monolithic digital-to-analog converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85 ns settling times with very low glitch energy and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full-scale trimming in most applications.

Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic input.

High voltage compliance complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp. All DAC08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as ±0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5 V to ±18 V power supply range, with 33 mW power consumption attainable at ±5 V supplies.

The compact size and low power consumption make the DAC08 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883, Level B are available.

DAC08 applications include 8-bit, 1 µs A/D converters, servo motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, LCD display drivers, high speed modems, and other applications where low cost, high speed, and complete input/output versatility are required.

FUNCTIONAL BLOCK DIAGRAM

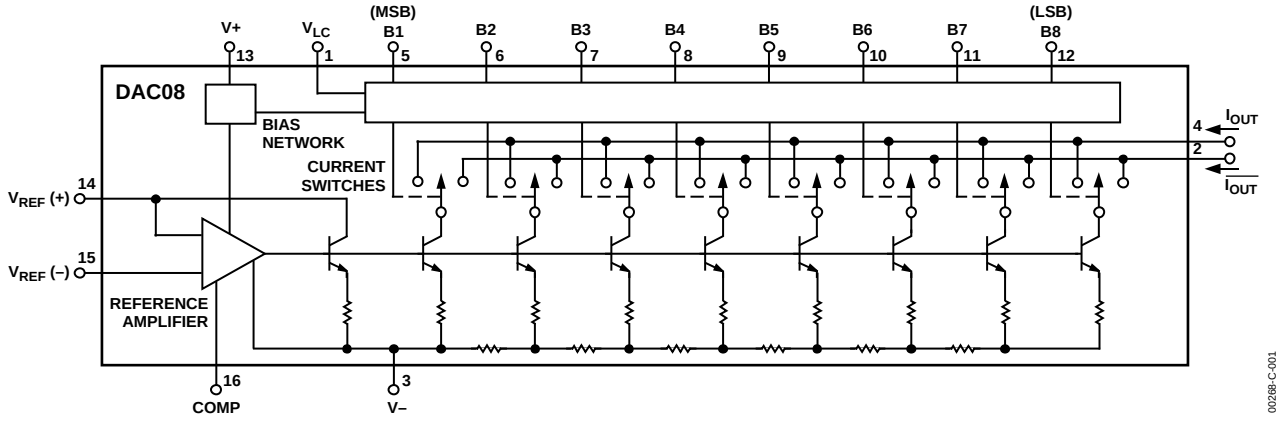

Figure 1.

Document Feedback

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REVISION HISTORY

3/16—Rev. C to Rev. D

Added Thermal Resistance Section ... 5
Changes to Table 4 ... 5
Change to Figure 29 ... 12
Updated Outline Dimensions ... 18
Changes to Ordering Guide ... 10

11/04—Rev. B to Rev. C

Changed SO to SOIC ... Universal
Removed DIE ... Universal
Changes to Figure 30, Figure 31, Figure 32 ... 12
Change to Figure 33 ... 15
Added Table 4 ... 16
Updated Outline Dimensions ... 17
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2/02—Rev. A to Rev. B

Edits to Specifications ... 2
Edits to Absolute Maximum Ratings ... 3
Edits to Ordering Guide ... 3
Edits to Wafer Test Limits ... 5
Edit to Figure 13 ... 8
Edits to Figures 14 and 15 ... 9

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = ±15 V, I_{REF} = 2.0 mA, −55°C ≤ T_A ≤ +125°C for DAC08/DAC08A, 0°C ≤ T_A ≤ +70°C for DAC08E and DAC08H, −40°C to +85°C for DAC08C, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

Table 1.

			DAC08A/DAC08H			DAC08E			DAC08C			
Parameter	**Symbol**	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION			8			8			8			Bits
MONOTONICITY			8			8			8			Bits
NONLINEARITY	NL				±0.1			±0.19			±0.39	%FS
SETTLING TIME	t_S	To ±1/2 LSB, all bits switched on or off, T_A = 25°C[1]		85	135		85	150		85	150	ns
PROPAGATION DELAY												
Each Bit	t_{PLH}	T_A = 25°C[1]		35	60		35	60		35	60	ns
All Bits Switched	t_{PHL}			35	60		35	60		35	60	ns
FULL-SCALE TEMPCO[1]	TCI_{FS}			±10	±50		±10	±80		±10	±80	ppm/°C
		DAC08E						±50				
OUTPUT VOLTAGE												
Compliance	V_{OC}	Full-scale current										
(True Compliance)		Change <1/2 LSB, R_{OUT} > 20 MΩ typ	−10		+18	−10		+18	−10		+18	V
FULL RANGE CURRENT	I_{FR4}	V_{REF} = 10.000 V R14, R15 = 5.000 kΩ T_A = 25°C	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
FULL RANGE SYMMETRY	I_{FRS}	$I_{FR4} - I_{FR2}$		±0.5	±4		±1	±8		±2	±16	µA
ZERO-SCALE CURRENT	I_{ZS}			0.1	1		0.2	2		0.2	4	µA
OUTPUT CURRENT RANGE	I_{OR1}	R14, R15 = 5.000 kΩ	2.1			2.1			2.1			mA
	I_{OR2}	V_{REF} = +15.0 V, V− = −10 V										
		V_{REF} = +25.0 V, V− = −12 V	4.2			4.2			4.2			mA
OUTPUT CURRENT NOISE		I_{REF} = 2 mA		25			25			25		nA
LOGIC INPUT LEVELS												
Logic 0	V_{IL}	V_{LC} = 0 V			0.8			0.8			0.8	V
Logic 1	V_{IL}		2			2			2			V
LOGIC INPUT CURRENT		V_{LC} = 0 V										
Logic 0	I_{IL}	V_{IN} = −10 V to +0.8 V		−2	−10		−2	−10		−2	−10	µA
Logic 1	I_{IH}	V_{IN} = 2.0 V to 18 V		0.002	10		0.002	10		0.002	10	µA
LOGIC INPUT SWING	V_{IS}	V− = −15 V	−10		+18	−10		+18	−10		+18	V
LOGIC THRESHOLD RANGE	V_{THR}	V_S = ±15 V[1]	−10		+13.5	−10		+13.5	−10		+13.5	V
REFERENCE BIAS CURRENT	I_{15}			−1	−3		−1	−3		−1	−3	µA
REFERENCE INPUT	dI/dt	R_{EQ} = 200 Ω	4	8		4	8		4	8		mA/µs
SLEW RATE		R_L = 100 Ω										
		C_C = 0 pF. See Figure 7.[1]										

Parameter	Symbol	Test Conditions/Comments	DAC08A/DAC08H Min	DAC08A/DAC08H Typ	DAC08A/DAC08H Max	DAC08E Min	DAC08E Typ	DAC08E Max	DAC08C Min	DAC08C Typ	DAC08C Max	Unit
POWER SUPPLY SENSITIVITY	$PSSI_{FS+}$	V+ = 4.5 V to 18 V		±0.0003	±0.01		±0.0003	±0.01		±0.0003	±0.01	$\%\Delta I_O/\%\Delta V+$
	$PSSI_{FS-}$	V− = −4.5 V to −18 V		±0.002	±0.01		±0.002	±0.01		±0.002	±0.01	$\%\Delta I_O/\%\Delta V-$
		I_{REF} = 1.0 mA										
POWER SUPPLY CURRENT	I+	V_S = ±5 V, I_{REF} = 1.0 mA		2.3	3.8		2.3	3.8		2.3	3.8	mA
	I−			−4.3	−5.8		−4.3	−5.8		−4.3	−5.8	mA
	I+	V_S = +5 V, −15 V		2.4	3.8		2.4	3.8		2.4	3.8	mA
	I−	I_{REF} = 2.0 mA		−6.4	−7.8		−6.4	−7.8		−6.4	−7.8	mA
	I+	V_S = ±15 V		2.5	3.8		2.5	3.8		2.5	3.8	mA
	I−	I_{REF} = 2.0 mA		−6.5	−7.8		−6.5	−7.8		−6.5	−7.8	mA
POWER DISSIPATION	P_D	±5 V, I_{REF} = 1.0 mA +5 V, −15 V		33	48		33	48		33	48	mW
		I_{REF} = 2.0 mA ±15 V, I_{REF} = 2.0 mA		108	136		103	136		108	136	mW
				135	174		135	174		135	174	mW

[1] Guaranteed by design.

TYPICAL ELECTRICAL CHARACTERISTICS

V_S = ±15 V, and I_{REF} = 2.0 mA, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.

Table 2.

Parameter	Symbol	Test Conditions/Comments	All Grades Typical	Unit
REFERENCE INPUT SLEW RATE	dI/dt		8	mA/µs
PROPAGATION DELAY	t_{PLH}, t_{PHL}	T_A = 25°C, any bit	35	ns
SETTLING TIME	t_S	To ±1/2 LSB, all bits switched on or off, T_A = 25°C	85	ns

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Operating Temperature	
DAC08AQ, DAC08Q	−55°C to +125°C
DAC08HQ, DAC08EQ, DAC08CQ	0°C to +70°C
DAC08CP, DAC08CS	−40°C to +85°C
Junction Temperature (T_J)	−65°C to +150°C
Storage Temperature Q Package	−65°C to +150°C
Storage Temperature P Package	−65°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C
V+ Supply to V− Supply	36 V
Logic Inputs	V− to V− + 36 V
V_{LC}	V− to V+
Analog Current Outputs (at V_{S-} = 15 V)	4.25 mA
Reference Input (V_{14} to V_{15})	V− to V+
Reference Input Differential Voltage (V_{14} to V_{15})	±18 V
Reference Input Current (I_{14})	5.0 mA

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for worst case mounting conditions, that is, θ_{JA} is specified for device in socket for CERDIP, PDIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead CERDIP (Q)	100	16	°C/W
16-Lead PDIP (P)	82	39	°C/W
20-Terminal LCC (RC)	76	36	°C/W
16-Lead SOIC (S)	111	35	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

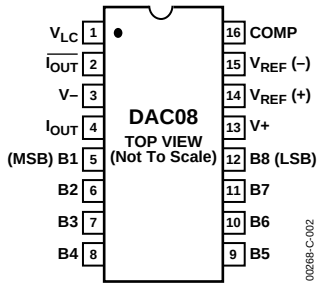


Figure 2. 16-Lead Dual In-Line Package (PDIP and CERDIP)

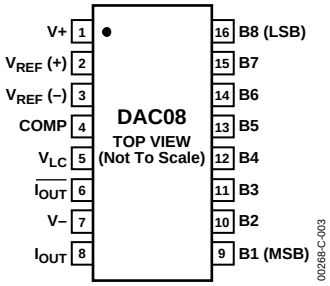


Figure 3. 16-Lead Standard Small Outline Package (SOIC_N)

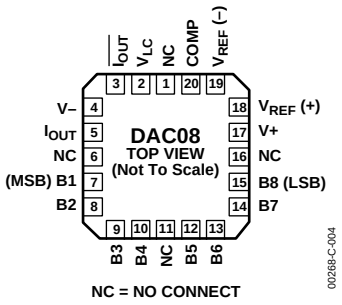


Figure 4. DAC08RC/883 20-Terminal Ceramic Leadless Chip Carrier (LCC)

TEST AND BURN-IN CIRCUITS

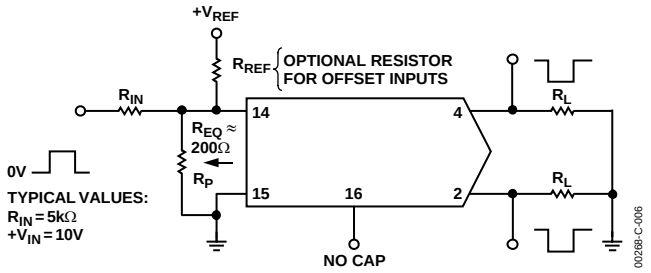


Figure 5. Pulsed Reference Operation

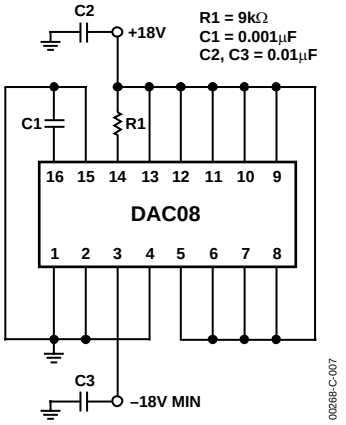


Figure 6. Burn-In Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

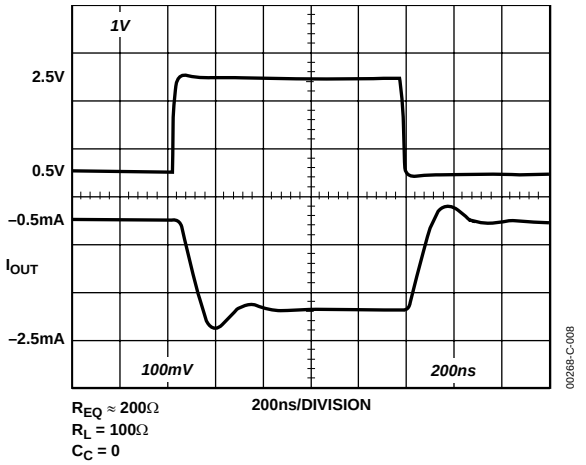


Figure 7. Fast Pulsed Reference Operation

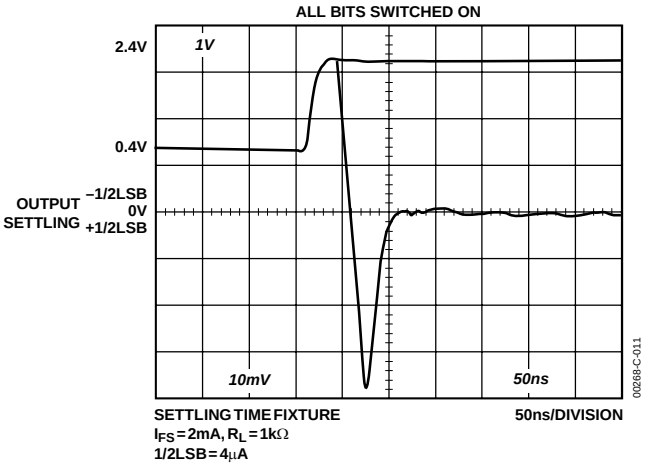


Figure 10. Full-Scale Settling Time

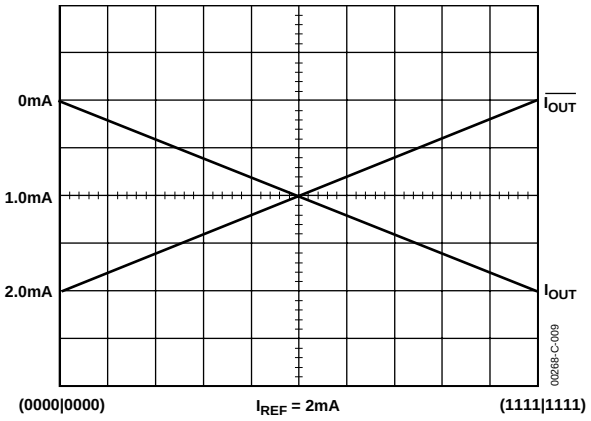


Figure 8. True and Complementary Output Operation

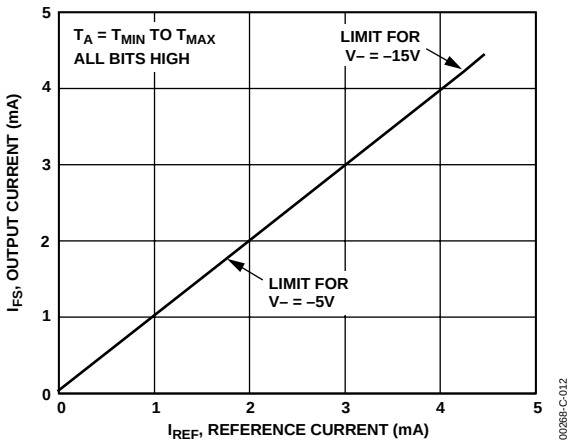


Figure 11. Full-Scale Current vs. Reference Current

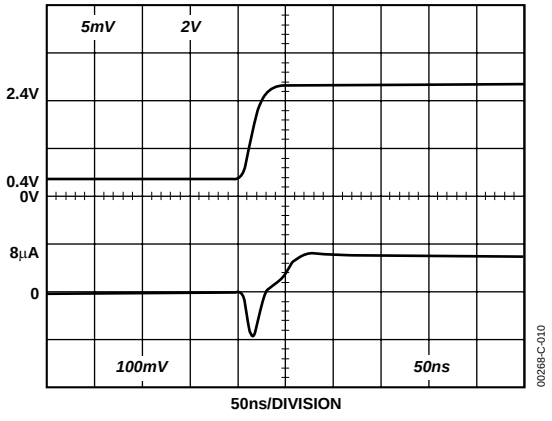


Figure 9. LSB Switching

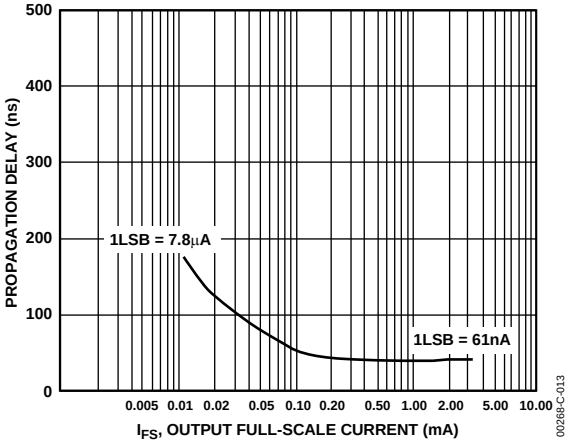


Figure 12. LSB Propagation Delay vs. I_{FS}

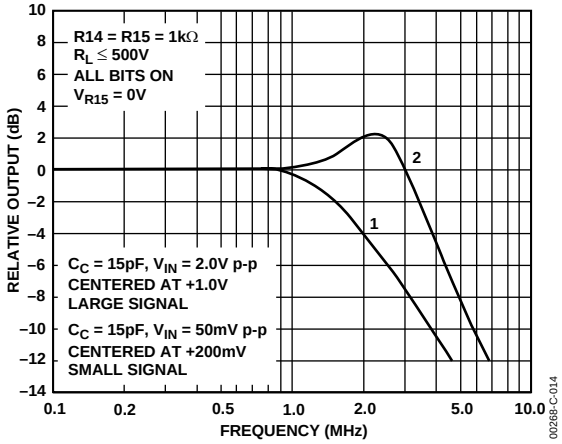


Figure 13. Reference Input Frequency Response

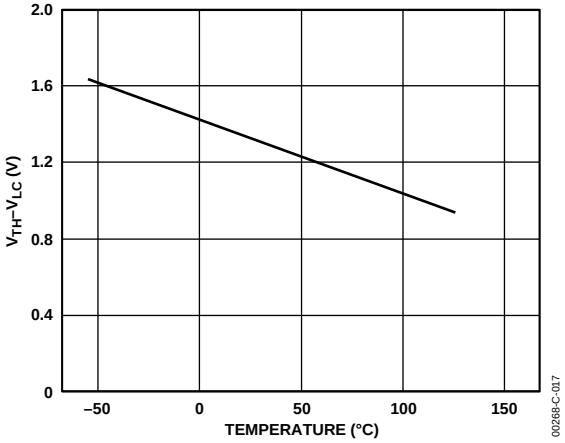


Figure 16. $V_{TH} - V_{LC}$ vs. Temperature

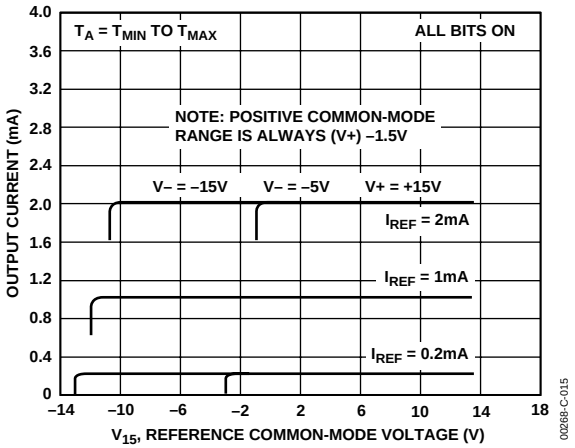


Figure 14. Reference Amplifier Common-Mode Range

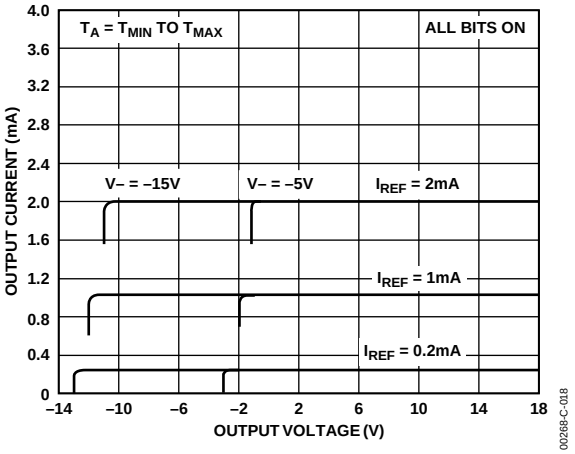


Figure 17. Output Current vs. Output Voltage (Output Voltage Compliance)

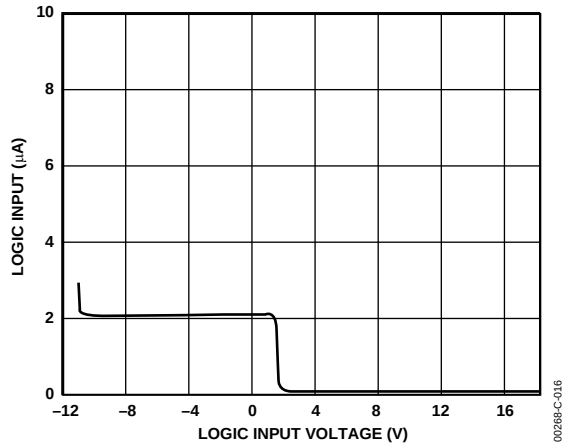


Figure 15. Logic Input Current vs. Input Voltage

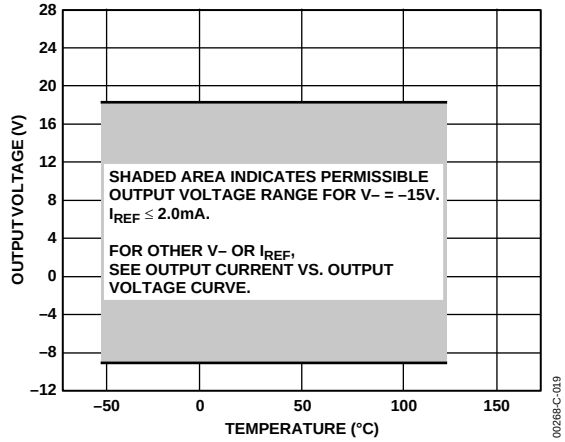
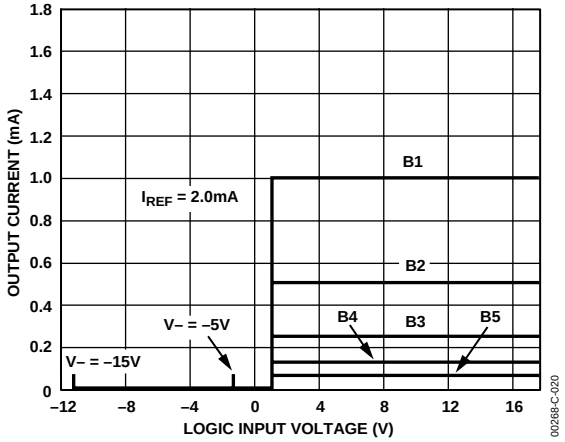


Figure 18. Output Voltage Compliance vs. Temperature



NOTE:
B1 THROUGH B8 HAVE IDENTICAL TRANSFER CHARACTERISTICS. BITS ARE FULLY SWITCHED WITH LESS THAN 1/2 LSB ERROR, AT LESS THAN ±100mV FROM ACTUAL THRESHOLD. THESE SWITCHING POINTS ARE GUARANTEED TO LIE BETWEEN 0.8V AND 2.0V OVER THE OPERATING TEMPERATURE RANGE (V_{LC} = 0.0V).

Figure 19. Bit Transfer Characteristics

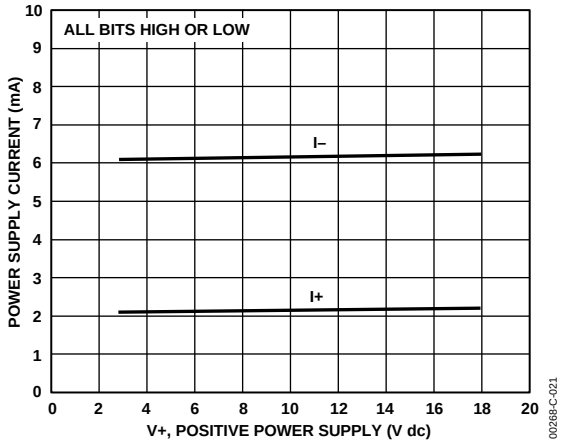


Figure 20. Power Supply vs. V+

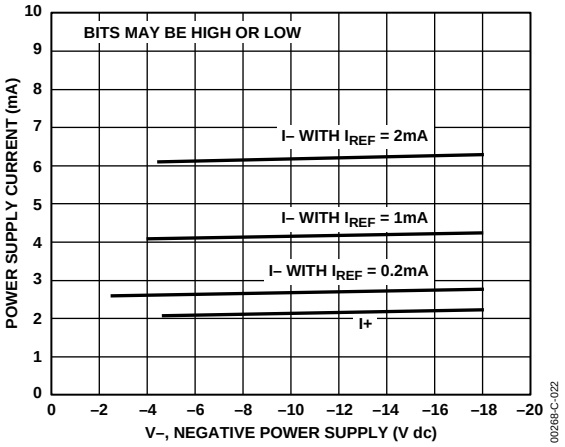


Figure 21. Power Supply Current vs. V–

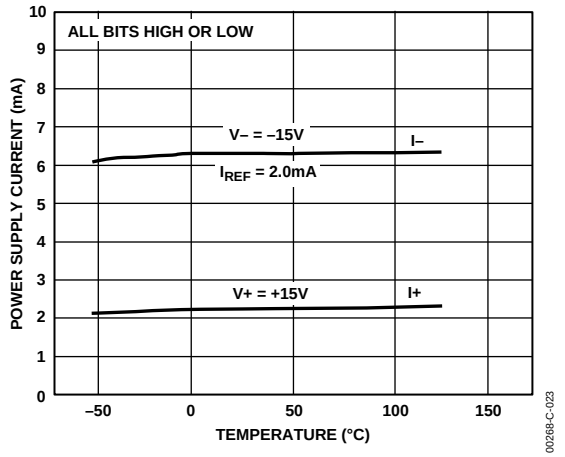


Figure 22. Power Supply Current vs. Temperature

BASIC CONNECTIONS

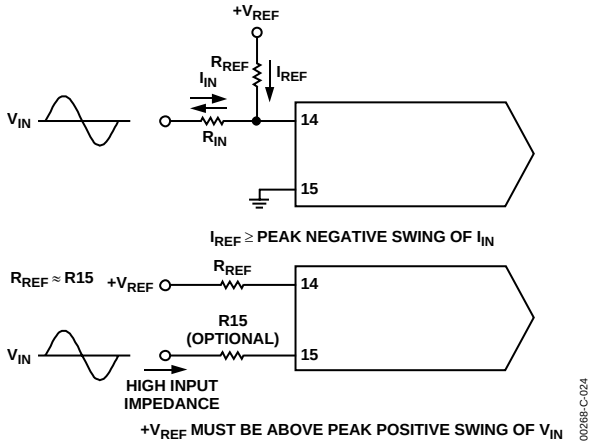


Figure 23. Accommodating Bipolar References

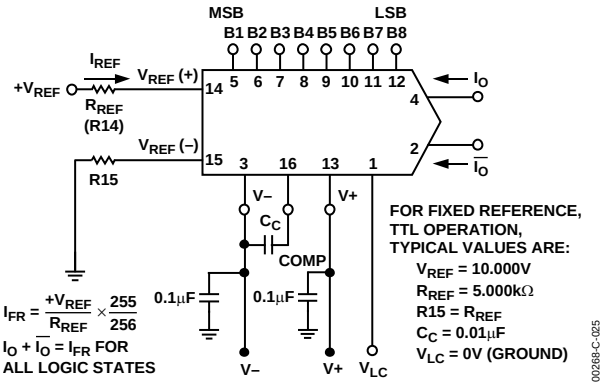
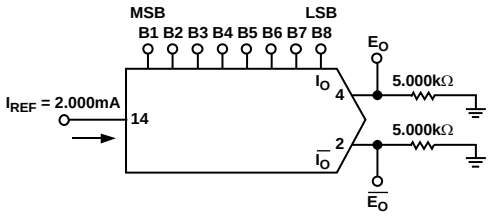


Figure 24. Basic Positive Reference Operation



	B1	B2	B3	B4	B5	B6	B7	B8	I_O	$\overline{I_O}$	E_O	$\overline{E_O}$
FULL RANGE	1	1	1	1	1	1	1	1	1.992	0.000	–9.960	–0.000
HALF SCALE +LSB	1	0	0	0	1	0	0	1	1.008	0.984	–5.040	–4.920
HALF SCALE	1	0	0	0	1	0	0	0	1.000	0.992	–5.000	–4.960
HALF SCALE –LSB	0	1	1	1	0	1	1	1	0.992	1.000	–4.960	–5.000
ZERO SCALE +LSB	0	0	0	0	0	0	0	1	0.008	1.984	–0.040	–9.920
ZERO SCALE	0	0	0	0	0	0	0	0	0.000	1.992	0.000	–9.960

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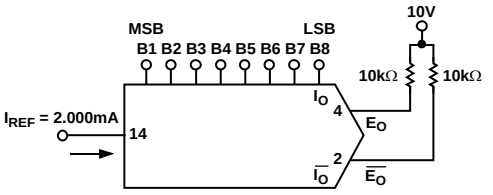
Figure 25. Basic Unipolar Negative Operation



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
POS. FULL RANGE	1	1	1	1	1	1	1	1	–9.920	+10.000
POS. FULL RANGE –LSB	1	1	1	1	1	1	1	0	–9.840	+9.920
ZERO SCALE +LSB	1	0	0	0	0	0	0	1	–0.080	+0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	+0.080
ZERO SCALE –LSB	0	1	1	1	1	1	1	1	+0.080	0.000
NEG. FULL SCALE +LSB	0	0	0	0	0	0	0	1	+9.920	–9.840
NEG. FULL SCALE	0	0	0	0	0	0	0	0	+10.000	–9.920

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Figure 26. Basic Bipolar Output Operation

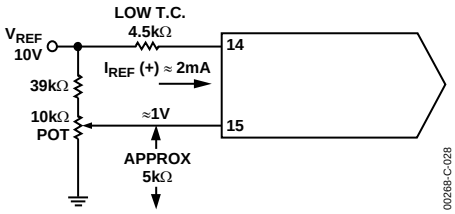


Figure 27. Recommended Full-Scale Adjustment Circuit

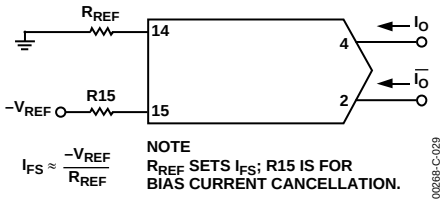
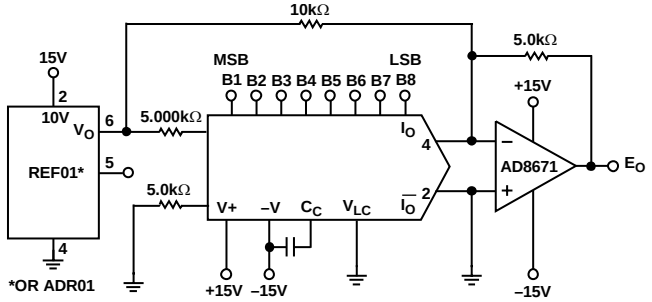


Figure 28. Basic Negative Reference Operation



	B1	B2	B3	B4	B5	B6	B7	B8	E_O
POS. FULL RANGE	1	1	1	1	1	1	1	1	+4.960
ZERO SCALE	1	0	0	0	0	0	0	0	0.000
NEG. FULL SCALE +1LSB	0	0	0	0	0	0	0	1	–4.960
NEG. FULL SCALE	0	0	0	0	0	0	0	0	–5.000

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Figure 29. Offset Binary Operation

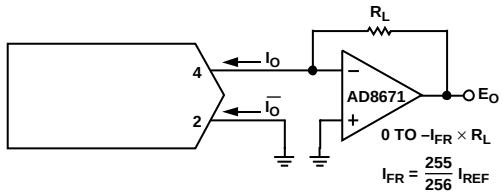


Figure 30. Positive Low Impedance Output Operation

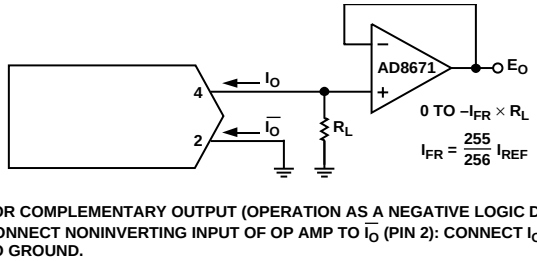


Figure 31. Negative Low Impedance Output Operation

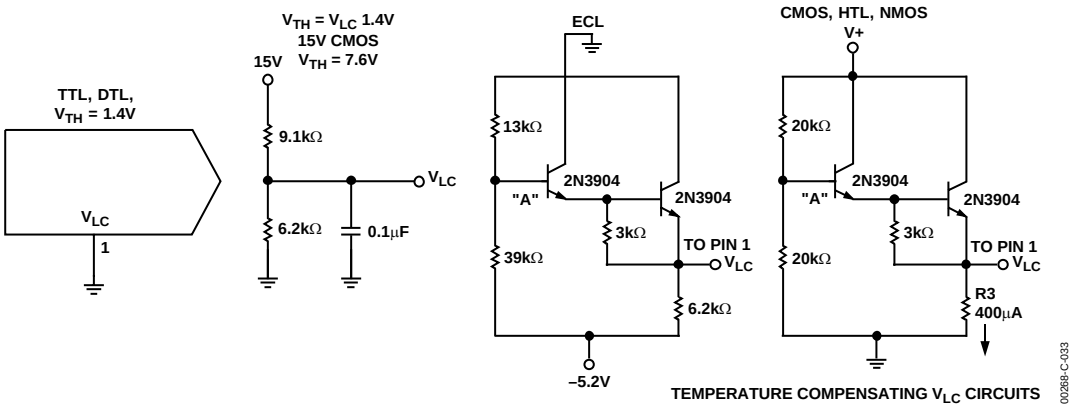


Figure 32. Interfacing with Various Logic Families

APPLICATION INFORMATION

REFERENCE AMPLIFIER SETUP

The DAC08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to 4.0 mA. The full-scale output current is a linear function of the reference current and is given by

$$I_{FR} = \frac{255}{256} \times I_{REF}$$

where $I_{REF} = I_{14}$

In positive reference applications, an external positive reference voltage forces current through R14 into the $V_{REF(+)}$ terminal (Pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at Pin 15; reference current flows from ground through R14 into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at Pin 15. The voltage at Pin 14 is equal to and tracks the voltage at Pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) cancels bias current errors; R15 may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or Pin 15. The negative common-mode range of the reference amplifier is given by V_{CM} – = V− plus (I_{REF} × 1 kΩ) plus 2.5 V. The positive common-mode range is V+ less 1.5 V.

When a dc reference is used, a reference bypass capacitor is recommended. A 5.0 V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 must be split into two resistors with the junction bypassed to ground with a 0.1 µF capacitor.

For most applications, the tight relationship between I_{REF} and I_{FS} eliminates the need for trimming I_{REF}. If required, full-scale trimming can be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full-scale trimming that eliminates potentiometer T.C. effects is shown in the recommended full-scale adjustment circuit (Figure 27).

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common-mode range. The recommended range for operation with a dc reference current is 0.2 mA to 4.0 mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications require the reference amplifier to be compensated using a capacitor from Pin 16 to V−. The value of this capacitor depends on the impedance presented to Pin 14; for R14 values of 1.0 kΩ, 2.5 kΩ, and 5.0 kΩ, minimum values of C_C are 15 pF, 37 pF, and 75 pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin, so the ratio of C_C (pF) to R14 (kΩ) = 15.

For fastest response to a pulse, low values of R14 enabling small C_C values must be used. If Pin 14 is driven by a high impedance such as a transistor current source, none of the preceding values suffice, and the amplifier must be heavily compensated, which decreases overall bandwidth and slew rate. For R14 = 1 kΩ and C_C = 15 pF, the reference amplifier slews at 4 mA/µs, enabling a transition from I_{REF} = 0 to I_{REF} = 2 mA in 500 ns.

Operation with pulse inputs to the reference amplifier can be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full-scale transition (0 mA to 2 mA) occurs in 120 ns when the equivalent impedance at Pin 14 is 200 Ω and C_C = 0. This yields a reference slew rate of 16 mA/µs, which is relatively independent of the R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC08 design incorporates a unique logic input circuit that enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2 µA logic input current, and completely adjustable logic threshold voltage. For V− = −15 V, the logic inputs may swing between −10 V and +18 V. This enables direct interface with 15 V CMOS logic, even when the DAC08 is powered from a 5 V supply. Minimum input logic swing and minimum logic threshold voltage are given by

$$V- + (I_{REF} \times 1\ k\Omega) + 2.5\ V$$

The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (Pin 1, V_{LC}). Figure 16 shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL and DTL interface, simply ground Pin 1. When interfacing ECL, an I_{REF} = 1 mA is recommended. For interfacing other logic families, see Figure 32. For general set-up of the logic control circuit, note that Pin 1 sources 100 µA typical; external circuitry must be designed to accommodate this current.

Fastest settling times are obtained when Pin 1 sees a low impedance. If Pin 1 is connected to a 1 kΩ divider, for example, it must be bypassed to ground by a 0.01 µF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FS}$. Current appears at the true (I_O) output when a 1 (logic high) is applied to each logic input. As the binary count increases, the sink current at Pin 4 increases proportionally, in the fashion of a positive logic DAC. When a 0 is applied to any input bit, that current is turned off at Pin 4 and turned on at Pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic DAC. Both outputs may be used simultaneously.

If one of the outputs is not required, it must be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current to voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36 V above V− and is independent of the positive supply. Negative compliance is given by

$$V- + (I_{REF} \times 1\ k\Omega) + 2.5\ V$$

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC08 operates over a wide range of power supply voltages from a total supply of 9 V to 36 V. When operating at supplies of ±5 V or lower, $I_{REF} \leq 1$ mA is recommended. Low reference current operation decreases power consumption and increases negative compliance (Figure 11), reference amplifier negative common-mode range (Figure 14), negative logic input range (Figure 15), and negative logic threshold range (Figure 16). For example, operation at −4.5 V with I_{REF} = 2 mA is not recommended because negative output compliance reduces to near zero. Operation from lower supplies is possible; however, at least 8 V total must be applied to ensure turn on of the internal bias network.

Symmetrical supplies are not required, as the DAC08 is quite insensitive to variations in supply voltage. Battery operation is feasible because no ground connection is required; however, an artificial ground can ensure logic swings, etc., remain between acceptable limits. Power consumption is calculated as follows:

$$P_D = (I+)(V+) + (I-)(V-)$$

A useful feature of the DAC08 design is that supply current is constant and independent of input logic states. This is useful in cryptographic applications and further reduces the size of the power supply bypass capacitors.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC08 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is low, typically ±10 ppm/°C, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 must match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC08 decrease approximately 10% at –55°C. At +125°C, an increase of about 15% is typical.

The reference amplifier must be compensated by using a capacitor from Pin 16 to V−. For fixed reference operation, a 0.01 µF capacitor is recommended. For variable reference applications, refer to the Reference Amplifier Compensation for Multiplying Applications section.

MULTIPLYING OPERATION

The DAC08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4 µA to 4 mA. Monotonic operation is maintained over a typical range of I_{REF} from 100 µA to 4.0 mA.

SETTLING TIME

The DAC08 is capable of extremely fast settling times, typically 85 ns at I_{REF} = 2.0 mA. Judicious circuit design and careful board layout must obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35 ns for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35 ns, with each progressively larger bit taking successively longer. The MSB settles in 85 ns, thus determining the overall settling time of 85 ns. Settling to 6-bit accuracy requires about 65 ns to 70 ns. The output capacitance of the DAC08, including the package, is approximately 15 pF; therefore the output RC time constant dominates settling time if $R_L > 500\ \Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measuring the settling time requires the ability to accurately resolve ±4 µA; therefore a 1 kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture shown in Figure 33 uses a cascade design to permit driving a 1 kΩ load with less than 5 pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1.0 mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling time is observed at lower values of I_{REF}.

DAC08 switching transients or “glitches” are very low and can be further reduced by small capacitive loads at the output at a minor sacrifice in settling time. Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors because the supply current drain is independent of input logic states; 0.1 µF capacitors at the supply pins provide full transient protection.

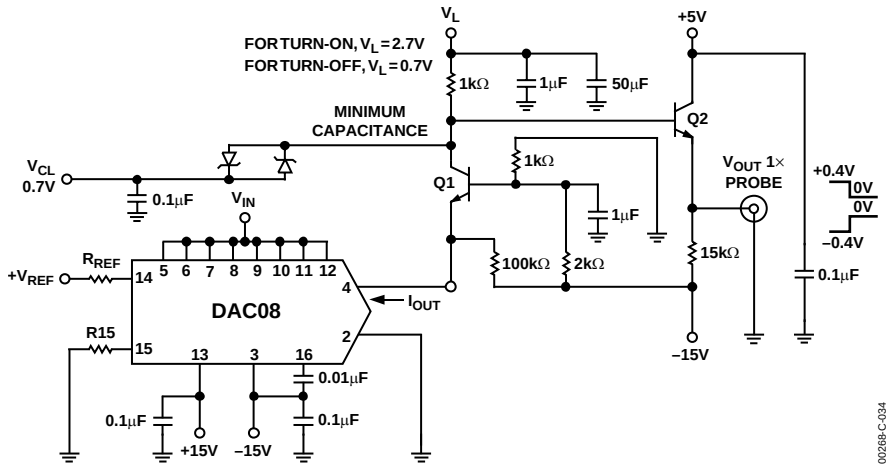


Figure 33. Settling Time Measurement

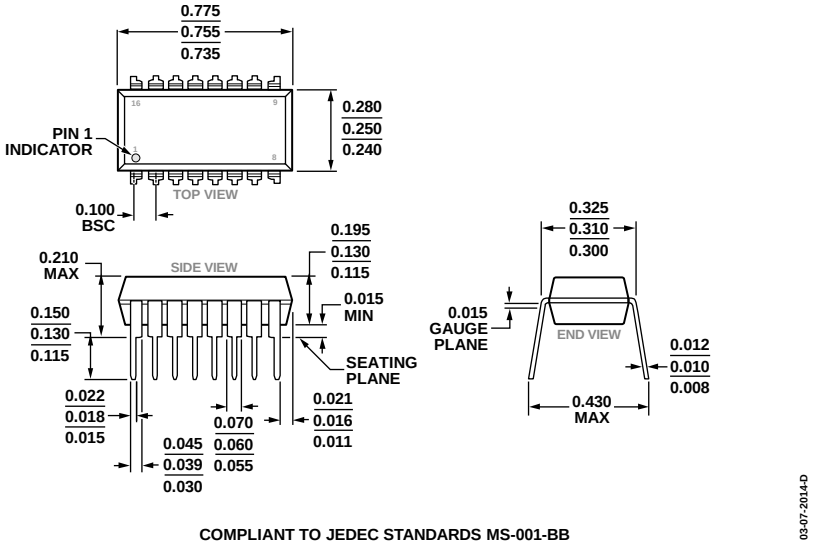
ANALOG DEVICES, INC., CURRENT OUTPUT DACs

Table 4 lists the latest DACs available from Analog Devices.

Table 5.

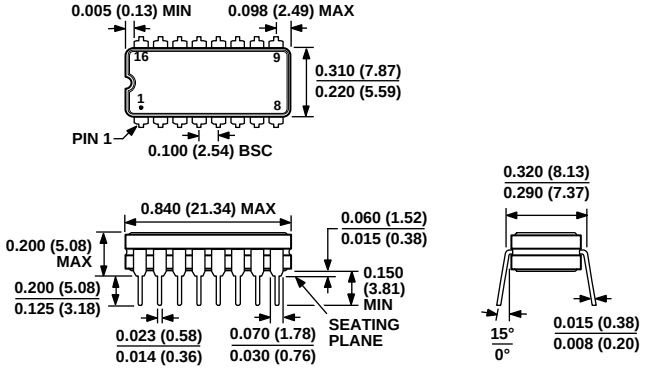
Model	Bits	Outputs	Interface	Package	Comments
AD5425	8	1	SPI, 8-bit load	MSOP-10	Fast 8-bit load; see also AD5426
AD5426	8	1	SPI	MSOP-10	See also AD5425 fast load
AD5450	8	1	SPI	SOT23-8	See also AD5425 fast load
AD5424	8	1	Parallel	TSSOP-16	
AD5429	8	2	SPI	TSSOP-16	
AD5428	8	2	Parallel	TSSOP-20	
AD5432	10	1	SPI	MSOP-10	
AD5451	10	1	SPI	SOT23-8	
AD5433	10	1	Parallel	TSSOP-20	
AD5439	10	2	SPI	TSSOP-16	
AD5440	10	2	Parallel	TSSOP-24	
AD5443	12	1	SPI	MSOP-10	See also AD5452 and AD5444
AD5452	12	1	SPI	SOT23-8	Higher accuracy version of AD5443; see also AD5444
AD5445	12	1	Parallel	TSSOP-20	
AD5444	12	1	SPI	MSOP-10	Higher accuracy version of AD5443; see also AD5452
AD5449	12	2	SPI	TSSOP-16	
AD5415	12	2	SPI	TSSOP-24	Uncommitted resistors
AD5447	12	2	Parallel	TSSOP-24	
AD5405	12	2	Parallel	LFCSP-40	Uncommitted resistors
AD5453	14	1	SPI	SOT23-8	
AD5553	14	1	SPI	MSOP-8	
AD5556	14	1	Parallel	TSSOP-28	
AD5446	14	1	SPI	MSOP-10	MSOP version of AD5453; compatible with AD5443, AD5432, and AD5426
AD5555	14	2	SPI	TSSOP-16	
AD5557	14	2	Parallel	TSSOP-38	
AD5543	16	1	SPI	MSOP-8	
AD5546	16	1	Parallel	TSSOP-28	
AD5545	16	2	SPI	TSSOP-16	
AD5547	16	2	Parallel	TSSOP-38	

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-BB

Figure 34. 16-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-16)
Dimensions shown in inches



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 35. 16-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-16)
Dimensions shown in inches and (millimeters)

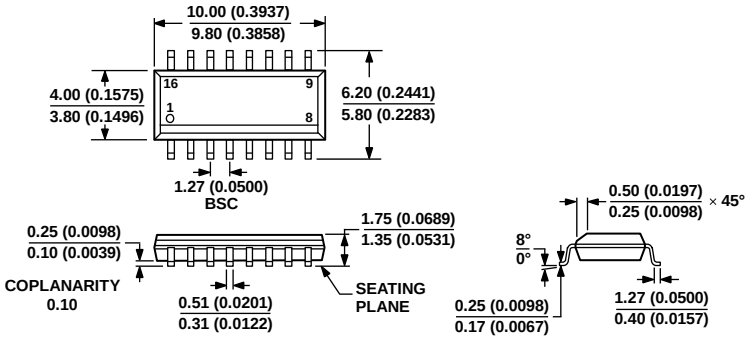


Figure 36. 16-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-16)
Dimensions shown in millimeters and (inches)

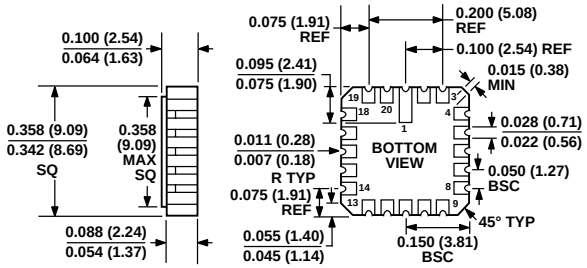


Figure 37. 20-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-20-1)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1, 2, 3]	NL	Temperature Range	Package Description	Package Option	No. Parts Per Container
DAC08AQ	±0.10%	−55°C to +125°C	16-Lead CERDIP	Q-16	25
DAC08AQ/883C	±0.10%	−55°C to +125°C	16-Lead CERDIP	Q-16	25
DAC08HQ	±0.10%	0°C to 70°C	16-Lead CERDIP	Q-16	25
DAC08Q	±0.19%	−55°C to +125°C	16-Lead CERDIP	Q-16	25
DAC08RC/883C	±0.19%	−55°C to +125°C	20-Terminal LCC	E-20-1	55
DAC08EQ	±0.19%	0°C to 70°C	16-Lead CERDIP	Q-16	25
DAC08ES	±0.19%	0°C to 70°C	16-Lead SOIC	R-16	47
DAC08ESZ	±0.19%	0°C to 70°C	16-Lead SOIC	R-16	47
DAC08ESZ-REEL	±0.19%	0°C to 70°C	16-Lead SOIC	R-16	2500
DAC08CP	±0.39%	−40°C to +85°C	16-Lead PDIP	N-16	25
DAC08CPZ	±0.39%	−40°C to +85°C	16-Lead PDIP	N-16	25
DAC08CS	±0.39%	−40°C to +85°C	16-Lead SOIC	R-16	47
DAC08CS-REEL	±0.39%	−40°C to +85°C	16-Lead SOIC	R-16	2500
DAC08CSZ	±0.39%	−40°C to +85°C	16-Lead SOIC	R-16	47
DAC08CSZ-REEL	±0.39%	−40°C to +85°C	16-Lead SOIC	R-16	2500
DAC08EPZ	±0.19%	0°C to 70°C	16-Lead PDIP	N-16	25

[1] Devices processed in total compliance to MIL-STD-883. Consult the factory for the 883 data sheet.
[2] For availability and burn-in information on the SOIC package, contact your local sales office.
[3] Z = RoHS Compliant Part.

NOTES

NOTES

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D00268-0-3/16(D)

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