

# AS1716

## Capacitive Sensor Interface

### 1 General Description

AS1716 is an analog front end specifically designed for unbiased Capacitive Sensors, as for instance Knock Sensors in Automotive, to be interfaced with Analog Digital Converters with Sample and Hold input stages.

The device provides differential inputs, a 1st order low pass filter to cutoff the high frequency noise components, differential to single ended conversion, programmable gain stage and a 2 pole low pass Multiple Feedback Filter.

The Knock Sensor is a Piezo Electric device that generates a voltage if it is stressed. It senses knock and transmits information to the electronic engine management control unit. This influences process control in the engine, for example timing and fuel injection until knock is eliminated.

The capacitive sensor is biased via resistors to a voltage level of  $V_{DDA}/2$ .

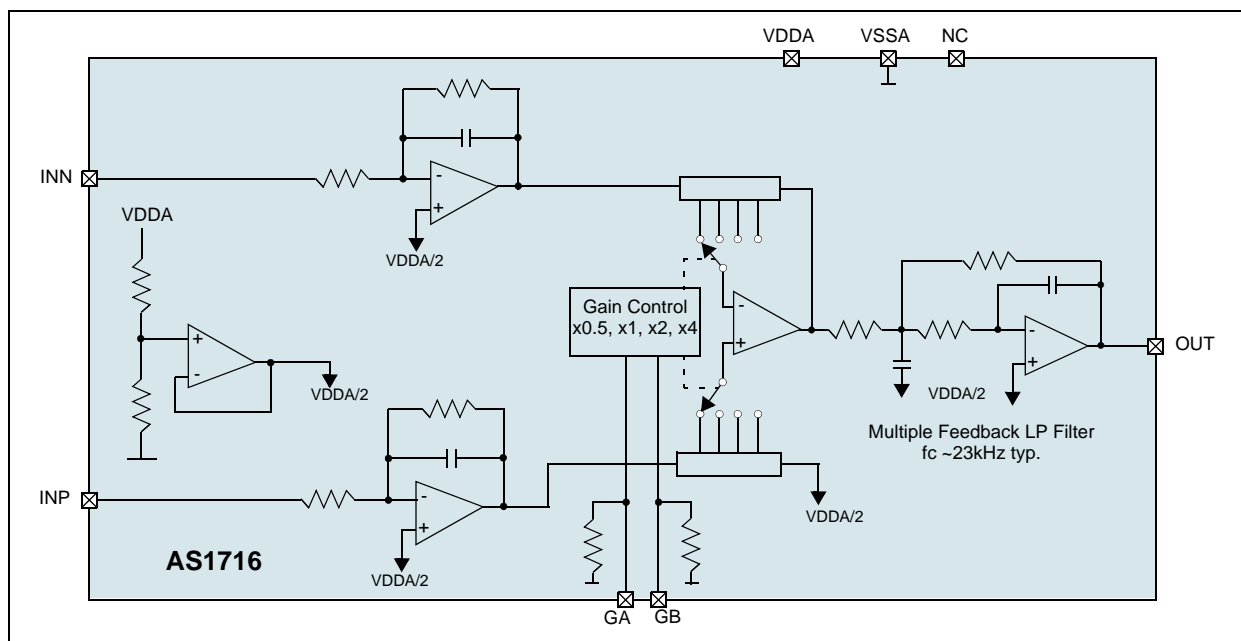
### 2 Key Features

- Differential input stage with wide input range
- Resistive sensor biasing ( $V_{DDA}/2$ )
- Programmable Gain (x0.5, x1, x2, x4)
- Internal 2<sup>nd</sup> order low pass Multiple Feedback Filter with a min. cut off frequency of 16kHz
- Single supply operation: 4.5V to 5.5V
- Operating Temperature range: -40°C to +125°C
- High CMRR: 55dB (min)
- EMC characterized by IEC 61967-4 (1Ω / 150Ω Method)
- EMC characterized by IEC 62132-4 (Direct Power Injection)
- Automotive qualified to AECQ100 for IC and PPAP level 3
- 8-pin SOIC Package

### 3 Applications

Analog front end for Capacitive Sensors to Analog to Digital Converters and DSP.

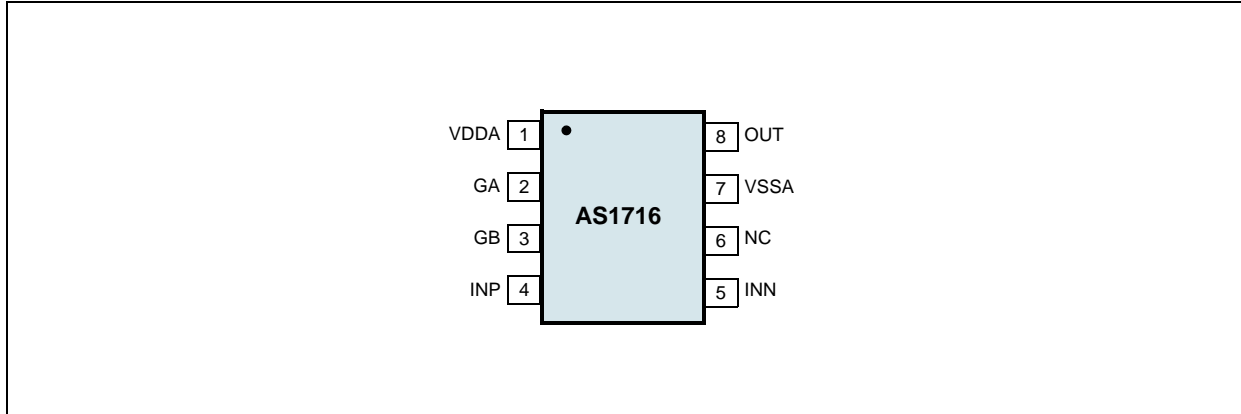
Figure 1. AS1716 - Block Diagram



## 4 Pinout

### Pin Assignment

Figure 2. Pin Assignments (Top View)



### Pin Description

Table 1. Pin Description

| Pin Name | Pin Number | Description  |
|----------|------------|--|
| VDDA     | 1          | Positive Supply  |
| GA       | 2          | Gain selection. Internal pull-down of 100kΩ                |
| GB       | 3          | Gain selection. Internal pull-down of 100kΩ                |
| INP      | 4          | Non-Inverting Input  |
| INN      | 5          | Inverting Input  |
| NC       | 6          | Not Connected. Must be left unconnected in the application |
| VSSA     | 7          | Negative Supply  |
| OUT      | 8          | Signal Output  |

## 5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Electrical Characteristics on page 4](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

| Parameter  | Min        | Max        | Units | Comments   |
|--|------------|------------|-------|--|
| <b>Electrical Parameters</b>                     |            |            |       |  |
| VDDA, VSSA                                       |            | +7         | V     |  |
| GA, GB, OUT, INP, INN, NC                        | VSSA - 0.3 | VDDA + 0.3 | V     | To get an overvoltage protection of up to +16V at the system level, apply external resistors (typ. 1k $\Omega$ ) on the pins INP and INN.  |
| Input Current (latch-up immunity)                | -100       | +100       | mA    | Norm: AEC-Q100-004, @T <sub>A</sub> = +25°C  |
| <b>Electrostatic Discharge</b>                   |            |            |       |  |
| Electrostatic Discharge HBM                      |            | ±4         | kV    | Norm: AEC-Q100-002, @T <sub>A</sub> = +25°C  |
| <b>Temperature Ranges and Storage Conditions</b> |            |            |       |  |
| Storage Temperature Range                        | -65        | +150       | °C    |  |
| Junction Temperature                             |            | +150       | °C    |  |
| Package Body Temperature                         |            | +260       | °C    | The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".<br>The lead finish for Pb-free leaded packages is matte tin (100% Sn). |
| Humidity non-condensing                          | 5          | 85         | %     |  |
| Moisture Sensitive Level                         |            | 3          |       | Represents a max. floor life time of 168h  |

## 6 Electrical Characteristics

Parameters are measured at  $V_{DDA} = 4.5V$  to  $5.5V$ ,  $R_{LOAD} = 100\Omega$  serial to  $C_{LOAD} = 10nF$ ,  $T_A = +25^\circ C$  and are referring to  $V_{SSA}$ , unless otherwise specified. Typical values are listed for reference only and will not be tested.

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 3. Electrical Characteristics

| Symbol                               | Parameter                          | Condition  | Min               | Typ              | Max               | Unit              |
|--------------------------------------|------------------------------------|--|-------------------|------------------|-------------------|-------------------|
| TAMB                                 | Operating Temperature Range        |  | -45               |                  | +125              | °C                |
| <b>DC Electrical Characteristics</b> |                                    |  |                   |                  |                   |                   |
| VDDA                                 | Supply Voltage Range               | @ pin VDDA   | 4.5               | 5                | 5.5               | V                 |
| IDDA                                 | Supply Current                     | @ pin VDDA   | 3                 | 4.5              | 9                 | mA                |
| PSRR <sup>1</sup>                    | Power Supply Rejection Ratio       |  |                   |                  | 6                 | dB                |
| VCM                                  | Common Mode input Range            | @ pins INN, INP  | VSSA              |                  | VDDA              | V                 |
| CMRR                                 | Common Mode Rejection Ratio        |  | 55                |                  |                   | dB                |
| RIN                                  | Differential Input Resistance      | between pins INN and INP   | 70                | 100              | 130               | kΩ                |
| VREF                                 | Internal Common Mode Input Voltage | INP shorted to INN   | $V_{DDA}/2 - 2\%$ | $V_{DDA}/2$      | $V_{DDA}/2 + 2\%$ | V                 |
| VOFF                                 | Offset Voltage                     | Gain1, $V_{INP} = V_{INN}$ @ $V_{CM} = V_{DDA}/2$ , @ pin OUT  | $V_{REF} - 10$    |                  | $V_{REF} + 10$    | mV                |
| VIL                                  | Logic Low (GA, GB)                 | @ pin GA and GB  |                   |                  | 1.2               | V                 |
| VIH                                  | Logic High (GA, GB)                | @ pin GA and GB  | 2.0               |                  |                   | V                 |
| I <sub>LEAK</sub>                    | Leakage Current (GA, GB)           | $V_{DDA} = 5V$ , Gain4   |                   | 1                |                   | μA                |
| VHYS <sup>1</sup>                    | Hysteresis                         | @ pin GA and GB  | 100               | 200              |                   | mV                |
| RPD                                  | Pull-Down Resistor                 | @ pin GA and GB  | 50                | 100              | 150               | kΩ                |
| Gain0.5                              | Overall gain 0.5                   | GA = GB = 1  | 0.5-10%           | 0.5              | 0.5+10%           |                   |
| Gain1                                | Overall gain 1                     | GA = 1, GB = 0   | 1-10%             | 1                | 1+10%             |                   |
| Gain2                                | Overall gain 2                     | GA = 0, GB = 1   | 2-5%              | 2                | 2+5%              |                   |
| Gain4                                | Overall gain 4                     | GA = GB = 0, default setting   | 4-5%              | 4                | 4+5%              |                   |
| RL                                   | External Serial Resistor           | RL serial to CL<br>(see Figure 13 on page 8)   | 100               |                  | 1k                | Ω                 |
| CL                                   | External Capacitive Load           |  | 0.01              |                  | 10                | nF                |
| ISHORT+                              | Positive Short Circuit Current     | V <sub>OUT</sub> is driven to V <sub>DDA</sub> and V <sub>OUT</sub> is connected to V <sub>SSA</sub> |                   | 25               |                   | mA                |
| ISHORT-                              | Negative Short Circuit Current     | V <sub>OUT</sub> is driven to V <sub>SSA</sub> and V <sub>OUT</sub> is connected to V <sub>DDA</sub> |                   | 25               |                   | mA                |
| V <sub>OUT-L</sub>                   | Output Range Low                   | @ pin V <sub>OUT</sub>   |                   | $V_{SSA} + 0.05$ |                   | V                 |
| V <sub>OUT-H</sub>                   | Output Range High                  | @ pin V <sub>OUT</sub>   |                   | $V_{DDA} - 0.05$ |                   | V                 |
| <b>AC Electrical Characteristics</b> |                                    |  |                   |                  |                   |                   |
| f <sub>c</sub>                       | Filter Cut-off Frequency           | $V_{DDA} = 4.5V$ , GA = GB = 0, INP-INN = 1V <sub>pp</sub> , f <sub>IN</sub> = 16kHz and 29kHz       | 16                | 23               | 29                | kHz               |
| THD                                  | Total Harmonic Distortion          | $V_{DDA} = 5V$ , f <sub>IN</sub> = 1kHz, INP-INN = 8V <sub>pp</sub> , Gain0.5                        |                   | 80               |                   | dB                |
| V <sub>NOISE</sub>                   | RMS noise at OUT                   | Gain4, f <sub>c</sub> = 50Hz - 23kHz   |                   |                  | 1                 | mV <sub>RMS</sub> |

1. Guaranteed by design

## 7 Typical Operating Characteristics

VDDA = 5.0V, T<sub>A</sub> = +25°C (unless otherwise specified).

Figure 3. CMRR vs. Temperature; G<sub>A</sub> = G<sub>B</sub> = 0

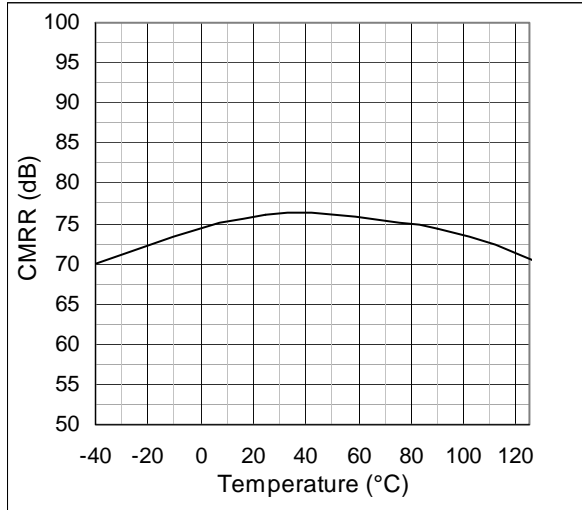


Figure 4. Supply Current vs. Temperature;

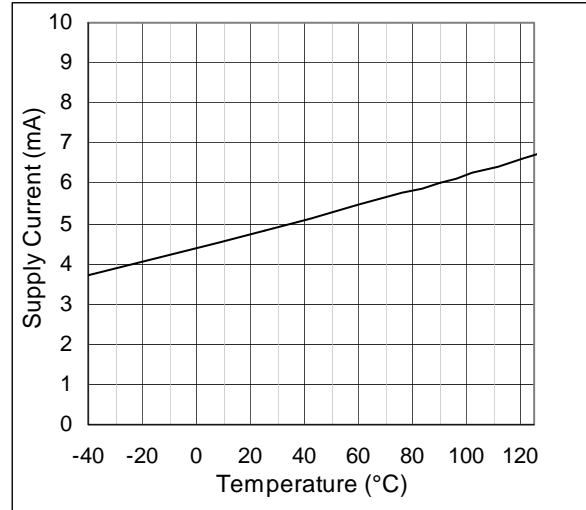


Figure 5. THD vs. Temperature

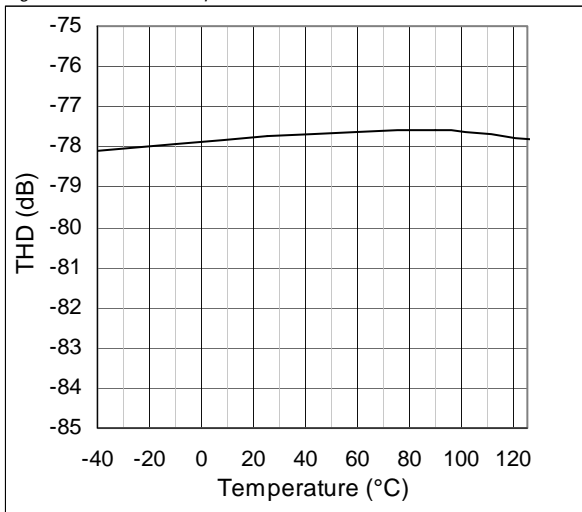


Figure 6. THD vs. Frequency

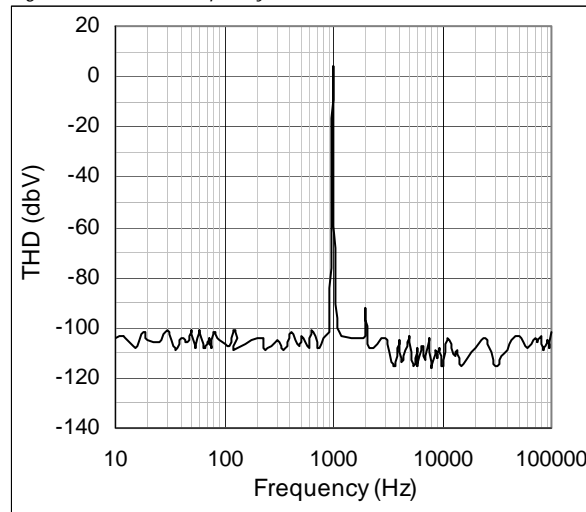


Figure 7. Transfer Characteristics

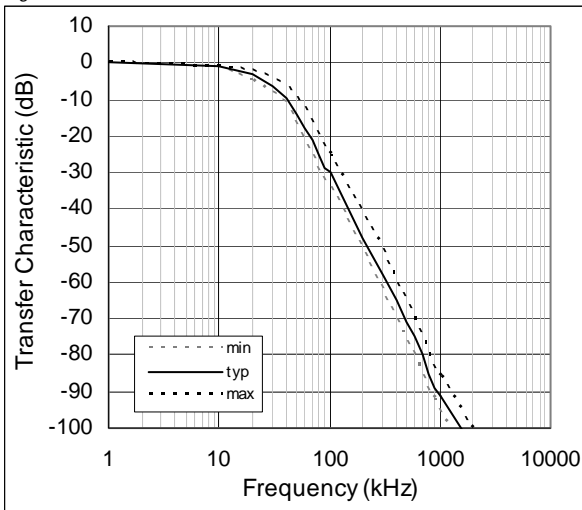
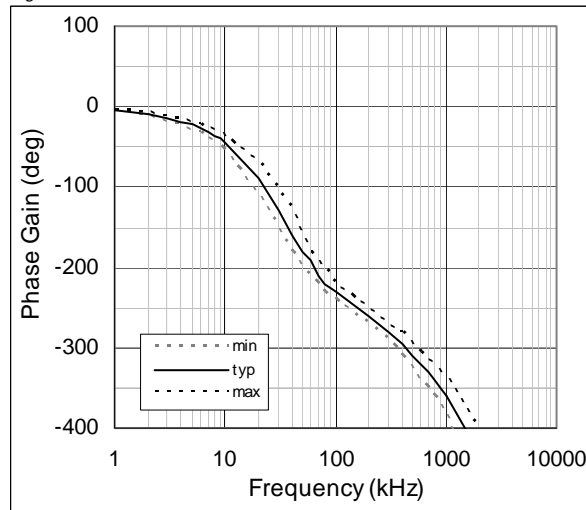


Figure 8. Phase Gain

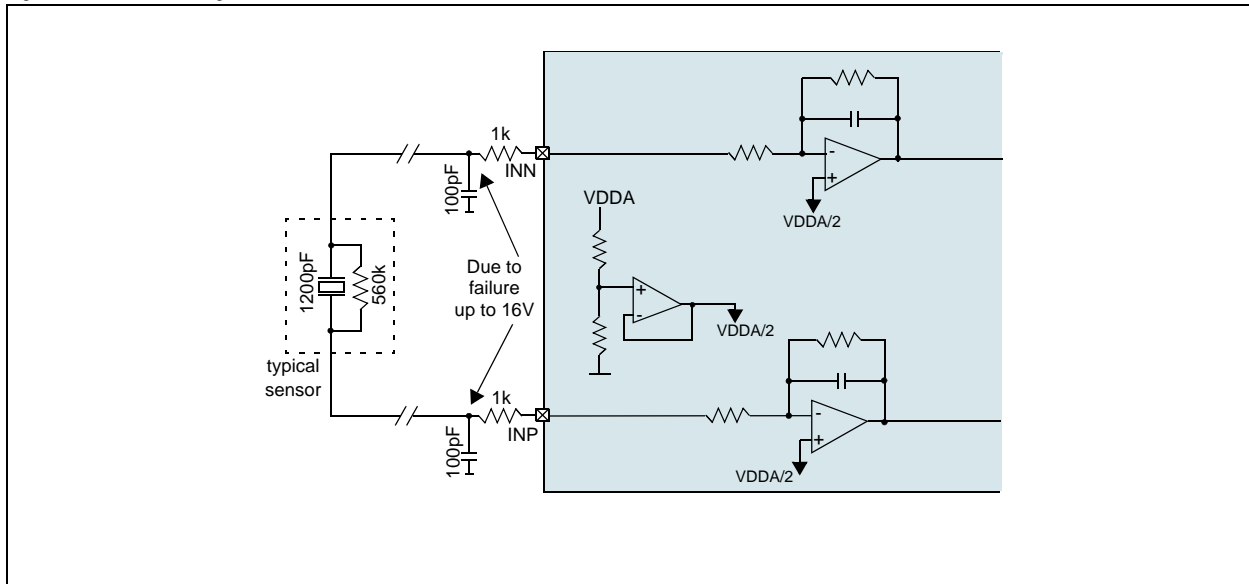


## 8 Detailed Description

### Sensor Biasing and Input Protection Resistors

Due to the capacitive and differential nature of the knock sensor, the common mode voltage for the sensor must be set. This is ensured by the first amplifier, whose virtual ground is biasing the sensor via a of  $50k\Omega$  resistor. Due to a failure, voltages up to 16V can occur on the input pins. In this case two external serial resistors of  $1k\Omega$  must be applied at the inputs. These resistors are limiting the current, when the on chip protection diode opens.

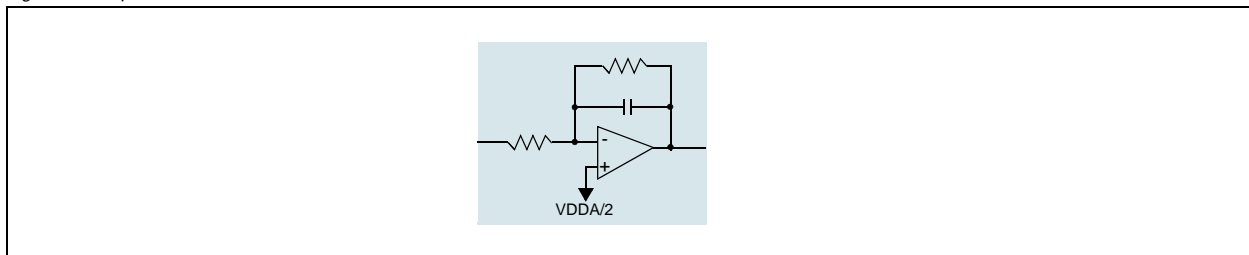
Figure 9. Sensor Biasing



### Inverting Input Structure

The Input Structure is a first order low-pass filter and fulfills two main functions. First, it is used for biasing the sensor and second, the first order low-pass filter characteristic is used for noise suppression.

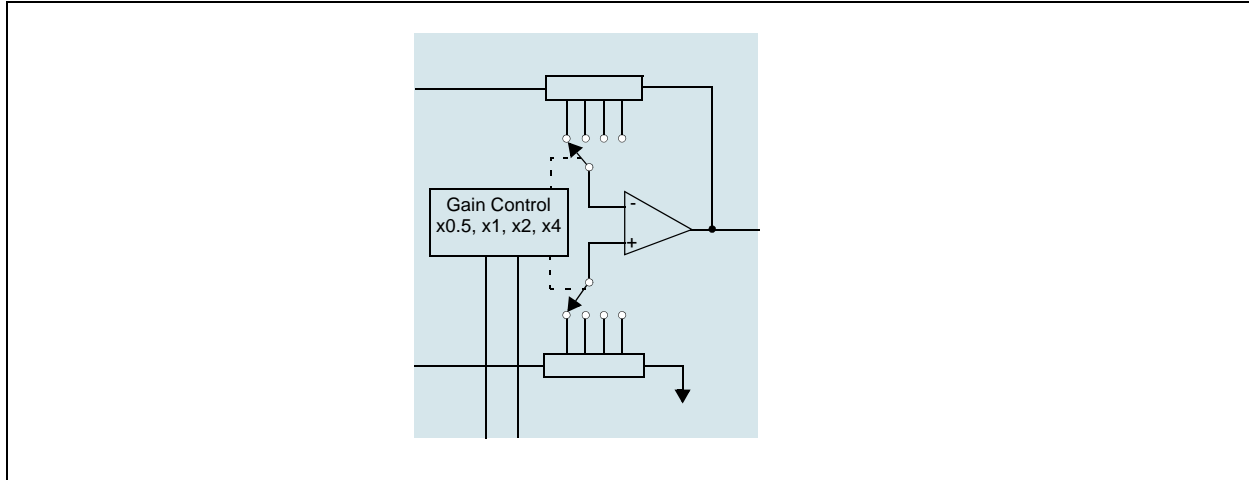
Figure 10. Input Buffer



## Fully Differential to Single Ended Conversion

The Subtractor block converts the filtered differential sensor signal into a single ended signal. Further this block provides also the gain setting (see Section Gain Settings).

Figure 11. Subtractor Block



## Gain Settings

By means of pins GA and GB, 4 gain settings (x0.5, x1, x2, x4) can be realized.

The default gain setting is 4, GA=0 and GB=0.

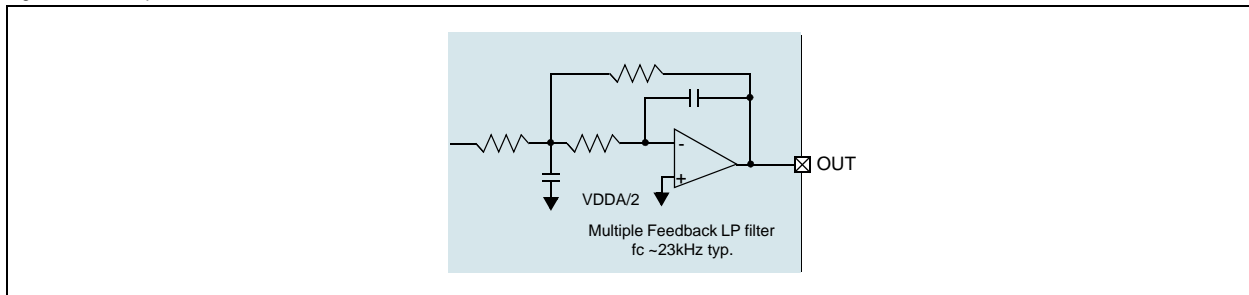
Table 4. Gain Settings

| Gain | GA | GB |
|------|----|----|
| 0.5  | 1  | 1  |
| 1    | 1  | 0  |
| 2    | 0  | 1  |
| 4    | 0  | 0  |

## Multiple Feedback Filter

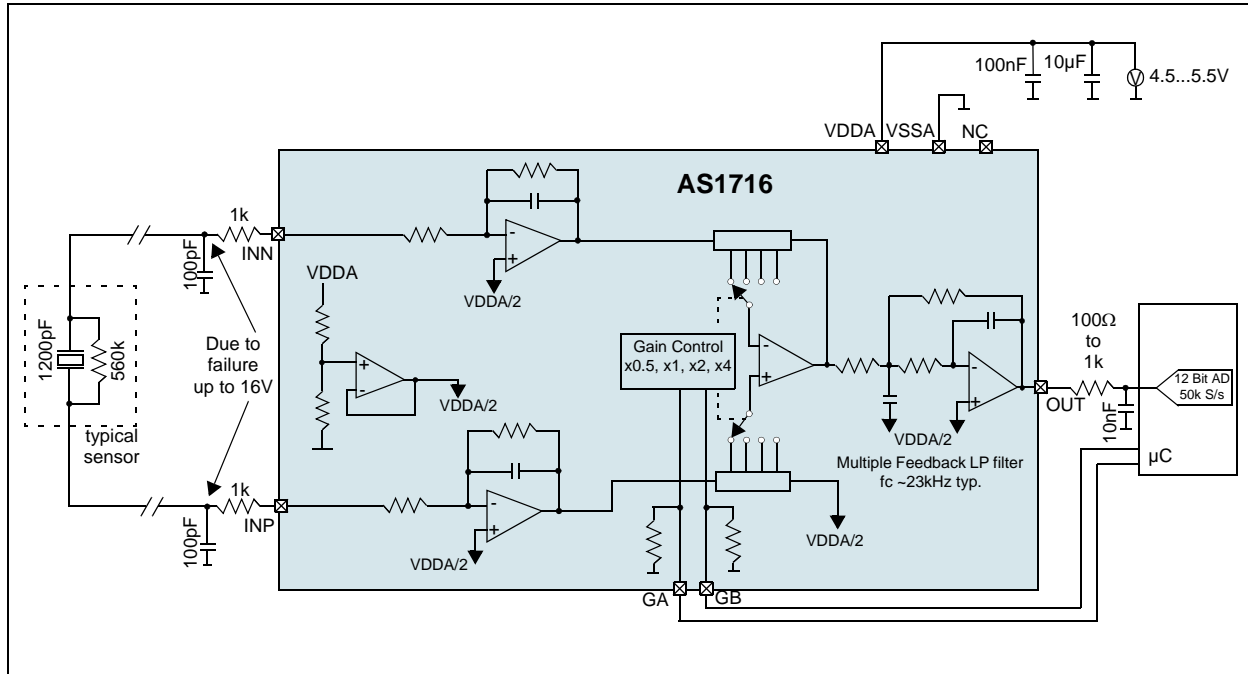
The Multiple Feedback Filter provides a second order low pass characteristics with a minimum cut-off frequency of 16kHz and a typical  $f_c$  of 23kHz. The Multiple Feedback configuration is used to avoid aliasing, to filter out high frequency components. The Output is able to drive a resistor from 100 $\Omega$  to 1k $\Omega$  serial to a 10nF capacitor.

Figure 12. Multiple Feedback Filter



## 9 Application Information

Figure 13. Application Diagram, minimal requirements



Values of the suggested external components are indicative and need to be characterized for each specific application.

### Typical Piezo Sensor:

- Resistor from 500kΩ to 1MΩ
- Capacity from 900nF to 1.5µF

### Typical wire equivalent circuit:

- Capacity to ground from 100pF to 400pF / meter
- Capacity between wires strongly depends on type of wires (twisted-pair strongly suggested)
- Resistance is typical 50mΩ / meter @ 20°C

### Layout rules

- Input Resistors and Capacitors at the inputs should be placed as close as possible to the stronger possible source of disturbances (i.e. the input connector).
- The input lines should be kept as short as possible and routed close to each other.
- The filter capacitor (100nF) on supply should be a ceramic type and placed as close as possible to the chip.
- VSSA and VDDA lines on PCB should have larger width than other signals to minimize resistance, especially if the 10µF capacitor is not very close to the chip.
- The output line should be kept as short as possible.



## 10 Package Drawings and Markings

Figure 14. 8-pin SOIC Marking

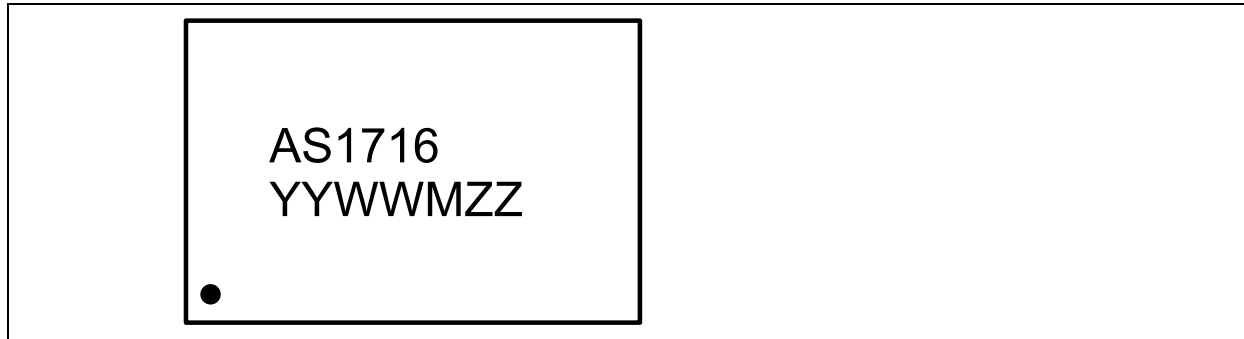
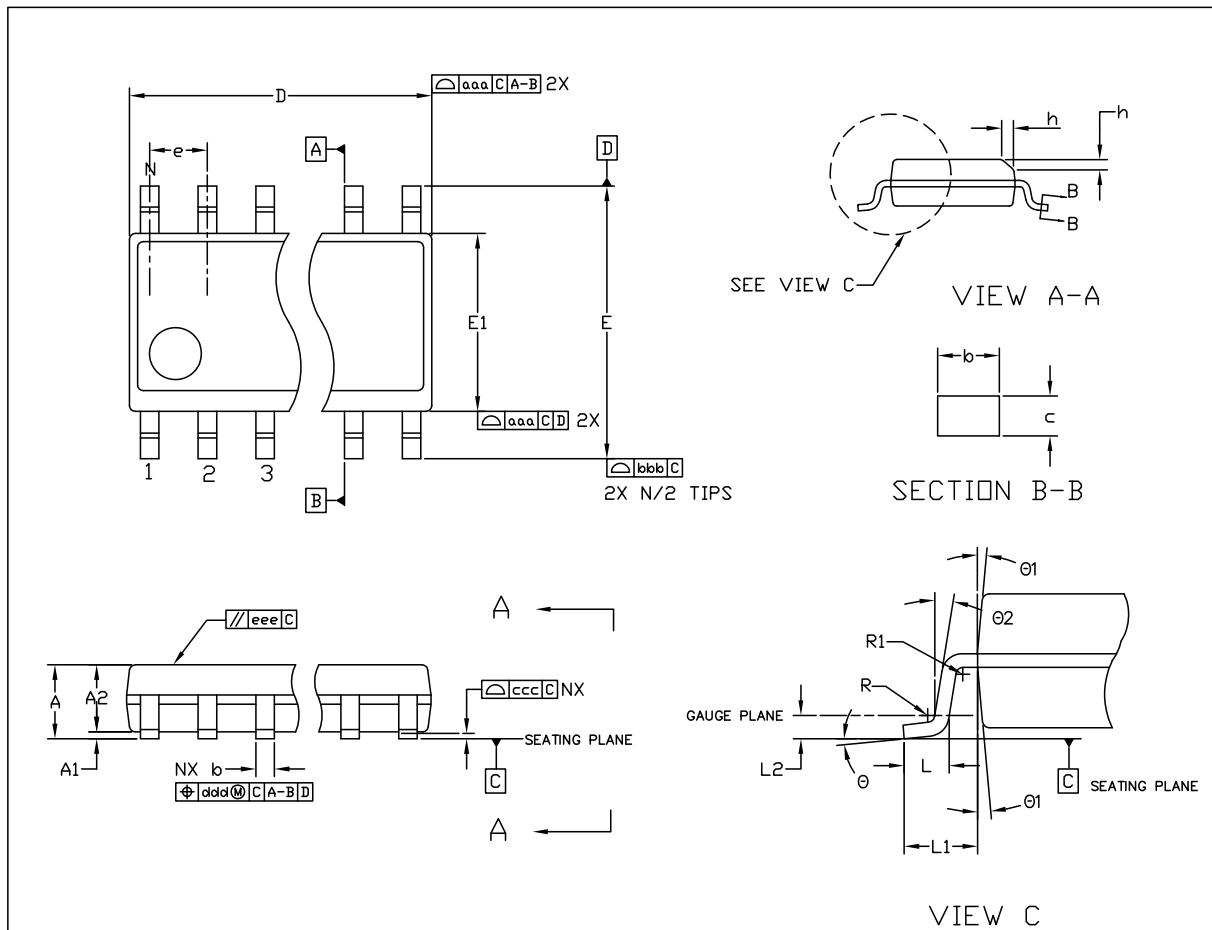


Table 5. Packaging Code YYWWMZZ

| YY                                  | WW                 | M                | ZZ                              |
|-------------------------------------|--------------------|------------------|---------------------------------|
| last two digits of the current year | manufacturing week | plant identifier | free choice / traceability code |

Figure 15. 8-pin SOIC Package Dimensions



| REF. | MIN  | NOM      | MAX  |
|------|------|----------|------|
| A    | —    | —        | 1.75 |
| A1   | 0.10 | —        | 0.25 |
| A2   | 1.25 | —        | —    |
| b    | 0.31 | —        | 0.51 |
| c    | 0.17 | —        | 0.25 |
| D    | —    | 4.90 BSC | —    |
| E    | —    | 6.00 BSC | —    |
| E1   | —    | 3.90 BSC | —    |
| e    | —    | 1.27 BSC | —    |
| L    | 0.40 | —        | 1.27 |
| L1   | —    | 1.40 REF | —    |
| L2   | —    | 0.25 BSC | —    |
| R    | 0.07 | —        | —    |
| R1   | 0.07 | —        | —    |
| h    | 0.25 | —        | 0.50 |
| θ    | 0°   | —        | 8°   |
| θ1   | 5°   | —        | 15°  |
| θ2   | 0°   | —        | —    |
| aaa  | —    | 0.10     | —    |
| bbb  | —    | 0.20     | —    |
| ccc  | —    | 0.10     | —    |
| ddd  | —    | 0.25     | —    |
| eee  | —    | 0.10     | —    |
| fff  | —    | 0.15     | —    |
| ggg  | —    | 0.15     | —    |
| N    | —    | 8        | —    |



NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.

|                        |  |  |                         |  |
|------------------------|--|--|-------------------------|--|
|                        |  |  | ASSEMBLY ENGINEERING    |  |
| a leap ahead in analog |  |  | TITLE                   |  |
| DRAWN                  |  |  | SOIC 150MIL, 8 LEAD     |  |
| RH8                    |  |  | REFERENCE DOCUMENT      |  |
| DATE                   |  |  | JEDEC MS - 012          |  |
| 2010.09.21             |  |  | LATEST REVISION         |  |
| REV.                   |  |  | DRAWING NO.             |  |
| N/C                    |  |  | JCQ                     |  |
| CHECKED                |  |  | UNIT                    |  |
| GBO                    |  |  | DIMENSION AND TOLERANCE |  |
| DATE                   |  |  | SCALE                   |  |
| 2010.09.21             |  |  | NOT IN SCALE            |  |
| APPROVED               |  |  | SHEET                   |  |
| MKR                    |  |  | 1 OF 1                  |  |

## 11 Ordering Information

The device is available as the standard product shown in [Table 6](#).

*Table 6. Ordering Information*

| Ordering Code | Marking | Description                        | Delivery Form | Package    |
|---------------|---------|------------------------------------|---------------|------------|
| AS1716-ASOT   | AS1716  | Capacitive Sensor Interface, 16kHz | Tape and Reel | 8-pin SOIC |

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## Contact Information

### Headquarters

austriamicrosystems AG  
Tobelbaderstrasse 30  
A-8141 Unterpremstaetten, Austria

Tel: +43 (0) 3136 500 0  
Fax: +43 (0) 3136 525 01

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