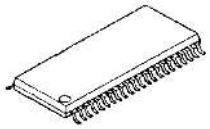
Digital Signal Processor with PWM Modulator for Correction of Sound

■ General Description

The NJU26060-05A is a high performance 24-bit digital signal processor included sampling rate converter (SRC), PWM modulators. The NJU26060-05A provides Stereo Expander II, Elevation, 256Tap FIR filter, 8band IIR filter, Dynamic Bass Boost, two systems Limiter, and Dynamic Range Compression.

The NJU26060-05A is suitable for TV, mini component, CD radio-cassette, speakers system and other audio products.

■ Package



NJU26060V-05A

■ Features

- Hardware

- 24bit Fixed-point Digital Signal Processing
- Clock Frequency : 24.576MHz, Embedded PLL Circuit
- Sampling rate converter (SRC) : Fs=8kHz to 192kHz → 48kHz
- PWM modulator : 4ch Outputs (2 stereos)
- Digital interface transmitter (DIT) : 1 port
- Digital Audio Interface : 3 Input ports / 2 Output ports (switch over from PWM output)
- Digital Audio Format : I^2S 24bit, Left-justified, Right-justified, BCK : 32/64fs
- Master / Slave Mode
  - Sampling Rate Converter: Slave mode
  - DSP: Master Mode
- Host Interface : I^2C Bus (Fast-mode/400kbps)
- Power Supply : V_{DD} = 3.3V
- Input terminal: : 5V Input tolerant
- Package : SSOP44 (Pb-Free)

- Software

- HPF
- Input Signal Detect
- Input Trim
- Stereo Expander **II**
- Elevation
- 256Taps FIR Filter
- 8Band IIR Filter (7、8Band PEQ + Shelf Filter)
- Master Volume
- DBB
- Xover (HPF/LPF)
- DRC
- SDO0 DRC Mixer
- SDO1 Cch : C/SW Mixer
- Delay
- Output Trimmer / Inverter
- Limiter
- BEEP

* The detail hardware specification of the NJU26060-05A is described in the “NJU26060 Series Hardware Specification”.

■ DSP Block Diagram

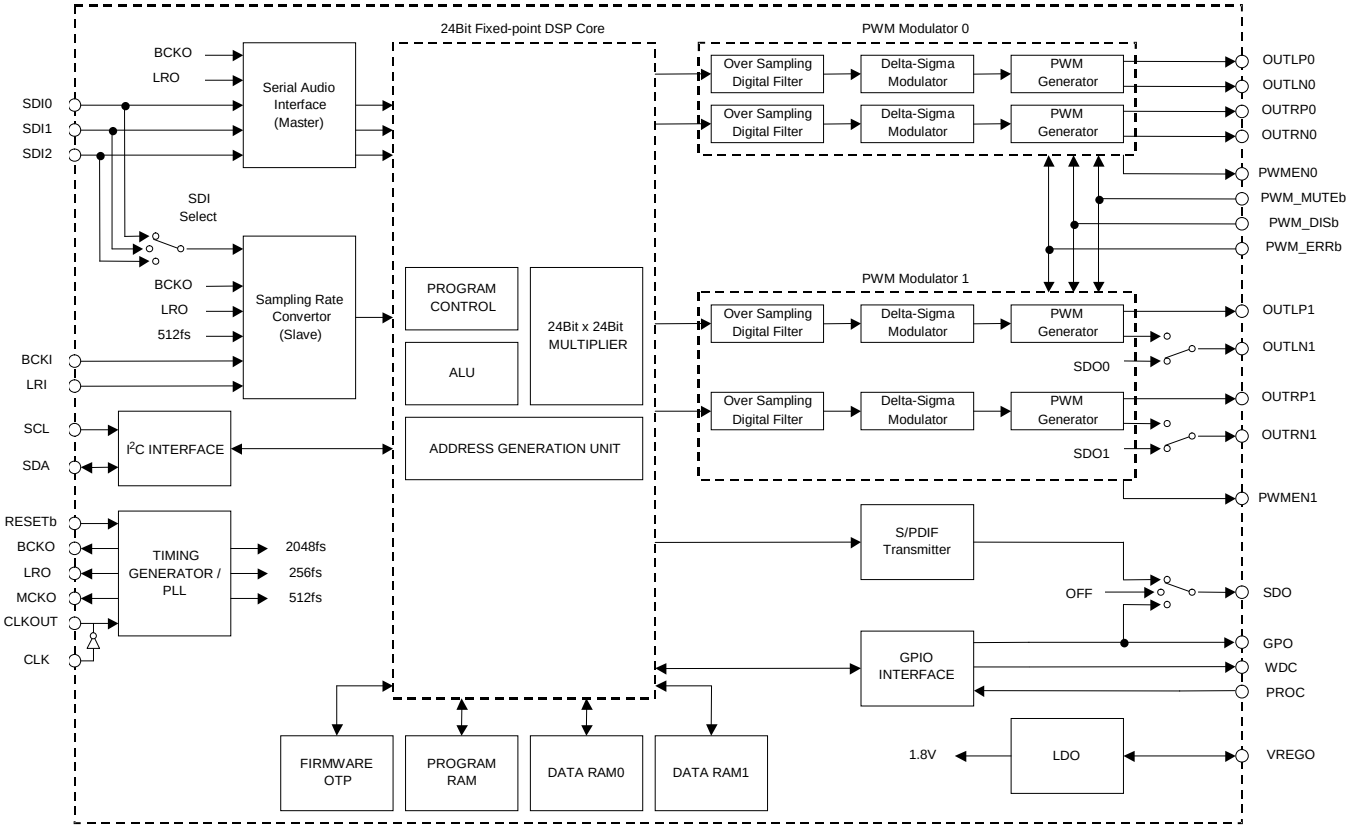


Fig 1. NJU26060-05A Hardware Block Diagram

■ Function Block Diagram

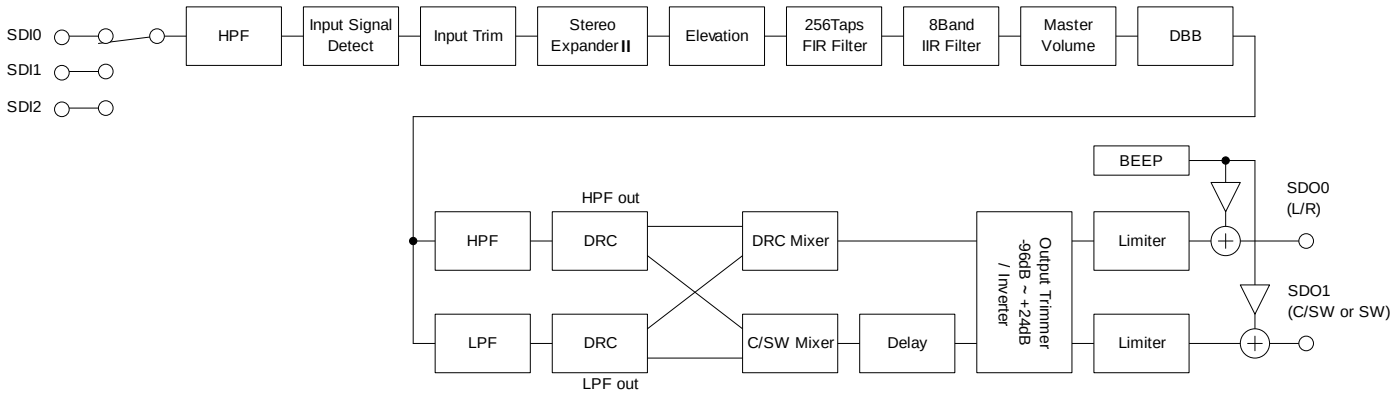


Fig 2. NJU26060-05A Block Diagram

■ Pin Configuration

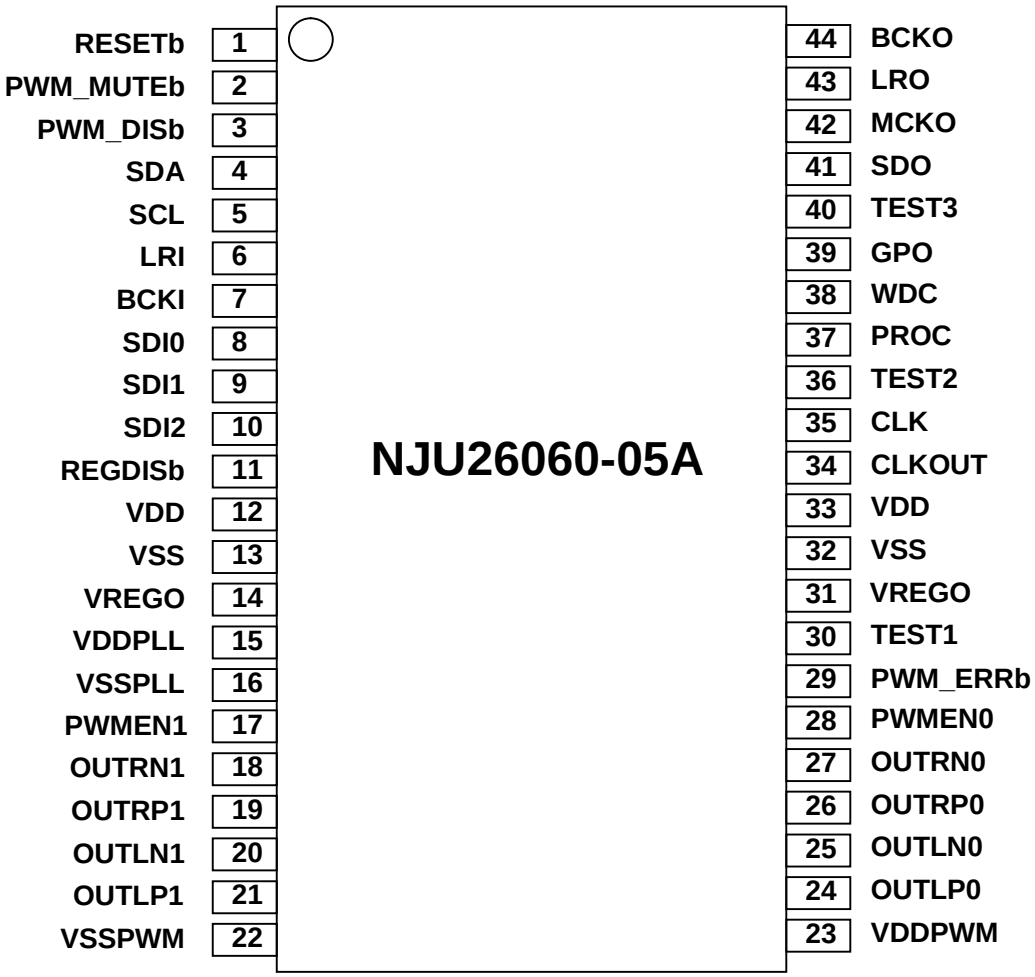


Fig 3. NJU26060-05A Pin Configuration

■ Pin Description

Table 1. Pin Description

Pin No.	Symbol	I/O	Description
1	RESETb	I	Reset (RESETb="Low" : DSP Reset)
2	PWM_MUTEb	I+	PWM Block Mute request input
3	PWM_DISb	I+	PWM Block Standby request input
4	SDA	OD	I^2C serial data I/O (connect to VSS with 3.3kohm when this is not used)
5	SCL	I	I^2C clock (connect to VSS when this is not used)
6	LRI	I-	LR Clock Input for Fs conversion side
7	BCKI	I-	Bit Clock Input for Fs conversion side
8	SDI0	I-	Audio Data Input 0
9	SDI1	I-	Audio Data Input 1
10	SDI2	I-	Audio Data Input 2
11	REGDISb	I	Built-in Power Supply Enable (connect to VDD)
12	VDD	P	Power Supply +3.3V
13	VSS	G	GND
14	VREGO	PI	Built-in Power Supply Bypass (connect capacitors 10uF and 0.01uF)
15	VDDPLL	PA	PLL Power Supply +1.8V (connect to VREGO)
16	VSSPLL	GA	PLL Power Supply GND
17	PWMEN1	O	PWM1 enable output (PWMEN1='1': enable)
18	OUTRN1	OP	PWM1 R- output / Audio Data output 1 (setting Firmware)
19	OUTRP1	OP	PWM1 R+ output
20	OUTLN1	OP	PWM1 L- output / Audio Data output 0 (setting Firmware)
21	OUTLP1	OP	PWM1 L+ output
22	VSSPWM	GP	PWM Power Supply GND
23	VDDPWM	PP	PWM Power Supply +3.3V (decoupling capacitor is required to stable power supply)
24	OUTLP0	OP	PWM0 L+ output
25	OUTLN0	OP	PWM0 L- output
26	OUTRP0	OP	PWM0 R+ output
27	OUTRN0	OP	PWM0 R- output
28	PWMEN0	O	PWM0 enable output (PWMEN0='1': enable)
29	PWM_ERRb	I+	PWM block stop request input (PWM_ERRb='0': PWM stop)
30	TEST1	I	for Test (connected to VSS)
31	VREGO	PI	Built-in Power Supply Bypass (connect capacitors 10uF and 0.01uF)
32	VSS	G	GND
33	VDD	P	Power Supply +3.3V
34	CLKOUT	O	OSC Output
35	CLK	I	OSC Clock Input
36	TEST2	I-	for Test (connected to VSS)
37	PROC	I+	PROC terminal
38	WDC	O+	Watch dog clock terminal
39	GPO	OD	Signal detection terminal
40	TEST3	I-	for Test (connected to VSS)
41	SDO	O	OFF / DIT output 0 / GPO(same function as pin#39) (selected by command)
42	MCKO	O	Master Clock Output for A/D, D/A
43	LRO	O	LR clock Output
44	BCKO	O	Bit clock Output

Note :
I : Input O: Output
I+ : Input (Pull-up) I -: Input (Pull-down)
OD : Bi-directional (Open Drain) This pin requires a pull-up resistance.
I/O : Bi-directional PI: Built-in Power Supply Bypass
OP : PWM output(supply for VDDPWM)

NOTICE: Does not keep the terminal without the pull-up resistance or the pull-down resistance open.
The functions of SDIO0 to SDIO2, SDO, OUTxxx depend on the IC specifications.

■ Audio Clock

Three kinds of clocks are needed for digital audio data transfer.

(1) LR clock (LRI, LRO) is needed by serial-data transmission. It is the same as the sampling frequency of a digital audio signal.

(2) Bit clock (BCKI, BCKO) is needed by serial-data transmission. It becomes the multiple of LR clock.

(3) Master clock (MCKO) needed by A/D, D/A converter, etc. It becomes the multiple of LR clock. It is not related to serial audio data transmission.

The NJU26060-05A support serial data format that includes 32(32fs) or 64(64fs) BCK clocks.

The NJU26060-05A supplies the clock necessary for digital audio data transmission to an external device as a master device by each terminal of MCKO, BCKO, and LRO. On the other hand, the sampling rate converter that works as a slave device takes digital audio data with the clock input to BCKI and the terminal LRI, and converts the sampling frequency into the clock system composed of MCKO/BCKO/LRO. After internal reset ends as a master clock, the terminal MCKO sets the buffer output or 2 dividing frequency the output of the input clock to the terminal CLK. The stop is also possible according to the command of the firmware.

The NJU26060-05A is used by 512 times the internal operation sampling frequency (It is 24.576MHz in the sampling frequency 48kHz). In that case, NJU26060-05A can output 64 times, 32 times the bit clock to of the LR clock one time the sampling frequency and of each, and 512 times and 256 times the master clock as a mastering device. Table 5 shows the relation of each clock.

The NJU26060 series support two clock frequencies (24.576kHz ,or 22.572kHz) as hardware specifications. However NJU26060-05A acceptable one clock frequency (24.576kHz), cause of the software on NJU26060-05A supports one clock frequency (24.576kHz).

Table 2. Supply Clock for CLK pin Frequency and BCKO,LRO,MCKO

Clock Signal	Multiple Frequency	Clock Frequency
		24.576MHz(for pin#35)
LRO	1Fs	48kHz
BCKO(32Fs)	32Fs	1.536MHz
BCKO(64Fs)*	64Fs	3.072MHz
MCKO(256Fs)*	256Fs	12.288MHz
MCKO(512Fs)	512Fs	24.576MHz

* default for starting up

■ Serial Audio Data Input/Output

Audio interface of the NJU26060-05A includes three data input ports: SDI0, SDI1 and SDI2 (Table 3), and three data output ports: SDO0, SDO1 and SDO2 (Table 4).

Table 3. Serial Audio Input Pin Description

Pin No.	Symbol	Description
8	SDI0	Audio Data Input 0
9	SDI1	Audio Data Input 1
10	SDI2	Audio Data Input 2

Table 4. Serial Audio Output Pin Description

Pin No.	Symbol	Description
20	OUTLN1	Audio Data Output 0 (L/R)
18	OUTRN1	Audio Data Output 1 (C/SW)
41	SDO	OFF

Pin#20, 18 can be change the function to PWM1 output. Pin#41 can be change the function to DIT (output 0) or GPO output (the function is same as Pin#39). Refer to table1.

■ I²C bus Interface

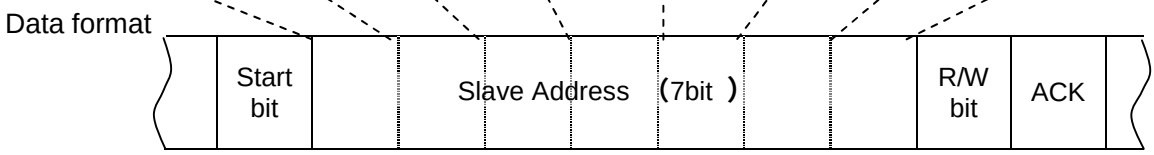
I²C bus interface transfers data to the SDA pin and clocks data to the SCL pin. SDA pin is a bi-directional open drain and requires a pull-up resister.

The slave address is set up as Table 5. When the initialization is finished (After reset NJU26060-05A), NJU26060-05A can be communicated with Host. However until finished the initialization, the Host can't be get any correct responses.

Note : The serial host interface supports "Standard-Mode (100kbps)" and "Fast-Mode (400kbps)" I²C bus data transfer.

Table 5. Serial Host Interface Pin Description

Fixed value							R/W
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	1	1	1	0	0	R/W



*: On "R/W bit", "0"="W", "1"="R".

■ General-purpose in/out pin

The NJU26060 Series has general-purpose in/out pin. On NJU26060-05A, these terminals operate as below functions (Table 6).

Table 6. General-purpose in/out pin and pin disposal

Pin No.	Symbol	Description
40	TEST3 (Pull-down I)	Terminal for a test. Connect to VSS
39	GPO (O)	Signal detection terminal. Default is Hi-Z. Connect to VDD with pull-up resistor. It outputs Low If it detects no signal.
38	WDC (O)	Output of the watchdog clock. This terminal is toggled between "Low" and "High" in the audio processing. Thus, this terminal notifies the correct operating to another devices. If monitored by watchdog IC, microcontroller, and so on, abnormal condition can be detected. The rate of WDC is 100msec (10Hz). .
37	PROC (I)	PROC terminal, H: However reset the NJU26060-05A, signal processing is not started. To start signal processing, start command is required. L: After reset the NJU26060-05A, signal processing is started (default setting: master volume is muted).

■ Command Table

Table 7. Command table

No.	Function
1	Set Task
2	System State
3	Smooth Control Config
4	Master Volume Control Command
5	Volume Control Command
6	Input Trim Command
7	Input Select Command
8	Elevation Gain Command
9	Time Alignment Command
10	IIR Filter Fo Command
11	IIR Filter Q Command
12	IIR Filter Gain Command
13	IIR Filter Mode Command
14	IIR Filter Smooth Command
15	FIR Bypass Trim Command
16	FIR New Coeff Send Lch Command
17	FIR New Coeff Send Rch Command
18	FIR Coeff Update Command
19	Expander Ⅱ Gain Command
20	Expander Ⅱ Low Boost Command
21	DBB LPF Fc Command
22	DBB Attack Time / Release Time Command
23	DBB Level Command
24	DBB Effect Command
25	DBB Treble Boost Level Command
26	DRC Mode Select Command
27	DRC Ratio And Attack Time / Release Time
28	DRC Threshole Level Set Up Command
29	Xover Fc Command
30	Xover Order Command
31	Ch Output Invert Command
32	DRC Mixer Command
33	Subsonic Filter Fc Command
34	Limiter Threshold Command
35	Input Signal Detect Command
36	Beep Start Command
37	PWM0 Set Command
38	PWM1 Set Command
39	Expander Ⅱ Mode Command
40	Version Number Request Command
41	Revision Number Request Command
42	DSP Software Reset Command
43	Start Command (Boot With Mute)
44	Start Command (Boot With Unmute)
45	Nop Command

Notes : In respect to detail command information, request New Japan Radio Co., Ltd.

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